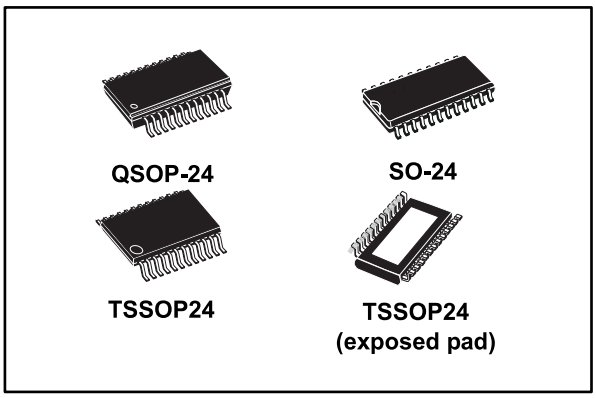
# STP16CPS05

## Low voltage 16-bit constant current LED sink driver with auto power saving

Datasheet - production data




## Features

- Low voltage power supply down to 3 V
- 16 constant current output channels
- Adjustable output current through external resistor
- Serial data IN/parallel data OUT
- Auto power-saving feature minimizes the quiescent current if no active data is detected on the latches
- Can be driven by a 3.3 V microcontroller
- Output current: 5-100 mA
- Max clock frequency 30 MHz
- ESD protection: 2 kV HBM, 200 V MM

## Description

The STP16CPS05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The STP16CPS05 contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bit, D-type storage register. In the output stage, sixteen regulated current sources provide from 5 mA to 100 mA constant current to drive the LEDs. The auto power shut-down and auto power-ON feature allows the device to save power without any external intervention. The output current setup time is 40 ns (typ.), thus improving the system performance. The LEDs' brightness can be controlled by using an external resistor to adjust the STP16CPS05 output current. The STP16CPS05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, makes the device suitable for high data rate transmission. The 3.3 V voltage supply is useful in applications that interface with a 3.3 V microcontroller.

**Table 1: Device summary**

| Order code | Package | Packing |
|---|---|---|
| STP16CPS05MTR | SO-24 | 1000 parts per reel |
| STP16CPS05TTR | TSSOP24 | 2500 parts per reel |
| STP16CPS05XTTR | TSSOP24 exposed pad | 2500 parts per reel |
| STP16CPS05PTR | QSOP-24 | 2500 parts per reel |



This is information on a product in full production.

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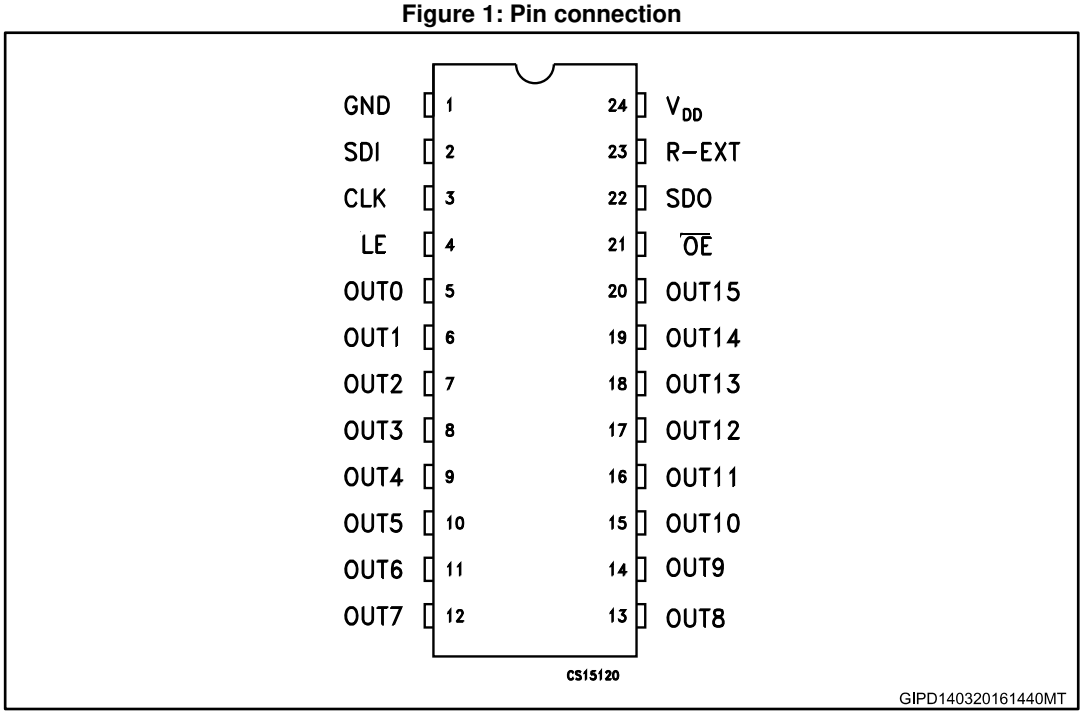
# 1 Summary description

Table 2: Typical current accuracy

| Output voltage | Current accuracy | | Output current | $V_{DD}$ | Temperature |
|---|---|---|---|---|---|
| | Between bits | Between ICs | | | |
| ≥ 1.3 V | ± 1.5 % | ± 5 % | 20 to 100 mA | 3.3 V to 5 V | 25 °C |

## 1.1 Pin connection and description

Figure 1: Pin connection




The exposed pad should be electrically connected to a metal land electrically isolated or connected to GND.

Table 3: Pin description

| Pin n° | Symbol | Name and function |
|---|---|---|
| 1 | GND | Ground terminal |
| 2 | SDI | Serial data input terminal |
| 3 | CLK | Clock input terminal |
| 4 | LE | Latch input terminal |
| 5-20 | OUT 0-15 | Output terminal |
| 21 | $\overline{OE}$ | Input terminal of output enable (active low) |
| 22 | SDO | Serial data out terminal |
| 23 | R-EXT | Input terminal for an external resistor for constant current programming |
| 24 | $V_{DD}$ | Supply voltage terminal |

# 2 Electrical ratings

## 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Table 4: Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | 0 to 7 | V |
| $V_O$ | Output voltage | -0.5 to 20 | V |
| $I_O$ | Output current | 100 | mA |
| $V_I$ | Input voltage | -0.4 to $V_{DD}$ | V |
| $I_{GND}$ | GND terminal current | 1600 | mA |
| $f_{CLK}$ | Clock frequency | 50 | MHz |
| $T_J$ | Junction temperature range(1) | -40 to +170 | °C |

**Notes:**

(1) Such absolute value is achieved according the thermal shutdown.

## 2.2 Thermal data

**Table 5: Thermal data**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $T_{OPR}$ | Operating temperature range | | -40 to + 125 | °C |
| $T_{STG}$ | Storage temperature range | | -55 to + 150 | °C |
| $R_{thJA}$ | Thermal resistance junction-ambient(1) | SO-24 | 42.7 | °C/W |
| | | TSSOP24 | 55 | °C/W |
| | | TSSOP24(2) exposed pad | 37.5 | °C/W |
| | | QSOP-24 | 55 | °C/W |

**Notes:**

(1) According to jedec standard 51-7B.

(2) The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

## 2.3 Recommended operating conditions

**Table 6: Recommended operating conditions at 25 °C**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | | 3.0 | | 5.5 | V |
| $V_O$ | Output voltage | | | | 20 | V |
| $I_O$ | Output current | OUTn | 5 | | 100 | mA |
| $I_{OH}$ | Output current | SERIAL-OUT | | | +1 | mA |
| $I_{OL}$ | Output current | SERIAL-OUT | | | -1 | mA |
| $V_{IH}$ | Input voltage | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| $V_{IL}$ | Input voltage | | -0.3 | | 0.3 $V_{DD}$ | V |
| $t_{wLAT}$ | LE pulse width | $V_{DD}$ = 3.0 V to 5.0 V | 10 | | | ns |
| $t_{wCLK}$ | CLK pulse width | | 8 | | | ns |
| $t_{wEN}$ | $\overline{OE}$ pulse width | | 100 | | | ns |
| $t_{SETUP(D)}$ | Setup time for DATA | | 14 | | | ns |
| $t_{HOLD(D)}$ | Hold time for DATA | | 5 | | | ns |
| $t_{SETUP(L)}$ | Setup time for LATCH | | 15 | | | ns |
| $f_{CLK}$ | Clock frequency | Cascade operation (1) | | | 30 | MHz |

**Notes:**

(1) If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please consider the timings carefully.

# 3 Electrical characteristics

**Table 7: Electrical characteristics (VDD = 3.3 V to 5 V, T = 25 °C, unless otherwise specified)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input voltage high level | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| $V_{IL}$ | Input voltage low level | | GND | | 0.3 $V_{DD}$ | V |
| $I_{OH}$ | Output leakage current | $V_{OH}$ = 20 V | | | 10 | µA |
| $V_{OL}$ | Output voltage (serial-OUT) | $I_{OL}$ = 1 mA | | | 0.4 | V |
| $V_{OH}$ | Output voltage (serial-OUT) | $I_{OH}$ = -1 mA | $V_{DD}$-0.4V | | | V |
| $I_{OL1}$ | Output current | $V_O$ = 0.3 V, $R_{ext}$ = 3.9 kΩ | 4.25 | 5 | 5.75 | mA |
| $I_{OL2}$ | | $V_O$ = 0.3 V, $R_{ext}$ = 970 Ω | 19 | 20 | 21 | |
| $I_{OL3}$ | | $V_O$ = 1.3 V, $R_{ext}$ = 190 Ω | 96 | 100 | 104 | |
| $\Delta I_{OL1}$ | Output current error between bit (all output ON) | $V_O$ = 0.3 V, $R_{ext}$ = 3.9 kΩ | | ± 5 | ± 8 | |
| $\Delta I_{OL2}$ | | $V_O$ = 0.3 V, $R_{ext}$ = 970 Ω | | ± 1.5 | ± 3 | % |
| $\Delta I_{OL3}$ | | $V_O$ = 1.3 V, $R_{ext}$ = 190 Ω | | ± 1.2 | ± 3 | |
| $R_{SIN(up)}$ | Pull-up resistor | | 150 | 300 | 600 | kΩ |
| $R_{SIN(down)}$ | Pull-down resistor | | 100 | 200 | 400 | kΩ |
| $I_{DD(SH)}$ | Shut-down current all latched data = L | $V_{DD}$ = 3.3 V | | 120 | 170 | µA |
| | | $V_{DD}$ = 5 V | | 140 | 200 | |
| $I_{DD(OFF1)}$ | Supply current (OFF) | $R_{ext}$ = 970 OUT 0 to 15 = OFF | | 5 | | mA |
| $I_{DD(OFF2)}$ | | $R_{ext}$ = 240 OUT 0 to 15 = OFF | | 12.5 | | |
| $I_{DD(ON1)}$ | Supply current (ON) | $R_{ext}$ = 970 OUT 0 to 15 = ON | | 5.5 | | |
| $I_{DD(ON2)}$ | | $R_{ext}$ = 240 OUT 0 to 15 = ON | | 13 | | |
| Thermal | Thermal protection | | | 170 | | °C |

**Table 8: Switching characteristics**

| Symbol | Parameter | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $t_{PLH1}$ | Propagation delay time, CLK- $\overline{OUTn}$ , LE = H, $\overline{OE}$ = L | $V_{IH} = V_{DD}$ $V_{IL} = GND$ $C_L = 10$ pF $I_O = 20$ mA $V_L = 3.0$ V $R_{ext} = 1$ KΩ $R_L = 60$ Ω | $V_{DD}$ = 3.3 V | | 35 | 55 | ns |
| | | | $V_{DD}$ = 5 V | | 17.5 | 26 | |
| $t_{PLH2}$ | Propagation delay time, LE- $\overline{OUTn}$ , $\overline{OE}$ = L | | $V_{DD}$ = 3.3 V | | 33.5 | 52 | ns |
| | | | $V_{DD}$ = 5 V | | 17 | 20 | |
| $t_{PLH3}$ | Propagation delay time, $\overline{OE}$ - $\overline{OUTn}$ , LE = H | | $V_{DD}$ = 3.3 V | | 53.5 | 84.5 | ns |
| | | | $V_{DD}$ = 5 V | | 28.5 | 40.5 | |
| $t_{PLH}$ | Propagation delay time, CLK-SDO | | $V_{DD}$ = 3.3 V | | 19 | 27.5 | ns |
| | | | $V_{DD}$ = 5 V | | 13 | 18.5 | |
| $t_{PHL1}$ | Propagation delay time, CLK- $\overline{OUTn}$ , LE = H, $\overline{OE}$ = L | | $V_{DD}$ = 3.3 V | | 13 | 19 | ns |
| | | | $V_{DD}$ = 5 V | | 8.5 | 12 | |
| $t_{PHL2}$ | Propagation delay time, LE -$\overline{OUTn}$ , $\overline{OE}$ = L | | $V_{DD}$ = 3.3 V | | 10 | 14.5 | ns |
| | | | $V_{DD}$ = 5 V | | 6.5 | 9 | |
| $t_{PHL3}$ | Propagation delay time, $\overline{OE}$ - $\overline{OUTn}$ , LE = H | | $V_{DD}$ = 3.3 V | | 10.5 | 15 | ns |
| | | | $V_{DD}$ = 5 V | | 7.5 | 10.5 | |
| $t_{PHL}$ | Propagation delay time, CLK-SDO | | $V_{DD}$ = 3.3 V | | 23 | 33 | ns |
| | | | $V_{DD}$ = 5 V | | 15.5 | 21.5 | |
| $t_{ON}$ | Output rise time 10~90% of voltage waveform | | $V_{DD}$ = 3.3 V | | 23.5 | 31.5 | ns |
| | | | $V_{DD}$ = 5 V | | 9 | 10.5 | |
| $t_{OFF}$ | Output fall time 90~10% of voltage waveform | | $V_{DD}$ = 3.3 V | | 4.6 | 5.5 | ns |
| | | | $V_{DD}$ = 5 V | | 3.5 | 5 | |
| $t_r$ | CLK rise time (1) | | | | | 5000 | ns |
| $t_f$ | CLK fall time (1) | | | | | 5000 | ns |

**Notes:**

(1) In order to achieve high cascade data transfer, please consider tr/tf timings carefully.

# 4 Equivalent circuit and outputs

**Figure 2: OE/DM2 terminal**

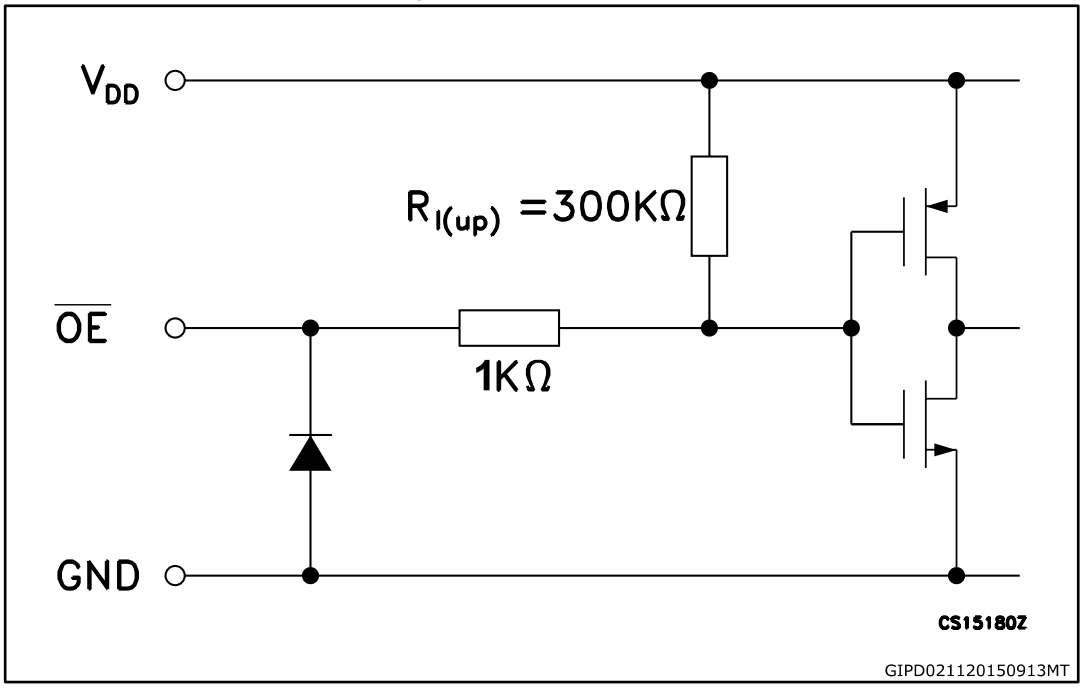



**Figure 3: LE/DM1 terminal**

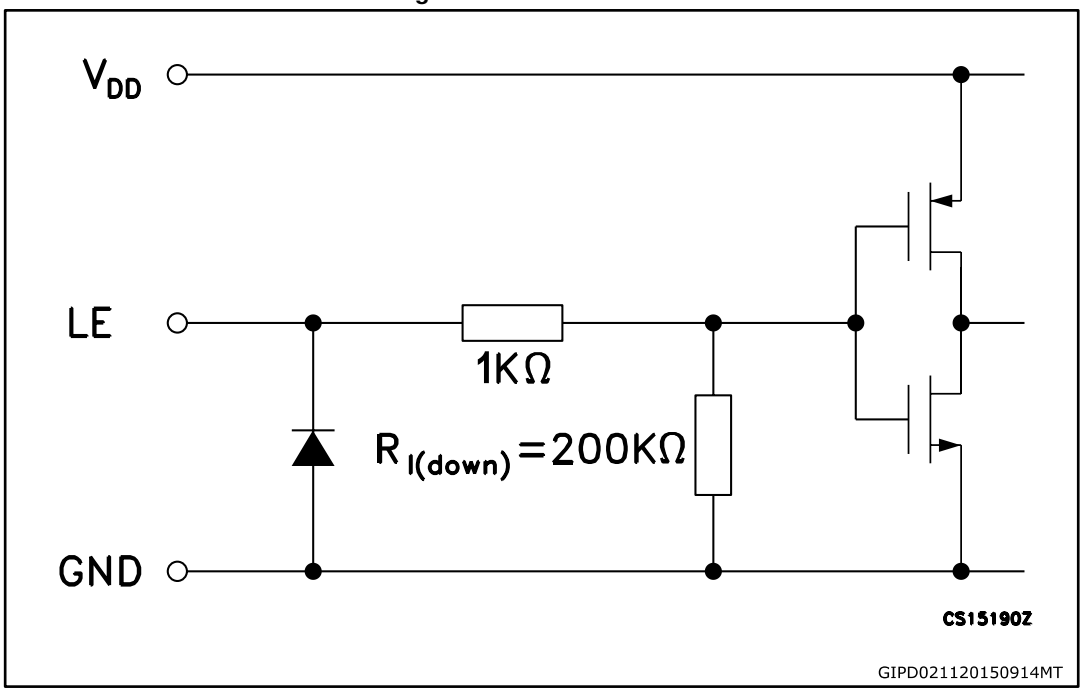


**Figure 4: CLK, SDI terminal**

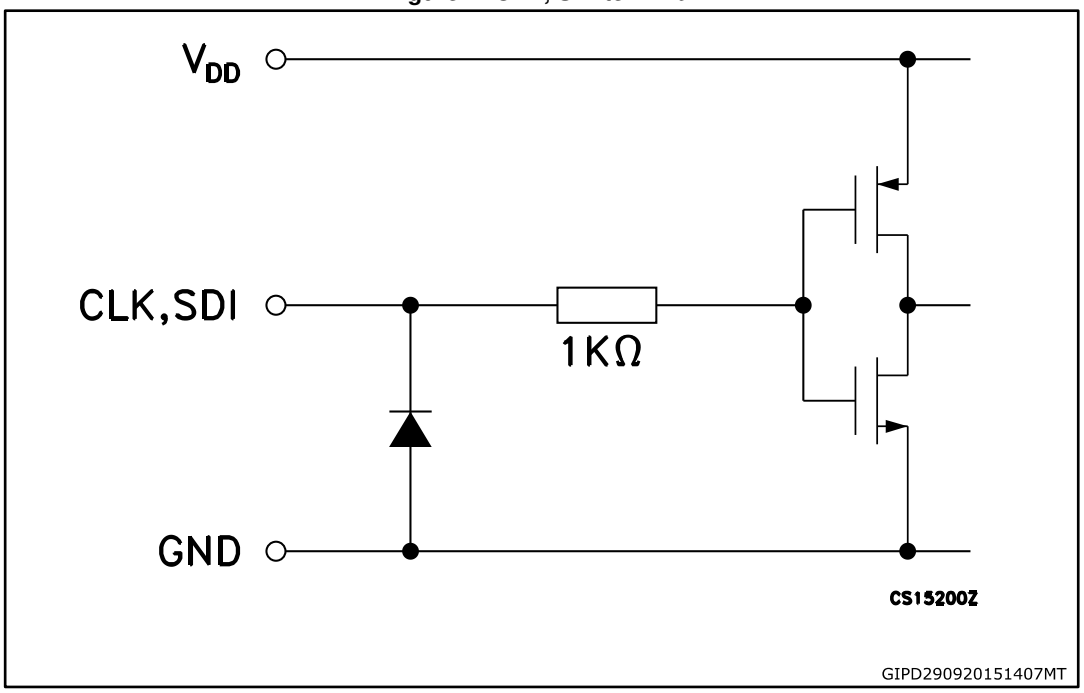



**Figure 5: SDO terminal**

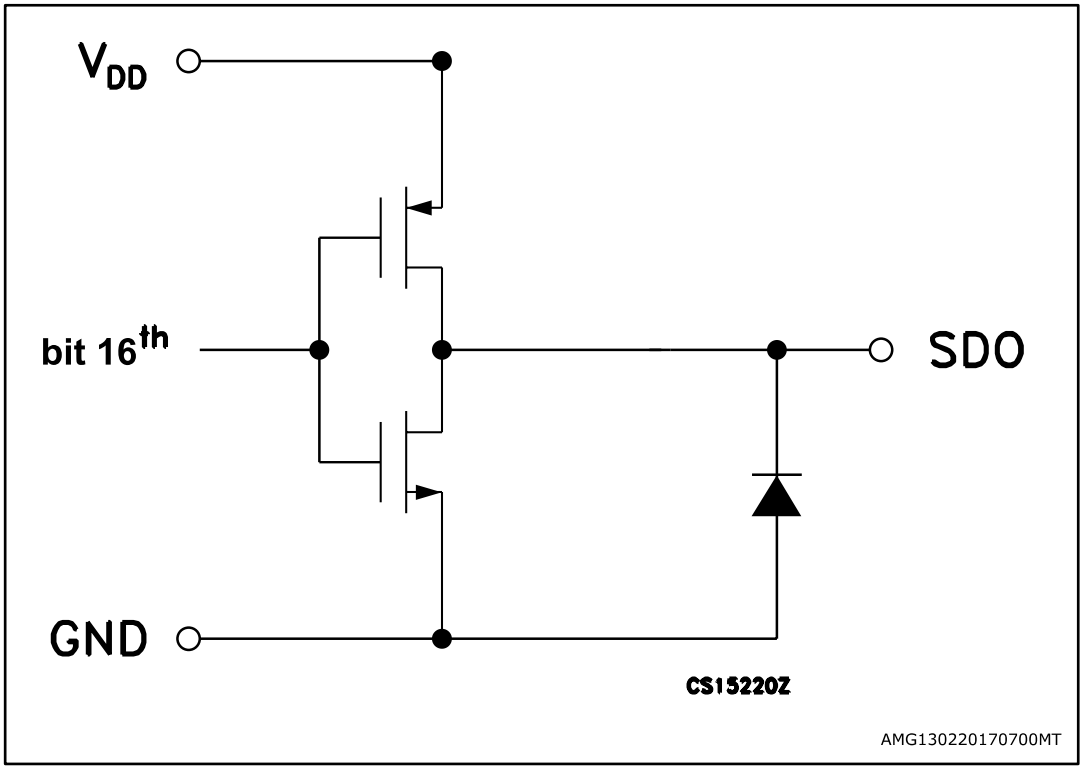
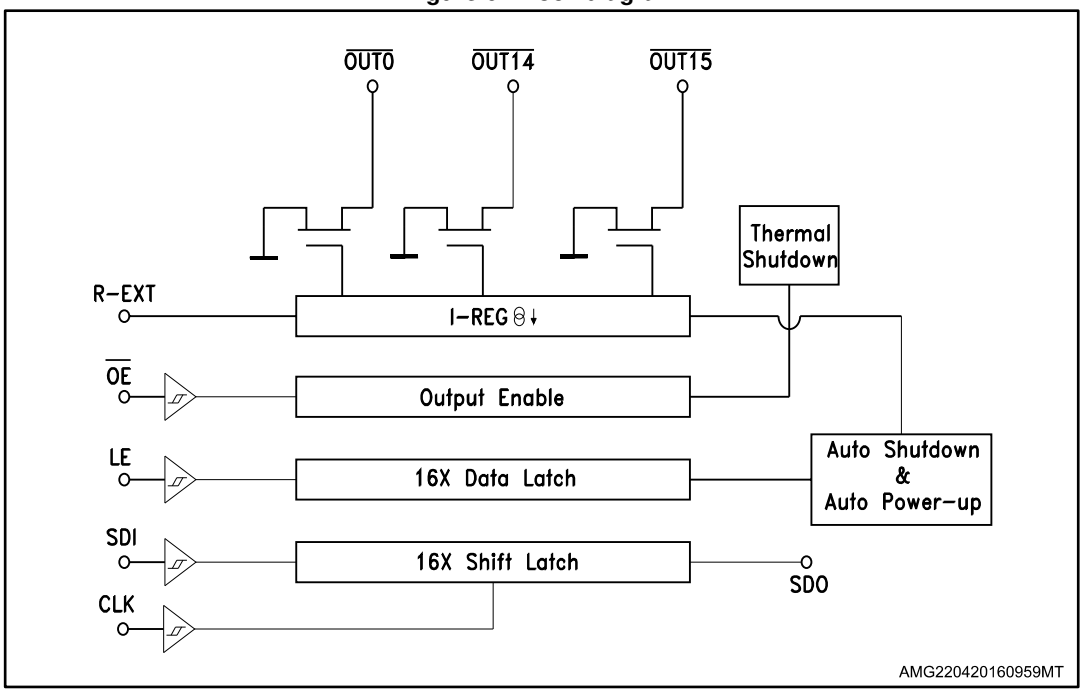


**Figure 6: Block diagram**



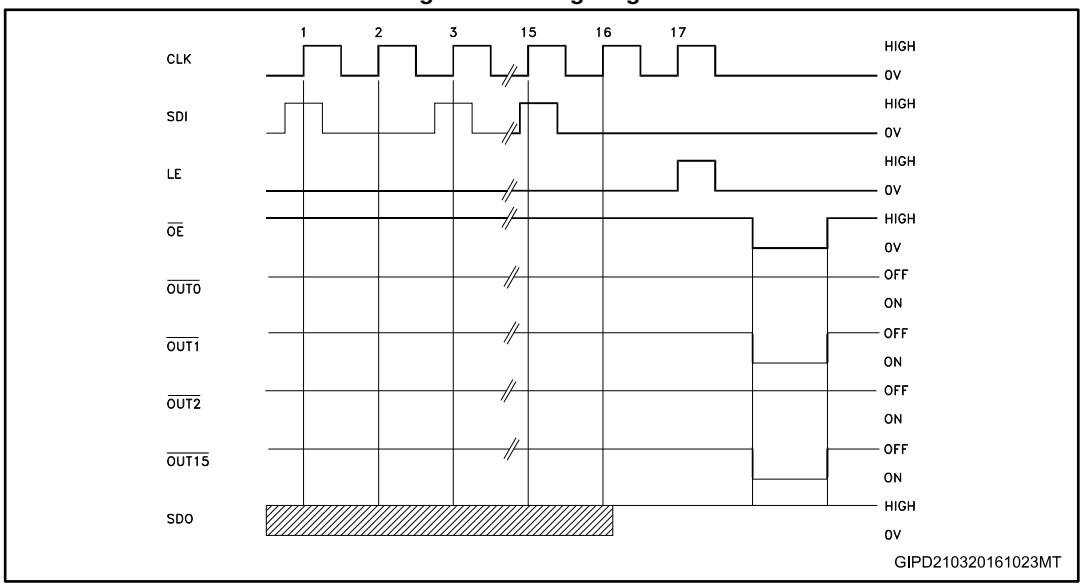
# 5 Timing diagrams

**Table 9: Truth table**

| CLOCK | LE | $\overline{OE}$ | SERIAL-IN | $\overline{OUT0}$ ..... $\overline{OUT7}$ ..... $\overline{OUT15}$ | SDO |
|---|---|---|---|---|---|
| _\|¯ | H | L | Dn | Dn ..... Dn - 7 ..... Dn -15 | Dn - 15 |
| _\|¯ | L | L | Dn + 1 | No change | Dn - 14 |
| _\|¯ | H | L | Dn + 2 | Dn + 2 ..... Dn - 5 ..... Dn -13 | Dn - 13 |
| ¯\|_ | X | L | Dn + 3 | Dn + 2 ..... Dn - 5 ..... Dn -13 | Dn - 13 |
| ¯\|_ | X | H | Dn + 3 | OFF | Dn - 13 |

OUTn = ON when Dn = H OUTn = OFF when Dn = L.

**Figure 7: Timing diagram**




1 Latch and output enable terminals are Level-sensitive and are not synchronized with rising or falling edge of CLK signal.

2 When LE terminal is at low level, the latch circuit holds previous set of data.

3 When LE terminal is at high level, the latch circuit refreshes new set of data from SDI chain.

4 When $\overline{OE}$ is at low level the output terminals Out 0 to Out 15 respond to data in the latch circuits, either '1' for ON or '0' for OFF.

5 When $\overline{OE}$ is at high level, all output terminals are switched OFF.

Table 10: Truth table

| CLOCK | LE | $SDI_0$ ..... $SDI_7$ ..... $SDI_{15}$ | SH | Auto power-up | OUTn |
|---|---|---|---|---|---|
| _\|¯ | H | All = L | Active | Not active | OFF |
| _\|¯ | L | No change | No change | No change | No change |
| _\|¯ | H | One or more = H | Not active | Active | X |

At the power-up the device starts in shut-down mode.

Figure 8: Clock, serial-in, serial-out

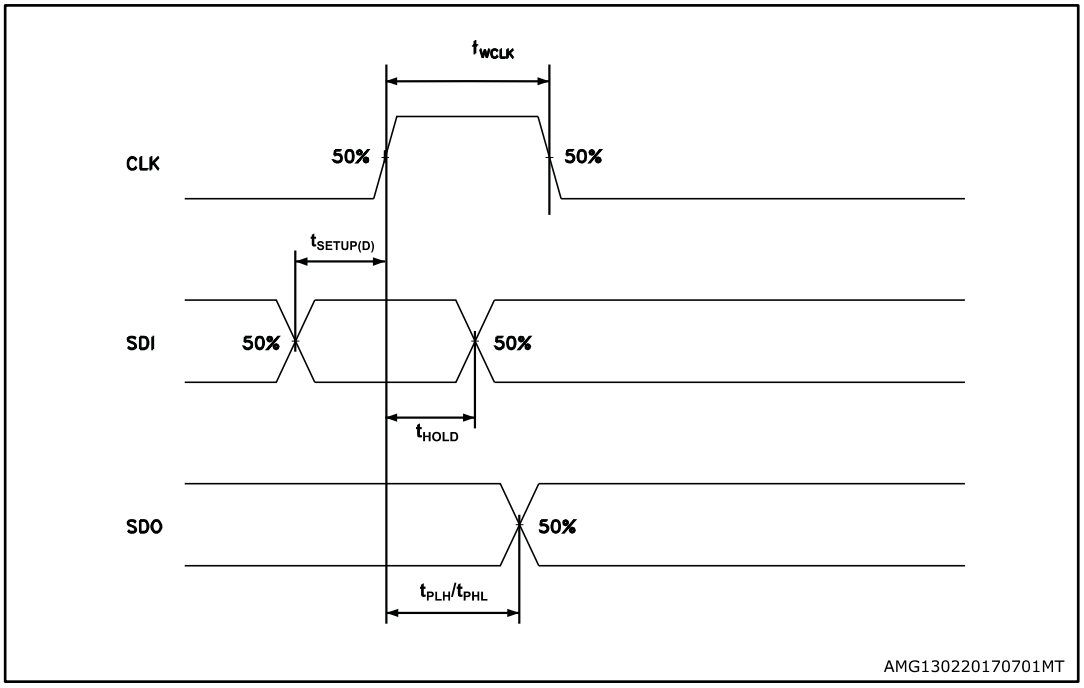


**Figure 9: Clock, serial-in, latch, enable, outputs**

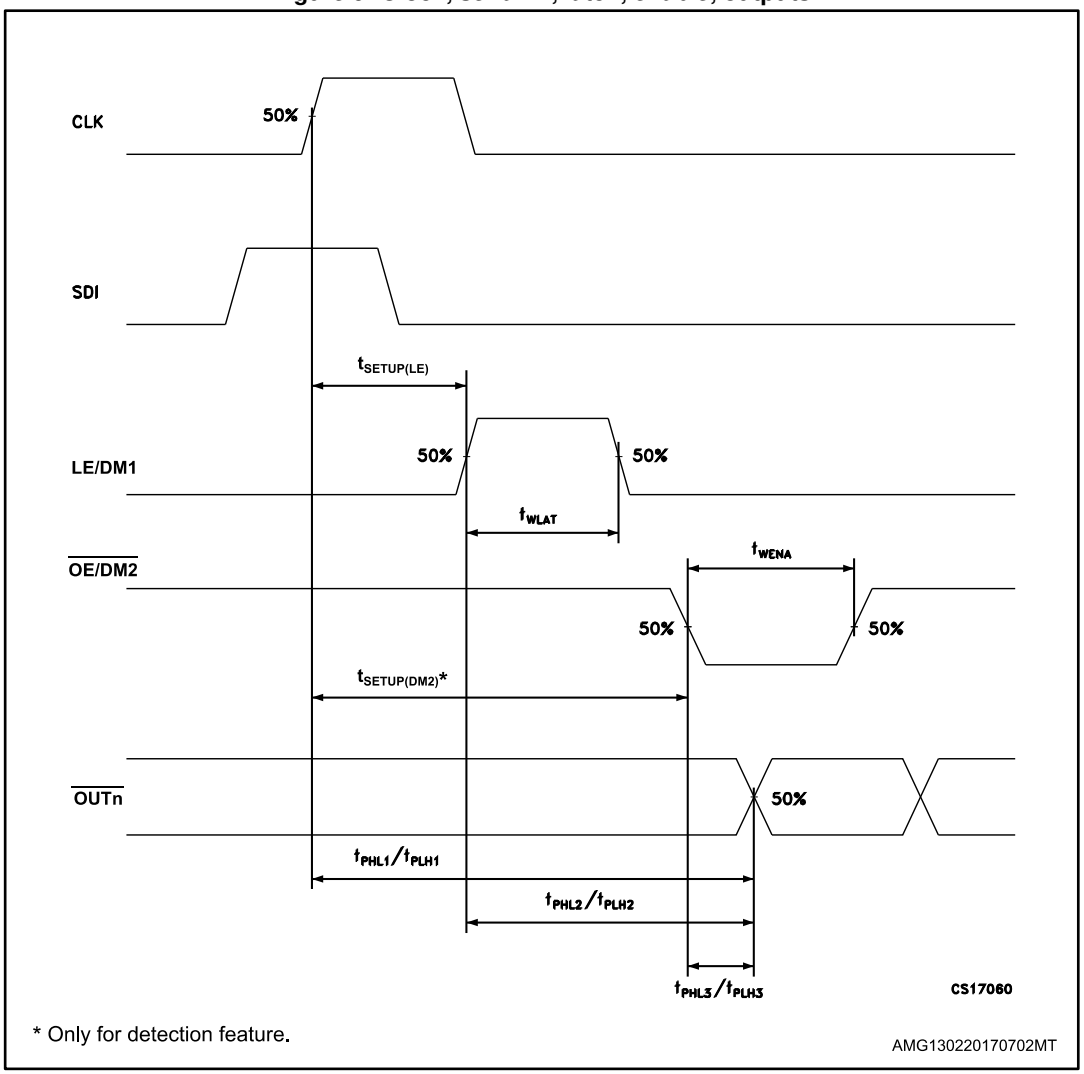
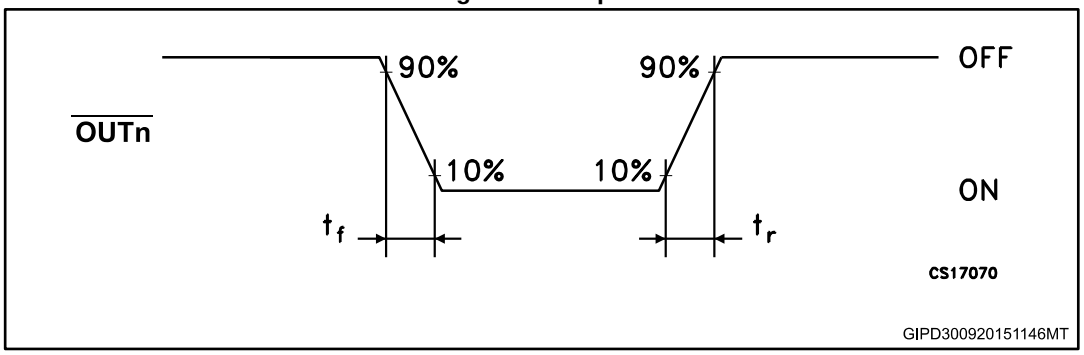



**Figure 10: Outputs**



# 6 Typical characteristics

**Figure 11: Output current-R-EXT resistor**

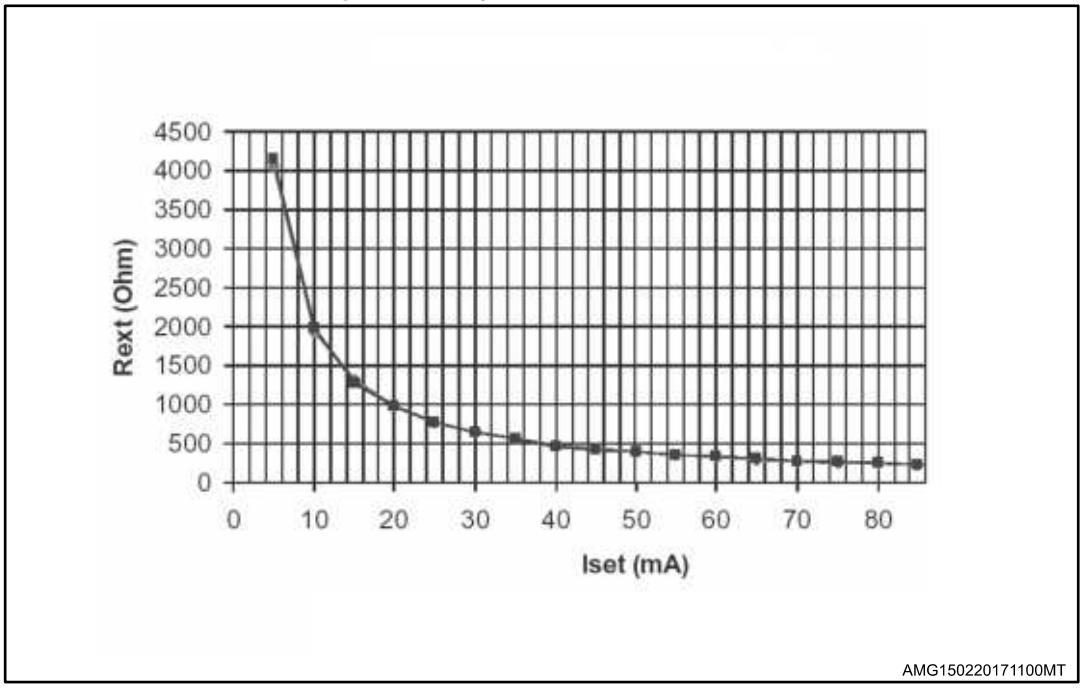



**Table 11: Output current-R-EXT resistor**

| R-EXT (Ω) | Output current (mA) |
|---|---|
| 976 | 20 |
| 780 | 25 |
| 652 | 30 |
| 560 | 35 |
| 488 | 40 |
| 433 | 45 |
| 389 | 50 |
| 354 | 55 |
| 325 | 60 |
| 300 | 65 |
| 278 | 70 |
| 259 | 75 |
| 241 | 80 |
| 229 | 85 |
| 215 | 90 |

**Figure 12: Output current vs ± $\Delta I_{OL}$(%)**

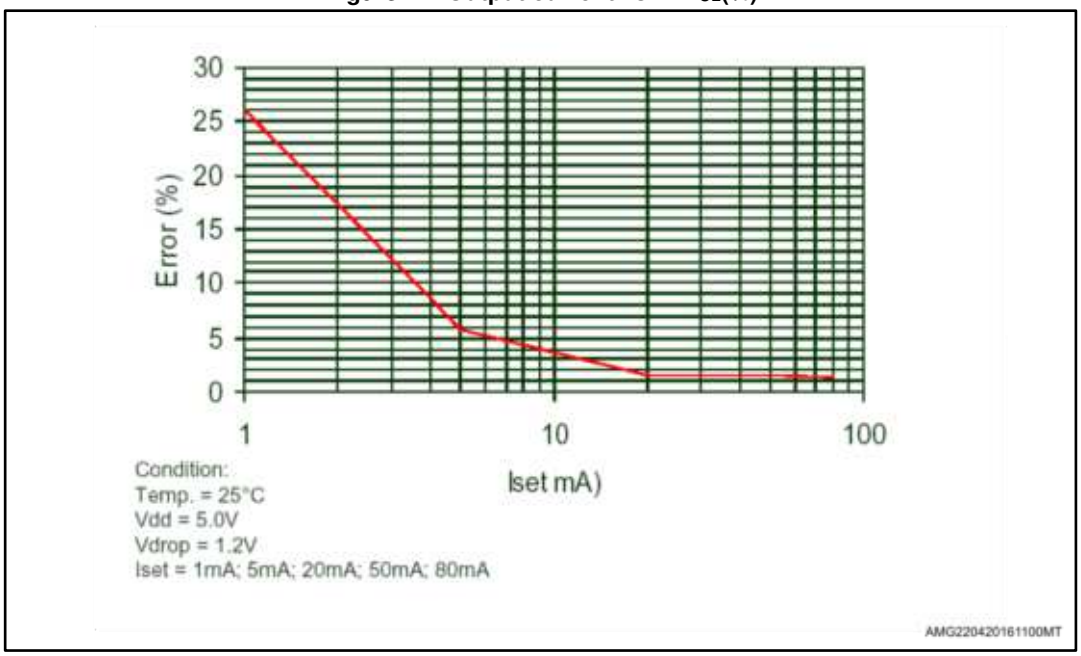
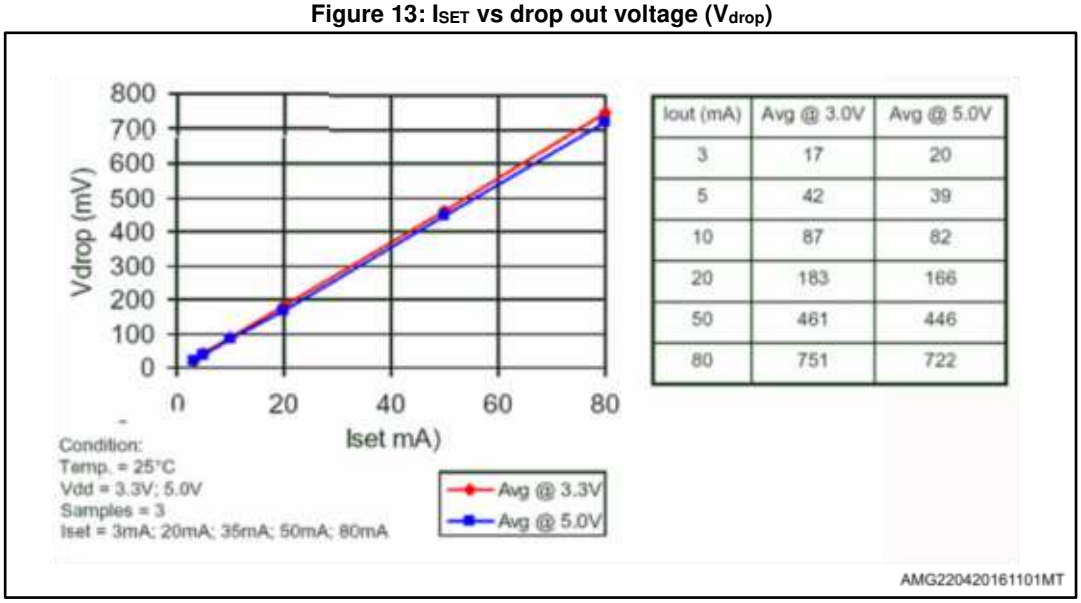



**Figure 13: $I_{SET}$ vs drop out voltage ($V_{drop}$)**




| Iout (mA) | Avg @ 3.0V | Avg @ 5.0V |
|---|---|---|
| 3 | 17 | 20 |
| 5 | 42 | 39 |
| 10 | 87 | 82 |
| 20 | 183 | 166 |
| 50 | 461 | 446 |
| 80 | 751 | 722 |

**Figure 14: $I_{DD}$ ON\OFF**

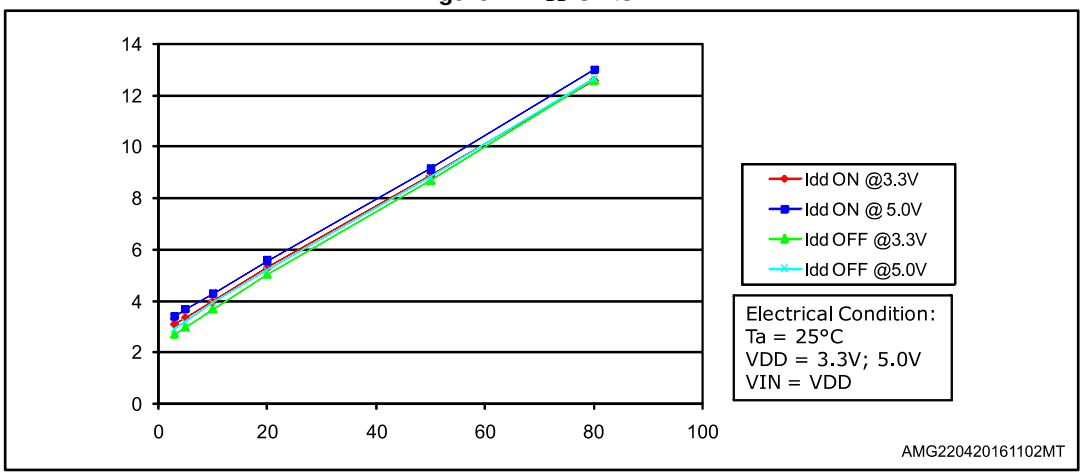
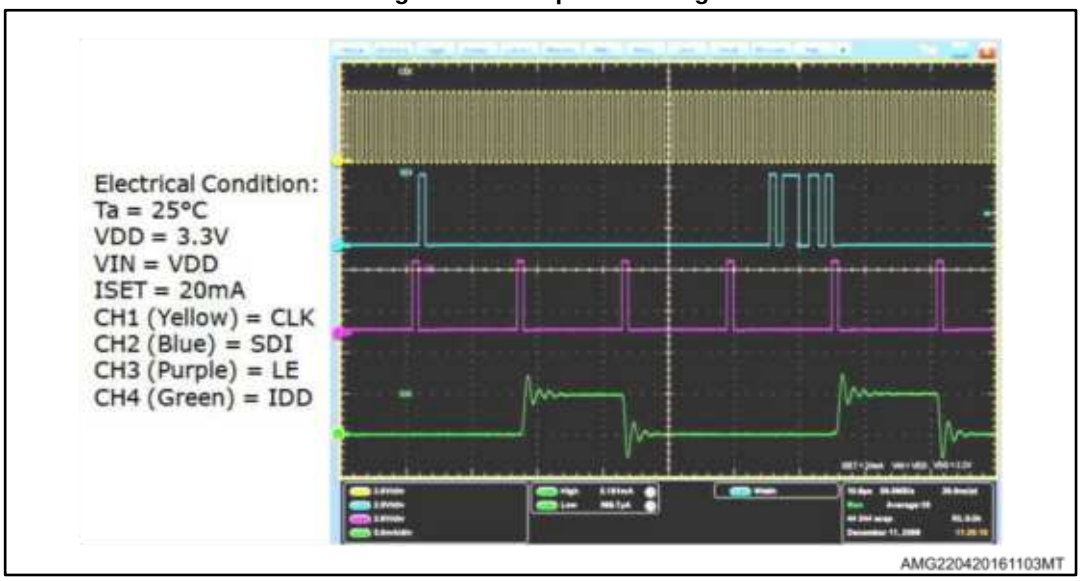
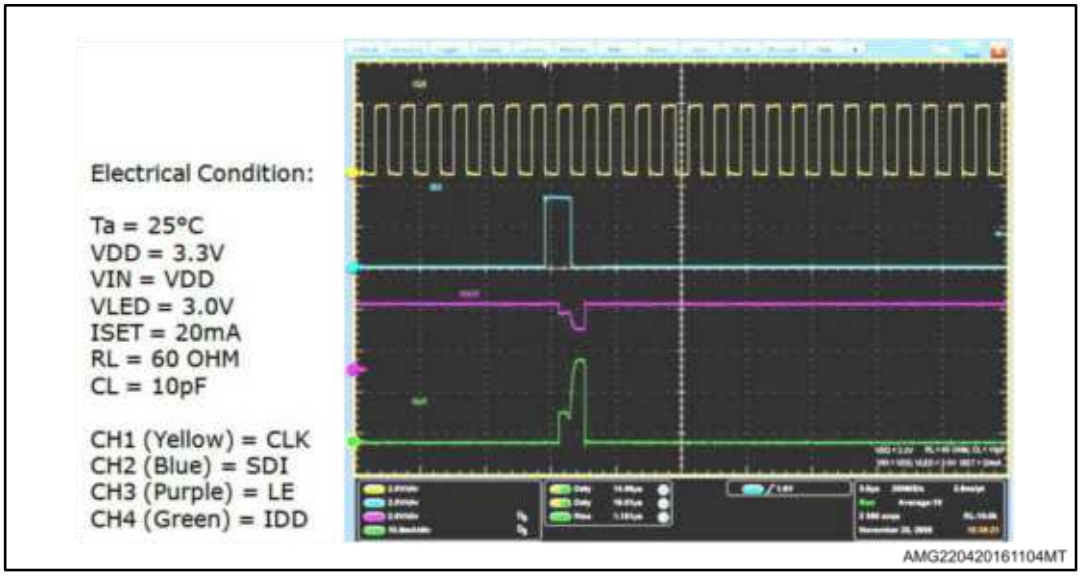



**Figure 15: Auto power saving**




Auto power-saving feature minimizes the quiescent current if no active data is detected on the latches and auto-power-up the device at fist active data latched.

**Figure 16: First output ON after switching from auto power saving to normal mode operating condition**




When the device goes from auto power saving to normal operative condition, the first output that switch ON shows TON condition as seen in the plot above.

# 7 Test circuit

Figure 17: DC characteristic

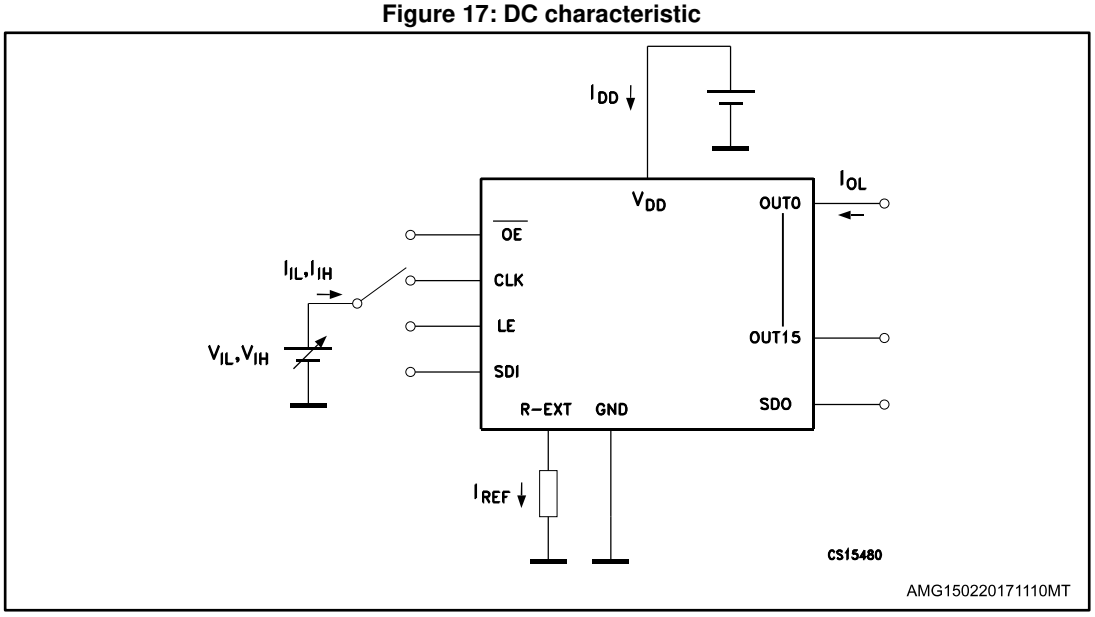



Figure 18: AC characteristic

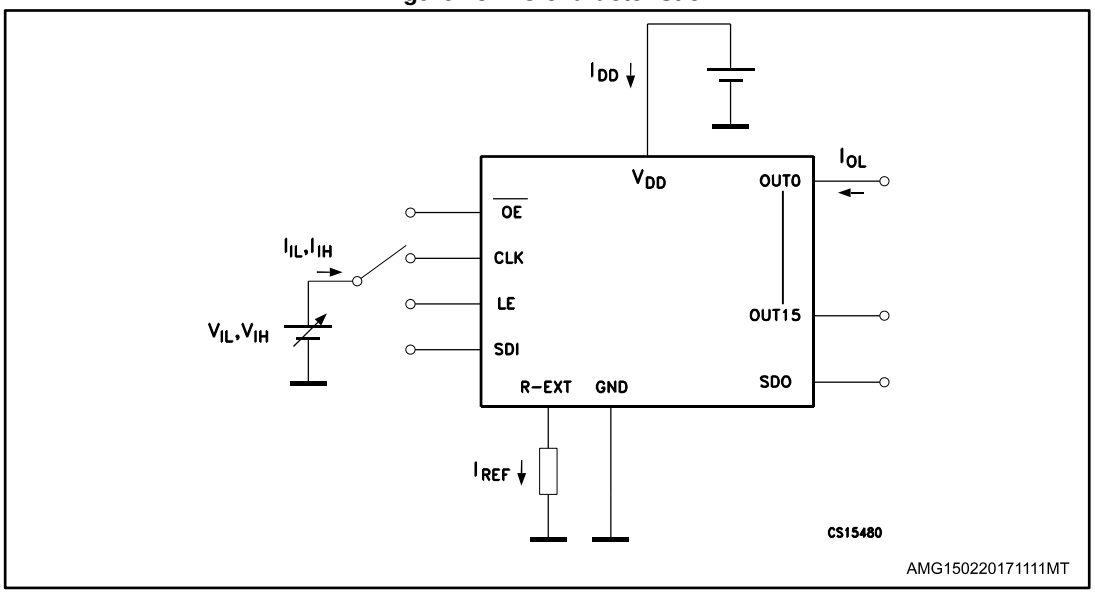
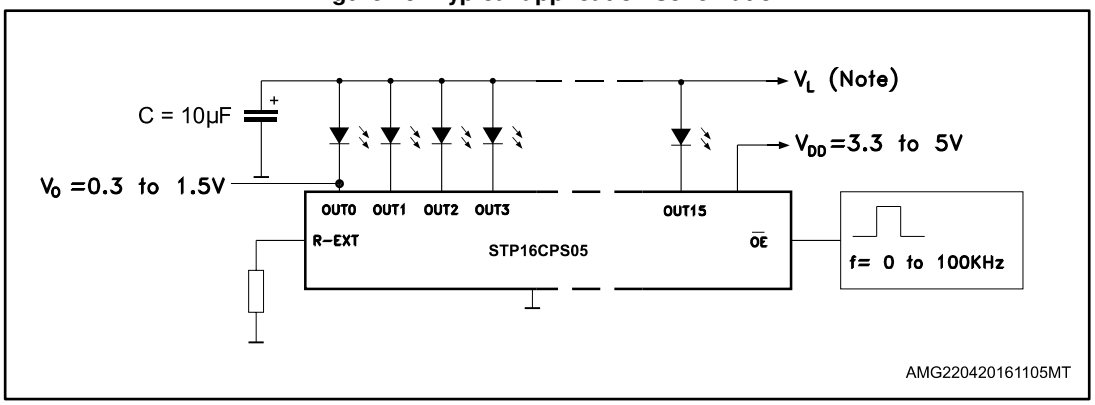


**Figure 19: Typical application schematic**




$V_L$ will be determined by the $V_F$ of the LEDs.

**Figure 20: Turn ON output current characteristics(1)**

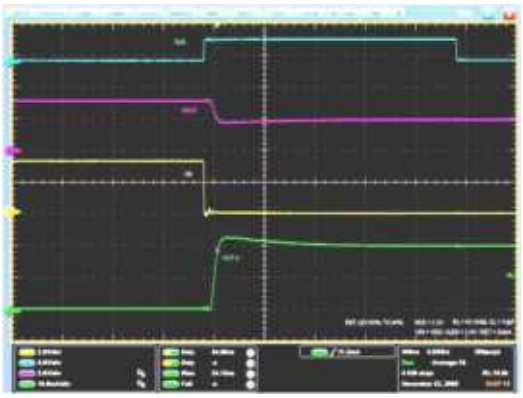
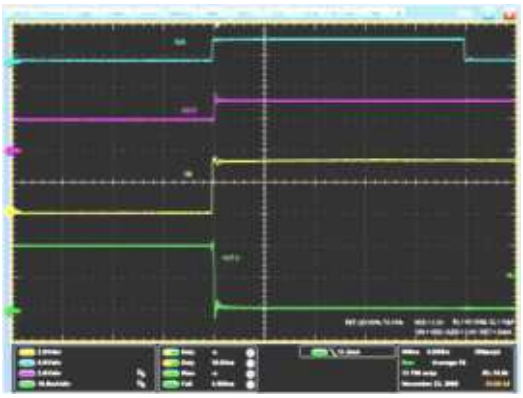



**Figure 21: Turn OFF output current characteristics(2)**




**Notes:**

(1) Reference level for the $T_{ON}$ characteristics is 50 % of OE signal to 90 % of output current.

(2) Reference level for the $T_{OFF}$ characteristics is 50 % of OE signal to 10 % of output current.

# 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 8.1 QSOP-24 package information

**Figure 22: QSOP-24 package outline**

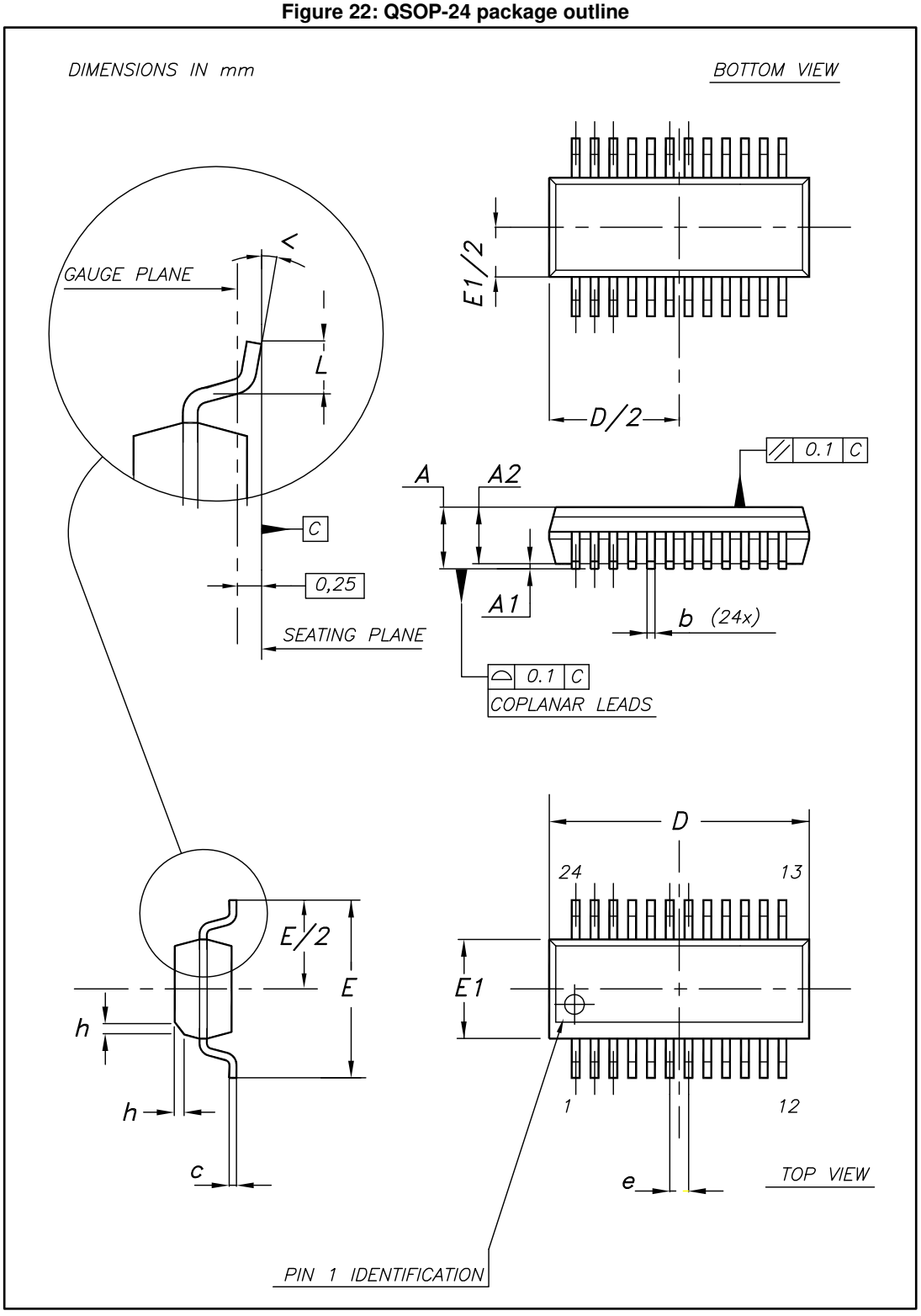


Table 12: QSOP-24 mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 1.54 | 1.62 | 1.73 |
| A1 | 0.10 | 0.15 | 0.25 |
| A2 | | 1.47 | |
| b | 0.20 | | 0.31 |
| c | 0.17 | | 0.254 |
| D | 8.56 | 8.66 | 8.76 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.91 | 4.01 |
| e | | 0.635 | |
| L | 0.40 | 0.635 | 0.89 |
| h | 0.25 | 0.33 | 0.41 |
| < | 0° | | 8° |

## 8.2 SO-24 package information

**Figure 23: SO-24 package outline**

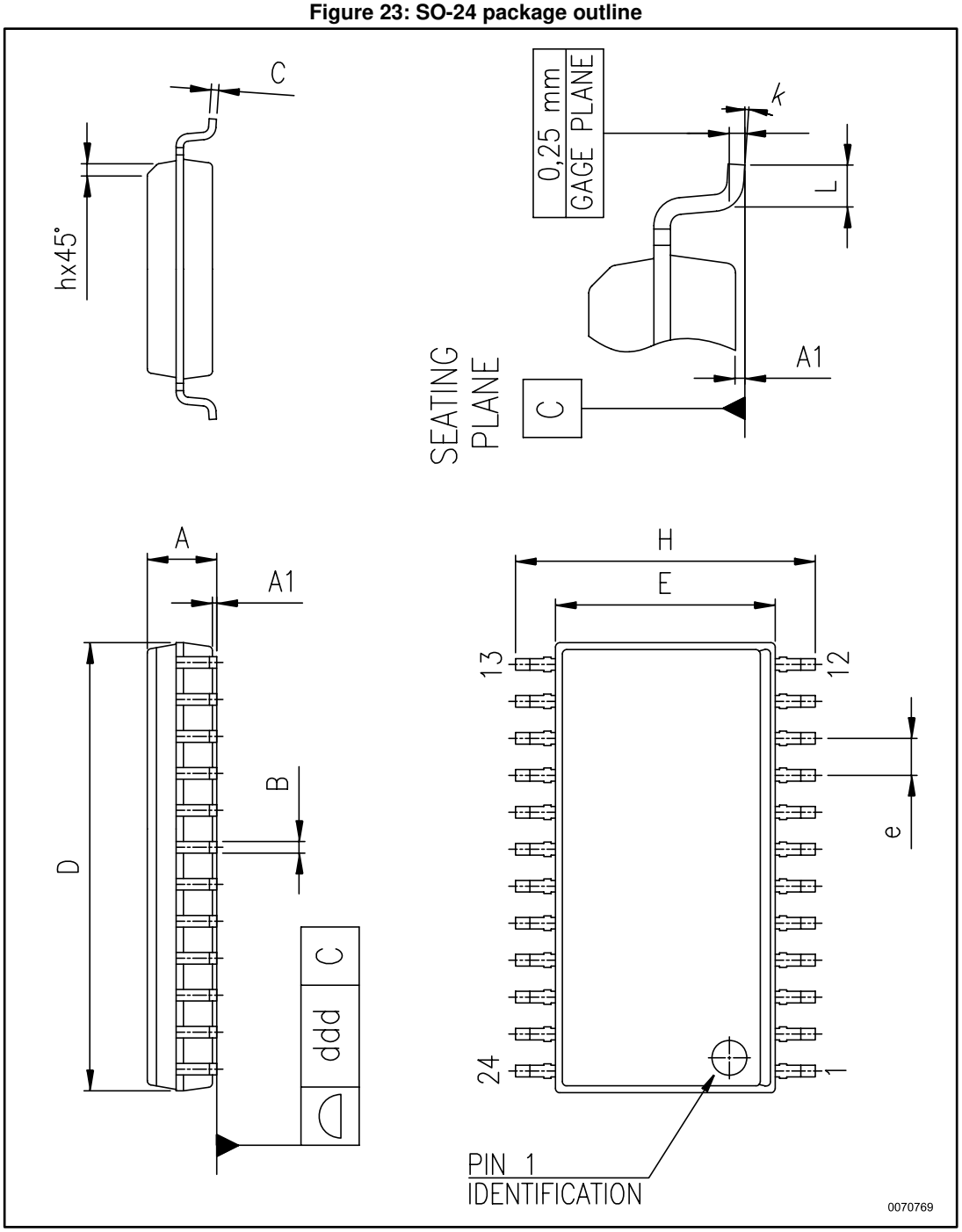


Table 13: SO-24 mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.35 | | 2.65 |
| A1 | 0.10 | | 0.30 |
| B | 0.33 | | 0.51 |
| C | 0.23 | | 0.32 |
| D | 15.20 | | 15.60 |
| E | 7.40 | | 7.60 |
| e | | 1.27 | |
| H | 10.00 | | 10.65 |
| h | 0.25 | | 0.75 |
| L | 0.40 | | 1.27 |
| k | 0 | | 8 |
| ddd | | | 0.10 |

## 8.3 TSSOP24 package information

Figure 24: TSSOP24 package outline

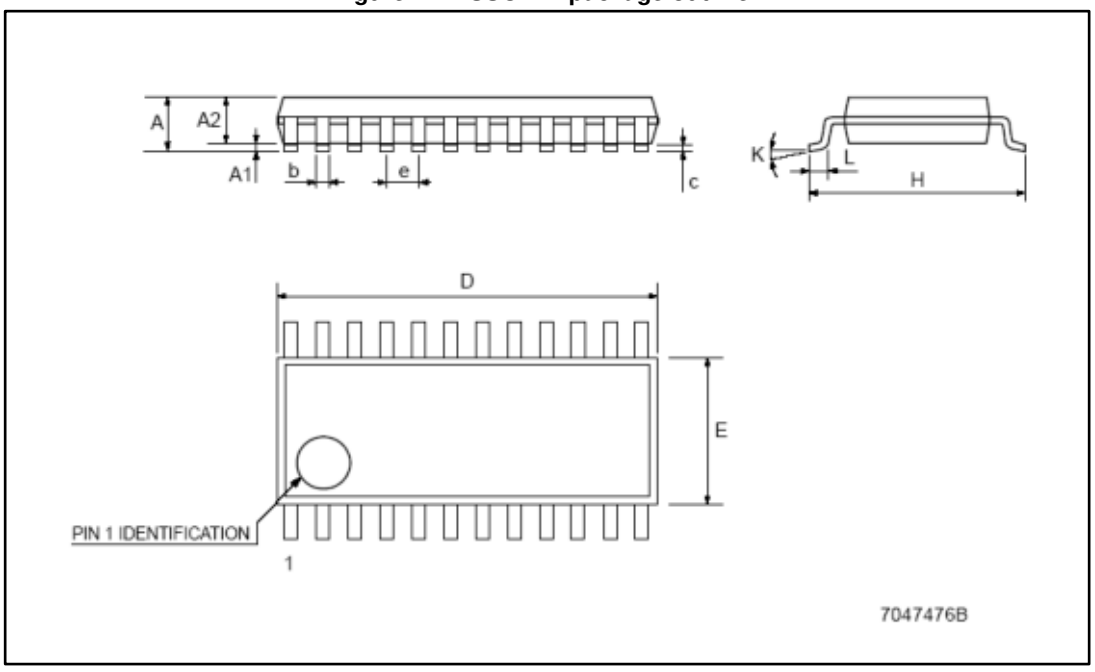


Table 14: TSSOP24 mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.1 |
| A1 | 0.05 | | 0.15 |
| A2 | | 0.9 | |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 7.7 | | 7.9 |
| E | 4.3 | | 4.5 |
| e | | 0.65 BSC | |
| H | 6.25 | | 6.5 |
| K | 0° | | 8° |
| L | 0.50 | | 0.70 |

## 8.4 TSSOP24 exposed pad package information

**Figure 25: TSSOP24 exposed pad package outline**

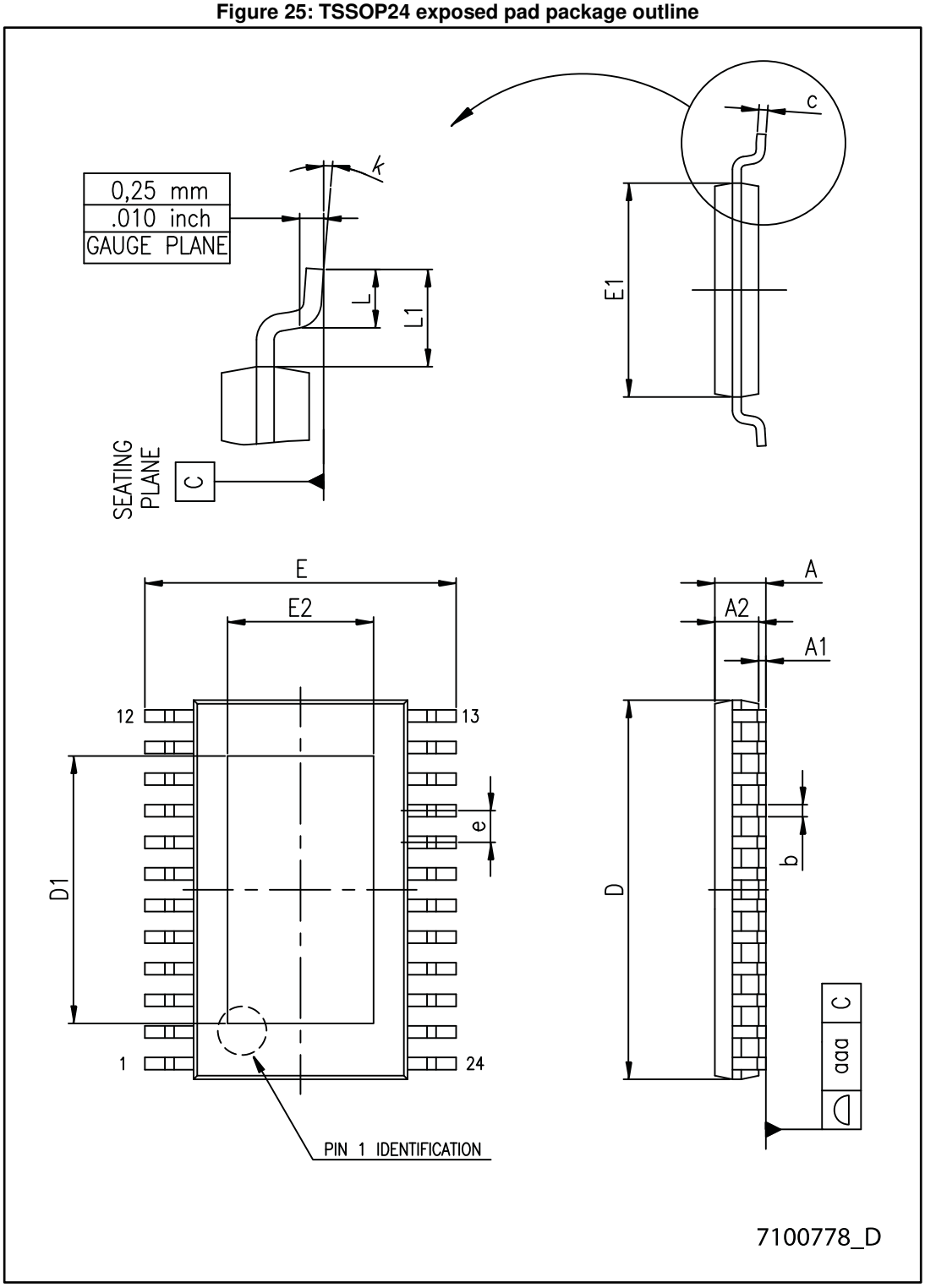


Table 15: TSSOP24 exposed pad mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.20 |
| A1 | | | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 7.70 | 7.80 | 7.90 |
| D1 | 4.80 | 5.00 | 5.2 |
| E | 6.20 | 6.40 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| E2 | 3.00 | 3.20 | 3.40 |
| e | | 0.65 | |
| L | 0.45 | 060 | 075 |
| L1 | | 1.00 | |
| k | 0° | | 8° |
| aaa | | | 0.10 |

## 8.5 TSSOP24, TSSOP24 exposed pad and SO-24 packing information

**Figure 26: TSSOP24, TSSOP24 exposed pad and SO-24 reel outline**

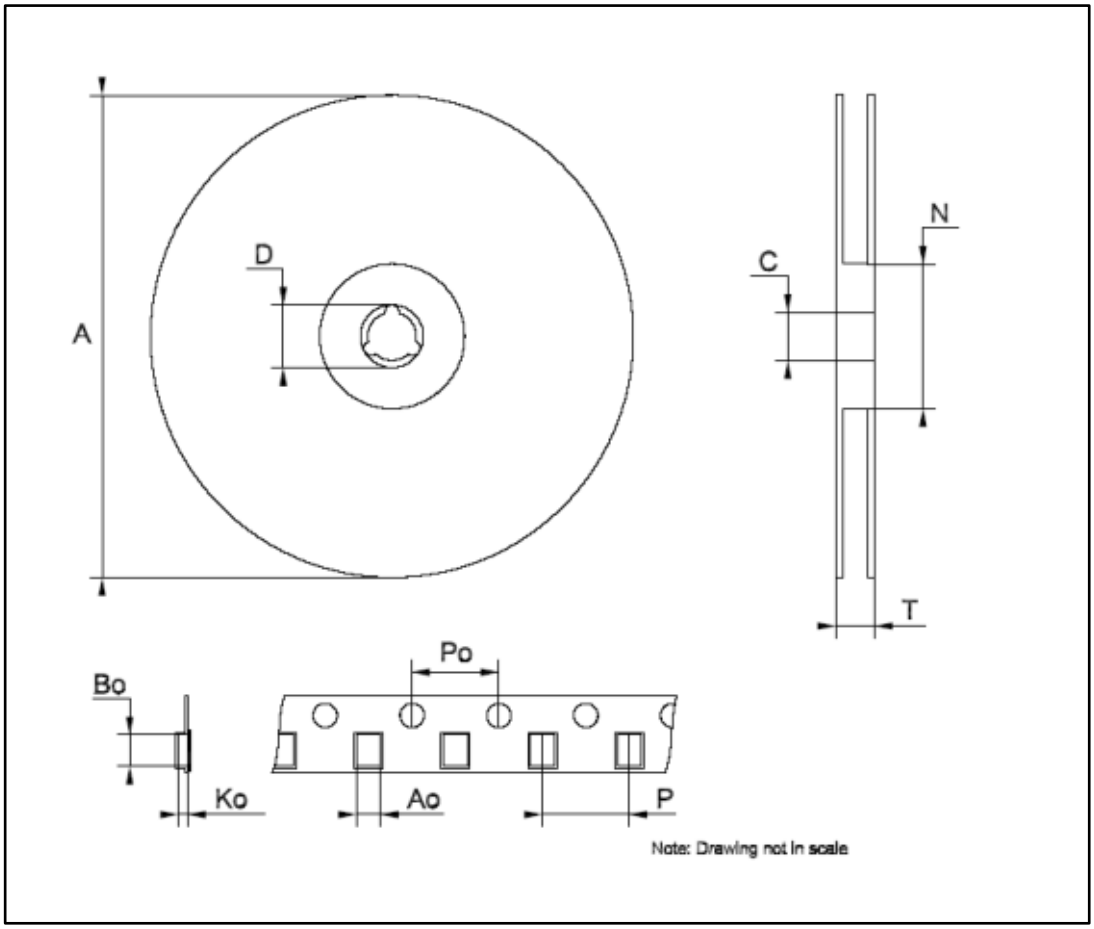



**Table 16: TSSOP24 and TSSOP24 exposed pad tape and reel mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | - | 330 |
| C | 12.8 | - | 13.2 |
| D | 20.2 | - | |
| N | 60 | - | |
| T | | - | 22.4 |
| Ao | 6.8 | - | 7 |
| Bo | 8.2 | - | 8.4 |
| Ko | 1.7 | - | 1.9 |
| Po | 3.9 | - | 4.1 |
| P | 11.9 | - | 12.1 |

Table 17: SO-24 tape and reel mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | - | 330 |
| C | 12.8 | - | 13.2 |
| D | 20.2 | - | |
| N | 60 | - | |
| T | | - | 30.4 |
| Ao | 10.8 | - | 11.0 |
| Bo | 15.7 | - | 15.9 |
| Ko | 2.9 | - | 3.1 |
| Po | 3.9 | - | 4.1 |
| P | 11.9 | - | 12.1 |

# 9 Revision history

Table 18: Document revision history

| Date | Revision | Changes |
|---|---|---|
| 28-Jul-2006 | 1 | First release |
| 22-Dec-2006 | 2 | Final datasheet |
| 17-May-2007 | 3 | Updated Table 8 on page 8 |
| 10-Jul-2007 | 4 | Updated Table 9: Truth table on page 11 |
| 28-Feb-2008 | 5 | Updated Table 19: TSSOP24 exposed pad on page 25<br>Added QSOP-24 package information<br>Table 14 and Figure 20 on page 21 |
| 19-Jan-2010 | 6 | Updated Table 6 on page 6 |
| 17-Jun-2014 | 7 | Updated Section 8: Package mechanical data.<br>Added Section 9: Packaging mechanical data.<br>Minor text changes. |
| 24-Mar-2017 | 8 | Updated *Figure 5: "SDO terminal"*, *Figure 8: "Clock, serial-in, serial-out"*, *Figure 9: "Clock, serial-in, latch, enable, outputs"* and *Section 8.1: "QSOP-24 package information"*.<br>Minor text changes. |

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