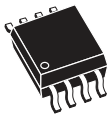
M41T82, M41T83

Serial I²C bus real-time clock (RTC) with battery switchover

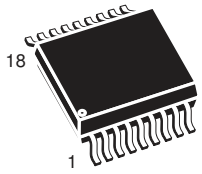
Datasheet - production data



QFN16 (4 mm x 4 mm)



SO8 (4.90 mm x 3.90 mm)



SOX18, embedded crystal
(11.61 mm x 7.62 mm)

Features

- Ultra-low battery supply current of 365 nA
- Factory-calibrated accuracy of ±5 ppm typical after 2 reflows (SOX18)
  - Much better accuracies achievable using built-in programmable analog and digital calibration circuits
- 2.0 V to 5.5 V clock operating voltage
- Counters for tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, year, and century
- Automatic switchover and reset output circuitry (fixed reference)
  - M41T83S: V_{CC} = 3.00 V to 5.50 V
  - M41T83R: V_{CC} = 2.70 V to 5.50 V
  - M41T83Z: V_{CC} = 2.38 V to 5.50 V
- Serial interface supports I²C bus (400 kHz protocol)
- Programmable alarm with interrupt function (valid even during battery backup mode)
- Optional 2nd programmable alarm available
- Square wave output defaults to 32 KHz on power-up (M41T83 only)
- RESET ($\overline{RST}$) output
- Watchdog timer
- Programmable 8-bit counter/timer
- 7 bytes of battery-backed user SRAM
- Battery low flag
- Low operating current of 80 µA
- Oscillator stop detection
- Battery or SuperCap™ backup
- Operating temperature of –40 °C to 85 °C
- Package options
  - a 16-lead QFN (M41T83)
  - an 8-lead SOIC (M41T82) or
  - an 18-lead embedded crystal SOIC (M41T83)
- RoHS compliance: lead-free components are compliant with the RoHS directive

This is information on a product in full production. www.st.com

Contents

1 **Description** 6

2 **Operation** 12

2.1 2-wire bus characteristics 13

2.1.1 Bus not busy 13

2.1.2 Start data transfer 13

2.1.3 Stop data transfer 13

2.1.4 Data valid 13

2.1.5 Acknowledge 14

2.2 Read mode 15

2.3 Write mode 17

2.4 Data retention and battery switchover (V_{SO} = V_{RST}) 18

2.5 Power-on reset (t_{rec}) 18

3 **Clock operation** 19

3.1 Clock data coherency 20

3.1.1 Example of incoherency 20

3.1.2 Accessing the device 21

3.2 Halt bit (HT) operation 21

3.2.1 Power-down time-stamp 22

3.3 Real-time clock accuracy 27

3.4 Clock calibration 28

3.4.1 Digital calibration (periodic counter correction) 28

3.4.2 Analog calibration (programmable load capacitance) 31

3.4.3 Pre-programmed calibration value 32

3.5 Setting the alarm clock registers 36

3.6 Optional second programmable alarm and user SRAM 37

3.7 Watchdog timer 37

3.8 8-bit (countdown) timer 38

3.8.1 M41T83 timer interrupt/output 38

3.8.2 Timer flag (TF) 40

3.8.3 Timer interrupt enable (TIE, M41T83 only) 40

3.8.4 Timer enable (TE) 40

3.8.5 TD1/0 40
3.9 Square wave output (M41T83 only) 41
3.10 Battery low warning 42
3.11 Century bits 43
3.12 Oscillator fail detection 44
3.13 Oscillator fail interrupt enable (M41T83 only) 44
3.14 $\overline{IRQ1}$/FT/OUT pin, frequency test, interrupts and the OUT bit (M41T83 only) 44
3.14.1 Active mode operation on V_{CC} 46
3.14.2 Backup mode 47
3.15 FT/$\overline{RST}$ pin, frequency test and reset output pin (M41T82 only) 48
3.16 Initial power-on defaults 48
3.17 OTP bit operation (M41T83 in SOX18 package only) 49

4 Maximum ratings 50

5 DC and AC parameters 51

6 Package mechanical data 56
6.1 QFN16 package information 56
6.2 SOX18 package information 59
6.3 SO8 package information 60
6.4 Carrier tape information 61

7 Part numbering 62

8 Revision history 63

List of tables

Table 1. Signal names . . . 8
Table 2. M41T82 clock/control register map (32 bytes) . . . 23
Table 3. Key to *Table 2: M41T82 clock/control register map (32 bytes)* . . . 24
Table 4. M41T83 clock/control register map (32 bytes) . . . 25
Table 5. Key to *Table 4: M41T83 clock/control register map (32 bytes)* . . . 26
Table 6. Digital calibration values . . . 30
Table 7. Analog calibration values . . . 32
Table 8. Alarm repeat modes . . . 37
Table 9. Watchdog register . . . 38
Table 10. Timer control register map . . . 39
Table 11. Timer interrupt operation in free-running mode (with $\overline{TI}$/TP = 1) . . . 39
Table 12. Timer source clock frequency selection (244.1 µs to 4.25 hrs) . . . 40
Table 13. Square wave output frequency . . . 41
Table 14. Priority for $\overline{IRQ1}$/FT/OUT pin when operating on V_{CC} . . . 46
Table 15. Priority for $\overline{IRQ1}$/FT/OUT pin when operating in backup mode . . . 47
Table 16. Initial power-on default values (part 1) . . . 48
Table 17. Initial power-up default values (part 2) . . . 48
Table 18. Absolute maximum ratings . . . 50
Table 19. Operating and AC measurement conditions . . . 51
Table 20. Capacitance . . . 51
Table 21. DC characteristics . . . 52
Table 22. Crystal electrical characteristics . . . 53
Table 23. Oscillator characteristics . . . 53
Table 24. Power down/up trip points DC characteristics . . . 54
Table 25. AC characteristics . . . 55
Table 26. QFN16 – 16-lead, quad, flat package, no lead, 4 x 4 mm package mechanical data . . . 57
Table 27. SOX18 – 18-lead plastic small outline, 300 mils, embedded crystal, package mechanical data . . . 59
Table 28. SO8 – 8-lead plastic small outline (150 mils body width) package mechanical data . . . 60
Table 29. Carrier tape dimensions for QFN16, SOX18, and SO8 packages . . . 61
Table 30. Ordering information . . . 62
Table 31. Document revision history . . . 63

List of figures

Figure 1. M41T82 logic diagram . . . 7
Figure 2. M41T83 logic diagram . . . 7
Figure 3. SO8 (M) connections (M41T82) . . . 9
Figure 4. QFN16 (QA) connections (M41T83) . . . 9
Figure 5. SOX18 (MY) connections (M41T83) . . . 9
Figure 6. M41T82 block diagram . . . 10
Figure 7. M41T82 hardware hookup . . . 10
Figure 8. M41T83 block diagram . . . 11
Figure 9. M41T83 hardware hookup . . . 11
Figure 10. Serial bus data transfer sequence . . . 14
Figure 11. Acknowledgement sequence . . . 14
Figure 12. Slave address location . . . 15
Figure 13. Read mode sequence . . . 16
Figure 14. Alternative read mode sequence . . . 16
Figure 15. Write mode sequence . . . 17
Figure 16. Clock data coherency . . . 20
Figure 17. Internal load capacitance adjustment . . . 27
Figure 18. Crystal accuracy across temperature . . . 32
Figure 19. Clock accuracy vs. on-chip load capacitance . . . 34
Figure 20. Clock divider chain and calibration circuits . . . 35
Figure 21. Crystal isolation example . . . 36
Figure 22. Timer output waveform in free-running mode (with $\overline{TI}$/TP = 1) . . . 39
Figure 23. Battery check . . . 42
Figure 24. Two-bit binary counter (century bits CB1:CB0) . . . 43
Figure 25. IRQ1/FT/OUT output pin circuit . . . 45
Figure 26. Measurement AC I/O waveform . . . 51
Figure 27. I_{CC2} vs. temperature . . . 53
Figure 28. Power down/up mode AC waveforms . . . 54
Figure 29. Bus timing requirement sequence . . . 55
Figure 30. QFN16 – 16-lead, quad, flat package, no lead, 4 x 4 mm body size package outline . . . 56
Figure 31. QFN16 – 16-lead, quad, flat package, no lead, 4 x 4 mm, recommended footprint . . . 57
Figure 32. 32 KHz crystal + QFN16 vs. VSOJ20 mechanical data . . . 58
Figure 33. SOX18 – 18-lead plastic small outline, 300 mils, embedded crystal package outline . . . 59
Figure 34. SO8 – 8-lead plastic small package outline . . . 60
Figure 35. Carrier tape for QFN16, SOX18, and SO8 packages . . . 61

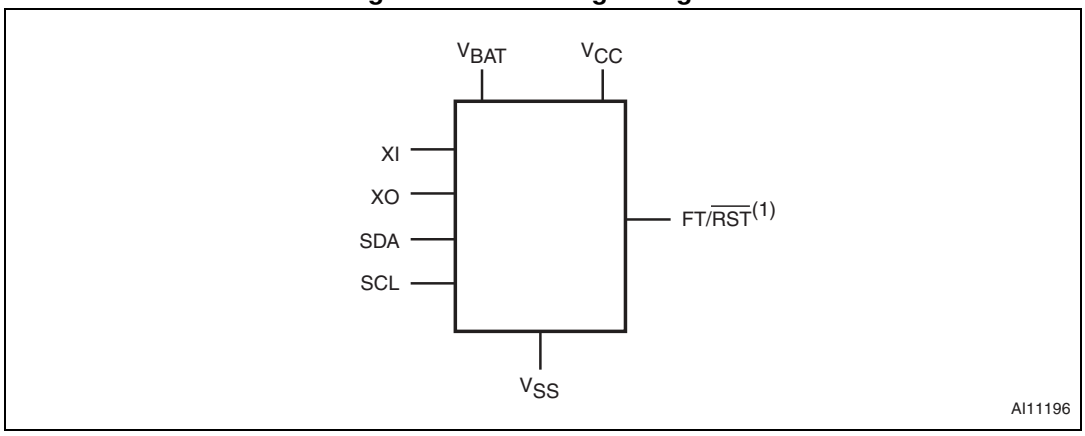
1 Description

The M41T8x are low-power serial I^2C real-time clocks (RTCs) with a built-in 32.768 kHz oscillator (external crystal-controlled for the QFN16 and SO8 packages, embedded crystal for the SOX18 package). Eight bytes of the register map (see *Table 2 on page 23*) are used for the clock/calendar function and are configured in binary-coded decimal (BCD) format. An additional 17 bytes of the register map provide status/control of the two alarms, watchdog, 8-bit counter, and square wave functions. An additional seven bytes are made available as user SRAM.

Addresses and data are transferred serially via a two-line, bidirectional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte. The M41T8x has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the clock operations can be supplied by a small lithium button battery when a power failure occurs.

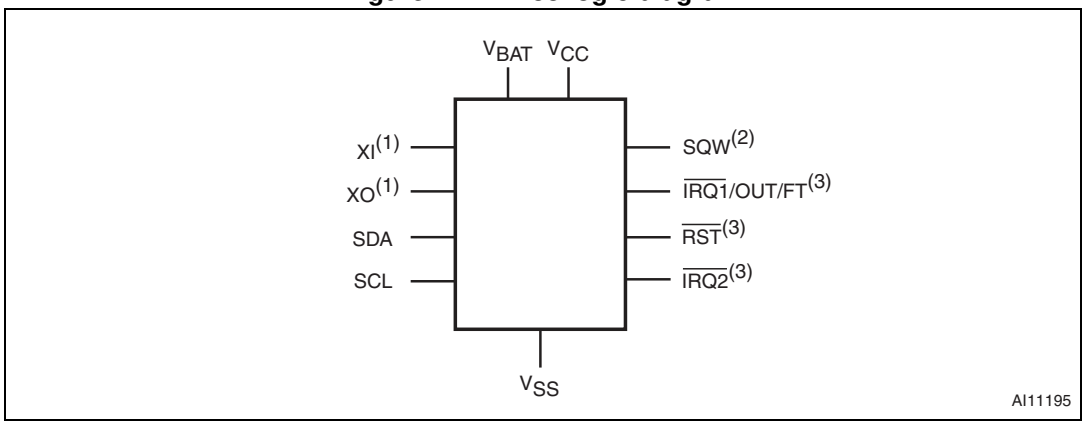
Functions available to the user include a non-volatile, time-of-day clock/calendar, two alarm interrupts, watchdog timer, programmable 8-bit counter, and square wave outputs. The eight clock address locations contain the century, year, month, date, day, hour, minute, second, and tenths/hundredths of a second in 24-hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. The M41T83 is supplied in either a QFN16 or an SOX18, 300 mil SOIC which includes an embedded 32 KHz crystal. The SOX18 package requires only a user-supplied battery to provide non-volatile operation. The M41T82 is available only in an SO8 package.

Figure 1. M41T82 logic diagram



1. Open drain

Figure 2. M41T83 logic diagram



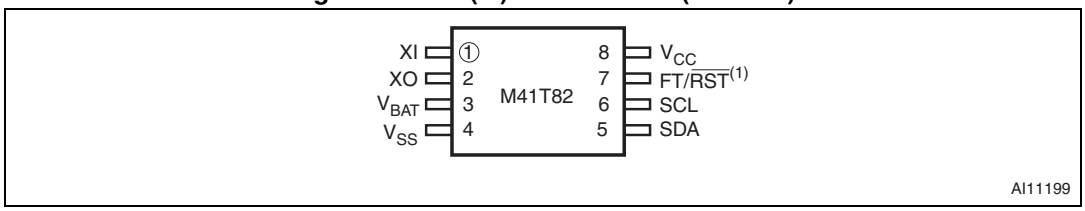
1. For QFN16 package only
2. Defaults to 32 KHz on power-up
3. Open drain

Table 1. Signal names

Symbol	Description
XI(1)	32 KHz oscillator input
XO(1)	32 KHz oscillator output
$\overline{IRQ1}$/OUT/FT(2)	Interrupt 1/output driver/frequency test output (open drain)
SQW(3)	32 KHz programmable square wave output
$\overline{RST}$	Power-on reset output (open drain)
FT/$\overline{RST}$	Frequency test output/power-on reset (open drain - M41T82 only)
$\overline{IRQ2}$(2)	Interrupt for alarm 2 (open drain)
SDA	Serial data address input/output
SCL	Serial clock input
V_{BAT}	Battery supply voltage (tie V_{BAT} to V_{SS} if no battery is connected.)
DU(4)	Do not use
V_{CC}	Supply voltage
V_{SS}	Ground

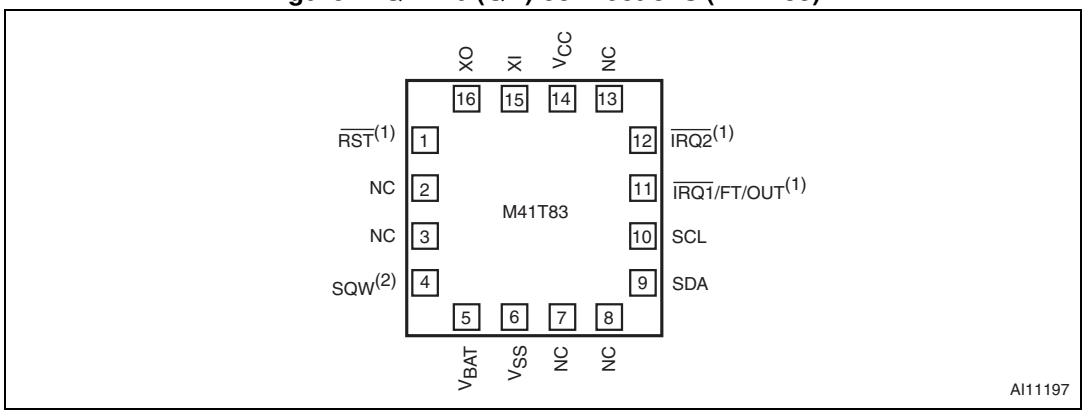
1. For SO8 and QFN16 packages only.
2. For SOX18 and QFN16 packages only.
3. Defaults to 32 KHz on power-up.
4. DU pin must be tied to V_{CC}.

Figure 3. SO8 (M) connections (M41T82)



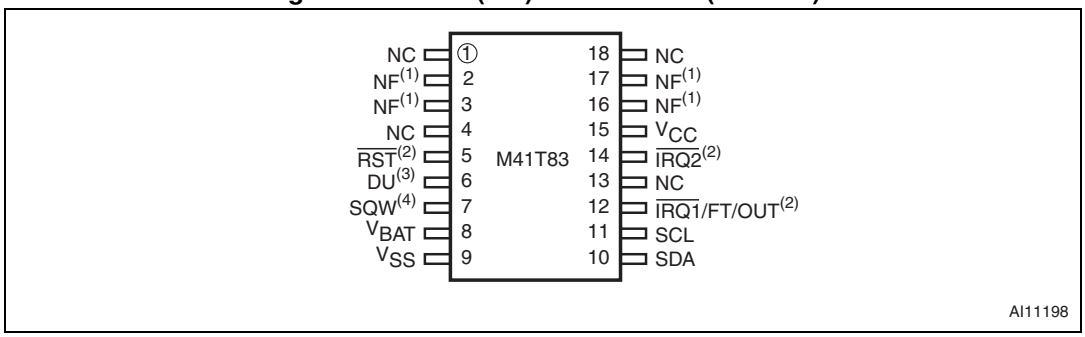
1. Open drain output

Figure 4. QFN16 (QA) connections (M41T83)



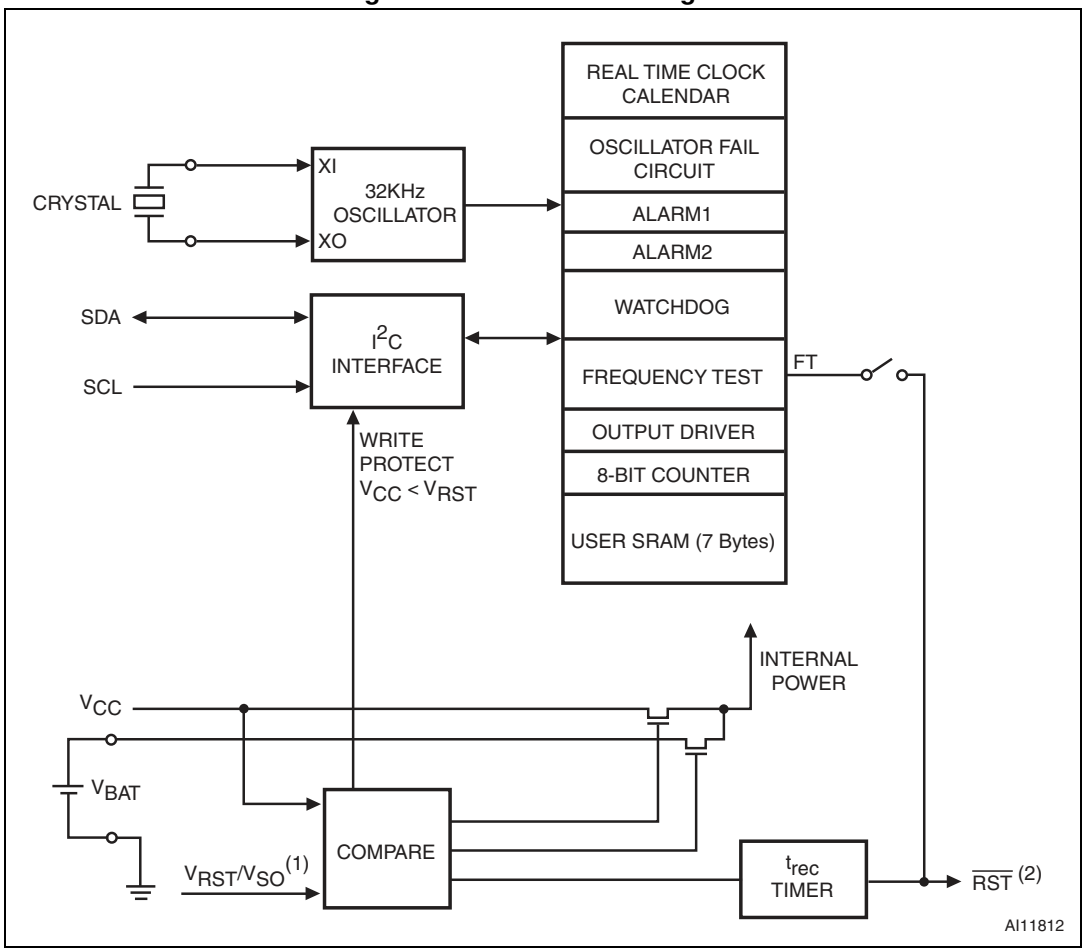
1. Open drain output.
2. Defaults to 32 KHz on power-up.

Figure 5. SOX18 (MY) connections (M41T83)



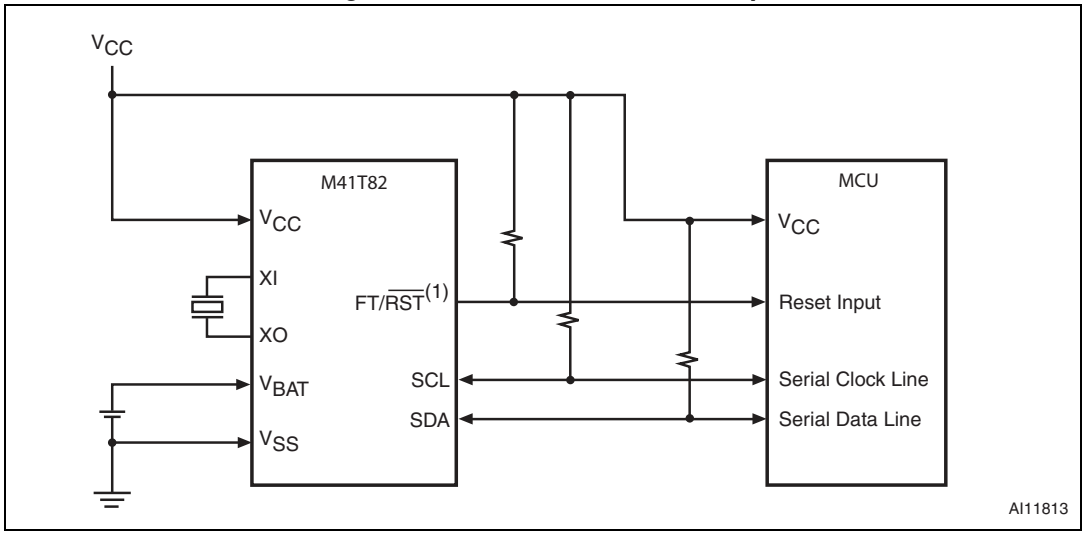
1. NF pins must be tied to V_{SS}. Pins 2 and 3, and 16 and 17 are internally shorted together.
2. Open drain output.
3. Do not use (must be tied to V_{CC}).
4. Defaults to 32 KHz on power-up.

Figure 6. M41T82 block diagram



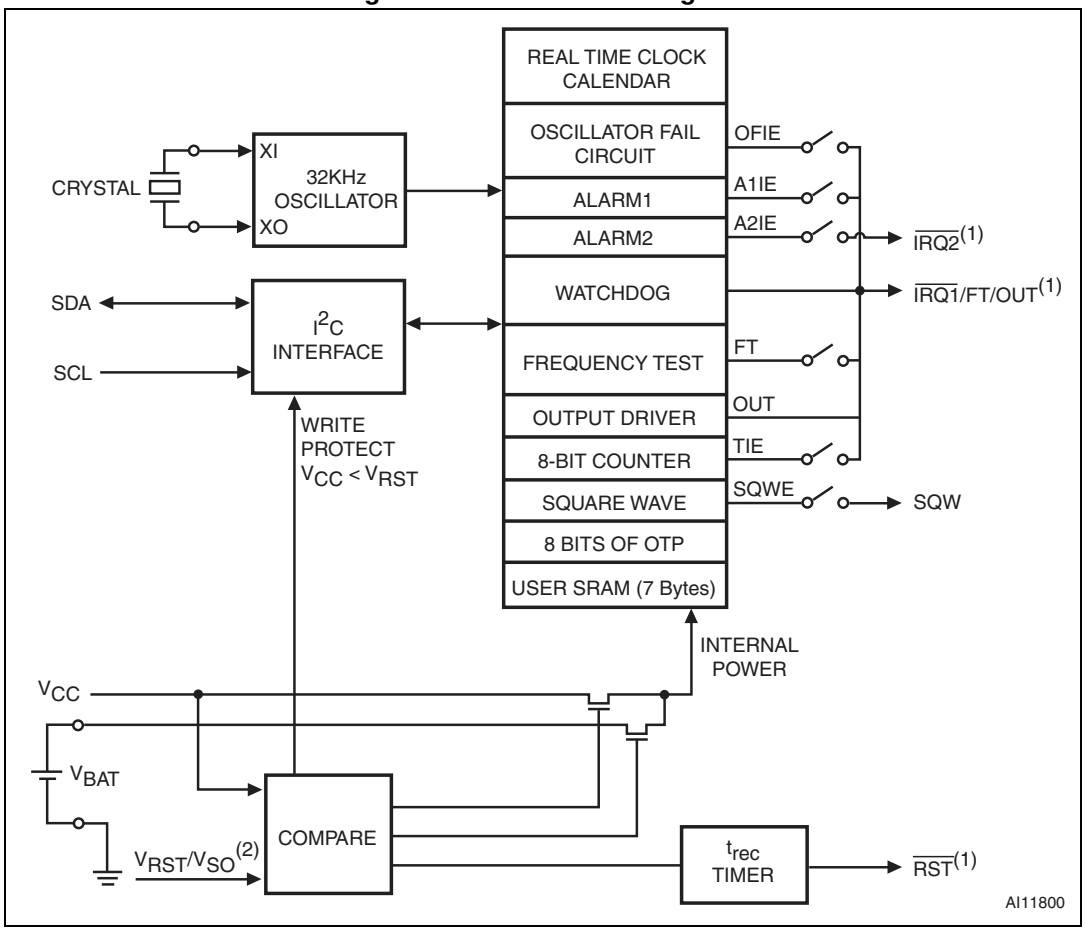
1. $V_{RST} = V_{SO}$ = 2.93 V (S), 2.63 V (R), and 2.32 V (Z).
2. Open drain output.

Figure 7. M41T82 hardware hookup



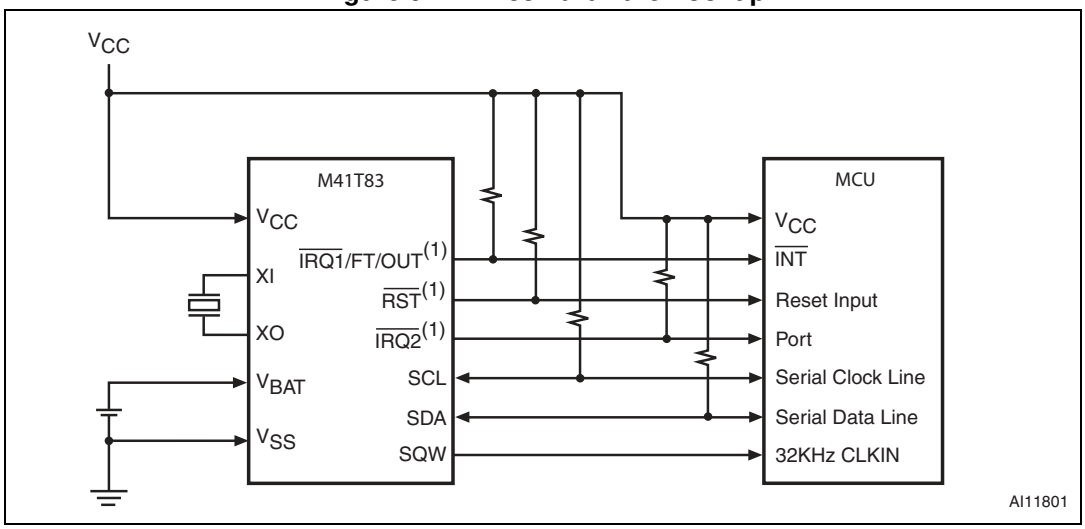
1. Open drain output.

Figure 8. M41T83 block diagram



1. Open drain output.
2. $V_{RST} = V_{SO}$ = 2.93 V (S), 2.63 V (R), and 2.32 V (Z).

Figure 9. M41T83 hardware hookup



1. Open drain output.

2 Operation

The M41T8x clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 32 bytes contained in the device can then be accessed sequentially in the following order:

- 1st byte: tenths/hundredths of a second register
- 2nd byte: seconds register
- 3rd byte: minutes register
- 4th byte: century/hours register
- 5th byte: day register
- 6th byte: date register
- 7th byte: month register
- 8th byte: year register
- 9th byte: digital calibration register
- 10th byte: watchdog register
- 11th - 15th bytes: alarm 1 registers
- 16th byte: flags register
- 17th byte: timer value register
- 18th byte: timer control register
- 19th byte: analog calibration register
- 20th byte: square wave register
- 21st - 25th bytes: alarm 2 registers
- 26th - 32nd bytes: user RAM

The M41T8x clock continually monitors V_{CC} for an out-of-tolerance condition. Should V_{CC} fall below V_{RST}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out-of-tolerance system. The power input will also be switched from the V_{CC} pin to the battery when V_{CC} falls below the battery back-up switchover voltage ($V_{SO} = V_{RST}$). At this time the clock registers will be maintained by the attached battery supply. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}.

2.1 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

2.1.1 Bus not busy

Both data and clock lines remain high.

2.1.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 10. Serial bus data transfer sequence

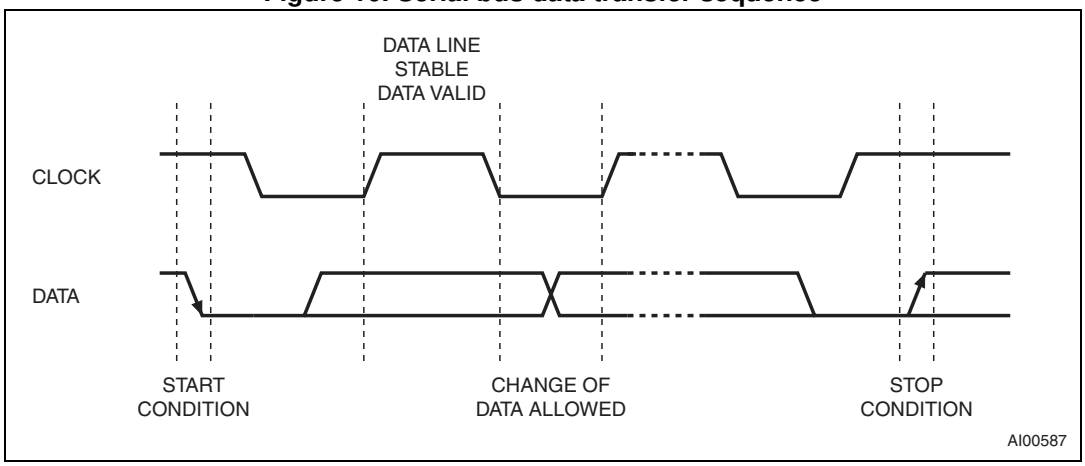
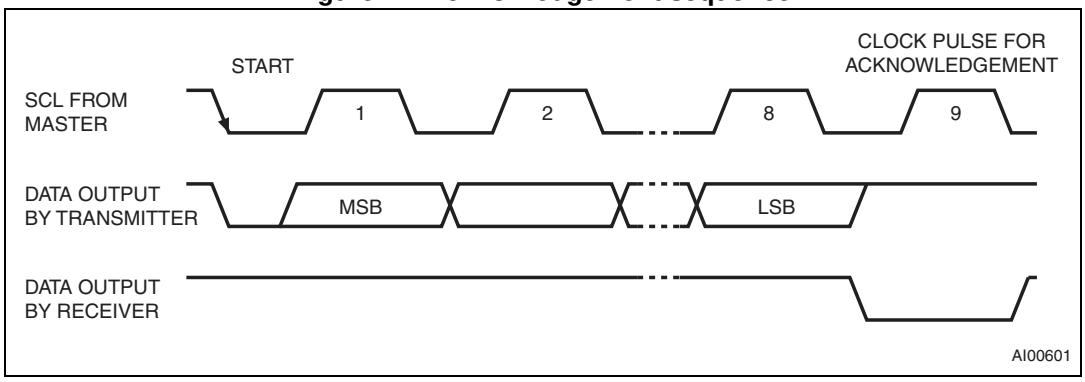


Figure 11. Acknowledgement sequence



2.2 Read mode

In this mode the master reads the M41T8x slave after setting the slave address (see *Figure 13 on page 16*). Following the WRITE mode control bit (R/W = 0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/W = 1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge clock. The M41T8x slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to An+2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter. Most of the registers and memory locations are accessed directly, but the RTC counters are accessed via a set of buffer/transfer registers at addresses 00h to 07h. The counters are not directly read nor written. Instead, at the start of a read or write cycle, the counters are copied into the eight buffer/transfer registers so that the user can read them out sequentially, receiving a coherent set of data, copied from the same instant in time.

An alternate READ mode may also be implemented whereby the master reads the M41T8x slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 14 on page 16*).

Figure 12. Slave address location

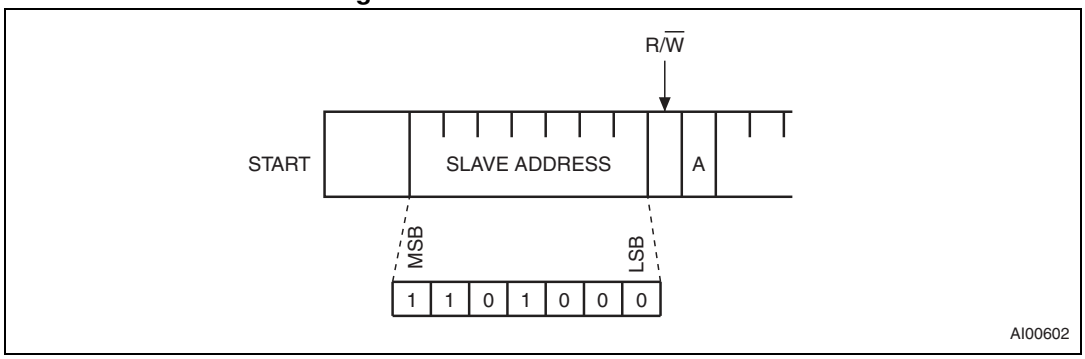


Figure 13. Read mode sequence

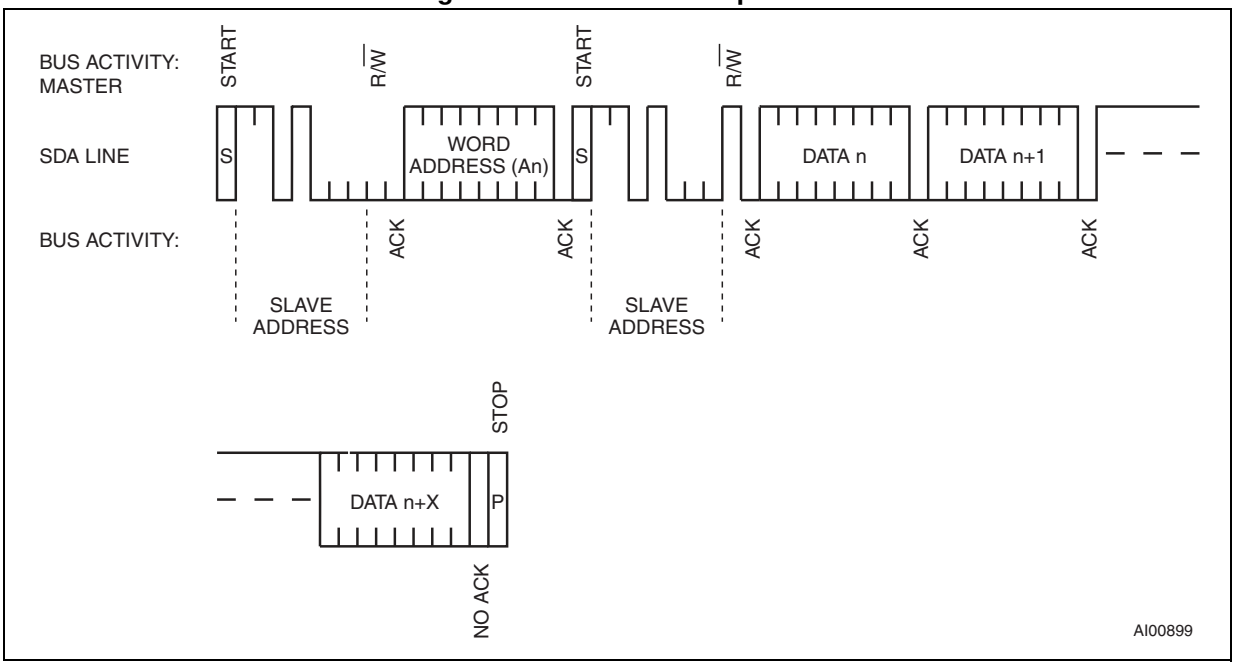
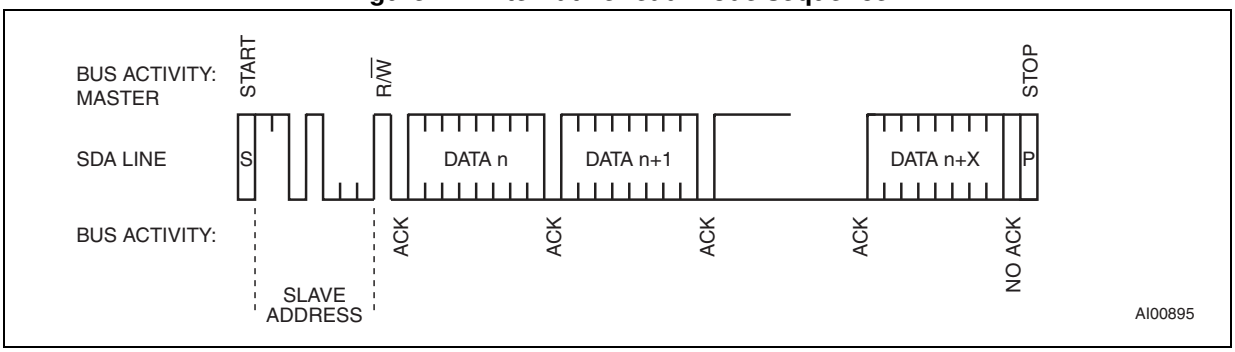


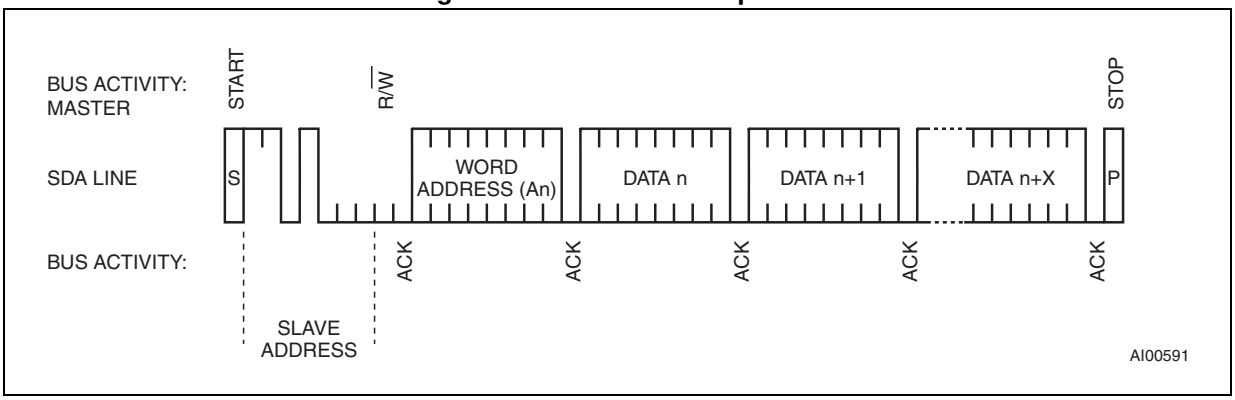
Figure 14. Alternative read mode sequence



2.3 Write mode

In this mode the master transmitter transmits to the M41T8x slave receiver. Bus protocol is shown in *Figure 15*. Following the START condition and slave address, a logic 0 (R/W = 0) is placed on the bus and indicates to the addressed device that word address “An” will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. The M41T8x slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address (see *Figure 12 on page 15*) and again after it has received the word address and each data byte.

Figure 15. Write mode sequence



As in the case of reading, some registers and memory locations are written directly, but the RTC counters are written via a set of eight buffer/transfer registers at addresses 00h to 07h. The user will write the date and time information sequentially, and then, at the end of the I^2C write cycle or when the address pointer increments beyond 07h, the buffer/transfer registers will be copied into the RTC counters. All the time parameters - fractions, seconds, minutes, hours, day, date, month, year, and century bits - are copied simultaneously.

Whatever value is in the buffer/transfer registers will be copied to the counters, so if the user only changes one of the eight bytes, the remaining seven bytes will receive the unchanged contents of the buffer/transfer registers, which will contain whatever was in the counters at the start of the write access.

For example, if the user starts a write cycle on Monday, November 16, 2009, at 17:52:27.03, and writes a 22 to the minutes registers, the value Monday, November 16, 2009, 17:52:22.03 will be written back into the counters. At the start of the write cycle, the eight bytes of counters were copied into the buffer/transfer registers. Then, the seconds register was overwritten. Finally, the eight bytes were copied back into the counters with the result that the seconds value was changed.

2.4 Data retention and battery switchover ($V_{SO} = V_{RST}$)

Once V_{CC} falls below the switchover voltage ($V_{SO} = V_{RST}$), the device automatically switches over to the battery and powers down into an ultra low current mode of operation to preserve battery life. If V_{BAT} is less than, or greater than V_{RST}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{RST} (see *Figure 28 on page 54*). At this time the clock registers and user RAM will be maintained by the attached battery supply.

When it is powered back up, the device switches back from battery to V_{CC} at V_{SO} + hysteresis. When V_{CC} rises above V_{RST}, it will recognize the inputs. For more information on battery storage life refer to Application Note AN1012.

2.5 Power-on reset (t_{rec})

The M41T8x continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ output pulls low (open drain) and remains low after power-up for t_{rec} (210 ms typical) after V_{CC} rises above V_{RST} (max).

Note: The t_{rec} period does not affect the RTC operation. Write protect only occurs when V_{CC} is below V_{RST}. When V_{CC} rises above V_{RST}, the RTC will be selectable immediately. Only the $\overline{RST}$ output is affected by the t_{rec} period.

The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor to V_{CC} should be chosen to control the rise time.

3 Clock operation

The M41T8x is driven by a quartz-controlled oscillator with a nominal frequency of 32.768 kHz. The accuracy of the real-time clock depends on the frequency of the quartz crystal that is used as the time-base for the RTC.

The 8-byte clock register (see *Table 2 on page 23* and *Table 4 on page 25*) is used to both set the clock and to read the date and time from the clock, in binary coded decimal format. Tenths/hundredths of seconds, seconds, minutes, and hours are contained within the first four registers.

Bit D7 of register 01h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. When reset to a 0 the oscillator restarts within one second (typical).

Note: Upon initial power-up, the user should set the ST bit to a '1,' then immediately reset the ST bit to 0. This provides an additional "kick-start" to the oscillator circuit.

Bits D6 and D7 of clock register 03h (century/ hours register) contain the CENTURY bit 0 (CB0) and CENTURY bit 1 (CB1). Bits D0 through D2 of register 04h contain the day (day of week). Registers 05h, 06h, and 07h contain the date (day of month), month, and years. The ninth clock register is the digital calibration register, while the analog calibration register is found at address 12h (these are both described in *Section 3.4: Clock calibration*). The RTC includes an oscillator fail detect circuit which sets the OF bit in the flags register (bit 2, register 0fh). For the M41T83, bit D7 of register 09h (watchdog register) contains the oscillator fail interrupt enable bit (OFIE) which can be used to enable an interrupt when the OF bit is set (see *Section 3.12: Oscillator fail detection on page 44*) will also generate an interrupt output.

Note: A WRITE to ANY location within the first eight bytes of the clock register (00h-07h), including the ST bit and CB0-CB1 bits will result in an update of the RTC counters and a reset of the divider chain. This could result in an inadvertent change of the current time. For example, the ST bit is in the seconds register (address 01h) and the century bits (CB0-CB1) are in the hours register (address 03h), so the user should take care to not alter these other parameters when changing the ST bit or the century bits.

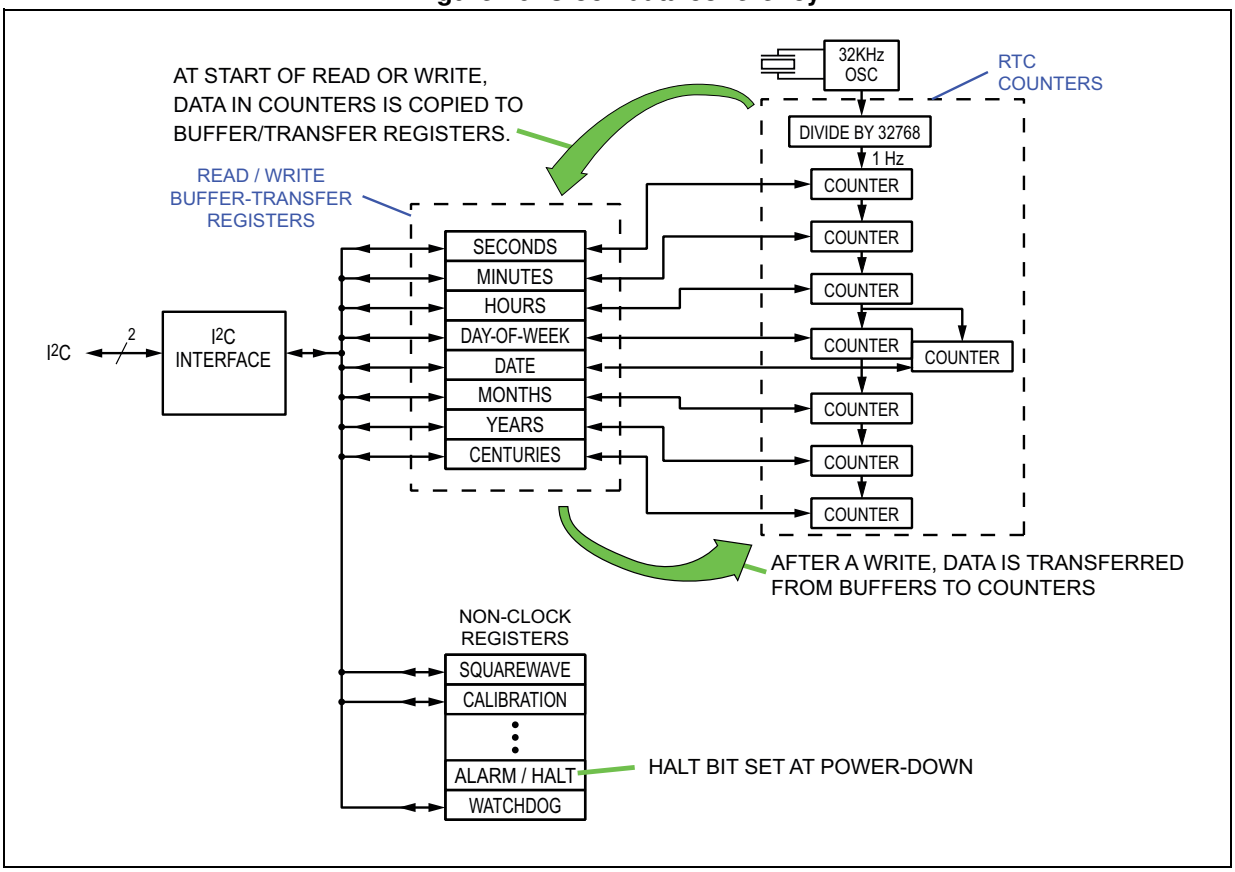
The eight clock registers may be read one byte at a time or in a sequential block. At the start of a read cycle, a copy of the time/date counters is placed in the buffer/transfer registers and can then be transferred out sequentially without concern that the time/date increments during the transfer and thus yields a corrupt value. For example, if the user were to read the seconds register, then start another bus cycle to read the minutes register, the minutes counter could have incremented during the time between the two read cycles. The seconds and minutes values would not be from the same instant in time; they would not be coherent. By using the sequential read feature, the values shifted out are from the same instant in time and are thus coherent.

Similarly, when writing to the RTC registers, during one write cycle, the user can sequentially transfer all eight bytes of time/date into the buffer/transfer registers whereupon they will be loaded simultaneously into the RTC counters thus ensuring a coherent update of the time/date.

3.1 Clock data coherency

In order to synchronize the data during reads and writes of the real-time clock device, a set of buffer transfer registers resides between the I^2C serial interface on the user side, and the clock/calendar counters in the part. While the read/write data is transferred in and out of the device one bit at a time to the user, the transfers between the buffer registers and counters occur such that all the bits are copied simultaneously. This keeps the data coherent and ensures that none of the counters are incremented while the data is being transferred.

Figure 16. Clock data coherency



3.1.1 Example of incoherency

Without having the intervening buffer/transfer registers, if the user began directly reading the counters at 23:59:59, a read of the seconds register would return 59 seconds. After the address pointer incremented, the next read would return 59 minutes. Then the next read should return 23 hours, but if the clock happened to increment between the reads, the user would see 00 hours. When the time was re-assembled, it would appear as 00:59:59, and thus be incorrect by one hour.

By using the buffer/transfer registers to hold a copy of the time, the user is able to read the entire set of registers without any values changing during the read.

Similarly, when the application needs to change the time in the counters, it is necessary that all the counters be loaded simultaneously. Thus, the user writes sequentially to the various buffer/transfer registers, then they are copied to the counters in a single transfer thereby coherently loading the counters.

3.1.2 Accessing the device

The M41T82/83 is comprised of 32 addresses which provide access to registers for time and date, digital and analog calibration, two alarms, watchdog, flags, timer, squarewave (M41T83 only) and NVRAM. The clock and alarm parameters are in binary coded decimal (BCD) format. The calibration, timer, watchdog, and squarewave parameters are in a binary format.

In the case of the M41T82 and M41T83, at the start of each read or write serial transfer, the counters are automatically copied to the buffer registers. In the event of a write to any register in the range 0-7, at the end of the serial transfer, the buffer registers are copied back into the counters thus revising the date/time. Any of the eight clock registers (addresses 0-7) not updated during the transfer will have its old value written back into the counters. For example, if only the seconds value is revised, the other seven counters will end up with the same values they had at the start of the serial transfer.

However, writes which do not affect the clock registers - that is, a write only to the non-clock registers (addresses 0x08 to 0x1F) - will not cause the buffer registers to be copied back to the counters. The counters are only updated if a register in the range 0-7 was written.

Whenever the RTC registers (addresses 0-7) are written, the divider chain from the oscillator is reset.

3.2 Halt bit (HT) operation

When the part is powered down into battery backup mode, a control bit, called the Halt or HT bit, is set automatically. This inhibits any subsequent transfers from the counters to the buffer registers thereby freezing in the buffer registers the time/date of the last access of the part.

Repeated reads of the clock registers will return the same value. After the HT bit is cleared, by writing bit 6 of address 0x0C to 0, the next read of the RTC will return the present time.

Note: Writes to the RTC registers (addresses 0-7) with the HT bit set can cause time corruption. Since the buffer registers contain the time of the last access prior to the HT bit being set, any write in the address range 0-7 will result in the time of the last access being copied back into the counters.

Example: The last access was November 17, 2009, at 16:15:07.77. The system later powered down thus setting the HT bit and freezing that value in the buffers. Later, on December 18, 2009, at 03:22:43.35, the system is powered up and the user writes the seconds to 46 without first clearing the HT bit. At the end of the serial transfer, the old time/date, with the seconds modified to 46, will be written back into the clock registers thereby corrupting them. The new, wrong time will be November 17, 2009, at 16:15:46.77. This makes it appear the RTC lost time during the power outage.

Thus, at power-up, the user should always clear the HT bit (write bit 6 to 0 at address 0x0C) before writing to any address in the range 0-7.

A typical power-up flow is to read the time of last access, then clear the HT bit, then read the current time.

3.2.1 Power-down time-stamp

Some applications may need to determine the amount of time spent in backup mode. That can be calculated if the time of power-down and the time of power-up are known. The latter is straightforward to obtain. But the time of power-down is only available if an access occurred just prior to power-down. That is, if there was an access of the device just prior to power-down, the time of the access would have been frozen in the buffer transfer registers and thus the approximate time of power-down could be obtained.

If an application requires the time of power-down, the best way to implement it is to set up the software to do frequent reads of the clock, such as once every 1 or 5 seconds. That way, at power-up, the buffer-transfer registers will contain a time value within 1 (or 5) seconds of the actual time of power-down. For more information, please refer to AN1572, “Power-down time-stamp function in serial real-time clocks (RTCs)”.

Table 2. M41T82 clock/control register map (32 bytes)(1)

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				seconds	00-99
01h	ST	10 seconds			seconds				seconds	00-59
02h	0	10 minutes			minutes				minutes	00-59
03h	CB1	CB0	10 hours		Hours (24 hour format)				Century/hours	0-3/00-23
04h	0	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 years				Year				Year	00-99
08h	0	FT	DCS	DC4	DC3	DC2	DC1	DC0	Digital calibration	
09h	0	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	0	0	ABE	AI1 10M	Alarm1 month				AI1 month	01-12
0Bh	RPT14	RPT15	AI1 10 date		Alarm1 date				AI1 date	01-31
0Ch	RPT13	HT	AI1 10 hour		Alarm1 hour				AI1 hour	00-23
0Dh	RPT12	Alarm1 10 minutes			Alarm1 minutes				AI1 min	00-59
0Eh	RPT11	Alarm1 10 seconds			Alarm1 seconds				AI1 sec	00-59
0Fh	WDF	AF1	AF2(2)	BL	TF	OF	0	0	Flags	
10h	Timer countdown value								Timer value	
11h	TE	0	0	0	0	0	TD1	TD0	Timer control	
12h	ACS	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Analog calibration	
13h	0	0	0	0	0	0	AL2E	0	SQW	
14h	0(3)	0(3)	0(3)	AI2 10M	Alarm2 month				SRAM/AI2 month	01-12
15h	RPT24	RPT25	AI2 10 date		Alarm2 month				SRAM/AI2 date	01-31
16h	RPT23	0(3)	AI2 10 hour		Alarm2 date				SRAM/AI2 hour	00-23
17h	RPT22	Alarm2 10 minutes			Alarm2 minutes				SRAM/AI2 min	00-59
18h	RPT21	Alarm2 10 seconds			Alarm2 seconds				SRAM/AI2 sec	00-59
19h-1Fh	User SRAM (7 bytes)								SRAM	

1. See *Table 3: Key to Table 2: M41T82 clock/control register map (32 bytes)*
2. AF2 will always read 0, if the AL2E bit is set to 0.
3. As indicated in *Table 3*, the 0 bits should be written to 0. But in the case of these four bits, when AL2E is 0, registers 14-18h are SRAM locations and these bits become SRAM cells which are thus excluded from that restriction.

Table 3. Key to *Table 2: M41T82 clock/control register map (32 bytes)*

Code	Explanation
0	Must be set to zero
ABE	Alarm in battery backup enable bit
AC0-AC6	Analog calibration bits
ACS	Analog calibration sign bit
AF1, AF2	Alarm flag bits
AL2E	Alarm 2 enable bit
BL	Battery low bit
BMB0-BMB4	Watchdog multiplier bits
CB0, CB1	Century bits
DC0-DC4	Digital calibration bits
DCS	Digital calibration sign bit
FT	Frequency test bit
HT	Halt update bit
OF	Oscillator fail bit
RB0-RB1	Watchdog resolution bits
RPT11-RPT15	Alarm 1 repeat mode bits
RPT21-RPT25	Alarm 2 repeat mode bits
ST	Stop bit
TD0, TD1	Timer frequency bits
TE	Timer enable bit
TF	Timer flag
WDF	Watchdog flag

Table 4. M41T83 clock/control register map (32 bytes)(1)

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				seconds	00-99
01h	ST	10 seconds			seconds				seconds	00-59
02h	0	10 minutes			Minutes				Minutes	00-59
03h	CB1	CB0	10 hours		Hours (24 hour format)				Century/hours	0-3/00-23
04h	0	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 years				Year				Year	00-99
08h	OUT	FT	DCS	DC4	DC3	DC2	DC1	DC0	Digital calibration	
09h	OFIE	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	A1IE	SQWE	ABE	AI1 10M	Alarm 1month				AI1 month	01-12
0Bh	RPT14	RPT15	AI1 10 date		Alarm1 date				AI1 date	01-31
0Ch	RPT13	HT	AI1 10 hour		Alarm1 hour				AI1 hour	00-23
0Dh	RPT12	Alarm1 10 minutes			Alarm1 minutes				AI1 min	00-59
0Eh	RPT11	Alarm1 10 seconds			Alarm1 seconds				AI1 sec	00-59
0Fh	WDF	AF1	AF2(2)	BL	TF	OF	0	0	Flags	
10h	Timer countdown value								Timer value	
11h	TE	$\overline{TI}$/TP	TIE	0	0	0	TD1	TD0	Timer control	
12h	ACS	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Analog calibration	
13h	RS3	RS2	RS1	RS0	0	0	AL2E	OTP	SQW	
14h	A2IE	0(3)	0(3)	AI2 10M	Alarm2 month				SRAM/AI2 month	01-12
15h	RPT24	RPT25	AI2 10 date		Alarm2 date				SRAM/AI2 date	01-31
16h	RPT23	0(3)	AI2 10 hour		Alarm2 hour				SRAM/AI2 hour	00-23
17h	RPT22	Alarm2 10 minutes			Alarm2 minutes				SRAM/AI2 min	00-59
18h	RPT21	Alarm2 10 seconds			Alarm2 seconds				SRAM/AI2 sec	00-59
19h-1Fh	User SRAM (7 bytes)								SRAM	

1. See *Table 5: Key to Table 4: M41T83 clock/control register map (32 bytes)*.
2. AF2 will always read 0, if the AL2E bit is set to 0.
3. As indicated in *Table 5*, the 0 bits should be written to 0. But in the case of these three bits, when AL2E is 0, registers 14-18h are SRAM locations and these bits become SRAM cells which are thus excluded from that restriction.

Table 5. Key to *Table 4: M41T83 clock/control register map (32 bytes)*

Code	Explanation
0	Must be set to zero
ABE	Alarm in battery back-up enable bit
A1IE, A2IE	Alarm interrupt enable bits
AC0-AC6	Analog calibration bits
ACS	Analog calibration sign bit
AF1, AF2	Alarm flag
AL2E	Alarm 2 enable bit
BL	Battery low bit
BMB0-BMB4	Watchdog multiplier bits
CB0, CB1	Century bits
DC0-DC4	Digital calibration bits
DCS	Digital calibration Sign bit
FT	Frequency test bit
HT	Halt update bit
OF	Oscillator fail bit
OUT	Output level
OFIE	Oscillator fail interrupt enable
OTP	OTP control bit
RB0-RB1	Watchdog resolution bits
RPT11-RPT15	Alarm 1 repeat mode bits
RPT21-RPT25	Alarm 2 repeat mode bits
RS0-RS3	SQW frequency
SQWE	Square wave enable
SRAM/$\overline{\text{ALM2}}$	SRAM/alarm 2 bit
ST	Stop bit
TD0, TD1	Timer frequency bits
TE	Timer enable bit
TF	Timer flag
$\overline{\text{TI}}$/TP	Timer interrupt or pulse
TIE	Timer interrupt enable
WDF	Watchdog flag

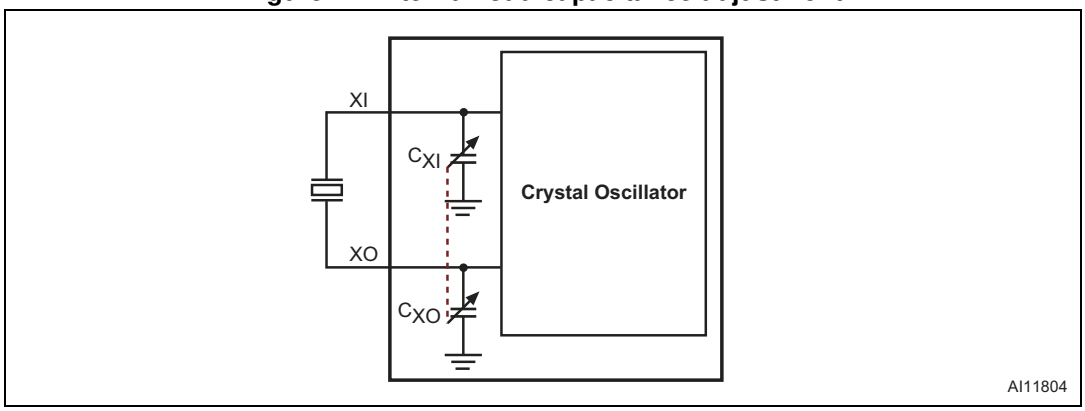
3.3 Real-time clock accuracy

The M41T8x is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The accuracy of the real-time clock is dependent upon the accuracy of the crystal, and the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Temperature also affects the crystal frequency, causing additional error (see *Figure 18 on page 32*).

The M41T8x provides the option of clock correction through either manufacturing calibration or in-application calibration. The total possible compensation is typically –93 ppm to +156 ppm. The two compensation circuits that are available are:

1. An analog calibration register (12h) can be used to adjust internal (on-chip) load capacitors for oscillator capacitance trimming. The individual load capacitors C_{XI} and C_{XO} (see *Figure 17*), are selectable from a range of –18 pF to +9.75 pF in steps of 0.25 pF. This translates to a calculated compensation of approximately ±30 ppm (see *Section 3.4.2: Analog calibration (programmable load capacitance) on page 31*).
2. A digital calibration register (08h) can also be used to adjust the clock counter by adding or subtracting a pulse at the 512 Hz divider stage. This approach provides periodic compensation of approximately –63 ppm to +126 ppm (see *Section 3.4.1: Digital calibration (periodic counter correction) on page 28*).

Figure 17. Internal load capacitance adjustment



3.4 Clock calibration

The M41T8x oscillator is designed for use with a 12.5 pF crystal load capacitance. When the calibration circuit is properly employed, accuracy improves to better than ±1 ppm at 25 °C.

The M41T8x design provides the following two methods for clock error correction.

3.4.1 Digital calibration (periodic counter correction)

This method employs the use of periodic counter correction by adjusting the ratio of the 100 Hz divider stage to the 512 Hz divider stage. Under normal operation, the 100 Hz divider stage outputs precisely 100 pulses for every 512 pulses of the 512 Hz input stage to provide the input frequency to the fraction of seconds clock register. By adjusting the number of 512 Hz input pulses used to generate 100 output pulses, the clock can be sped up or slowed down, as shown in *Figure 20 on page 35*.

When a non-zero value is loaded into the five calibration bits (DC4 – DC0) found in the digital calibration register (08h) and the sign bit is 1, (indicating positive calibration), the 100 Hz stage outputs 100 pulses for every 511 input pulses instead of the normal 512. Since the 100 pulses are now being output in a shorter window, this has the effect of speeding up the clock by 1/512 seconds for each second the circuit is active. Similarly, when the sign bit is 0, indicating negative calibration, the block outputs 100 pulses for every 513 input pulses. Since the 100 pulses are then being output in a longer window, this has the effect of slowing down the clock by 1/512 seconds for each second the circuit is active.

The amount of calibration is controlled by using the value in the calibration register (N) to generate the adjustment in one second increments. This is done for the first N seconds once every *eight* minutes for positive calibration, and for N seconds once every *sixteen* minutes for negative calibration (see *Table 6 on page 30*).

For example, if the calibration register is set to 100010, then the adjustment will occur for two seconds in every minute. Similarly, if the calibration register is set to 000011, then the adjustment will occur for 3 seconds in every alternating minute.

The digital calibration bits (DC4 – DC0) occupy the five lower order bits in the digital calibration register (08h). These bits can be set to represent any value between 0 and 31 in binary form. The sixth bit (DCS) is a sign bit; 1 indicates positive calibration, 0 indicates negative calibration. Calibration occurs within an 8-minute (positive) or 16-minute (negative) cycle. Therefore, each calibration step has an effect on clock accuracy of +4.068 or –2.034 ppm. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month, which corresponds to a total range of +5.5 or –2.75 minutes per month.

One method of determining the amount of digital calibration required is to use the frequency test output (FT) of the device (see *Section 3.14 on page 44* for more information on enabling the FT output).

When FT is enabled, a 512 Hz signal is output in the $\overline{\text{IRQ1}}$/FT/OUT pin on the M41T83, and on the FT/$\overline{\text{RST}}$ pin on the M41T82. This signal can be measured using a highly accurate timing device such as a frequency counter. The measured value is then compared to 512 Hz and the oscillator error in ppm is then determined.

The user should keep in mind that changes in the digital calibration value will not affect the signal measured on the FT pin. While the analog calibration circuit does affect the oscillator,

the digital calibration circuitry uses periodic counter correction which occurs downstream of the 512 Hz divider chain and hence has no effect on the FT pin.

Note: 1 The modified pulses are not observable on the frequency test (FT) output, nor will the effect of the calibration be measurable real-time, due to the periodic nature of the error compensation.

2 Positive digital calibration is performed on an eight minute cycle, therefore the value in the calibration register should not be modified more frequently than once every eight minutes for positive values of calibration. Negative digital calibration is performed on a sixteen minute cycle, therefore negative values in the calibration register should not be modified more frequently than once every sixteen minutes.

Table 6. Digital calibration values

Calibration value (binary)	Calibration value rounded to the nearest ppm	
DC4 – DC0	Negative calibration (DCS = 0) to slow a fast clock	Positive calibration (DCS = 1) to speed up a slow clock
0 (00000)	0	0
1 (00001)	–2	4
2 (00010)	–4	8
3 (00011)	–6	12
4 (00100)	–8	16
5 (00101)	–10	20
6 (00110)	–12	24
7 (00111)	–14	28
8 (01000)	–16	33
9 (01001)	–18	37
10 (01010)	–20	41
11 (01011)	–22	45
12 (01100)	–24	49
13 (01101)	–26	53
14 (01110)	–28	57
15 (01111)	–31	61
16 (10000)	–33	65
17 (10001)	–35	69
18 (10010)	–37	73
19 (10011)	–39	77
20 (10100)	–41	81
21 (10101)	–43	85
22 (10110)	–45	90
23 (10111)	–47	94
24 (11000)	–49	98
25 (11001)	–51	102
26 (11010)	–53	106
27 (11011)	–55	110
28 (11100)	–57	114
29 (11101)	–59	118
30 (11110)	–61	122
31 (11111)	–63	126
N	N/491520 (per minute)	N/245760 (per minute)

3.4.2 Analog calibration (programmable load capacitance)

A second method of calibration employs the use of programmable internal load capacitors to adjust (or trim) the oscillator frequency. As discussed in *Section 3.4.1*, the 512 Hz frequency test output can be used to determine the amount of frequency error in the oscillator. Changes in the analog calibration value will affect the frequency test output, thus the user can immediately see the effects of these changes (see *Section 3.14 on page 44* for more information on enabling the FT output).

By design, the oscillator is intended to be 0 ppm (± crystal accuracy) at room temperature (25 °C, see *Figure 18 on page 32*) when a 12.5 pF crystal is connected. Referring to *Figure 19 on page 34*, the device has two load capacitors, C_{XI} and C_{XO}, connected from the XI and XO pins to ground. These are nominally 25 pF each. The effective load capacitance is the series equivalent of these two:

$$C_{LOAD} = \frac{C_{XI} \bullet C_{XO}}{C_{XI} + C_{XO}}$$

For the nominal case of $C_{XI} = C_{XO} = 25$ pF,

$$C_{LOAD} = \frac{25 \bullet 25}{25 + 25} = 12.5\text{pF}$$

Thus, the nominal effective load capacitance matches the crystal specification of 12.5 pF.

The analog calibration register can be digitally adjusted, up or down, in increments of 0.25 pF, to change the capacitance of C_{XI} and C_{XO}. The default value is 25 pF. The maximum is 34.75 pF, to slow the clock, and the minimum is 7 pF, to speed up the clock.

The analog calibration value is in sign-magnitude format with the most significant bit the sign bit. The table below shows the approximate weighting for each of the bits.

b7	b6	b5	b4	b3	b2	b1	b0	
sign	16	8	4	2	1	0.5	0.25	pF

While the 7 bits plus sign suggest a total adjustment range of ±31.75 pF, the logic inside the device limits this to the range +9.75 pF / –18 pF. The table below summarizes the nominal, upper and lower limits of the load capacitance and the expected effect on the operating frequency of the oscillator.

C_{LOAD} (pF)	C_{XI}, C_{XO} (pF)	ACAL (Addr 0x12)	Oscillator frequency
12.5	25 (default)	0x00	0 ppm
17.4	34.75 (+9.75)	0x27	–15 ppm (slow)
3.5	7 (–18)	0xC8	+95 ppm (fast)

The asymmetrical nature of the adjustment range (+9.75 pF / –18 pF) is due to the nature of the frequency versus temperature curve (*Figure 18*) of 32.768 kHz watch crystals. The oscillator will slow down at temperatures both above and below room level (~25 °C). Hence, it usually needs to be sped up, so more adjustment range is provided to remove capacitance than to increase it.

As shown in *Figure 19*, the relationship between oscillator speed and load capacitance is not linear. When operating on the left end of the curve, small changes in load capacitance have more effect than when operating on the right end of the curve. For example, at –15 pF, a 3 pF reduction to –18 pF should result in the part running about 30 ppm faster (from +65 ppm to +95 ppm). Conversely, at +5 pF, adding 3 pF to get to +8 pF should only slow the part by about 4 ppm (from –8 ppm to –12 ppm).

3.4.3 Pre-programmed calibration value

Users of the M41T83 in the embedded crystal package have the option of using the factory programmed analog calibration value (refer to *Section 3.17 on page 49*).

Figure 18. Crystal accuracy across temperature

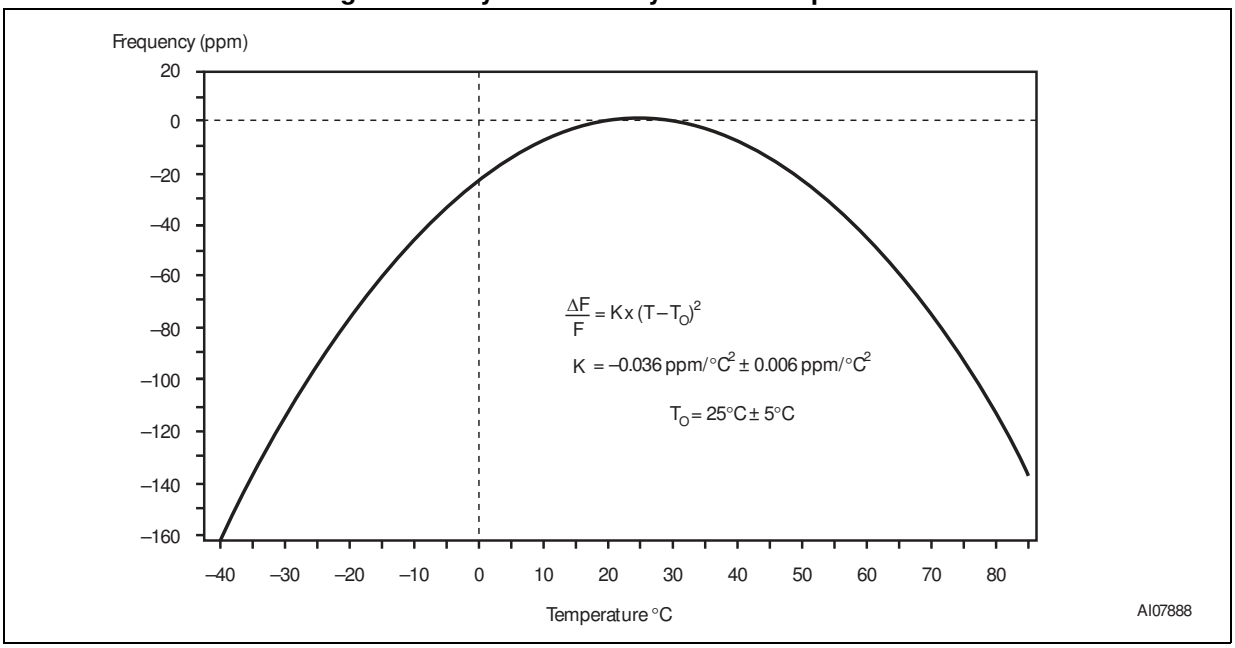


Table 7. Analog calibration values

Addr	Analog calibration value	D7	D6	D5	D4	D3	D2	D1	D0	C_{XI}, C_{XO}	C_{LOAD}(1)
		ACS (±)	AC6 (16 pF)	AC5 (8 pF)	AC4 (4 pF)	AC3 (2 pF)	AC2 (1 pF)	AC1 (0.5 pF)	AC0 (0.25 pF)		½(C_{XI}, C_{XO})
12h	0 pF	x	0	0	0	0	0	0	0	25 pF	12.5 pF
	3 pF	0	0	0	0	1	1	0	0	28 pF	14 pF
	5 pF	0	0	0	1	0	1	0	0	30 pF	15 pF
	–7 pF	1	0	0	1	1	1	0	0	18 pF	9 pF
	9.75 pF(2)	0	0	1	0	0	1	1	1	34.75 pF	17.4 pF
	–18 pF(3)	1	1	0	0	1	0	0	0	7 pF	3.5 pF

1. $C_{LOAD} = 1/(1/C_{XI} + 1/C_{XO})$.
2. Maximum negative calibration value.
3. Maximum positive calibration value.

The on-chip capacitance can be calculated as follows:

$$C_{LOAD} = 12.5 + [ACS:(AC6:AC0\ value,\ decimal)] \bullet 0.125\ pF$$

where ACS is the sign.

Examples:

ACAL (addr 12h) = 0 → C_{LOAD} = 12.5 pF

ACAL = 10111100b → C_{LOAD} = 5 pF

ACAL = 00010100b → C_{LOAD} = 15 pF

With the analog calibration adjusted to its lowest value, the oscillator will see a minimum of 3.5 pF load capacitance as shown on the bottom row of *Table 7*.

Note: These are typical values, and the total load capacitance seen by the crystal will include approximately 1-2 pF of package and board capacitance in addition to the analog calibration register value.

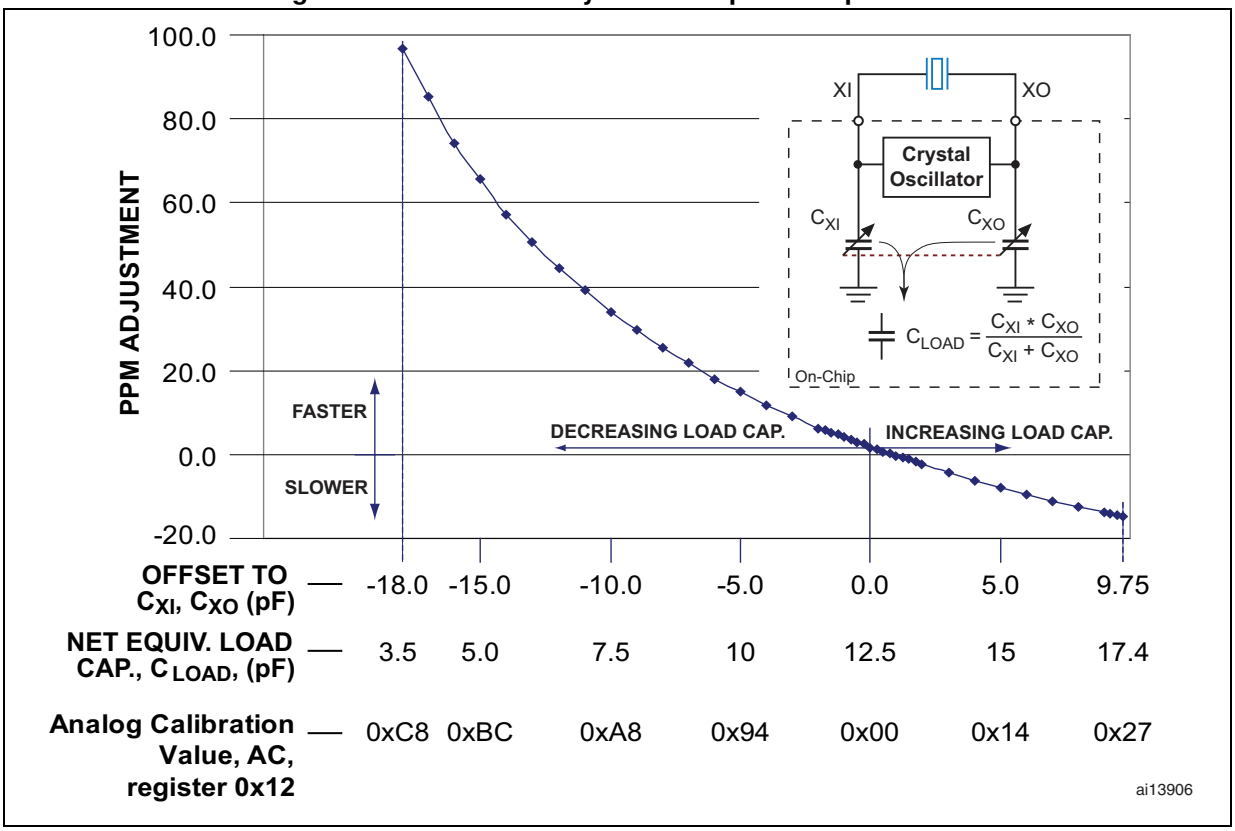
Any invalid value of analog calibration will result in the default capacitance of 25 pF (for C_{XI} and C_{XO}).

Combining the digital adjustment range (–63 to +126 ppm) and analog adjustment range (–15 to +95 ppm), the approximate overall adjustment range of the M41T82-83's timekeeping is –78 to +221 ppm.

Figure 19 represents a typical curve of clock ppm adjustment versus the analog calibration value. Actual crystals may vary, so users should evaluate the crystals to be used with an M41T82-83 device before establishing the adjustment values for a given application.

.

Figure 19. Clock accuracy vs. on-chip load capacitance



Two methods are available for ascertaining how much calibration a given M41T8x may require:

- The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses either or both of the calibration bytes.
- The second approach is better suited to a manufacturing environment, and uses the 512 Hz frequency test output. This is the $\overline{\text{IRQ1}}$/FT/OUT pin on the M41T83, and the FT/$\overline{\text{RST}}$ pin on the M41T82 (see *Section 3.14* and *Section 3.15* for more information on enabling the FT output). The 512 Hz frequency test signal can be measured using a highly accurate timing device such as a frequency counter. The measured value is then compared to 512 Hz and the oscillator error in ppm is then determined.

  Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring either a –10 (xx001010) to be loaded into the digital calibration byte, or +6 pF (00011000) into the analog calibration byte for correction.

Note: Setting or changing the digital calibration byte does not affect the frequency test, square wave, or watchdog timer frequency, but changing the analog calibration byte DOES affect all functions derived from the low current oscillator (see Figure 20).

Figure 20. Clock divider chain and calibration circuits

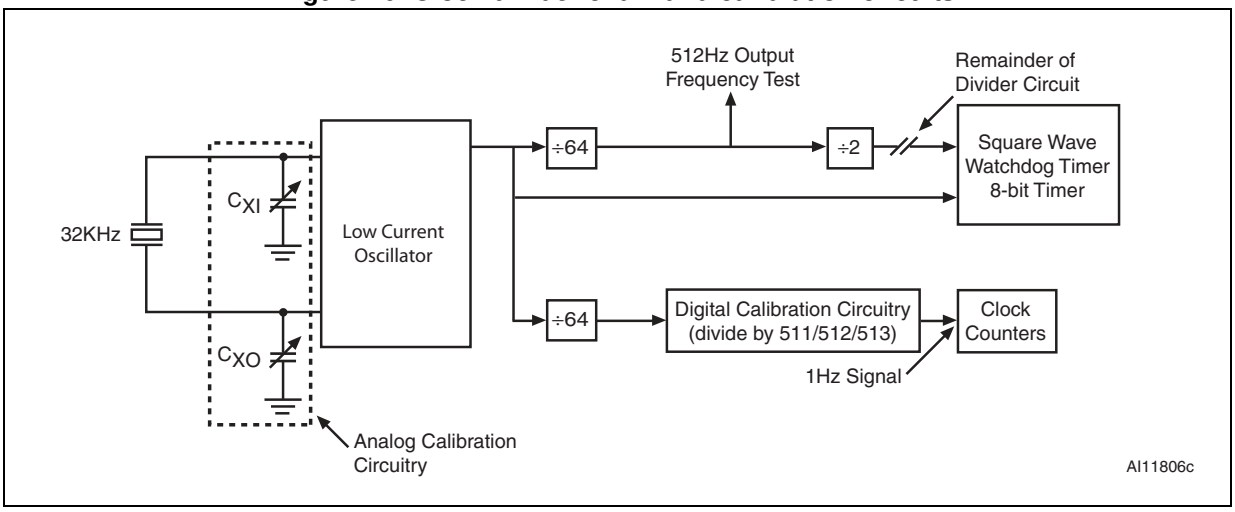
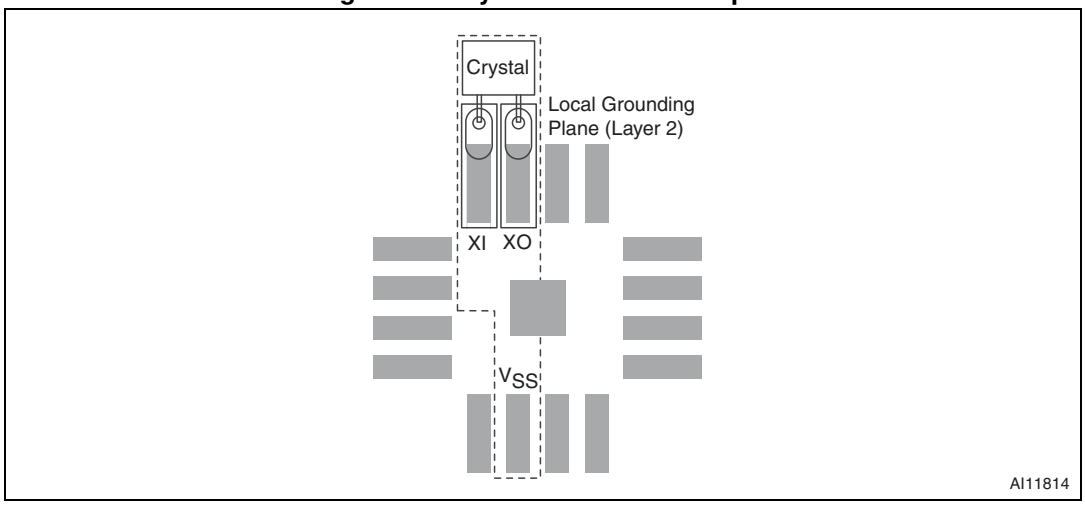


Figure 21. Crystal isolation example



1. Substrate pad should be tied to V_{SS}.

3.5 Setting the alarm clock registers

Codes not listed in the table default to the once-per-second mode to quickly alert the user of an incorrect alarm setting. When the clock information matches the alarm clock settings based on the match criteria defined by RPTx5–RPTx1 (x = 1 for alarm 1 or 2 for alarm 2), the alarm flag, AFx, is set. Reading the flags register clears the alarm flags. A subsequent read of the flags register is necessary to see that the value of the alarm flag has been reset to 0.

M41T83 interrupts on alarm

In the M41T83, for alarm 1, setting the alarm interrupt enable, A1IE, allows an interrupt output to be asserted upon AF1 being set provided that other configuration bits are set accordingly (see *Section 3.14* for more information on the $\overline{\text{IRQ}}$/FT/OUT output).

Likewise for alarm 2, with A2IE set, $\overline{\text{IRQ2}}$ will be asserted upon AF2 going high. To disable either of the alarms, write a 0 to the alarm date registers and to the RPTx5–RPTx1 bits.

Note: If the address pointer is allowed to increment to the flag register address, or the last address written is "Alarm Seconds," the address pointer will increment to the flag address, and an alarm condition will not cause the interrupt/flag to occur until the address pointer is moved to a different address.

Alarm IRQ outputs are de-asserted when the alarm flags are cleared by reading the flags register (0Fh).

The $\overline{\text{IRQ1}}$/FT/OUT pin can also be activated in the battery backup mode. This requires the ABE bit (alarm in backup enable) to be set (see *Section 3.14.2: Backup mode* for additional conditions which apply). Once an interrupt is asserted in backup mode, it will remain true until V_{CC} is restored and a subsequent read of the flags register occurs.

3.6 Optional second programmable alarm and user SRAM

When the alarm 2 enable (AL2E) bit (D1 of address 13h) is set to a logic 1, registers 14h through 18h provide control for a second programmable alarm which operates in the same manner as the alarm function described in *Section 3.5*. The AL2E bit defaults on initial power-up to a logic 0 (alarm 2 disabled). In this mode, the five alarm 2 bytes (14h-18h) function as additional user SRAM, for a total of 12 bytes of user SRAM.

With AL2E set to 1, the alarm is enabled, and will cause the AF2 bit to be set when the alarm condition is met. On the M41T83, if the A2IE (alarm 2 interrupt enable) bit is set, an interrupt will be asserted on $\overline{\text{IRQ2}}$. The interrupt is de-asserted when the alarm flags are cleared by reading the flags register (0Fh).

$\overline{\text{IRQ2}}$ can be enabled in backup mode by setting ABE to 1 (in conjuction with setting A2IE).

Table 8. Alarm repeat modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

3.7 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the watchdog register, address 09h. Bits BMB4-BMB0 store a binary multiplier and the two lower order bits RB1-RB0 select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the watchdog register = 3*1, or 3 seconds). If the processor does not reset the timer within the specified period, the M41T8x sets the WDF (watchdog flag).

The watchdog timer is reset by writing to the watchdog register. The time-out period then starts over.

M41T83 watchdog interrupt

On the M41T83, provided that the necessary configuration bits are set, the $\overline{\text{IRQ}}$/FT/OUT output will be asserted when the watchdog times out (see *Section 3.14* for additional conditions which apply).

Should the watchdog time out, to de-assert the $\overline{\text{IRQ1}}$/FT/OUT output, the lower seven bits of the watchdog register (09h) must be written. This will de-assert the output and re-initialize the watchdog. Writing these seven bits to 0 will de-assert the output and disable the watchdog.

A READ of the flags register will reset the watchdog flag (bit D7; register 0Fh) but not de-assert the IRQ1/FT/OUT output. The watchdog function is automatically disabled upon power-up and the watchdog register is cleared.

Table 9. Watchdog register

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function
09h	OFIE	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog

3.8 8-bit (countdown) timer

The timer value register is an 8-bit binary countdown timer. It is enabled and disabled via the timer control register (11h) TE bit. Other timer properties such as the source clock, or interrupt generation are also selected in the timer control register (see *Table 10*). For accurate read back of the countdown value, the I^2C-bus clock (SCL) must be operating at a frequency of at least twice the selected timer clock.

The timer control register selects one of four source clock frequencies for the timer (4096, 64, 1, or 1/60 Hz), and enables/disables the timer. The timer counts down from a software-loaded 8-bit binary value (register 10h) and decrements to 1. On the next tick of the counter, it reloads the timer countdown value and sets the timer flag (TF) bit. The TF bit can only be cleared by software. When asserted, the timer flag (TF) can also be used to generate an interrupt (IRQ1/FT/OUT) on the M41T83. Writing the timer countdown value (10h) has no effect on the TF bit or the IRQ1/FT/OUT output.

3.8.1 M41T83 timer interrupt/output

On the M41T83, there are two choices for the output depending on the TI/TP configuration bit (timer interrupt/timer pulse, bit 6, register 11h).

Normal interrupt mode

With TI/TP = 0, the output will assert like a normal interrupt, staying low until the TF bit is cleared by software by reading the flags register (0Fh).

Free-running mode

When TI/TP is a 1, the output is a free-running waveform as depicted in *Figure 22*. After being low for the specified time (as shown in *Table 11*), the output automatically goes high without need of software clearing any bits. The TF bit will still be set each time the timer reloads, but it is not necessary for the software to clear it in this mode. Furthermore, clearing the TF bit has no effect on the output in this mode.

While writes to the timer countdown register (10h) control the reload value, reads of this register return the current countdown timer value.

Table 10. Timer control register map(1)

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function
0Fh	WDF	AF1	AF2	BL	TF	OF	0	0	Flags
10h	Timer countdown value(2)								Timer value
11h	TE	$\overline{TI}$/TP	TIE	0	0	0	TD1	TD0	Timer control

1. Bit positions labeled with 0 should always be written with logic 0.
2. Writing to the timer register will not reset the TF bit nor clear the interrupt.

When the timer is in the free-running mode, with a value of n programmed into the timer countdown value, the output will nominally be low for one cycle of the specified clock source and high for n-1 cycles with an overal period of n cycles. Thus, the countdown period is n/source clock frequency.

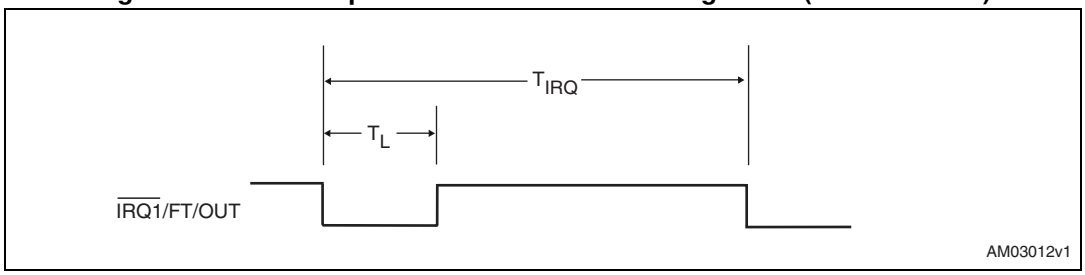
For the special case of n = 1, as shown in *Table 11*, when the clock source is 4096 or 64 Hz, the low time (T_L) is half the clock period instead of a full clock period.

Table 11. Timer interrupt operation in free-running mode (with $\overline{TI}$/TP = 1)

Source clock (Hz)	$\overline{IRQ}$ low time – T_L (seconds)(1)		$\overline{IRQ}$ period – $T_{\overline{IRQ}}$ (seconds)	
	n = 1(2)	n > 1	n = 1	n > 1
4096	1/8192 = 122 µs	1/4096 = 244 µs	1/4096 = 244 µs	n / 4096
64	1/128 = 7.8 ms	1/64 = 15.6 ms	1/64 = 15.6 ms	n / 64
1	1/64	1/64	1	n
1/60	1/64	1/64	1 minute	n minutes

1. $\overline{IRQ1}$/FT/OUT is asserted coincident with TF going true.
2. n = loaded countdown timer value (0 < n < 255). The timer is stopped when n = 0.

Figure 22. Timer output waveform in free-running mode (with $\overline{TI}$/TP = 1)



3.8.2 Timer flag (TF)

At the end of a timer countdown, when the timer reloads, TF is set to logic '1.' Regardless of the state of TF bit (or $\overline{TI}$/TP bit), the timer will continue decrementing and reloading.

If both timer and alarm interrupts are used in the application, the source of the interrupt can be determined by reading the flag bits. Refer to *Section 3.14* for more information on the interaction of these bits. The TF bit is cleared by reading the flags register. This will de-assert an interrupt output due to the timer.

3.8.3 Timer interrupt enable (TIE, M41T83 only)

In normal interrupt mode ($\overline{TI}$/TP = 0), when TF is asserted, the interrupt output is asserted (if TIE = 1). To de-assert the interrupt, the TF bit or the TIE bit must be reset. Disabling the interrupt by clearing the TIE bit will de-assert the output, but does not clear the TF bit. Thus, if TIE is re-enabled prior to clearing TF, the interrupt will assert immediately.

3.8.4 Timer enable (TE)

- TE = 0

  When the timer register (10h) is set to 0, the timer is disabled.
- TE = 1

  The timer is enabled. TE is reset (disabled) on power-down. When re-enabled, the counter will begin counting from the same value as when it was disabled.

3.8.5 TD1/0

These are the timer source clock frequency selection bits (see *Table 12*). These bits determine the source clock for the countdown timer (see *Table 10 on page 39*). When not in use, the TD1 and TD0 bits should be set to 11 (1/60 Hz) for power saving.

Table 12. Timer source clock frequency selection (244.1 µs to 4.25 hrs)

TD1	TD0	Timer source clock frequency (Hz)
0	0	4096 (244.1 µs)
0	1	64 (15.6 ms)
1	0	1 (1 s)
1	1	1/60 (60 s)

3.9 Square wave output (M41T83 only)

The M41T83 offers the user a programmable square wave function which is output on the SQW pin. RS3-RS0 bits located in 13h establish the square wave output frequency. These frequencies are listed in *Table 13*. Once the selection of the SQW frequency has been completed, the SQW pin can be turned on and off under software control with the square wave enable bit (SQWE) located in register 0Ah.

Note: If the SQWE bit is set to '1' and V_{CC} falls below the switchover (V_{SO}) voltage, the square wave output will be disabled.

Table 13. Square wave output frequency

Square wave bits				Square wave	
RS3	RS2	RS1	RS0	Frequency	Units
0	0	0	0	None	–
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

3.10 Battery low warning

The M41T8x automatically checks the battery each time V_{CC} powers up and each time the clock rolls over at midnight.

V_{BAT} is compared to V_{BL} (approximately 2.5 V), then the battery low (BL) bit, D4 of flags register 0Fh, is set if the battery voltage is found to be less than V_{BL}. Similarly, if V_{BAT} is greater than V_{BL}, the BL bit is cleared during battery check.

The BL bit retains its state until the next battery check occurs. This means the BL bit will not clear immediately upon battery replacement, but only after the next battery check occurs at the next power-up or midnight rollover.

If a battery low is generated during a power-up sequence, this indicates that the battery is below approximately 2.5 volts and may not be able to maintain data integrity. Clock data should be considered suspect and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to ensure data integrity during subsequent periods of battery backup mode, the battery should be replaced.

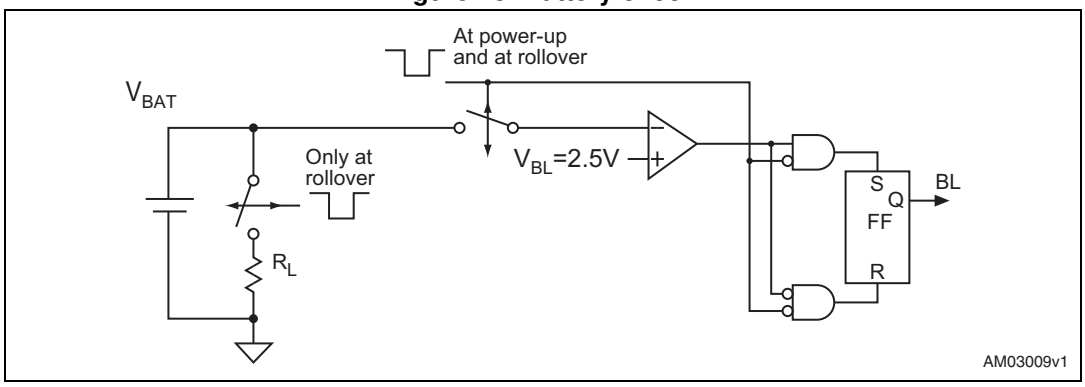
Midnight rollover check

As shown in *Figure 23*, during the midnight rollover check, the M41T8x applies a load to the battery, then compares V_{BAT} to V_{BL} and updates the BL bit accordingly. Because a load is present, an open condition on the V_{BAT} pin will result in the BL bit being set. After the check is performed, the RTC removes the load.

Power-up battery check

During the power-up check, no load is applied to the battery under the assumption the battery has already been stressed to its working level by having powered the RTC in backup mode. If no battery is present, V_{BAT} will be floating and the battery check result will be indeterminate.

Figure 23. Battery check



The M41T8x only checks the battery when powered by V_{CC}. It does not check the battery while in backup mode. Thus, users are advised that during long periods in backup mode, the battery can drop to a level at which timekeeping may fail or data becomes corrupted. If, at power-up, a battery low is indicated, data integrity should be verified.

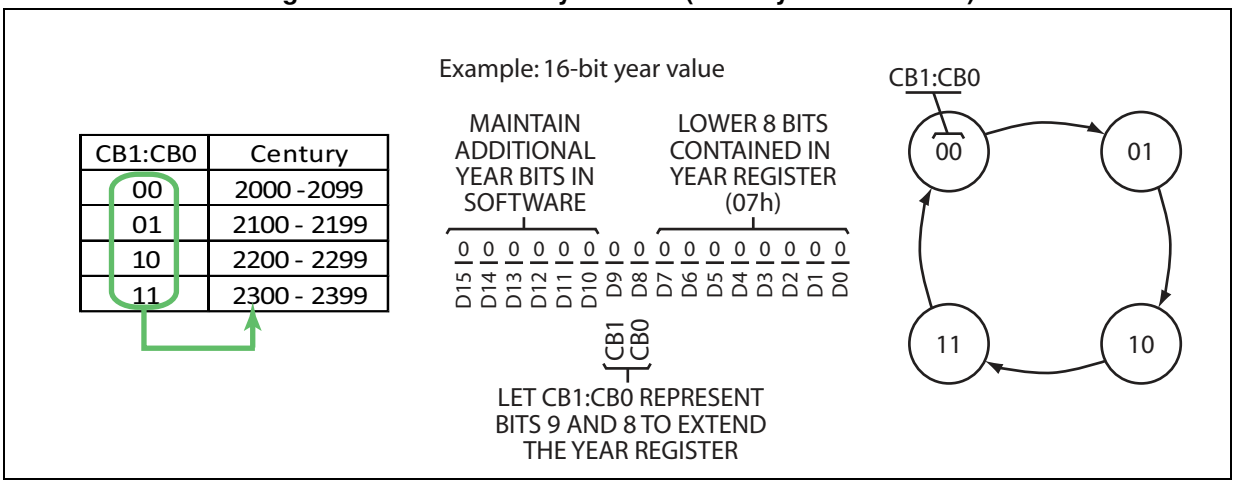
Forcing a battery check

If it is desired to check the battery at an arbitrary time, one common technique is for the application software to write the time to just before midnight, 23:59:59, and then wait two seconds thereby letting the clock rollover and causing the BL bit to update. The application then restores the time back to its previous value plus two seconds.

3.11 Century bits

The M41T82-83 includes 2 century bits (CB1, CB0) which function as a 2-bit binary counter that increments at the end of each century. The user may arbitrarily assign the meaning of CB1:CB0 to represent any century value, but the simplest way of using these bits is to extend the year register by mapping them directly to bits 9 and 8 (with the year register comprising bits 7:0). Higher order century bits can be maintained in the application software.

Figure 24. Two-bit binary counter (century bits CB1:CB0)



In this example, CB1:CB0 represent the two lower bits of the century byte.

Leap year

Leap year occurs every four years, in years which are multiples of 4. For example, 2012 was a leap year. An exception to that is any year which is a multiple of 100. For example, the year 2100 is not a leap year. A contradiction to that is that years which are multiples of 400 are indeed leap years. Hence, while 2100 is not a leap year, 2400 is.

During any year which is a multiple of 4, ST RTC and TIMEKEEPER devices will automatically insert leap day, February 29. Therefore, the application software must correct for this during the exception years (2100, 2200, etc.) as noted above.

3.12 Oscillator fail detection

If the oscillator fail (OF) bit is internally set to a '1,' this indicates that the oscillator has either stopped, or was stopped for some period of time. This bit can be used to judge the validity of the clock and date data. This bit will be set to '1' any time the oscillator stops.

In the event the OF bit is found to be set to '1' at any time other than the initial power-up, the STOP bit (ST) should be written to a '1,' then immediately reset to 0. This will restart the oscillator. The following conditions can cause the OF bit to be set:

- The first time power is applied (defaults to a '1' on power-up).

Note: If the OF bit cannot be written to '0' four seconds after the initial power-up, the STOP bit (ST) should be written to a '1,' then immediately reset to 0.

- The voltage present on V_{CC} or battery is insufficient to support oscillation.
- The ST bit is set to '1.'
- External interference of the crystal

For the M41T83, if the oscillator fail interrupt enable bit (OFIE) is set to a '1,' the $\overline{\text{IRQ1}}$/FT/OUT pin will also be asserted (see *Section 3.13* and *Section 3.14* for additional conditions which apply). The $\overline{\text{IRQ1}}$/FT/OUT output is de-asserted by resetting the OF bit to 0, NOT by reading the flags register. The OF bit will remain a '1' until written to 0. Reading the flags register has no effect on OF.

The oscillator must start and have run for at least 4 seconds before attempting to reset the OF bit to 0.

The oscillator fail detect circuit funtions during backup mode. If a triggering event occurs to disrupt the oscillator during a power-down condition, the OF bit will be set accordingly.

3.13 Oscillator fail interrupt enable (M41T83 only)

With the OFIE bit set, the OF bit will cause the $\overline{\text{IRQ1}}$/FT/OUT output to be asserted (see *Section 3.14.1* and *3.14.2* for additional conditions that apply). The $\overline{\text{IRQ1}}$/FT/OUT output is cleared by resetting the OF bit to 0 (NOT by reading the flags register). Clearing the OFIE bit will also cause the $\overline{\text{IRQ1}}$/FT/OUT output to de-assert, but if OFIE is subsequently set prior to clearing OF, the $\overline{\text{IRQ1}}$/FT/OUT output will assert immediately upon setting OFIE. Clearing the OF bit is necessary to prevent such an inadvertent interrupt.

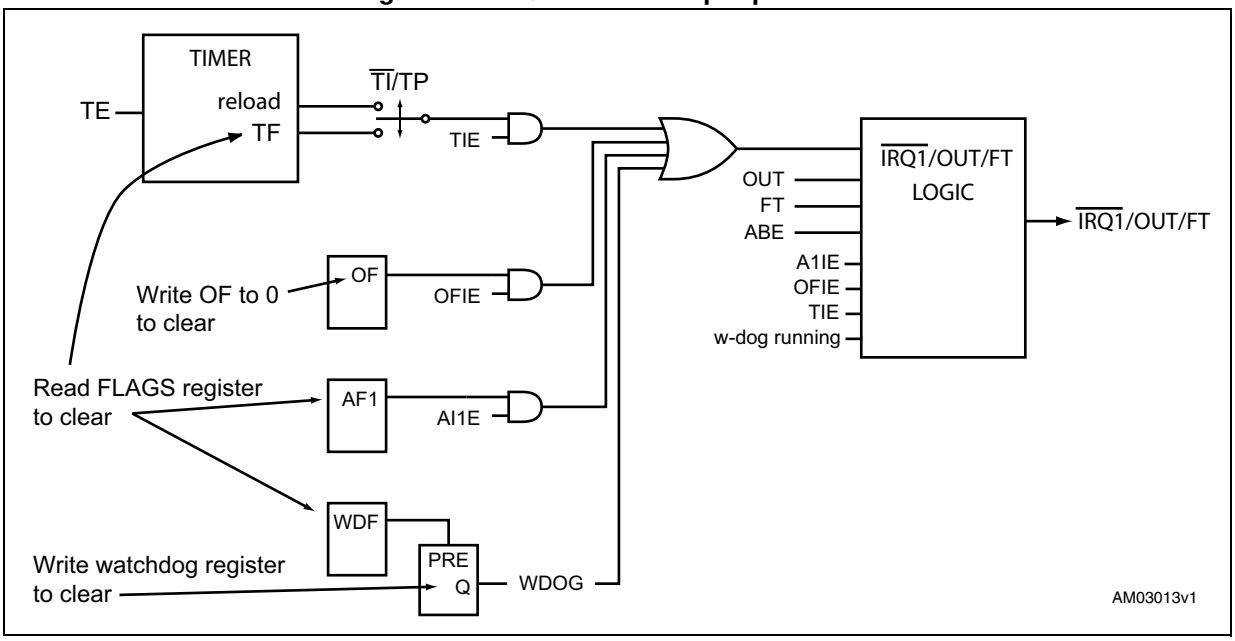
If the alarm in backup enable bit, ABE, is set (along with OFIE), the oscillator fail detect will cause an interrupt in the $\overline{\text{IRQ1}}$/FT/OUT pin during backup mode. For additional information on this, refer to *Section 3.14.2*.

3.14 $\overline{\text{IRQ1}}$/FT/OUT pin, frequency test, interrupts and the OUT bit (M41T83 only)

Four interrupt sources, the frequency test function, and the discrete output bit OUT all share the $\overline{\text{IRQ1}}$/FT/OUT pin. Priority is built into the part such that some functions dominate others. Additionally, the priority depends on configuration bits such as OUT and ABE, and on whether the part is operating on V_{CC} or is in the backup mode. This pin is an open drain output and requires an external pull-up resistor.

Figure 25 shows the various signal sources and controlling bits for the $\overline{\text{IRQ1}}$/FT/OUT output pin.

Figure 25. $\overline{IRQ1}$/FT/OUT output pin circuit



The timer, oscillator fail detect circuit, alarm 1, and watchdog are ORed together as the primary interrupt sources. The frequency test signal, FT, is used to enable a 512 Hz output on the $\overline{IRQ1}$/FT/OUT pin for calibrating the RTC. When not used as an interrupt or frequency test output, the pin can be used as a discrete logic output controlled by the OUT bit. The ABE bit is used to enable interrupts during backup mode.

Operating on V_{CC}, all four interrupt sources are available. During backup, the timer and watchdog are disabled, and the only interrupt sources are alarm 1 and the oscillator fail detect circuit.

3.14.1 Active mode operation on V_{CC}

On V_{CC}, the operation of the output circuit is as shown in *Table 14*.

Table 14. Priority for $\overline{IRQ1}$/FT/OUT pin when operating on V_{CC}

OUT(1)	FT(2)	A1IE(3) + OFIE(4) + TIE(5) + watchdog(6) running	Pin	Comment
0	0	x	0	When OUT is 0 and FT is not enabled, OUT dominates and none of the interrupt sources have any effect.
0	1	x	512 Hz	When FT = 1 and OUT = 1 and no interrupts are enabled, the output will be the 512 Hz frequency test (FT) signal.
x	1	0		
1	x	1	$\overline{IRQ}$	When one or more interrupts are enabled, and OUT is a 1, the pin stays high until one of the interrupts is asserted.
1	0	0	1	When OUT is 1, FT is 0 and no interrupts are enabled, the pin is high.

1. OUT is bit 7 of register 08h (digital calibration).
2. FT is bit 6 of register 08h (digital calibration).
3. A1IE is bit 7 of register 0Ah (alarm 1, month).
4. OFIE is bit 7 of register 09h (watchdog).
5. TIE is bit 5 of register 11h (timer control).
6. The watchdog is controlled by register 09h (watchdog).

When OUT is 0 and FT is 0, the pin will be 0 regardless of whether any interrupts are enabled.

When FT is a 1, the 512 Hz signal will be output if OUT is 0 or if no interrupts are enabled.

The interrupt sources control the pin when OUT is 1 and one or more of the interrupts are enabled.

If OUT is 1, FT is 0 and no interrupts are enabled, then the pin will be 1.

3.14.2 Backup mode

In backup mode, the operation of the output circuit is as shown in *Table 15*.

Table 15. Priority for $\overline{\text{IRQ1}}$/FT/OUT pin when operating in backup mode

OUT(1)	ABE(2)	A1IE(3) + OFIE(4)	Pin	Comment
x	0	x	1	When ABE is 0, the pin is 1 regardless of OUT or the interrupt sources.
1	x	0	1	When OUT is 1 and no interrupts are enabled, the pin is 1. (A1IE and OFIE are the only interrupts applicable in this mode).
0	1	x	0	When ABE is 1 and OUT is 0, OUT dominates and regardless of the interrupt sources.
1	1	1	$\overline{\text{IRQ}}$	When one or more interrupts are enabled, ABE is a 1, and OUT is a 1, the pin stays high until one of the interrupts is asserted.

1. OUT is bit 7 of register 08h (digital calibration).
2. ABE is bit 5 of register 0Ah (alarm 1, month).
3. A1IE is bit 7 of register 0Ah (alarm 1, month).
4. OFIE is bit 7 of register 09h (watchdog).

In backup mode, frequency test is disabled. Thus, the FT bit is a ‘don’t care’.

ABE enables interrupts in backup. If it is 0, the output pin is a 1 regardless of the other bits.

The pin is also a 1 when OUT is a 1 and no interrupts are enabled.

When OUT is 0 and ABE is a 1, the pin is 0 regardless of the interrupts.

Thus, in order to enable interrupts in backup mode, OUT must be a 1 and ABE must be a 1, and one or more of the interrupt enables must be a 1.

Simultaneous interrupts

Since more than one interrupt source can cause the $\overline{\text{IRQ1}}$/FT/OUT pin to go low, more than one interrupt may be pending when the microprocessor services the interrupt. Therefore, the application software should read the flags register (0Fh) to discern which condition or conditions are causing the pin to be asserted.

Also be aware that once a flag causes the pin to assert, other flags could subsequently also go true. Since the pin is already low due to the first, no additional output transition will occur. That is why the software must check the flags register.

Example: If the watchdog is in use and the oscillator fail detect interrupt is enabled, and the watchdog times out, the $\overline{\text{IRQ1}}$/FT/OUT pin will go low. If, in the intervening time before the processor services the interrupt, something disturbs the oscillator, such as a drop of moisture landing on the crystal pins, the OF bit will also be set. Thus, when the software services the interrupt, it must service both sources: it must re-initialize the watchdog *and* clear the OF bit in order to de-assert the $\overline{\text{IRQ1}}$/FT/OUT pin. By reading the flags register, the software will know both flags were set and that both need service.

3.15 FT/$\overline{RST}$ pin, frequency test and reset output pin (M41T82 only)

On the M41T82, the 512 Hz frequency test signal and the reset output share the same pin, FT/$\overline{RST}$. When the FT bit (bit 6 of register 08h) is a 1, the 512 Hz test signal is activated on the pin. With FT a 0 and V_{CC} good (above V_{RST}), the output will be high. If the 512 Hz is enabled when V_{CC} fails, the FT bit will be cleared and the output will go low to assert reset. At power-up, FT will be 0 leaving the pin functioning as the reset output.

3.16 Initial power-on defaults

Upon initial application of power to the device, the register bits will initially power-on in the state indicated in *Table 16* and *Table 17*.

Table 16. Initial power-on default values (part 1)

Condition(1)	ST	CB1	CB0	OUT	FT	DCS ACS	Digital calib.	Analog calib.	OFIE(2)	Watch-dog(3)	A1IE (2)	SQWE(2)	ABE
Initial power-up	0	0	0	1	0	0	0	0	0	0	0	1	0
Subsequent power-up(4)(5)	UC	UC	UC	UC	0	UC	UC	UC	UC	0	UC	UC	UC

1. All other control bits power-up in an undetermined state.
2. M41T83 only
3. BMB0-BMB4, RB0, RB1
4. With battery backup
5. UC = unchanged

Table 17. Initial power-up default values (part 2)

Condition(1)	RPT11-15	HT	OF	TE	$\overline{TI}$/TP (2)	TIE(2)	TD1	TD0	RS0	RS1-3	OTP (2)	A2IE(2)	RPT21-25	AL2E
Initial power-up	0	1	1	0	0	0	1	1	1	0	0	0	0	0
Subsequent power-up(3)(4)	UC	1	UC	0	UC	UC	UC	UC	UC	UC	UC	UC	UC	UC

1. All other control bits power-up in an undetermined state.
2. M41T83 only
3. With battery backup
4. UC = unchanged

3.17 OTP bit operation (M41T83 in SOX18 package only)

Using the factory-supplied analog calibration value

When the OTP (one time programmable) bit is set to a 1, the factory calibration value in the internal OTP register will be transferred to the analog calibration register (12h) and is “read only.” The OTP value is programmed by the manufacturer, and will contain the value necessary to achieve typically ±5 ppm [(a)] at room temperature (V_{CC} only) after two SMT reflows. This clock accuracy can then be guaranteed to drift no more than ±3 ppm the first year, and ±1 ppm for each following year due to crystal aging.

If the OTP bit is set to 0, the analog calibration register will become a WRITE/READ register and function like an ordinary register, allowing the user to implement any desired value of analog calibration.

When the user sets the OTP bit, they must wait for approximately 8 ms while the device transfers the OTP value into the analog calibration register.

a. Max. value = +12 ppm / –5 ppm based on limited data

4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 18. Absolute maximum ratings

Sym	Parameter		Value(1)	Unit
T_{STG}	Storage temperature (V_{CC} off, oscillator off)		–55 to 125	°C
V_{CC}	Supply voltage		–0.3 to 7.0	V
T_{SLD}	Lead solder temperature for 10 seconds		260(2)	°C
V_{IO}	Input or output voltages		–0.2 to V_{CC}+0.3	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W
θ_{JA}	Thermal resistance, junction to ambient	QFN16	35.7	°C/W
		SO8	128.4	
		SOX18		

1. Data based on characterization results, not tested in production.
2. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds (according to JEDEC J-STD-020D).

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the dc and ac characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 19. Operating and AC measurement conditions

Parameter[1]	M41T8x
Supply voltage (V_{CC})	2.38 V to 5.5 V
Ambient operating temperature (T_A)	–40 to 85 °C
Load capacitance (C_L)	50 pF
Input rise and fall times	≤ 5 ns
Input pulse voltages	0.2 V_{CC} to 0.8 V_{CC}
Input and output timing ref. voltages	0.3 V_{CC} to 0.7 V_{CC}

1. Output Hi-Z is defined as the point where data is no longer driven.

Figure 26. Measurement AC I/O waveform

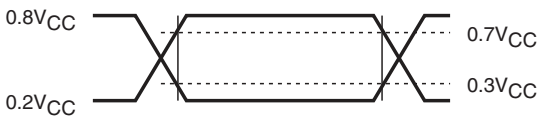


Table 20. Capacitance

Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance		7	pF
C_{OUT}[3]	Output capacitance		10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		50	ns

1. Effective capacitance measured with power supply at 3.6 V; sampled only, not 100% tested.
2. At 25 °C, f = 1 MHz
3. Outputs deselected

Table 21. DC characteristics

Sym	Parameter	Test condition(1)		Min	Typ	Max	Unit
V_{CC}	Operating voltage (S)	–40 to 85 °C		3.00		5.50	V
	Operating voltage (R)	–40 to 85 °C		2.70		5.50	V
	Operating voltage (Z)	–40 to 85 °C		2.38		5.50	V
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$				±1	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$				±1	µA
I_{CC1}	Supply current	SCL = 400 kHz (No load)	5.5 V		125	150	µA
			3.0 V		55		µA
			2.5 (Z only)		45		µA
I_{CC2}	Supply current (standby)	SCL = 0 Hz; All inputs ≥ V_{CC} – 0.2 V or ≤ V_{SS} + 0.2 V (SQWE bit = 0)	5.5 V		8	10	µA
			3.0 V		6.5		µA
V_{IL}	Input low voltage			–0.3		$0.3V_{CC}$	V
V_{IH}	Input high voltage			$0.7V_{CC}$		V_{CC}+0.3	V
V_{OL}	Output low voltage	$\overline{RST}$, FT/$\overline{RST}$	V_{CC}/V_{BAT} = 3.0 V, I_{OL} = 1.0 mA			0.4	V
		SQW, $\overline{IRQ1}$/FT/OUT, $\overline{IRQ2}$	V_{CC} = 3.0 V, I_{OL} = 1.0 mA			0.4	V
		SCL, SDA	V_{CC} = 3.0 V, I_{OL} = 3.0 mA			0.4	V
V_{OH}	Output high voltage	V_{CC} = 3.0 V, I_{OH} = –1.0 mA (push-pull)		2.4			V
	Pull-up supply voltage (open drain)	$\overline{IRQ1}$/FT/OUT, $\overline{IRQ2}$, FT/$\overline{RST}$, $\overline{RST}$				5.5	V
V_{BAT}	Backup supply voltage (battery or capacitor)			2.0		5.5	V
V_{BL}	Battery low (BL bit) threshold				2.5		V
I_{BAT}	Battery supply current	25 °C; V_{CC} = 0 V; OSC on; V_{BAT} = 3 V; SQW off			365	450	nA

1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 2.38 V to 5.5 V (except where noted)

Figure 27. I_{CC2} vs. temperature

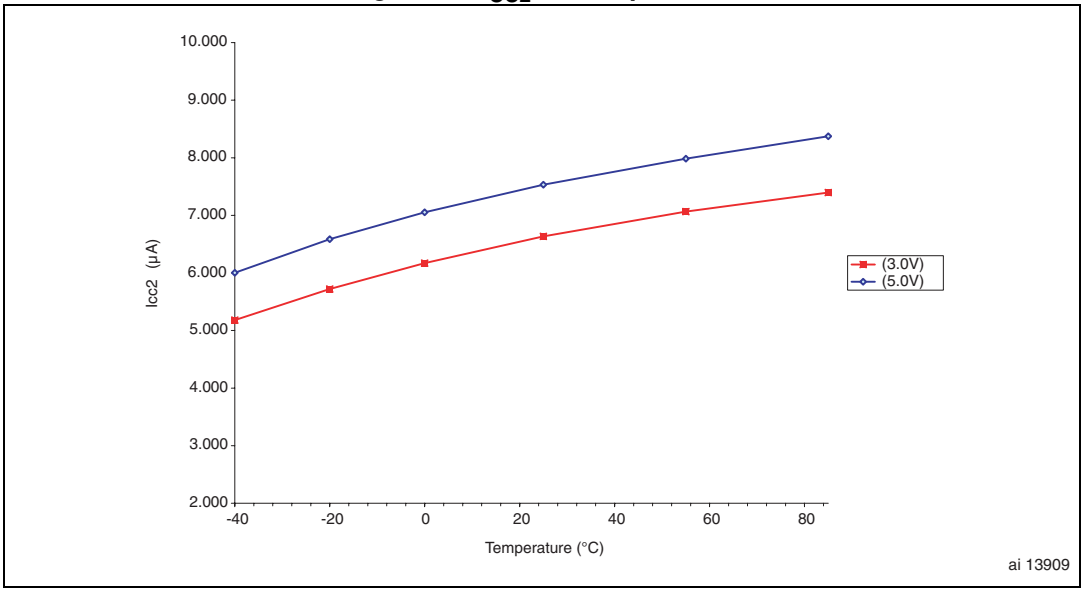


Table 22. Crystal electrical characteristics

Symbol	Parameter[1][2]	Min	Typ	Max	Units
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			65[3]	kΩ
C_L	Load capacitance		12.5		pF

1. Externally supplied if using the QFN16 or SO8 package. STMicroelectronics recommends the Citizen CFS-145 (1.5 x 5 mm) and the KDS DT-38 (3 x 8 mm) for thru-hole, or the KDS DMX-26S (3.2 x 8 mm) or Micro Crystal MS3V-T1R (1.5 x 5 mm) for surface-mount, tuning fork-type quartz crystals.
2. Load capacitors are integrated within the M41T8x. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.
3. Guaranteed by design.

Table 23. Oscillator characteristics

Symbol	Parameter[1][2]	Conditions	Min	Typ	Max	Units
V_{STA}	Oscillator start voltage	≤ 4 s	2.0			V
t_{STA}	Oscillator start time	$V_{CC} = V_{SO}$			1	s
C_{XI}, C_{XO}[1]	Capacitor input, capacitor output			25		pF
	IC-to-IC frequency variation[2][3]		–10		+10	ppm

1. With default analog calibration value (= 0)
2. Reference value
3. T_A = 25 °C, V_{CC} = 5.0 V

Figure 28. Power down/up mode AC waveforms

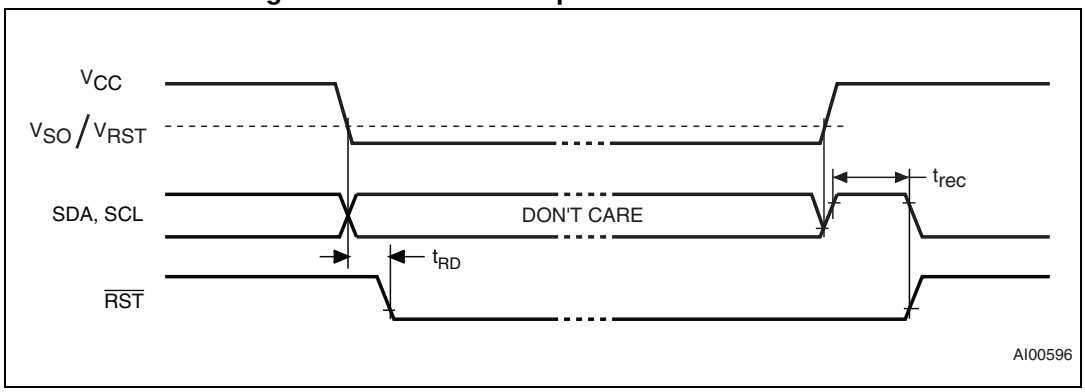


Table 24. Power down/up trip points DC characteristics

Sym	Parameter[1][2]		Min	Typ	Max	Unit
V_{RST}	Reset threshold voltage	S	2.85	2.93	3.0	V
		R	2.55	2.63	2.7	V
		Z	2.25	2.32	2.38	V
V_{SO}	Battery backup switchover			V_{RST}		V
	Hysteresis			25		mV
t_{rec}	$\overline{RST}$ duration after V_{CC} high		140		280	ms
t_{RD}	V_{CC} to reset delay[3]			2.5		µs

1. All voltages referenced to V_{SS}
2. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 2.38 to 5.5 V (except where noted)
3. Measured with V_{CC} falling slew rate of 10 mV/µs for V_{CC} in the range V_{RST} + 100 mV to V_{RST} – 100 mV

Figure 29. Bus timing requirement sequence

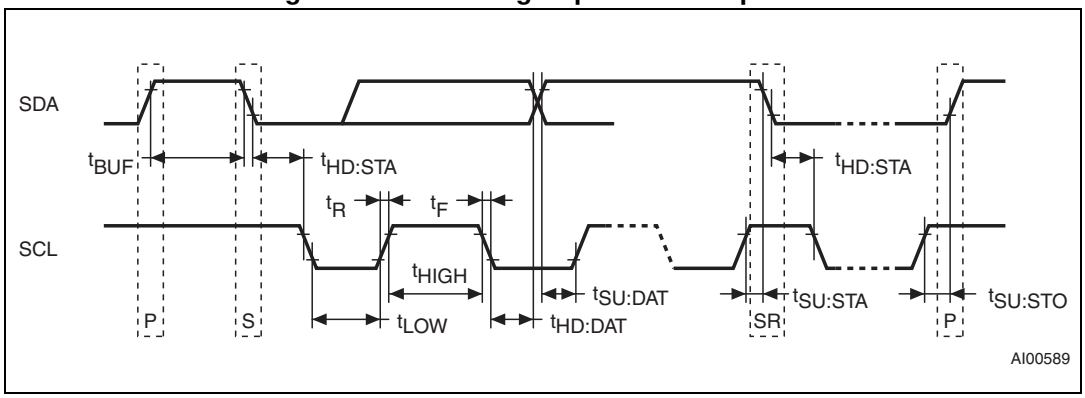


Table 25. AC characteristics

Sym	Parameter[1]	Min	Typ	Max	Units
f_{SCL}	SCL clock frequency	0		400	kHz
t_{LOW}	Clock low period	1.3			µs
t_{HIGH}	Clock high period	600			ns
t_R	SDA and SCL rise time			300	ns
t_F	SDA and SCL fall time			300	ns
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)	600			ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)	600			ns
$t_{SU:DAT}$[2]	Data setup time	100			ns
$t_{HD:DAT}$	Data hold time	0			µs
$t_{SU:STO}$	STOP condition setup time	600			ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3			µs

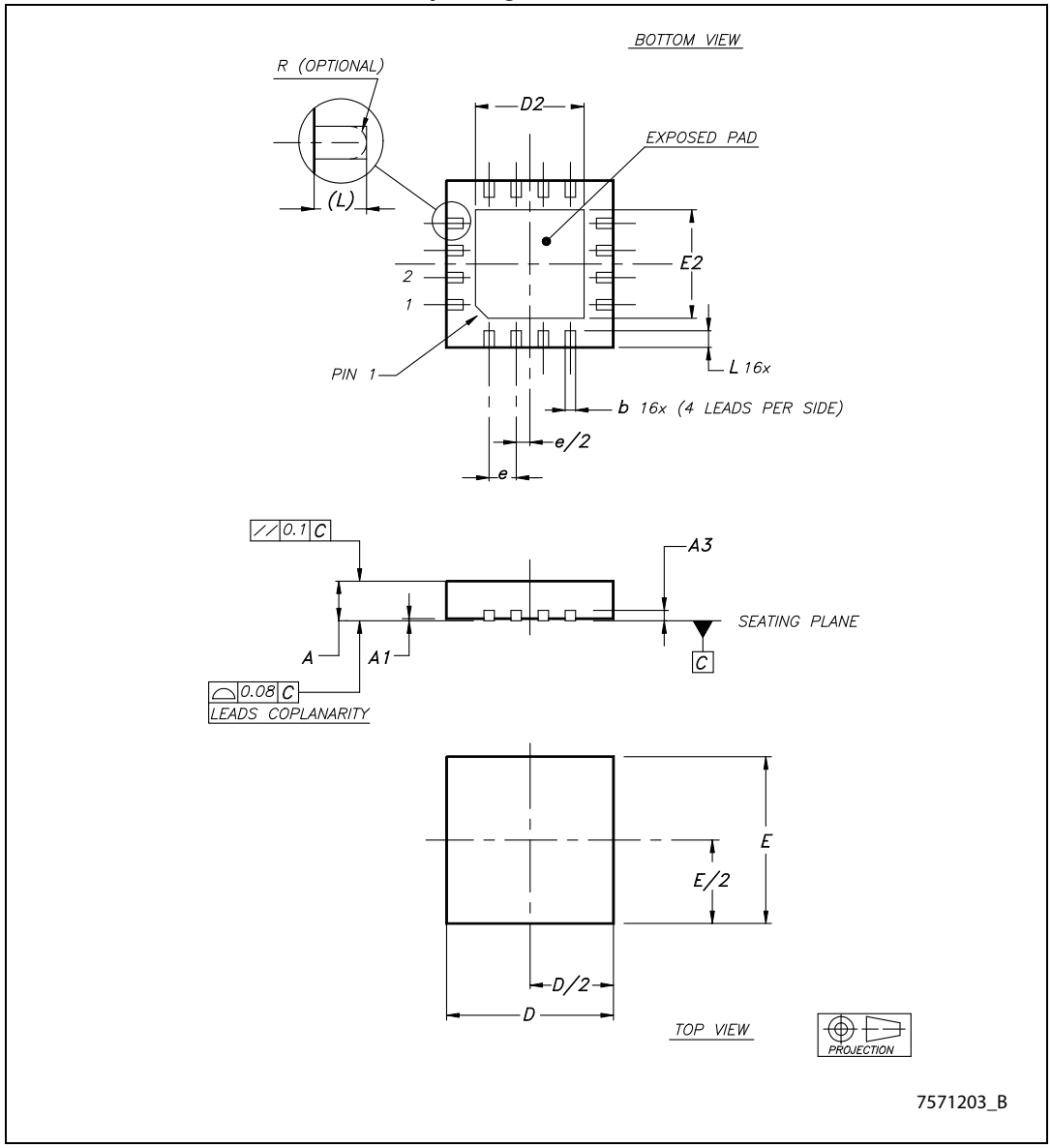
1. Valid for ambient operating temperature: T_A = –40 to 85 °C; V_{CC} = 2.38 to 5.5 V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300 ns max) of the falling edge of SCL.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 QFN16 package information

Figure 30. QFN16 – 16-lead, quad, flat package, no lead, 4 x 4 mm body size package outline

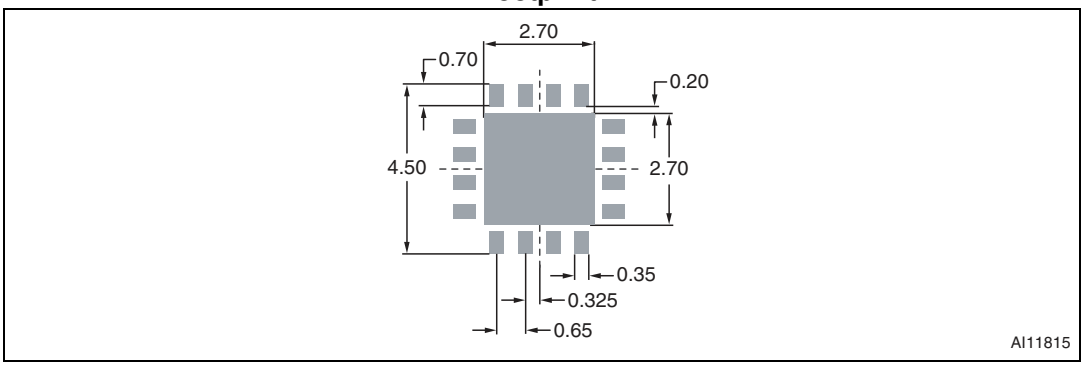


Note: Drawing is not to scale.

Table 26. QFN16 – 16-lead, quad, flat package, no lead, 4 x 4 mm package mechanical data

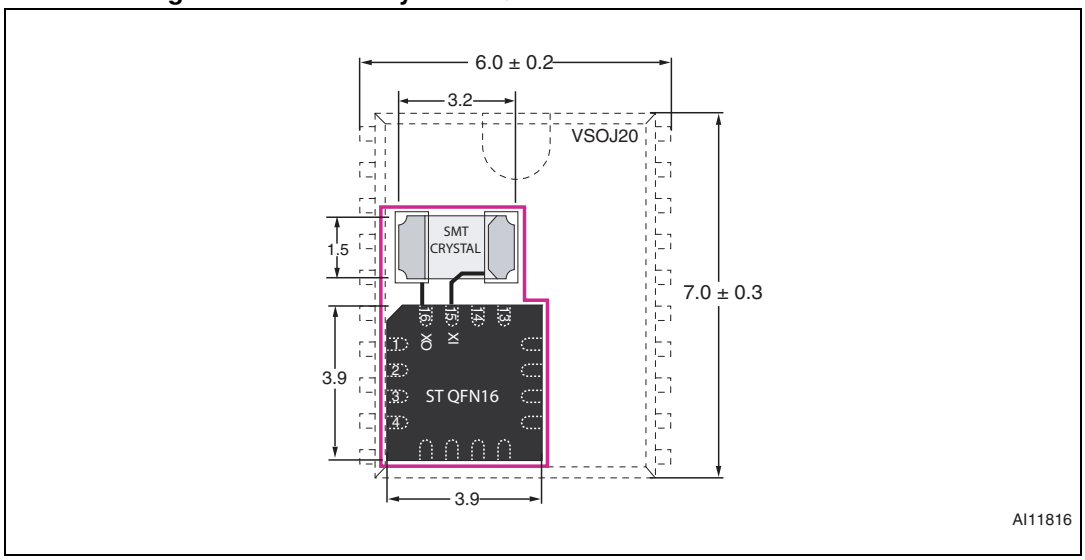
Sym	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	–	0.20	–	–	0.008	–
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.90	4.00	4.10	0.154	0.157	0.161
D2	2.50	–	2.80	0.098	–	0.110
E	3.90	4.00	4.10	0.154	0.157	0.161
E2	2.50	–	2.80	0.098	–	0.110
e	–	0.65	–	–	0.026	–
L	0.30	0.40	0.50	0.012	0.016	0.020

Figure 31. QFN16 – 16-lead, quad, flat package, no lead, 4 x 4 mm, recommended footprint



Note: Dimensions are shown in millimeters (mm).

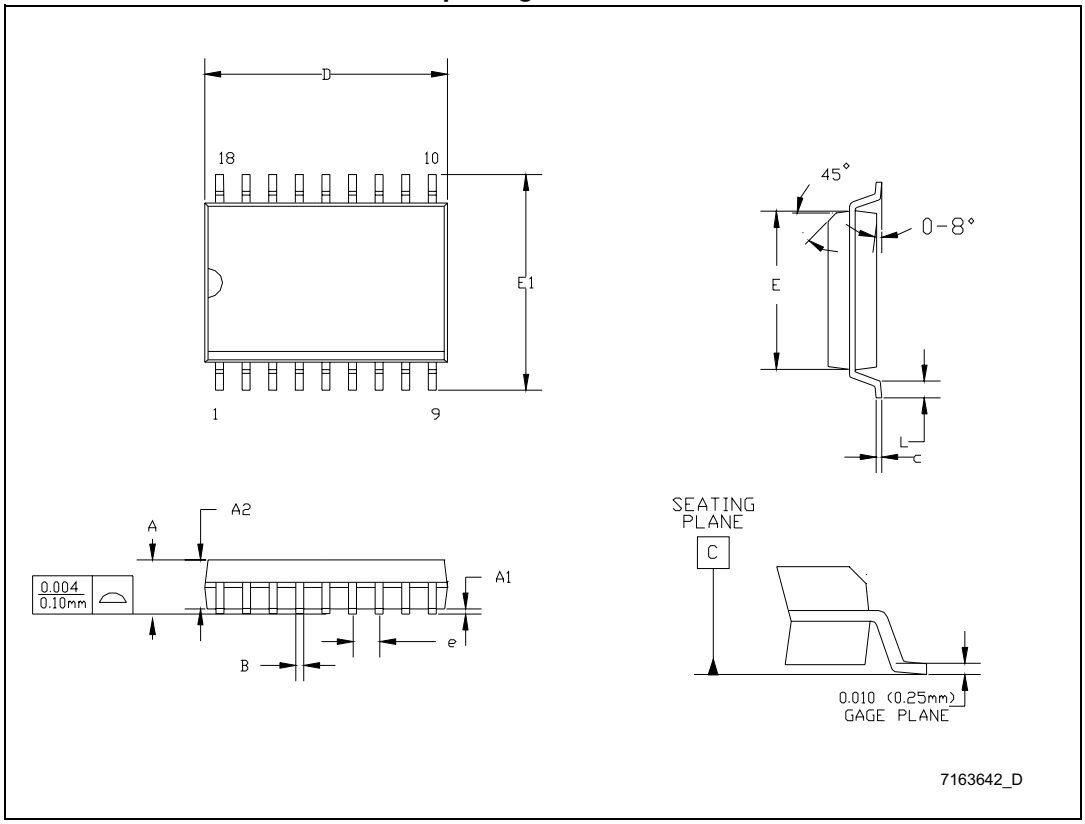
Figure 32. 32 KHz crystal + QFN16 vs. VSOJ20 mechanical data



Note: Dimensions shown are in millimeters (mm).

6.2 SOX18 package information

Figure 33. SOX18 – 18-lead plastic small outline, 300 mils, embedded crystal package outline



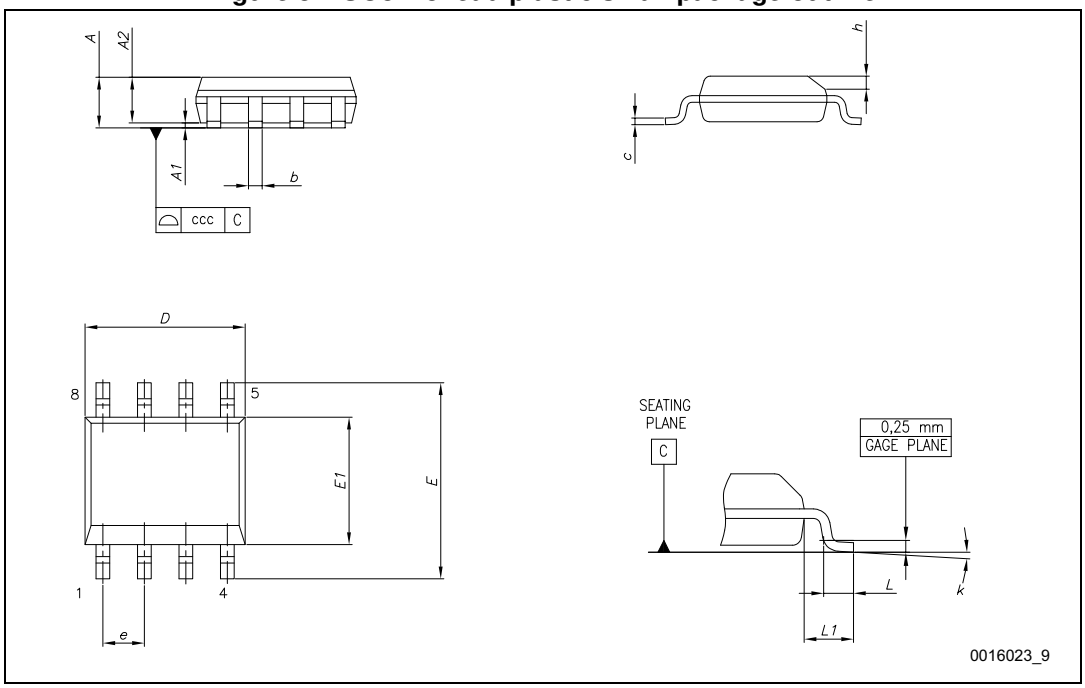
Note: Drawing is not to scale.

Table 27. SOX18 – 18-lead plastic small outline, 300 mils, embedded crystal, package mechanical data

Symbol	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.44	2.57	2.69	0.096	0.101	0.106
A1	0.15	0.23	0.31	0.006	0.009	0.012
A2	2.29	2.34	2.39	0.090	0.092	0.094
B	0.41	0.46	0.51	0.016	0.018	0.020
c	0.20	0.25	0.31	0.008	0.010	0.012
D	11.56	11.61	11.66	0.455	0.457	0.459
E	7.57	7.62	7.67	0.298	0.300	0.302
E1	10.16	10.34	10.52	0.400	0.407	0.414
e	–	1.27	–	–	0.050	–
L	0.51	0.66	0.81	0.020	0.026	0.032

6.3 SO8 package information

Figure 34. SO8 – 8-lead plastic small package outline



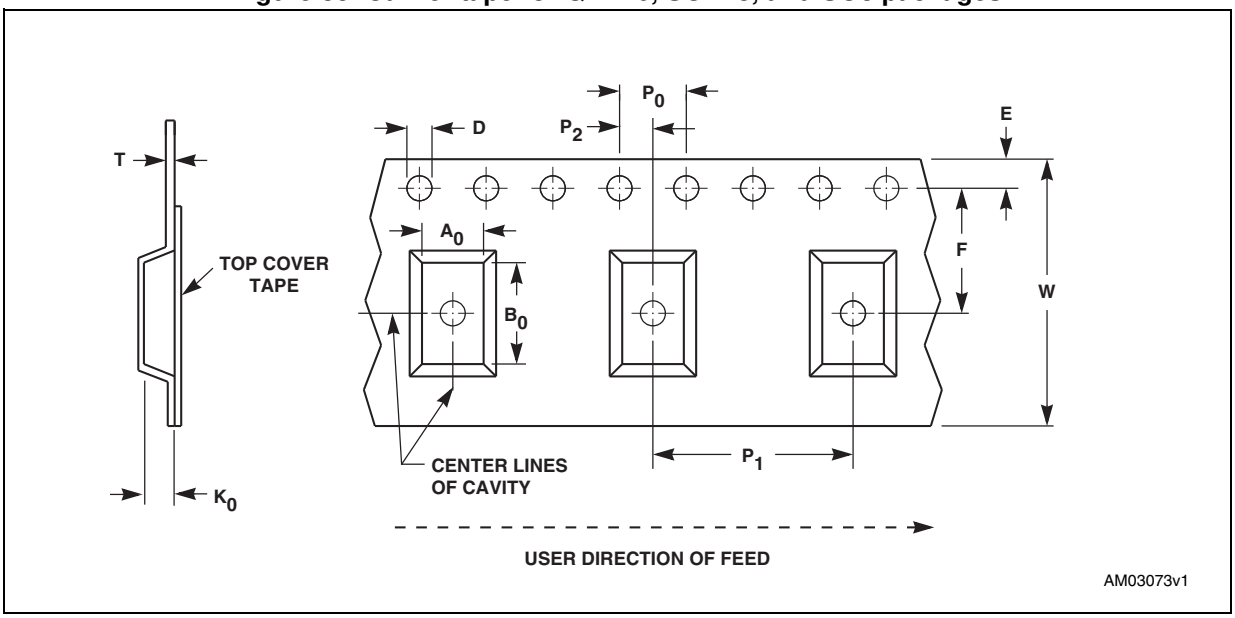
Note: Drawing is not to scale.

Table 28. SO8 – 8-lead plastic small outline (150 mils body width) package mechanical data

Symbol	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.31		0.51	0.012		0.020
c	0.17		0.25	0.007		0.010
ccc			0.10			0.004
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	-	1.27	-	-	0.050	-
h	0.25		0.50	0.010		0.020
k	0°		8°	0°		8°
L	0.40		1.27	0.016		0.050
L1		1.04			0.041	

6.4 Carrier tape information

Figure 35. Carrier tape for QFN16, SOX18, and SO8 packages



Note: Pin 1 orientation is according to EIA standards.

Table 29. Carrier tape dimensions for QFN16, SOX18, and SO8 packages

Package	W	D	E	P_0	P_2	F	A_0	B_0	K_0	P_1	T	Unit	Bulk Qty
QFN16	12.00 ±0.30	1.50 +0.10/ −0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	5.50 ±0.05	4.30 ±0.10	4.30 ±0.10	1.10 ±0.10	8.00 ±0.10	0.30 ±0.05	mm	1000
SOX18	24.00 ±0.30	1.50 +0.10/ −0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	11.50 ±0.10	12.70 ±0.10	11.90 ±0.10	3.20 ±0.10	16.00 ±0.10	0.30 ±0.05	mm	1000
SO8	12.00 ±0.30	1.50 +0.10/ −0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	5.50 ±0.05	6.50 ±0.10	5.30 ±0.10	2.20 ±0.10	8.00 ±0.10	0.30 ±0.05	mm	2500

7 Part numbering

Table 30. Ordering information

Example: M41T 83 S QA 6 F

Device family

M41T

Device type

82 (SO8 package only)

83

Operating voltage

S = V_{CC} = 3.00 to 5.5 V

R = V_{CC} = 2.70 to 5.5 V

Z = V_{CC} = 2.38 to 5.5 V

Package

QA = QFN16 (4 mm x 4 mm)

M(1) = SO8

MY(2) = SOX18

Temperature range

6 = –40 °C to 85 °C

Shipping method

F = ECOPACK® package, tape & reel

1. M41T82 only
2. The SOX18 package includes an embedded 32,768 Hz crystal.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

8 Revision history

Table 31. Document revision history

Date	Revision	Changes
09-Apr-2009	9	Updated Table 1, 2, 4, 6, 10, 11, 21, Figure 20, 28, Section 3, Section 3.4.1, Section 3.4.2, Section 3.5, Section 3.6, Section 3.7, Section 3.8, Section 3.8.2, Section 3.8.3, Section 3.8.4, Section 3.8.5, Section 3.12, Section 3.13, Section 6; added Section 3.8.1, Section 3.14, Section 3.15, Table 9, 14, 15, Figure 22, 25; removed “output driver pin” section, “alarm interrupt reset waveform” figure, “backup mode alarm waveform” figure, “timer countdown value register bits (addr 11h)” table; added tape and reel information Figure 35, Table 29.
05-Jan-2010	10	Updated Section 2.2: Read mode, Section 2.3: Write mode, Section 3: Clock operation, Section 3.1, Section 3.2, Table 25.
25-Mar-2010	11	Updated Figure 28; Table 24.
19-Oct-2010	12	Updated Note in Section 3.12: Oscillator fail detection.
12-Oct-2011	13	Updated Features, title, Section 3.1: Clock data coherency, Section 3.2: Halt bit (HT) operation; added Figure 16, added footnote 3 to Table 30: Ordering information.
16-May-2012	14	Added reference to AN1572 in Section 3.2.1: Power-down time-stamp; textual update to Section 3.17: OTP bit operation (M41T83 in SOX18 package only); updated test condition for IBAT in Table 21: DC characteristics; removed shipping method in tubes from Table 30: Ordering information.
26-Oct-2012	15	Textual update concerning reflow (Features, Section 3.17); removed footnote 3 of Table 18; updated footnote 1 of Table 22; removed Section 8: References.
04-Dec-2013	16	Updated Section 3.4.2: Analog calibration (programmable load capacitance); moved and updated Section 3.4.3: Pre-programmed calibration value; updated Section 3.11: Century bits and added Figure 24; updated Section 3.17; updated footnote 2 of Table 18: Absolute maximum ratings.
08-Jan-2015	17	Added clarification concerning pin 1 orientation in carrier tape (Figure 35: Carrier tape for QFN16, SOX18, and SO8 packages).
02-Jun-2015	18	Updated Figure 30, Figure 33, Figure 34 and dimensions b, c, and L in Table 28. Removed dimension ddd from Table 26.
08-Apr-2024	19	Updated code watchdog resolution bits in *Table 3* and *Table 5*.

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