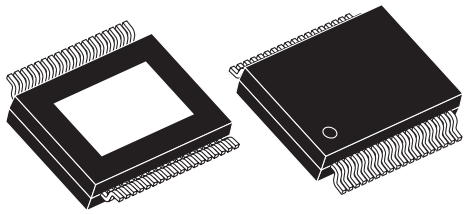
TDA7491LP

2 x 5-watt dual BTL class-D audio amplifier

Features

- 5 W + 5 W continuous output power: R_L = 8 Ω, THD = 10% at V_{CC} = 9 V
- 5 W + 5 W continuous output power: R_L = 4 Ω, THD = 10% at V_{CC} = 6.6 V
- Wide range single supply operation (5 V - 14 V)
- High efficiency (η = 90%)
- Four selectable, fixed gain settings of nominally 20 dB, 26 dB, 30 dB and 32 dB
- Differential inputs minimize common-mode noise
- Filterless operation
- No ‘pop’ at turn-on/off
- Standby and mute features
- Short-circuit protection
- Thermal overload protection
- Externally synchronizable



PowerSSO-36 with exposed pad down

Description

The TDA7491LP is a dual BTL class-D audio amplifier with single power supply designed for LCD TVs and monitors.

Thanks to the high efficiency and exposed-pad-down (EPD) package no separate heatsink is required.

Furthermore, the filterless operation allows a reduction in the external component count.

The TDA7491LP is pin-to-pin compatible with the TDA7491P and TDA7491HV.

Table 1. Device summary

Order code	Operating temperature	Package	Packaging
TDA7491LP	-40 to 85 °C	PowerSSO-36 EPD	Tube
TDA7491LP13TR	-40 to 85 °C	PowerSSO-36 EPD	Tape and reel

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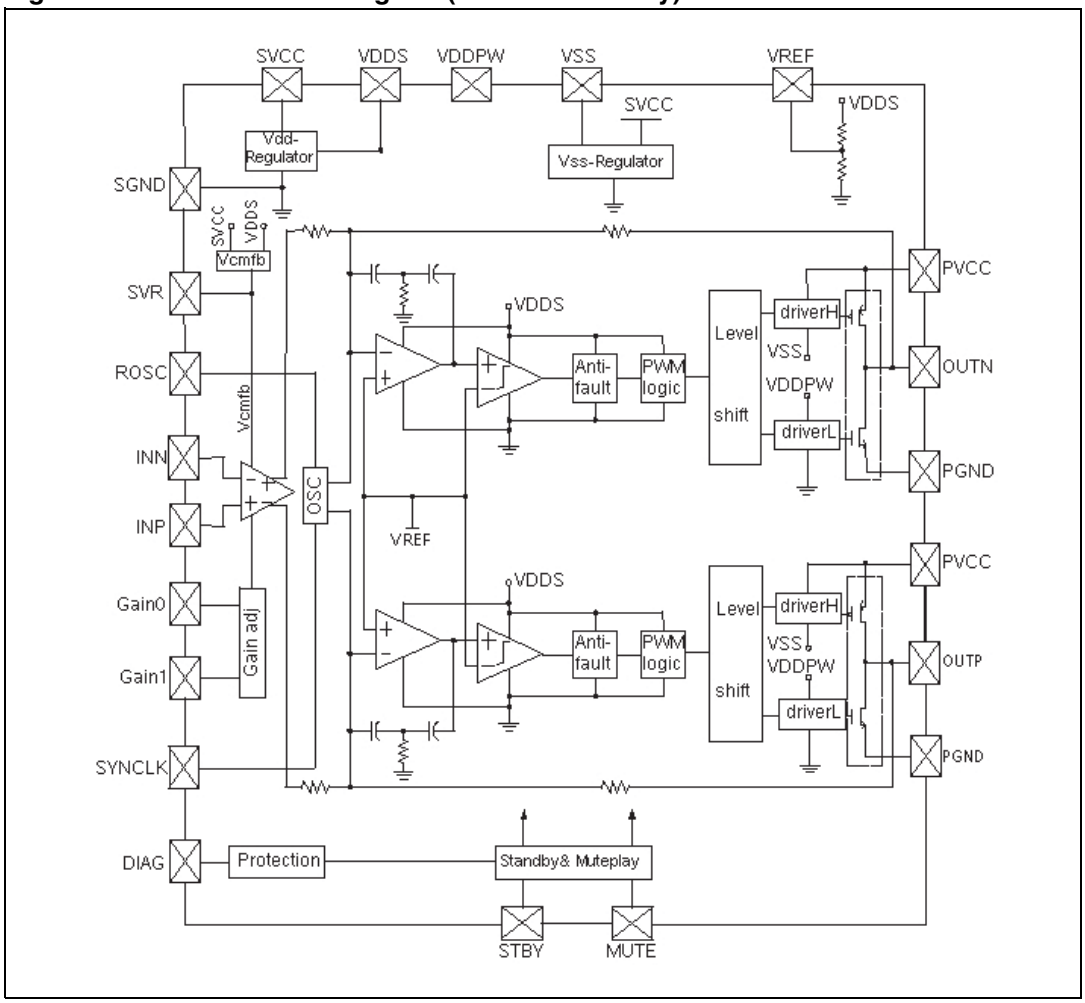
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1 Device block diagram

Figure 1 shows the block diagram of one of the two identical channels of the TDA7491LP.

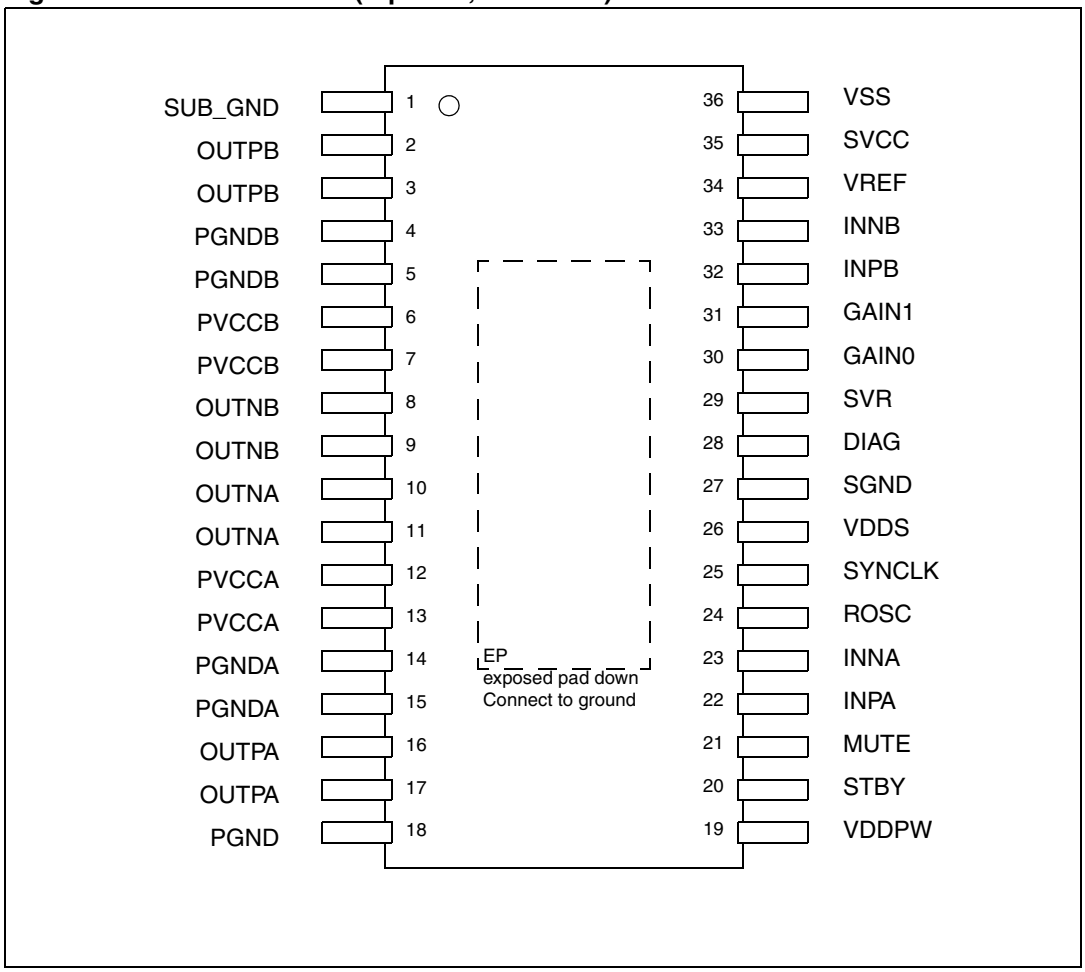
Figure 1. Internal block diagram (one channel only)



2 Pin description

2.1 Pin out

Figure 2. Pin connection (top view, PCB view)



2.2 Pin list

Table 2. Pin description list

Number	Name	Type	Description
1	SUB_GND	POWER	Connect to the frame
2,3	OUTPB	OUT	Positive PWM output for right channel
4,5	PGNDB	POWER	Power stage ground for right channel
6,7	PVCCB	POWER	Power supply for right channel
8,9	OUTNB	OUT	Negative PWM output for right channel
10,11	OUTNA	OUT	Negative PWM output for left channel
12,13	PVCCA	POWER	Power supply for left channel
14,15	PGNDA	POWER	Power stage ground for left channel
16,17	OUTPA	OUT	Positive PWM output for left channel
18	PGND	POWER	Power stage ground
19	VDDPW	OUT	3.3-V (nominal) regulator output referred to ground for power stage
20	STBY	INPUT	Standby mode control
21	MUTE	INPUT	Mute mode control
22	INPA	INPUT	Positive differential input of left channel
23	INNA	INPUT	Negative differential input of left channel
24	ROSC	OUT	Master oscillator frequency-setting pin
25	SYNCLCK	IN/OUT	Clock in/out for external oscillator
26	VDDS	OUT	3.3-V (nominal) regulator output referred to ground for signal blocks
27	SGND	POWER	Signal ground
28	DIAG	OUT	Open-drain diagnostic output
29	SVR	OUT	Supply voltage rejection
30	GAIN0	INPUT	Gain setting input 1
31	GAIN1	INPUT	Gain setting input 2
32	INPB	INPUT	Positive differential input of right channel
33	INNB	INPUT	Negative differential input of right channel
34	VREF	OUT	Half VDDS (nominal) referred to ground
35	SVCC	POWER	Signal power supply
36	VSS	OUT	3.3-V (nominal) regulator output referred to power supply
-	EP	-	Exposed pad for ground-plane heatsink, to be connected to GND

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	18	V
V_I	Voltage limits for input pins STBY, MUTE, INNA, INPA, INNB, INPB, GAIN0, GAIN1	-0.3 to 3.6	V
T_{op}	Operating temperature	-40 to 85	°C
T_j	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-40 to 150	°C

3.2 Thermal data

Refer also to *Section 5.9: Heatsink requirements on page 32*.

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j\text{-}case}$	Thermal resistance, junction to case	-	2	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance, junction to ambient	-	24	-	

3.3 Electrical specifications

Unless otherwise stated, the results in *Table 5* below are given for the conditions: V_{CC} = 9 V, R_L (load) = 8Ω, R_{OSC} = R3 = 39 kΩ, C8 = 100 nF, f = 1 kHz, G_V = 20 dB, and T_{amb} = 25 °C.

Table 5. Electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage	-	5	-	14	V
I_q	Total quiescent current	Without LC filter	-	26	35	mA
I_{qSTBY}	Quiescent current in standby	-	-	-	10	µA
V_{OS}	Output offset voltage	Play mode	-100	-	100	mV
		Mute mode	-60	-	60	mV
I_{OCP}	Overcurrent protection threshold	R_L = 0 Ω	3	-	-	A
T_j	Junction temperature at thermal shutdown	-	-	150	-	°C
R_i	Input resistance	Differential input	54	68	-	kΩ
V_{UVP}	Undervoltage protection threshold	-	-	-	4.5	V
R_{dsON}	Power transistor on resistance	High side	-	0.2	-	Ω
		Low side	-	0.2	-	
P_o	Output power	THD = 10%	-	5.0	-	W
		THD = 1%	-	4.0	-	
P_o	Output power	R_L = 4 Ω, THD = 10%, V_{CC} = 6.6 V	-	5.0	-	W
		R_L = 4 Ω, THD = 1%, V_{CC} = 6.6 V	-	4.0	-	
P_D	Dissipated power	P_o = 5 W + 5 W, THD = 10%	-	1.0	-	W
η	Efficiency	P_o = 5 W + 5 W, R_L = 8 Ω, THD = 10%, V_{CC} = 9 V	-	90	-	%
THD	Total harmonic distortion	P_o = 1 W	-	0.1	-	%
G_V	Closed loop gain	GAIN0 = L, GAIN1 = L	18	20	22	dB
		GAIN0 = L, GAIN1 = H	24	26	28	
		GAIN0 = H, GAIN1 = L	28	30	32	
		GAIN0 = H, GAIN1 = H	30	32	34	
ΔG_V	Gain matching	-	-1	-	1	dB
CT	Crosstalk	f = 1 kHz, P_o = 1 W	-	70	-	dB
eN	Total input noise	A Curve, G_V = 20 dB	-	15	-	µV
		f = 22 Hz to 22 kHz	-	20	-	

Table 5. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SVRR	Supply voltage rejection ratio	fr = 100 Hz, Vr = 1 Vpp, C_{SVR} = 10 µF	-	50	-	dB
T_r, T_f	Rise and fall times	-	-	40	-	ns
f_{SW}	Switching frequency	Internal oscillator, master mode	290	320	350	kHz
f_{SWR}	Switching frequency range	(1)	250	-	400	kHz
V_{inH}	Digital input high (H)	-	2.3	-	-	V
V_{inL}	Digital input low (L)		-	-	0.8	
A_{MUTE}	Mute attenuation	V_{MUTE} = low, V_{STBY} = high	-	80	-	dB
Function mode	Standby, mute and play modes	V_{STBY} < 0.5 V V_{MUTE} = X	Standby			-
		V_{STBY} > 2.9 V V_{MUTE} < 0.8 V	Mute			-
		V_{STBY} > 2.9 V V_{MUTE} > 2.9 V	Play			-

1. Refer to *Section 5.5: Internal and external clocks on page 27*.

4 Characterization curves

The following characterization curves were made using the TDA7491LP demo board. The LC filter for the 4-Ω load uses components of 15 µH and 470 nF and that for the 8-Ω load uses 33 µH and 220 nF.

4.1 With 4-Ω load at V_{CC} = 6.6 V

Figure 3. Output power vs. supply voltage

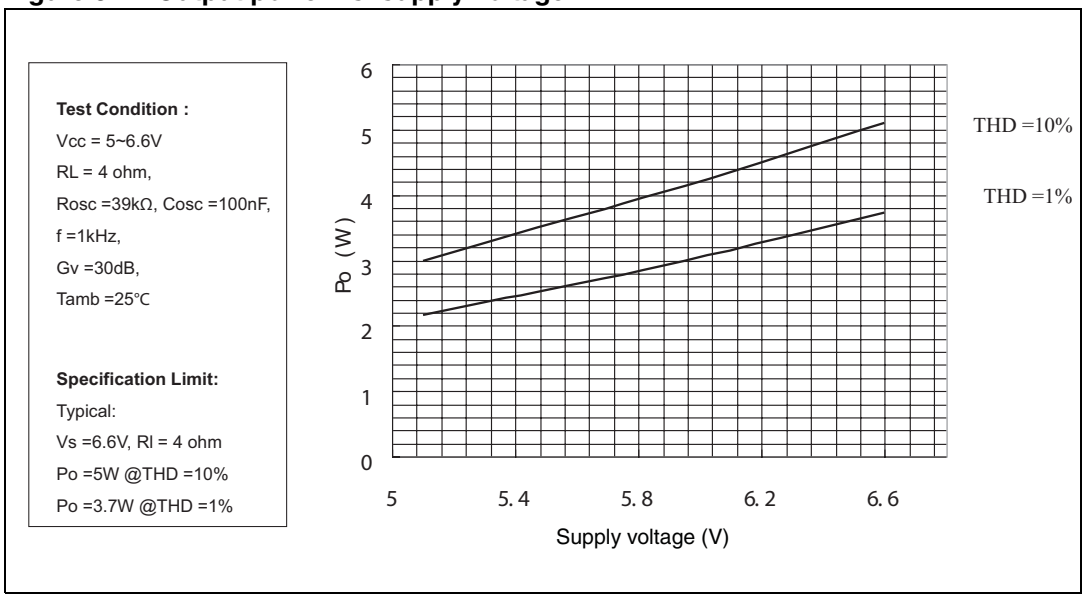


Figure 4. THD vs. output power (1 kHz)

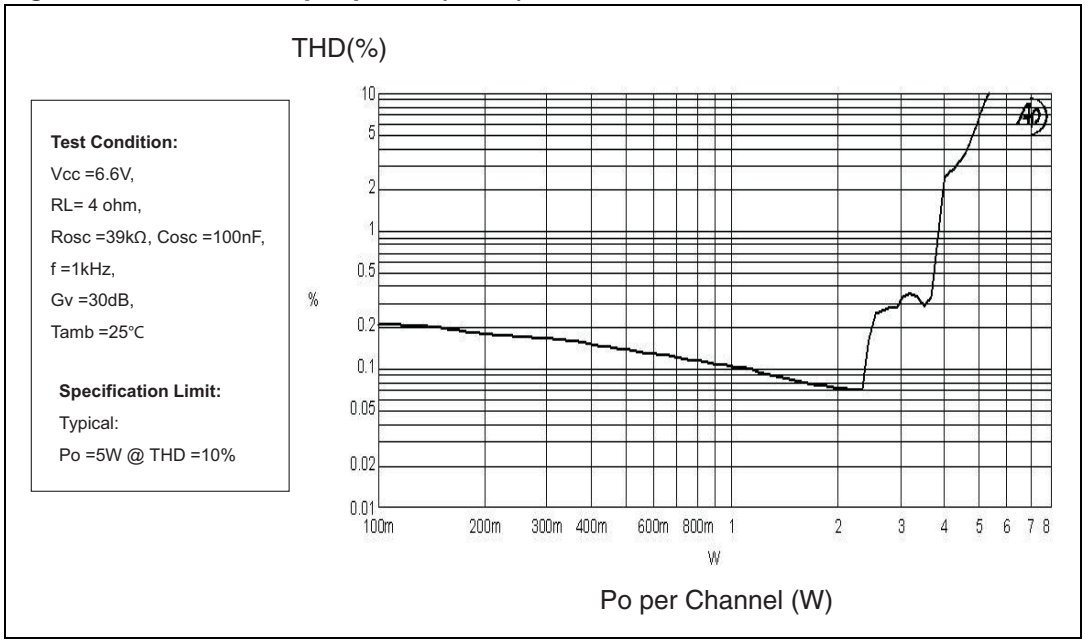


Figure 5. THD vs. output power (100 Hz)

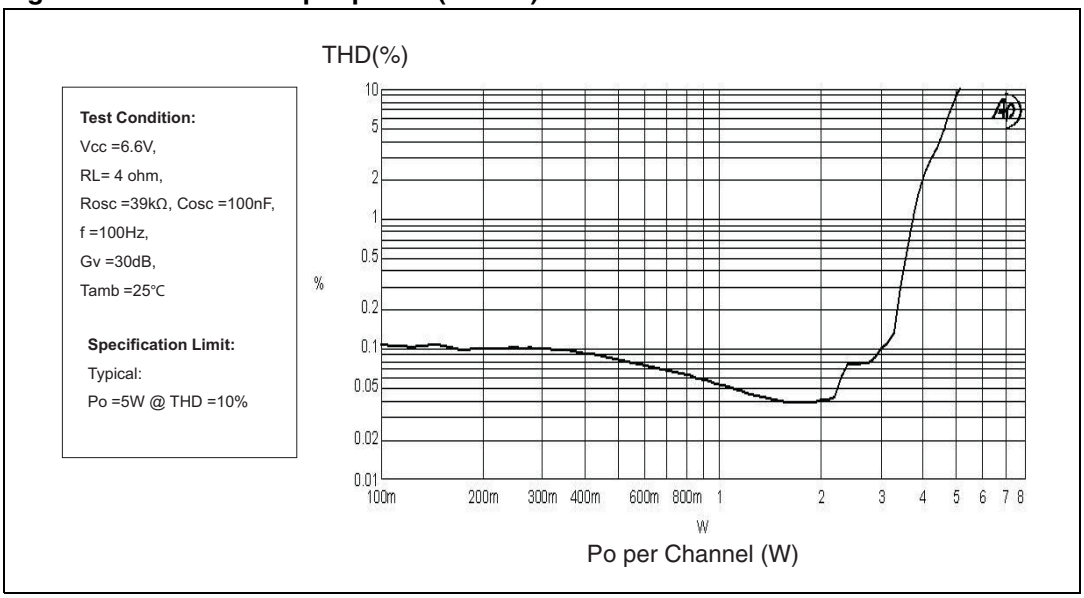


Figure 6. THD vs. frequency

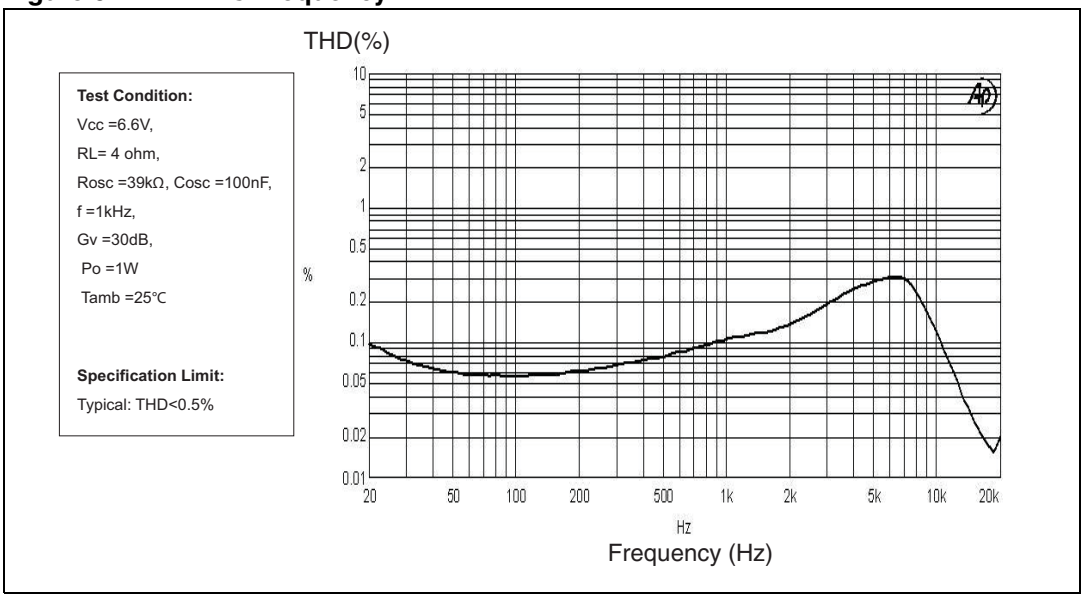


Figure 7. Frequency response

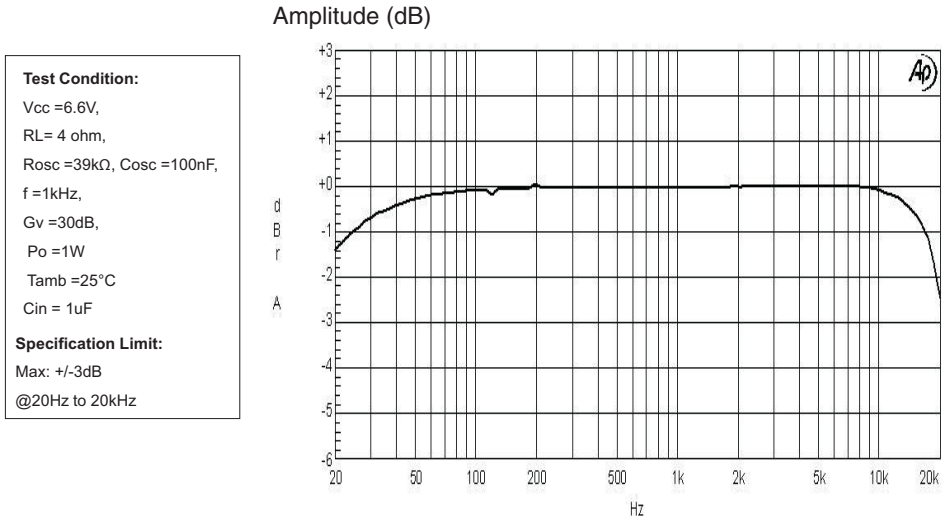


Figure 8. Crosstalk vs. frequency

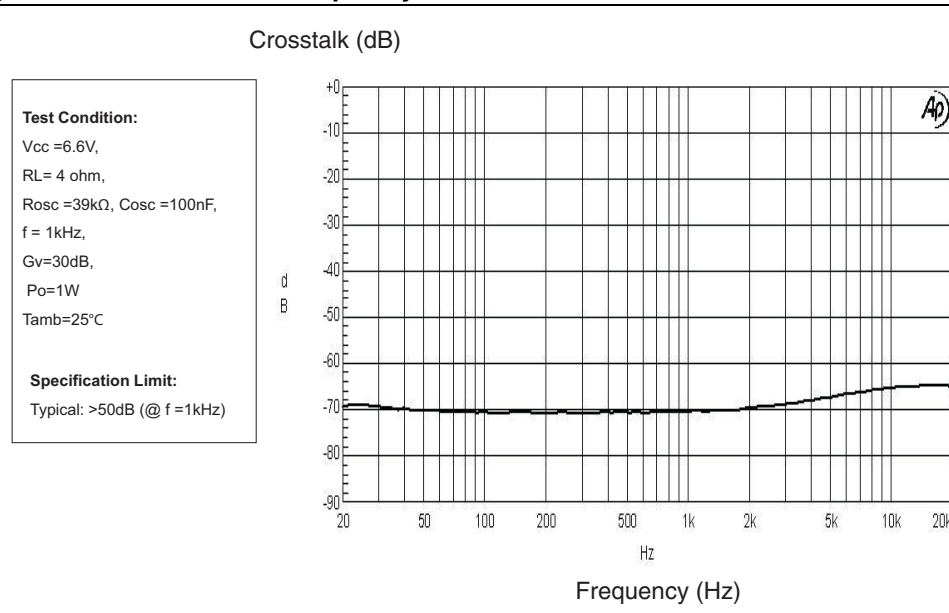


Figure 9. FFT (0 dB)

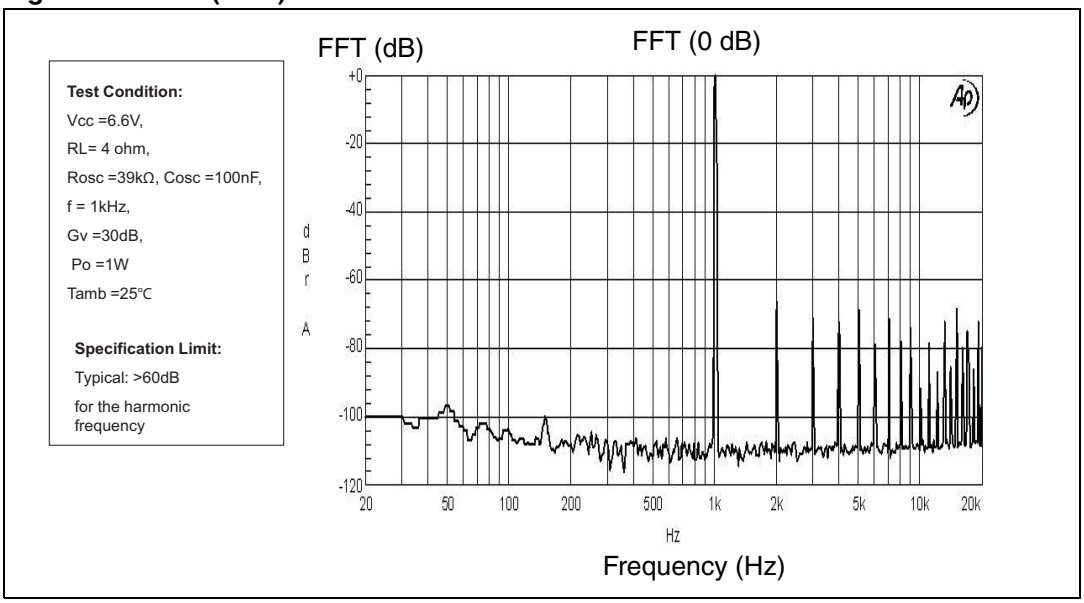


Figure 10. FFT (-60 dB)

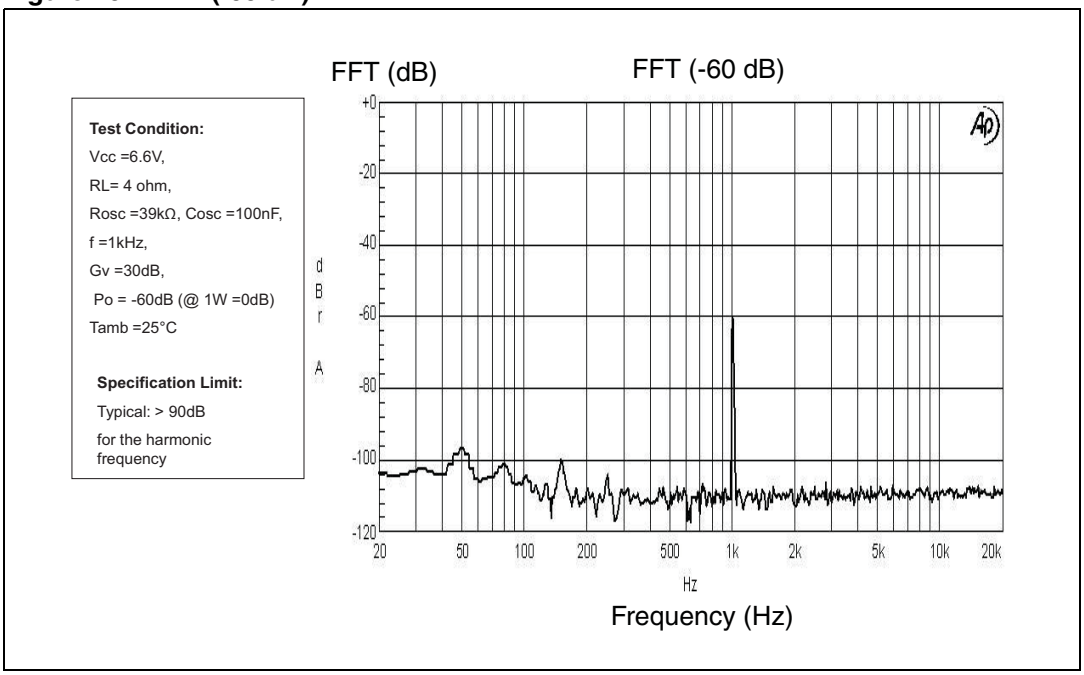


Figure 11. Power supply rejection ratio vs. frequency

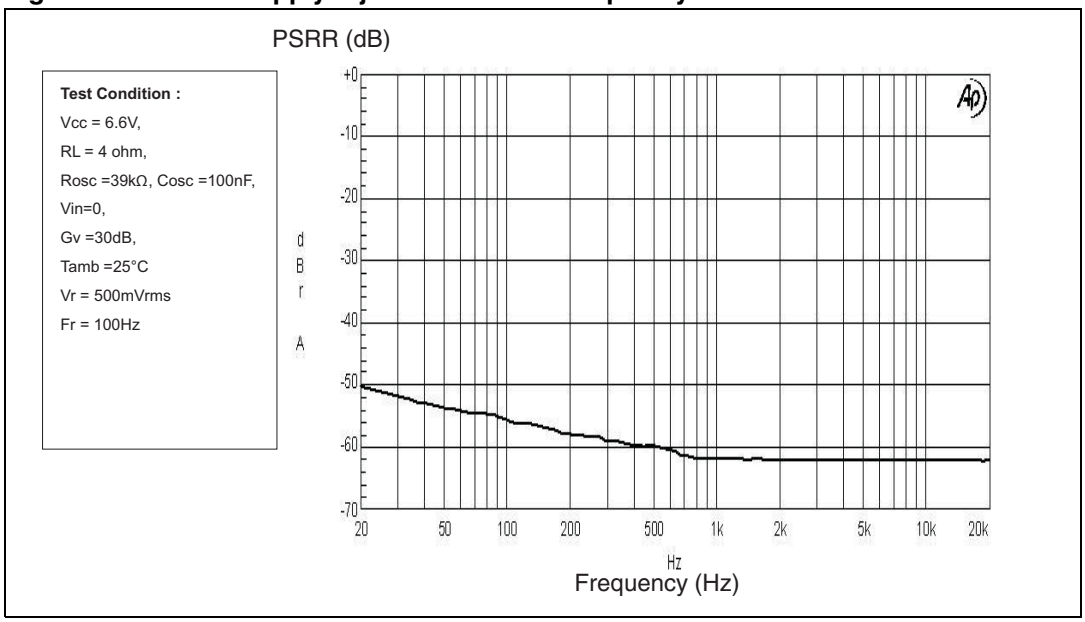


Figure 12. Power dissipation and efficiency vs. output power

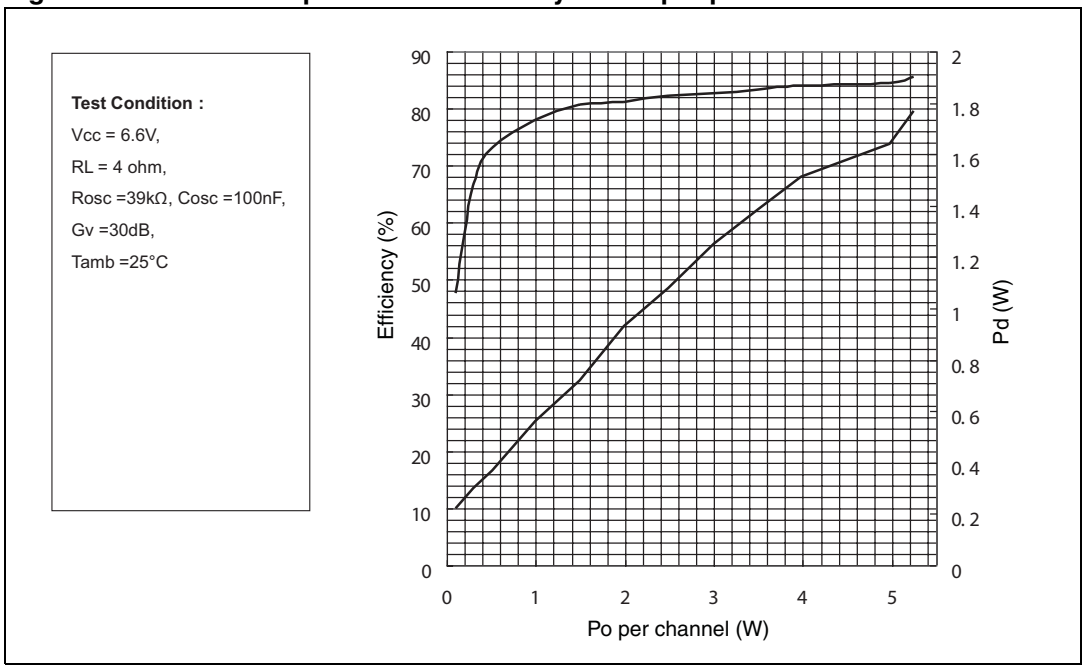


Figure 13. Attenuation vs. voltage on pin MUTE

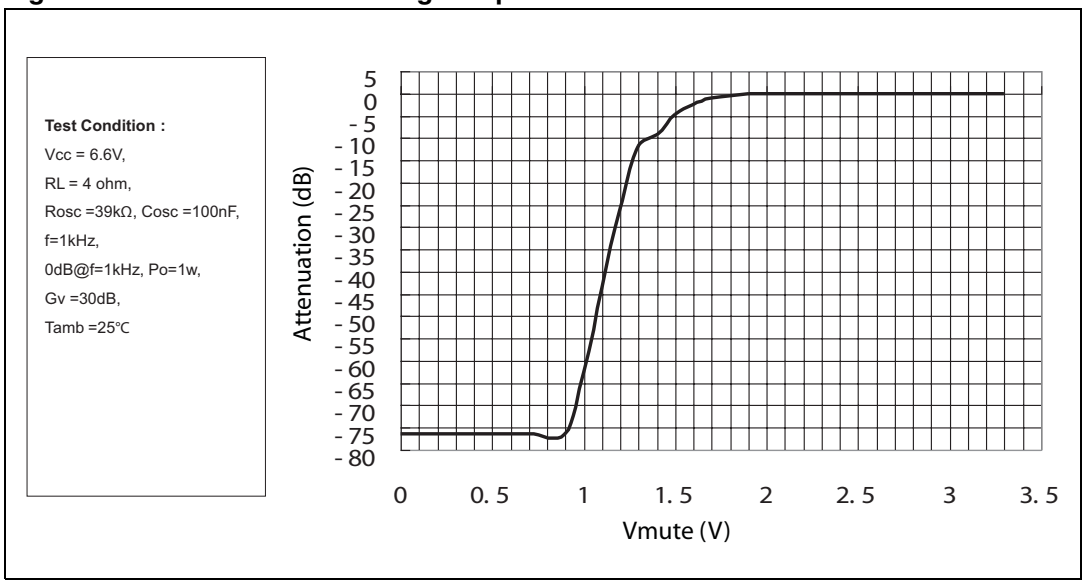


Figure 14. Current consumption vs. voltage on pin STBY

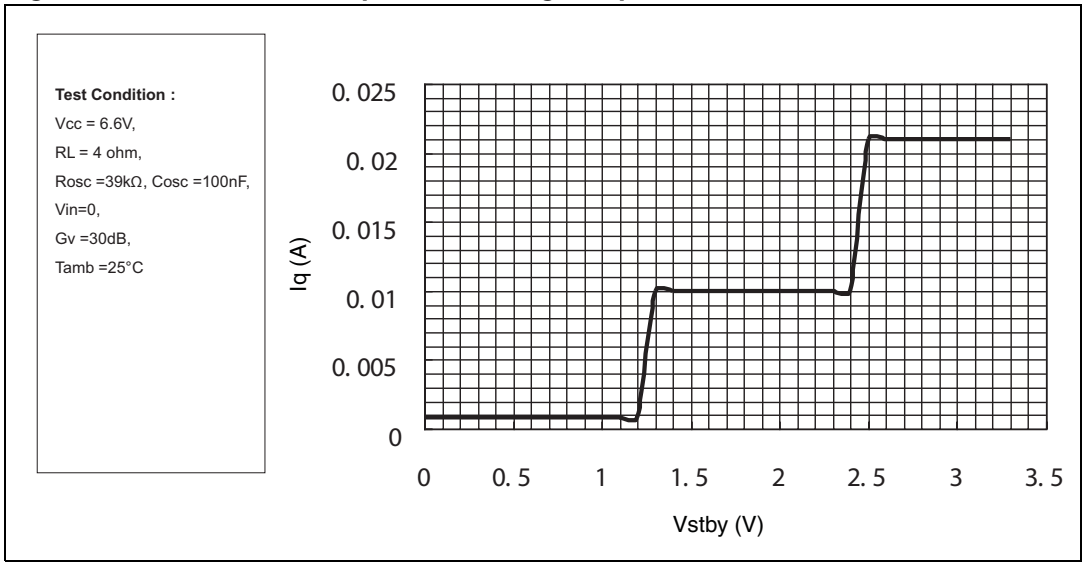
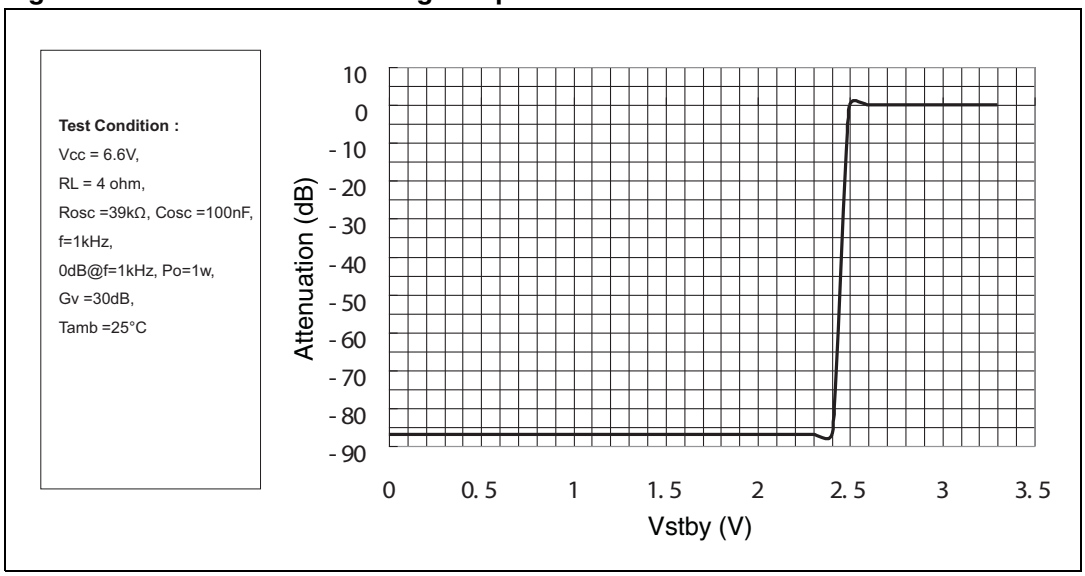


Figure 15. Attenuation vs. voltage on pin STBY



4.2 With 8-Ω load at V_{CC} = 9 V

Figure 16. Output power vs. supply voltage

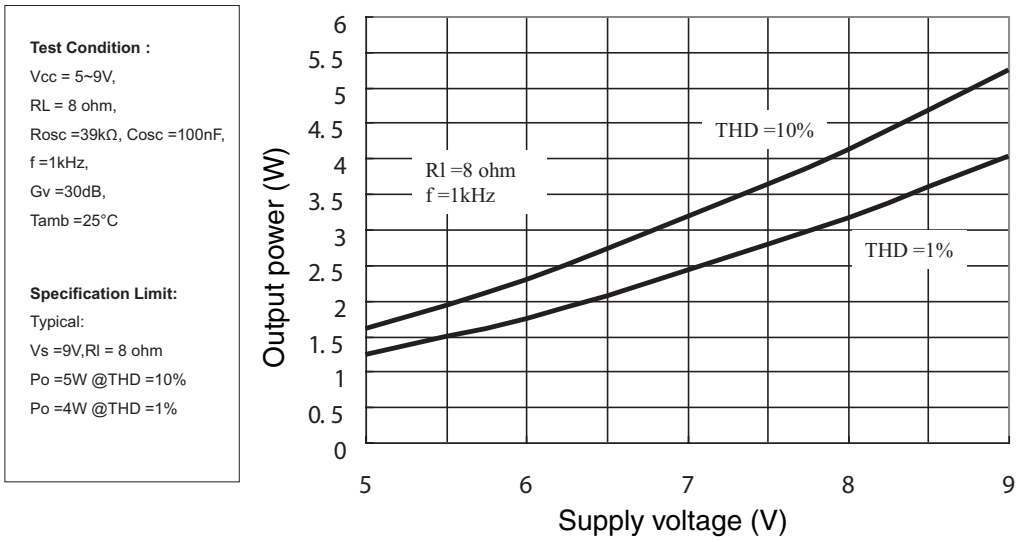


Figure 17. THD vs. output power (1 kHz)

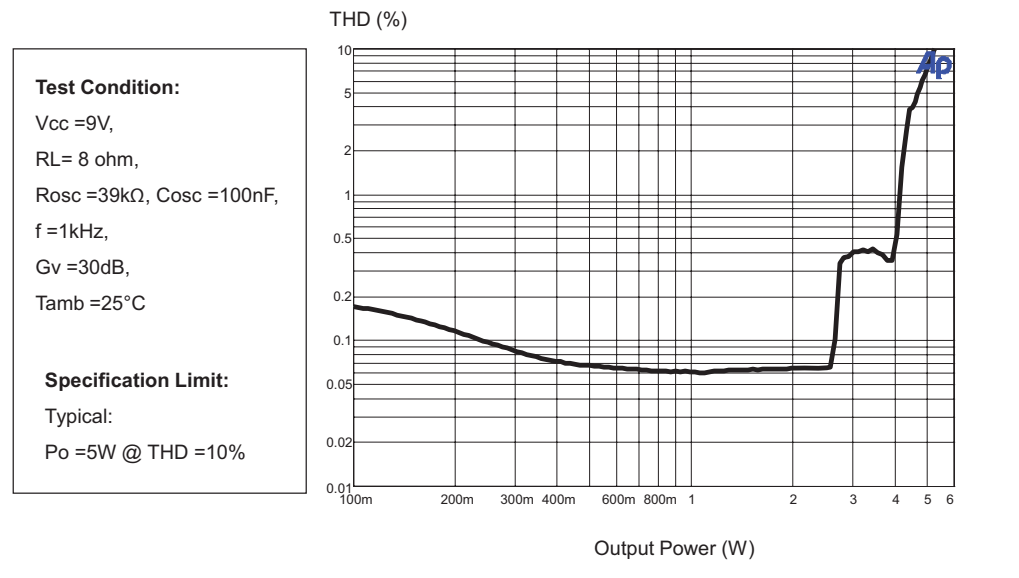


Figure 18. THD vs. output power (100 Hz)

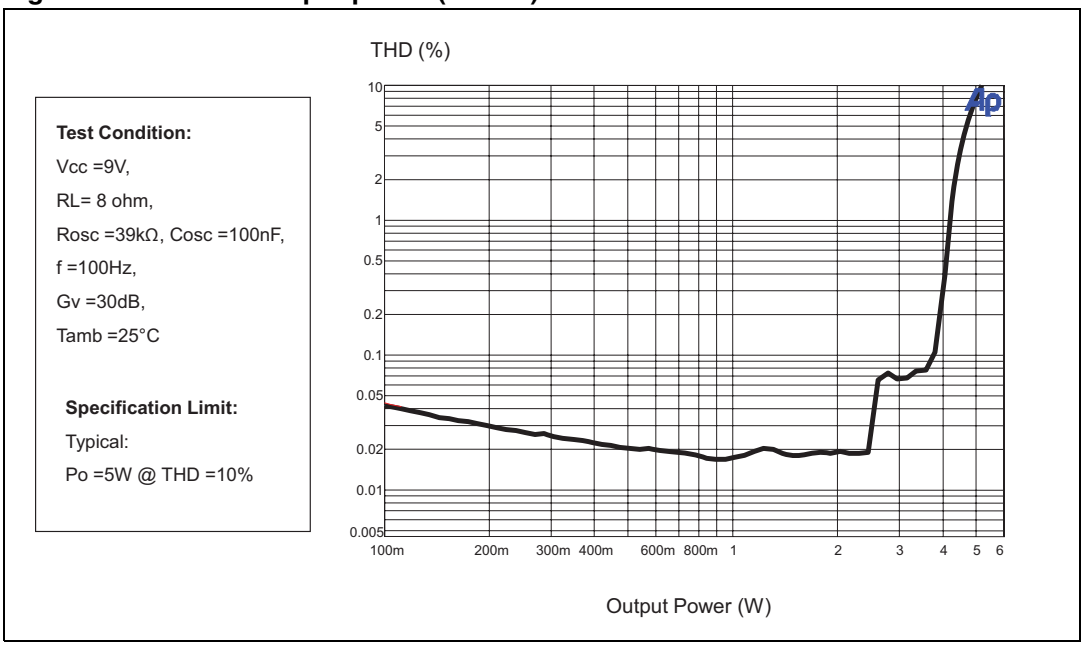


Figure 19. THD vs. frequency

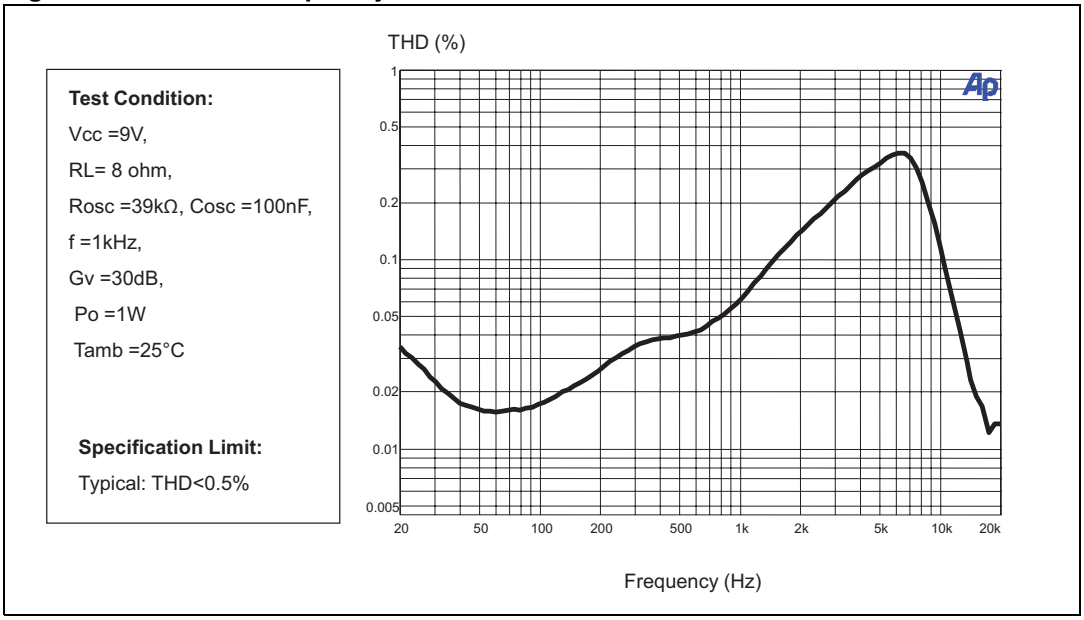


Figure 20. Frequency response

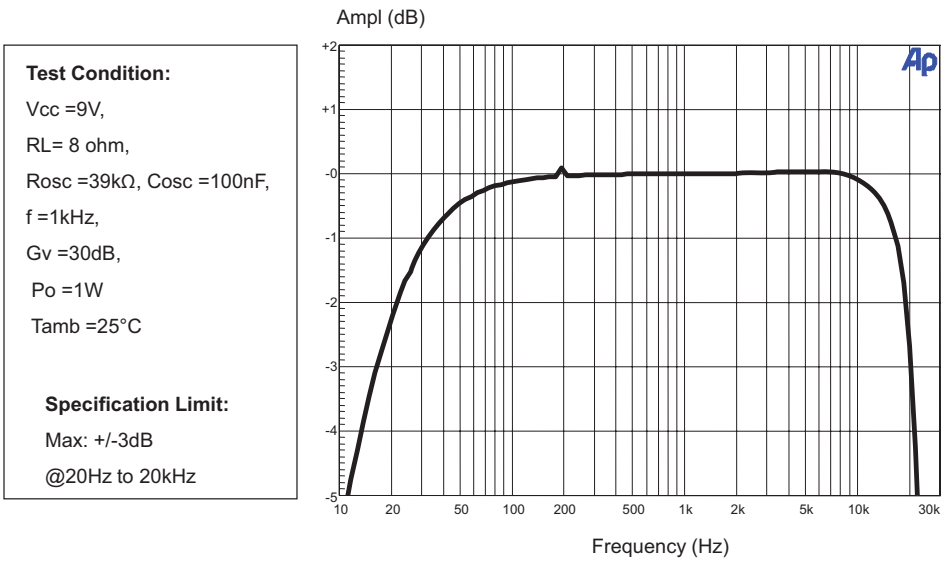


Figure 21. Crosstalk vs. frequency

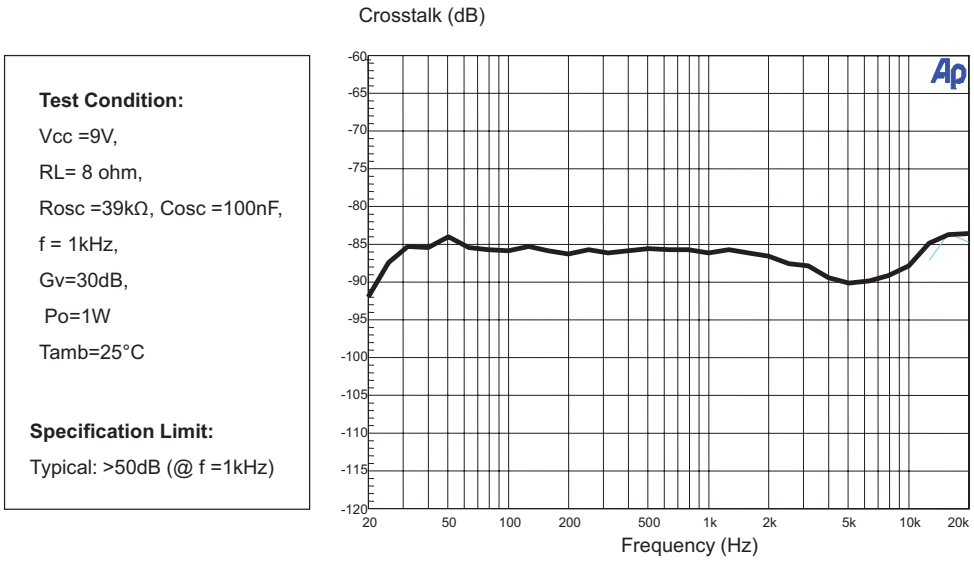


Figure 22. FFT (0 dB)

Test Condition:
Vcc =9V,
RL= 8 ohm,
Rosc =39kΩ, Cosc =100nF,
f = 1kHz,
Gv =30dB,
Po =1W
Tamb =25°C

Specification Limit:
Typical: >60dB
for the harmonic frequency

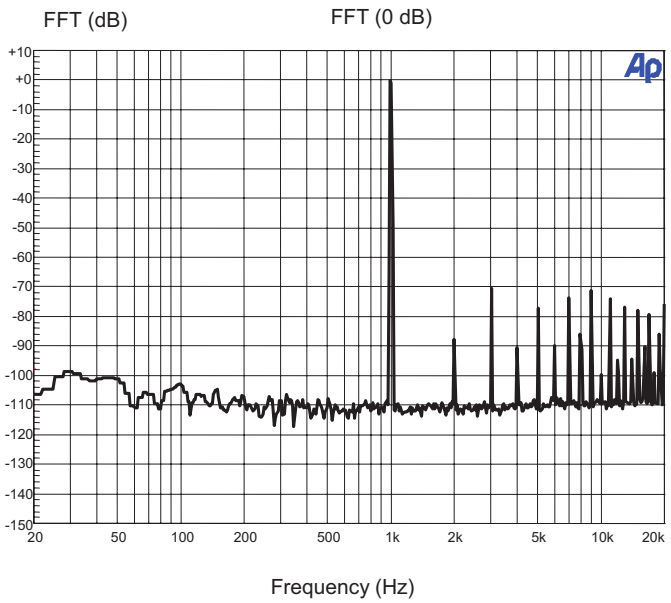


Figure 23. FFT (-60 dB)

Test Condition:
Vcc =9V,
RL= 8 ohm,
Rosc =39kΩ, Cosc =100nF,
f =1kHz,
Gv =30dB,
Po = -60dB (@ 1W =0dB)
Tamb =25°C

Specification Limit:
Typical: > 90dB
for the harmonic frequency

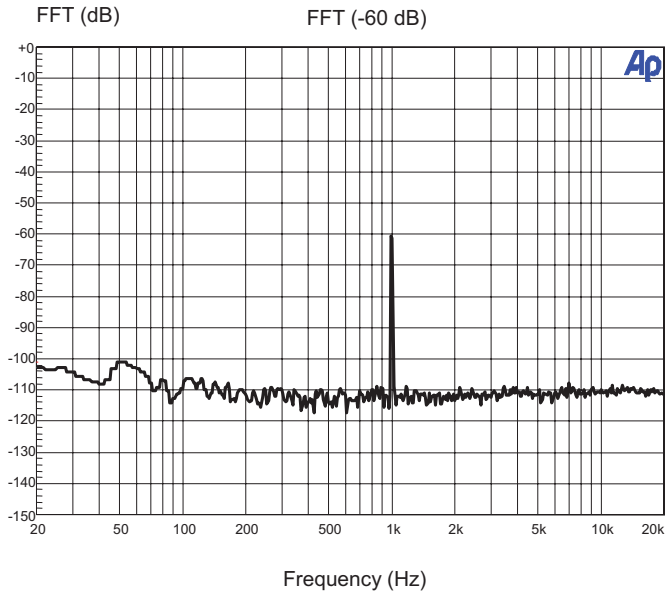


Figure 24. Power supply rejection ratio vs. frequency

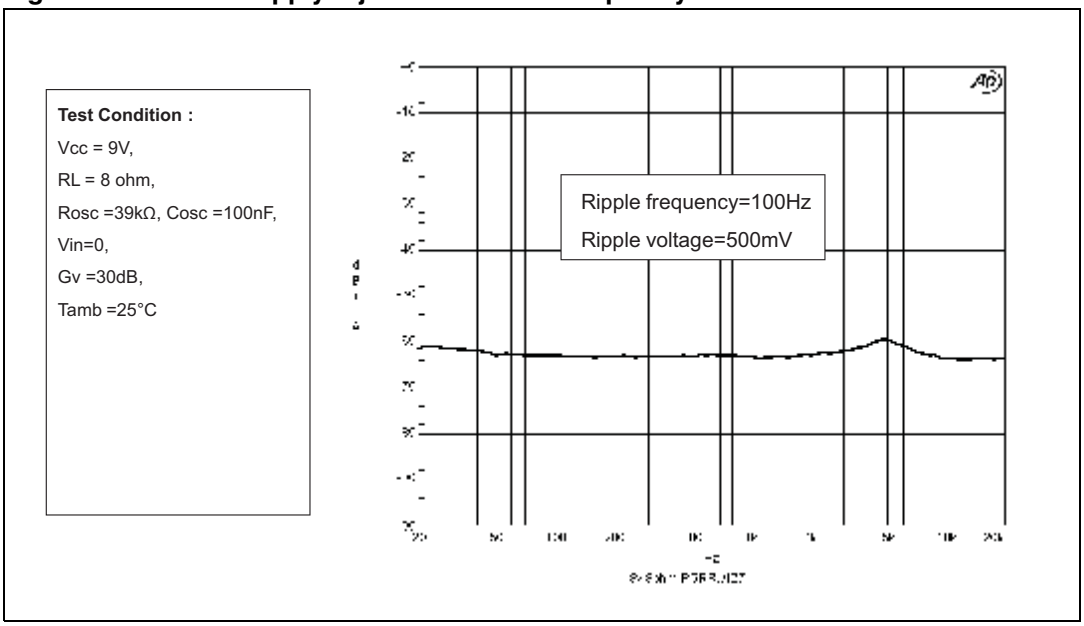
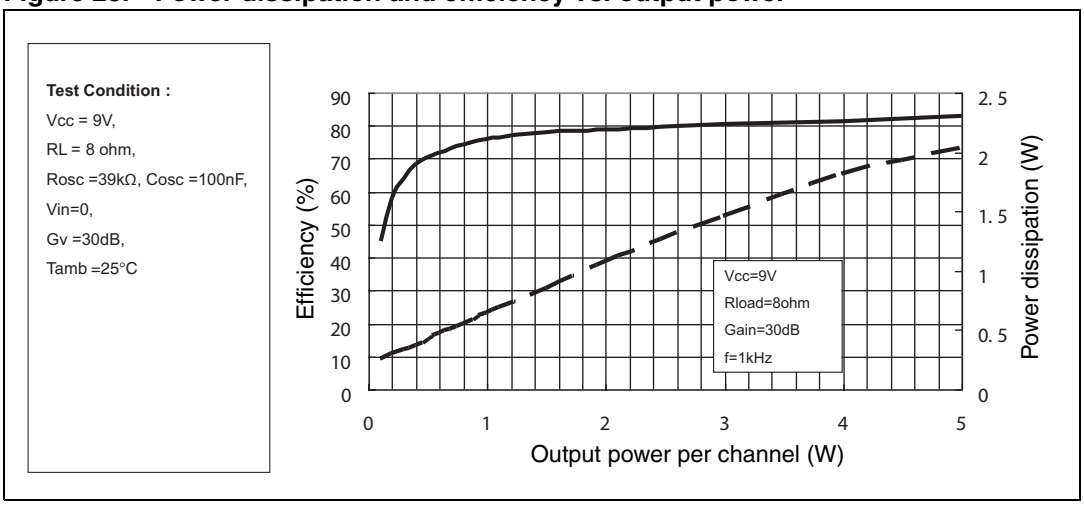


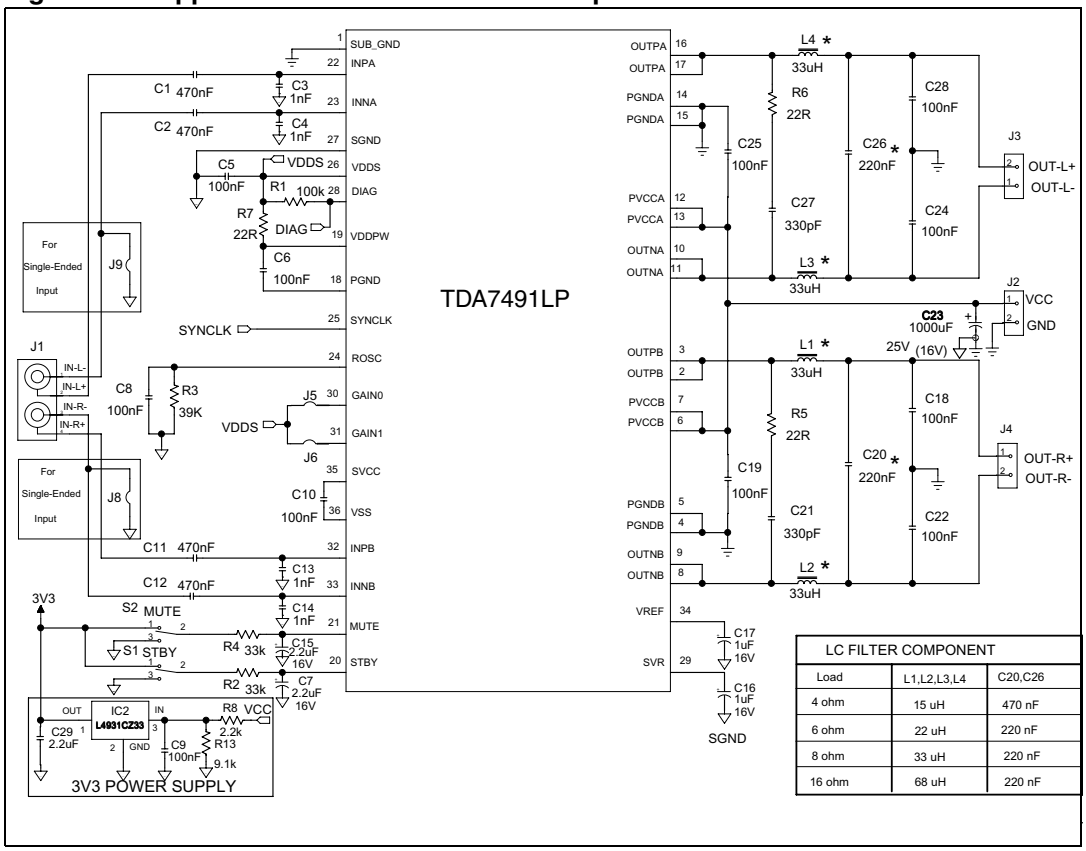
Figure 25. Power dissipation and efficiency vs. output power



5 Applications information

5.1 Applications circuit

Figure 26. Applications circuit for class-D amplifier



LC FILTER COMPONENT		
Load	L1,L2,L3,L4	C20,C26
4 ohm	15 uH	470 nF
6 ohm	22 uH	220 nF
8 ohm	33 uH	220 nF
16 ohm	68 uH	220 nF

5.2 Mode selection

The three operating modes, defined below, of the TDA7491LP are set by the two inputs STBY (pin 20) and MUTE (pin 21) as shown in *Table 6*.

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.
- Play mode: the amplifiers are active.

The protection functions of the TDA7491LP are implemented by pulling down the voltages of the STBY and MUTE inputs shown in *Figure 27*. The input current of the corresponding pins must be limited to 200 µA.

Table 6. Mode settings

Mode	Voltage level on pin STBY	Voltage level on pin MUTE
Standby	L (1)	X (don't care)
Mute	H (1)	L
Play	H	H

1. Refer to V_{STBY} and V_{MUTE} in *Table 5: Electrical specifications on page 10* for the drive levels for L and H

Figure 27. Standby and mute circuits

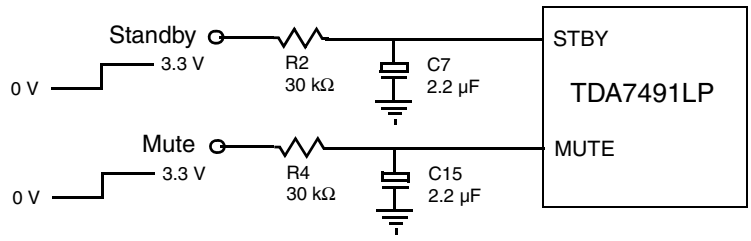
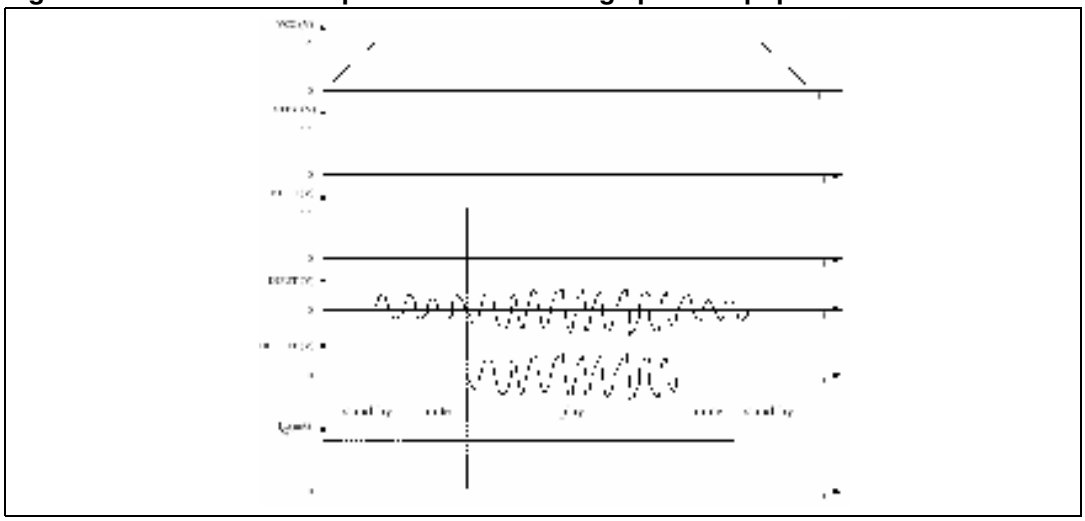


Figure 28. Turn-on/off sequence for minimizing speaker "pop"



5.3 Gain setting

The gain of the TDA7491LP is set by the two inputs, GAIN0 (pin 30) and GAIN1 (pin 31). Internally, the gain is set by changing the feedback resistors of the amplifier.

Table 7. Gain settings

Voltage level on pin GAIN0	Voltage level on pin GAIN1	Nominal gain, G_V (dB)
L(1)	H(1)	20
L	H	26
H	L	30
H	H	32

1. Refer to V_{inL} and V_{inH} in *Table 5: Electrical specifications on page 10* for the drive levels for L and H

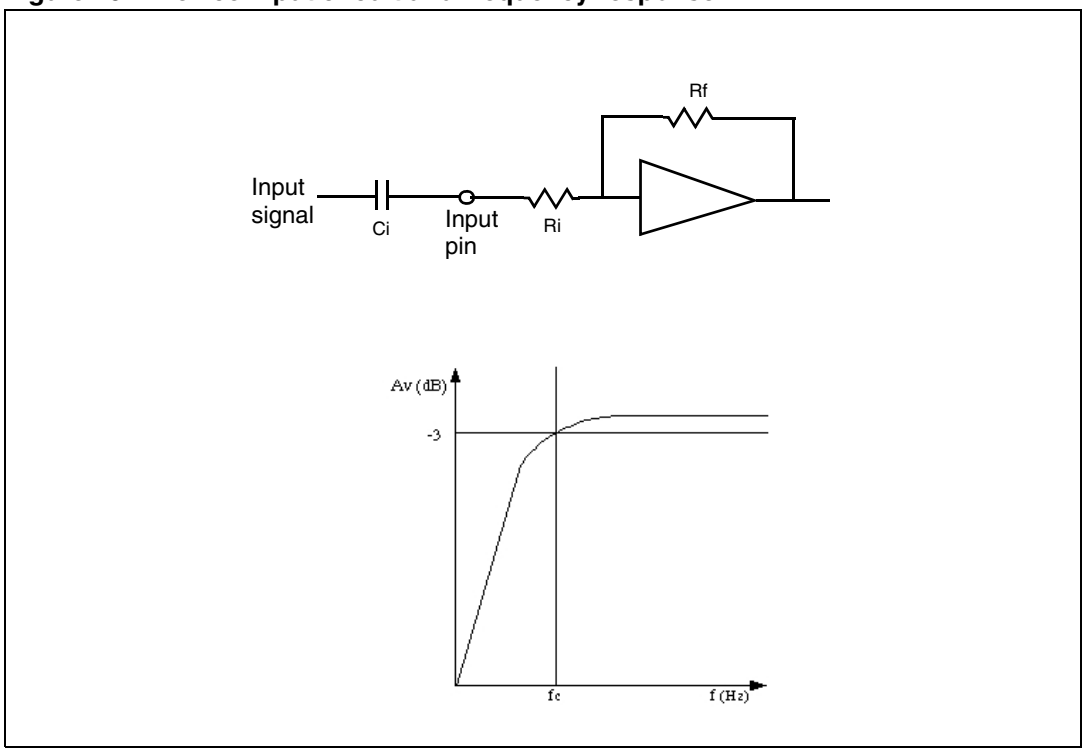
5.4 Input resistance and capacitance

The input impedance is set by an internal resistor Ri = 68 kΩ (typical). An input capacitor (Ci) is required to couple the AC input signal.

The equivalent circuit and frequency response of the input components are shown in *Figure 29*. For Ci = 220 nF the high-pass filter cut-off frequency is below 20 Hz:

$$fc = 1 / (2 * \pi * Ri * Ci)$$

Figure 29. Device input circuit and frequency response



5.5 Internal and external clocks

The clock of the class-D amplifier can be generated internally or can be driven by an external source.

If two or more class-D amplifiers are used in the same system, it is recommended that all devices operate at the same clock frequency. This can be implemented by using one TDA7491LP as master clock, while the other devices are in slave mode, that is, externally clocked. The clock interconnect is via pin SYNCLK of each device. As explained below, SYNCLK is an output in master mode and an input in slave mode.

5.5.1 Master mode (internal clock)

Using the internal oscillator, the output switching frequency, f_{SW}, is controlled by the resistor, R_{OSC}, connected to pin ROSC:

$$f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4) \text{ kHz}$$

where R_{OSC} is in kΩ.

In master mode, pin SYNCLK is used as a clock output pin, whose frequency is:

$$f_{SYNCLK} = 2 * f_{SW}$$

For master mode to operate correctly then resistor R_{OSC} must be less than 60 kΩ as given below in *Table 8*.

5.5.2 Slave mode (external clock)

In order to accept an external clock input, pin ROSC must be left open, that is, floating. This forces pin SYNCLK to be internally configured as an input as given in *Table 8*.

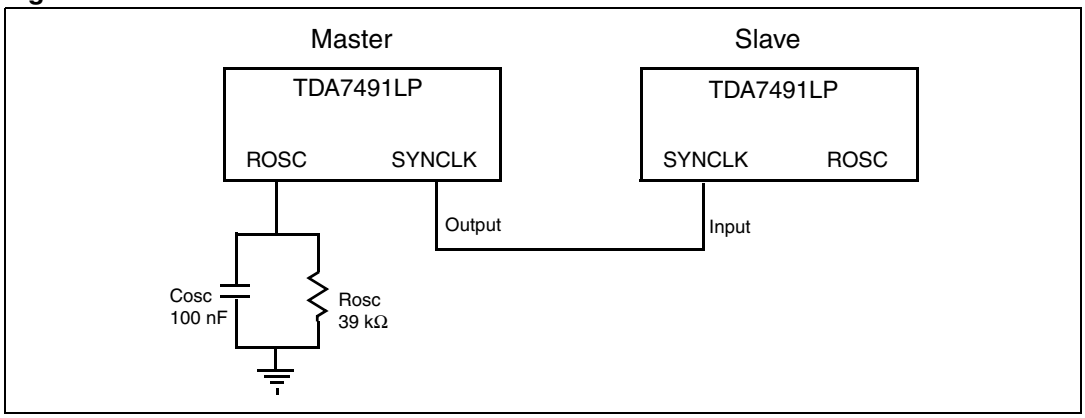
The output switching frequency of the slave devices is:

$$f_{SW} = f_{SYNCLK} / 2$$

Table 8. How to set up SYNCLK

Mode	ROSC	SYNCLK
Master	R_{OSC} < 60 kΩ	Output
Slave	Floating (not connected)	Input

Figure 30. Master and slave connection



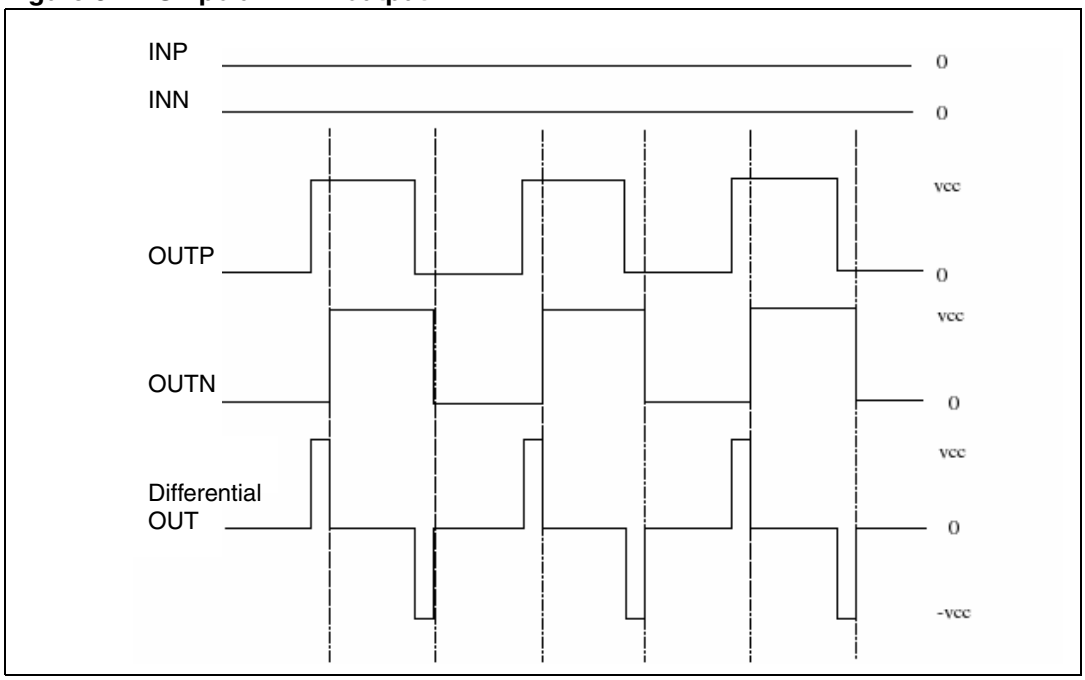
5.6 Modulation

The output modulation scheme of the BTL is called unipolar pulse width modulation (PWM). The differential output voltages change between 0 V and $+V_{CC}$ and between 0 V and $-V_{CC}$. This is in contrast to the traditional bipolar PWM outputs which change between $+V_{CC}$ and $-V_{CC}$.

An advantage of this scheme is that it effectively doubles the switching frequency of the differential output waveform on the load then reducing the current ripple accordingly. The OUTP and OUTN are in the same phase almost overlapped when the input is zero under this condition, then the switching current is low and the related losses in the load are low. In practice, a short delay is introduced between these two outputs in order to avoid the BTL outputs switching simultaneously when the input is zero.

Figure 31 shows the resulting differential output voltage and current when a positive, zero and negative input signal is applied. The resulting differential voltage on the load has a double frequency with respect to outputs OUTP and OUTN then resulting in reduced current ripple.

Figure 31. Unipolar PWM output



5.6.1 Reconstruction low-pass filter

Standard applications use a low-pass filter before the speaker. The cut-off frequency should be higher than 22 kHz and much lower than the output switching frequency. It is necessary to choose the L-C component values depending on the loud speaker impedance. Some typical values, which give a cut-off frequency of 27 kHz, are shown in *Figure 32* and *Figure 33* below.

Figure 32. Typical LC filter for an 8-Ω speaker

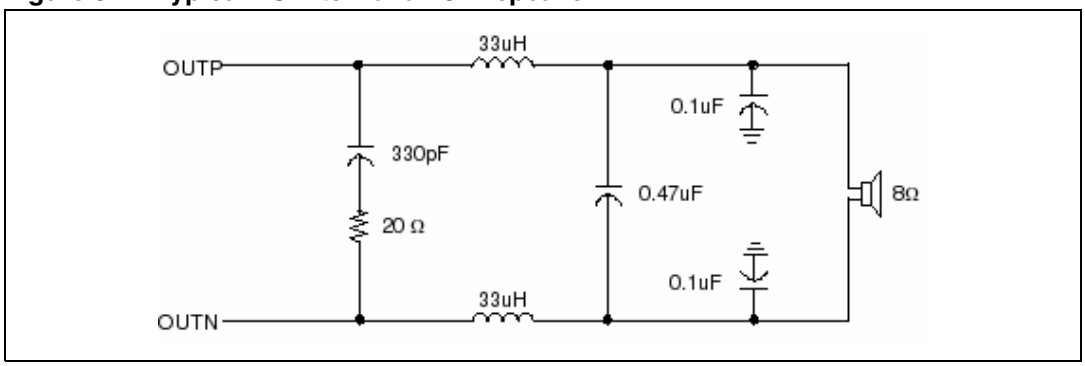
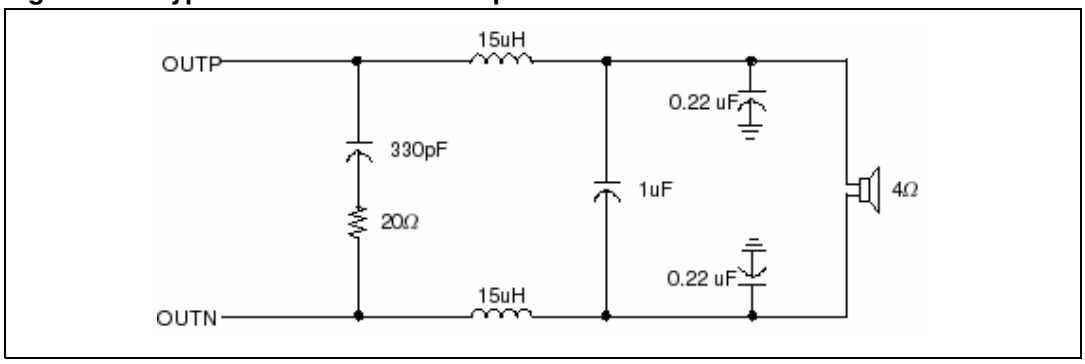


Figure 33. Typical LC filter for a 4-Ω speaker



5.6.2 Filterless modulation

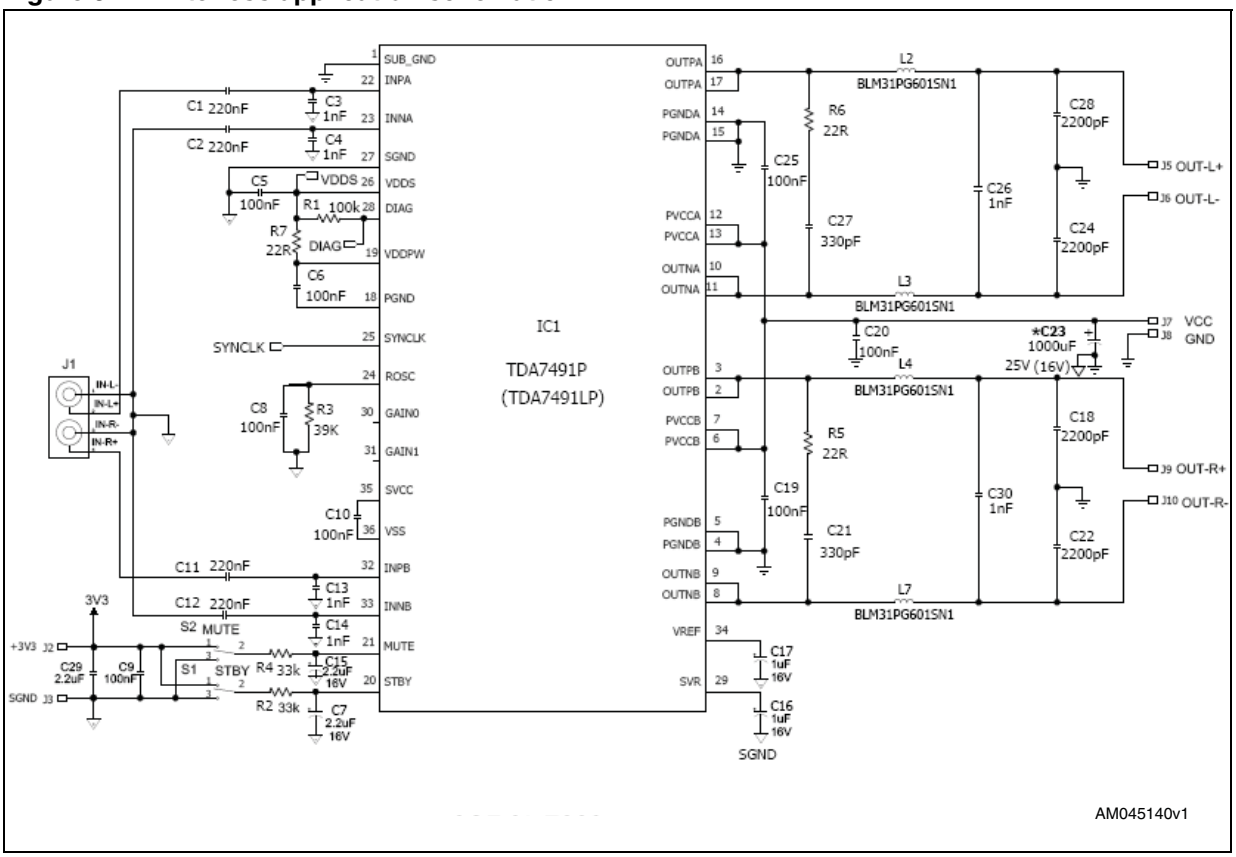
TDA7491LP can be used without a filter at the IC outputs, because the frequency of the TDA7491LP output is beyond the audio frequency, the audio signal can be recovered by the inherent inductance of the speaker and natural filter of the human ear.

The reconstruction of the audio signal on the load is usually achieved using a complete LC filter (such as a Butterworth) solution that guarantees good audio performance, high efficiency and EMI suppression. The LC component values should be computed by considering the target audio band and the PWM switching frequency. The cut-off frequency must lie well below the switching frequency and above the upper audio frequency. In particular, the following schematic gives a guideline for a cut-off frequency of about 30 kHz for both 6- and 8-Ω speakers.

Thanks to its advanced modulation approach, aimed to improve both driving efficiency and radiating emissions, the device is even able to drive a load with a very low component count. With this cost-saving filtering scheme the TDA7491P complies with the EMI specifications FCC class B. *Figure 34 on page 30* shows the simplified schematic adopted for the test and the relevant emission curve at full output power.

Emission tests have been performed with a 1-m length of twisted speaker wire with ferrite beads. Changing the type of the ferrite bead requires care due to factors such as its effectiveness in the EMC frequency range and impedance stability over the rated current range. An output snubber network further improves the emissions and this should be tuned according to the actual PCB, layout and component characteristics.

Figure 34. Filterless application schematic



5.7 Protection functions

The TDA7491LP is fully protected against undervoltages, overcurrents and thermal overloads as explained here.

Undervoltage protection (UVP)

If the supply voltage drops below the value of V_{UVP} given in *Table 5: Electrical specifications on page 10* the undervoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers the device restarts.

Overcurrent protection (OCP)

If the output current exceeds the value of I_{OCP} given in *Table 5: Electrical specifications on page 10* the overcurrent protection is activated which forces the outputs to the high-impedance state. Periodically, the device attempts to restart. If the overcurrent condition is still present then the OCP remains active. The restart time, T_{OC}, is determined by the R-C components connected to pin STBY.

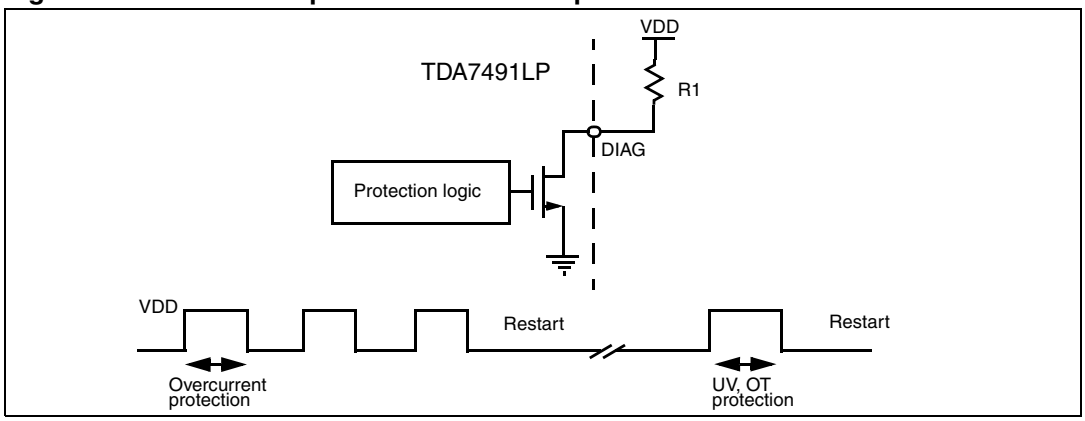
Thermal protection (OTP)

If the junction temperature, T_j, reaches 145 °C (nominal), the device goes to mute mode and the positive and negative PWM outputs are forced to 50% duty cycle. If the junction temperature reaches the value for Tj given in *Table 5: Electrical specifications on page 10* the device shuts down and the output is forced to the high impedance state. When the device cools sufficiently the device restarts.

5.8 Diagnostic output

The output pin DIAG is an open drain transistor. When the protection is activated it is in the high-impedance state. The pin can be connected to a power supply (<18 V) by a pull-up resistor whose value is limited by the maximum sinking current (200 µA) of the pin.

Figure 35. Behavior of pin DIAG for various protection conditions



5.9 Heatsink requirements

Due to the high efficiency of the class-D amplifier a 2-layer PCB can easily provide the heatsinking capability for low to medium power outputs.

Using such a PCB with a copper ground layer of 3 x 3 cm^2 and 16 vias connecting it to the contact area for the exposed pad, a thermal resistance, junction to ambient (in natural air convection), of 24 °C/W can be achieved.

The dissipated power within the device depends primarily on the supply voltage, load impedance and output modulation level. With the TDA7491LP driving 2 x8 Ω with a supply of 9 V then the maximum device dissipation is approximately 1 W.

When this power is dissipated at the maximum ambient temperature of 85 °C and the device is mounted on the above PCB then the junction temperature could reach:

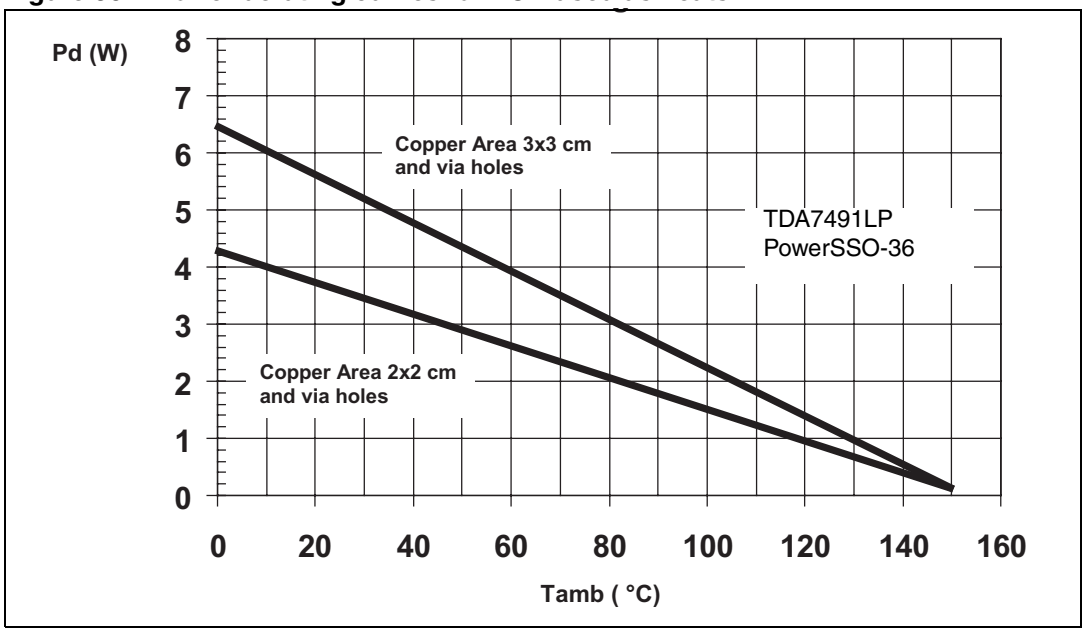
Tj = Tamb + Pd * Rj-amb = 85 + 1 * 24 = 109 °C

However, this temperature is sufficiently low to avoid triggering thermal warning.

With a musical program the dissipated power is about 40% less than the above maximum value. This leads to a junction temperature of around only 99 °C with the 9 cm2 copper ground. A commensurately smaller heatsink can thus be used.

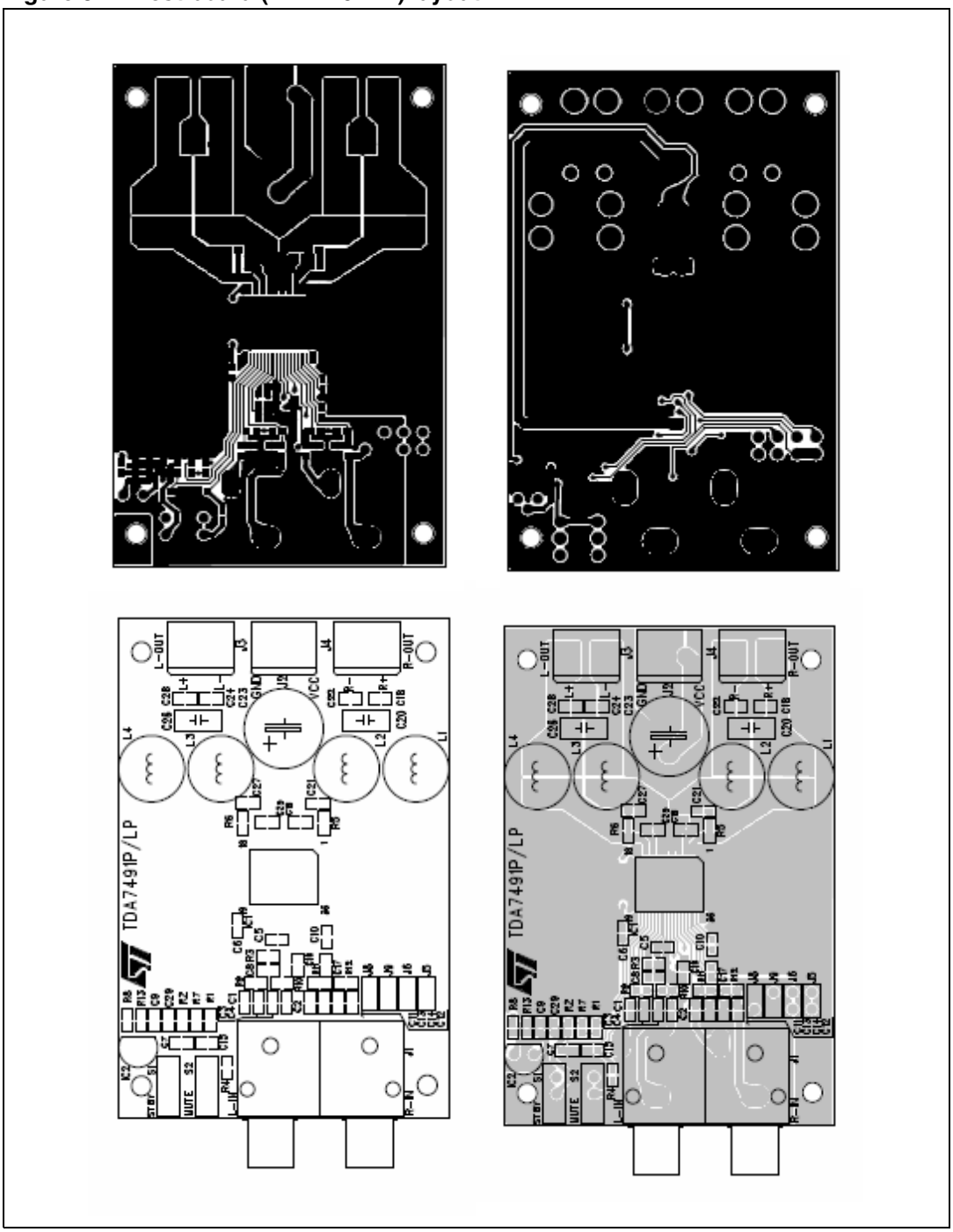
Figure 36 shows the power derating curve for the PowerSSO-36 package on PCBs with copper areas of 2 x 2 cm^2 and 3 x 3 cm^2.

Figure 36. Power derating curves for PCB used as heatsink



5.10 Test board

Figure 37. Test board (TDA7491LP) layout



6 Package mechanical data

The TDA7491LP comes in a 36-pin PowerSSO package with exposed pad down (EPD).

Figure 38 below shows the package outline and *Table 9* gives the dimensions.

Table 9. PowerSSO-36 EPD dimensions

Symbol	Dimensions in mm			Dimensions in inches		
	Min	Typ	Max	Min	Typ	Max
A	2.15	-	2.47	0.085	-	0.097
A2	2.15	-	2.40	0.085	-	0.094
a1	0.00	-	0.10	0.000	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	-
e3	-	8.5	-	-	0.335	-
F	-	2.3	-	-	0.091	-
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398	-	0.413
h	-	-	0.40	-	-	0.016
k	0	-	8 degrees	0	-	8 degrees
L	0.60	-	1.00	0.024	-	0.039
M	-	4.30	-	-	0.169	-
N	-	-	10 degrees	-	-	10 degrees
O	-	1.20	-	-	0.047	-
Q	-	0.80	-	-	0.031	-
S	-	2.90	-	-	0.114	-
T	-	3.65	-	-	0.144	-
U	-	1.00	-	-	0.039	-
X	4.10	-	4.70	0.161	-	0.185
Y	6.50	-	7.10	0.256	-	0.280

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

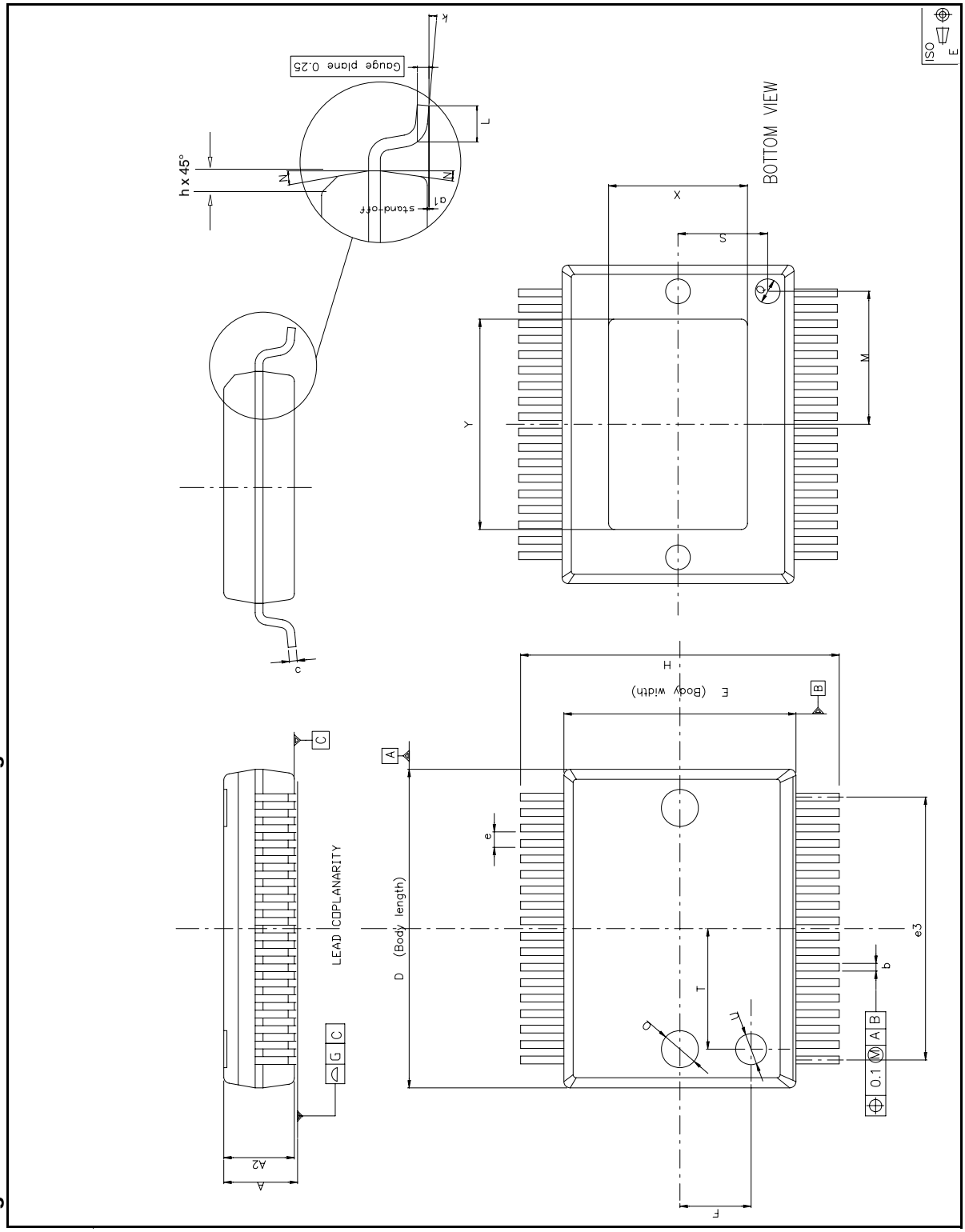


Figure 38. PowerSSO-36 EPD outline drawing

7 Revision history

Table 10. Document revision history

Date	Revision	Changes
02-Jul-2007	1	Initial release.
15-Oct-2008	2	Updated characterization curves.
23-Jun-2009	3	Updated text concerning oscillator R and C in *Section 3.3: Electrical specifications on page 10* Updated condition for Iq test, added V_{UVP} maximum value, updated THD maximum value, updated STBY and MUTE voltages in *Table 5: Electrical specifications on page 10* Updated equation for f_{SW} *on page 11* and *on page 27* Updated *Figure 26: Applications circuit for class-D amplifier on page 24* Updated *Section 5.7: Protection functions on page 31*.
04-Sep-2009	4	Added text for exposed pad in *Figure 2 on page 7* Added text for exposed pad in *Table 2 on page 8* Updated exposed pad Y (Min) dimension in *Table 9 on page 34* Updated supply voltage for pin DIAG pull-up resistor in *Section 5.8 on page 31*.
23-Mar-2011	5	Updated operating temperature range in *Table 1 on page 1* Modified description of pins 10, 11 in *Table 2 on page 8* Added V_I and updated operating temperature range in *Table 3: Absolute maximum ratings on page 9* Updated *Table 4: Thermal data on page 9* Updated *Table 5: Electrical specifications on page 10* Updated introduction and characterization curves in *Section 4 on page 12* Moved test board layout to *Section 5.10 on page 33* Moved package mechanical data to *Section 6 on page 34* Updated applications circuit in *Figure 26 on page 24* Updated *Table 7: Gain settings on page 26* Updated *Section 5.6: Modulation on page 28* Added *Figure 34: Filterless application schematic on page 30* Removed overvoltage protection from *Section 5.7: Protection functions on page 31* Updated *Section 5.9: Heatsink requirements on page 32* Updated exposed pad dimension Y in *Table 9 on page 34*

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