# STA540

## 4 x 13 W dual/quad power amplifier

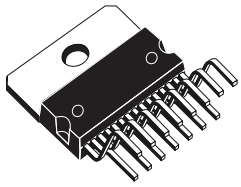
**Datasheet – production data**

## Features

- High output power capability
  - 2x 38 W into 4 Ω at 18 V, 1 kHz, 10% THD
  - 2x 34 W into 8 Ω at 22 V, 1 kHz, 10% THD
  - 2x 24W into 4Ω at 14.4 V, 1 kHz, 10% THD
  - 2x 15 W into 8 Ω at 16 V, 1 kHz, 10% THD
  - 4x 13 W into 2 Ω at 15 V, 1 kHz, 10% THD
  - 4x 11 W into 4 Ω at 18 V, 1 kHz, 10% THD
  - 4x 7 W into 4 Ω at 14.4 V, 1 kHz, 10% THD
- Minimum external components count:
  - no bootstrap capacitors
  - no Boucherot cells
  - internally fixed gain 20 dB
- Standby function (CMOS compatible)
- No audible pop during standby operations
- Diagnostic facilities:
  - clip detector
  - output to GND short-circuit detector
  - output to VS short-circuit detector
  - soft short-circuit check at turn-on
  - thermal shutdown warning

### Protection

- Output AC/DC short circuit
- Soft short-circuit check at turn-on
- Thermal cutoff/limiter to prevent chip from overheating
- High inductive loads
- ESD



**Multiwatt15**

## Description

The STA540 is a 4-channel, class-AB audio amplifier designed for high quality sound applications.

The amplifiers have single-ended outputs with integrated short-circuit protection, thermal protection and diagnostic functions.

The chip is housed in the 15-pin Multiwatt ECOPACK® Pb-free package which is RoHS (2002/95/EC) compliant.

**Table 1. Device summary**

| Order code | Temperature range | Package | Packing |
|---|---|---|---|
| STA540 | -40 to 150° C | Multiwatt15 | Tube |



This is information on a product in full production. www.st.com

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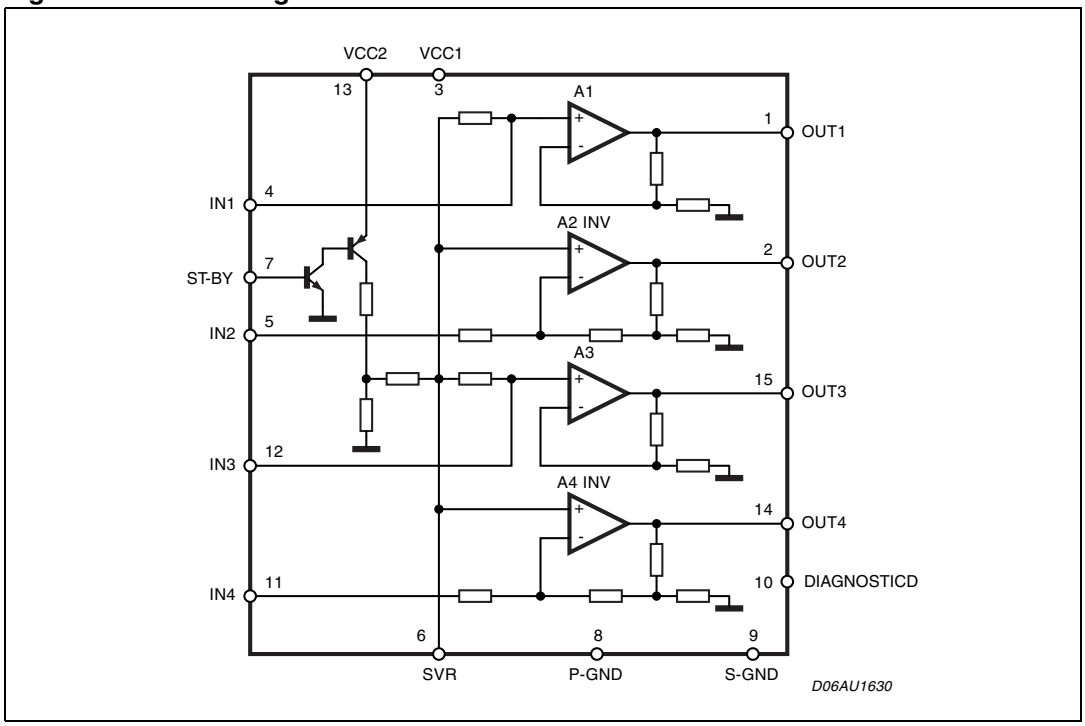
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# 1 Block diagram and pin description

## 1.1 Block diagram

**Figure 1. Block diagram**



## 1.2 Pin description

**Figure 2. Pin connection (top view)**

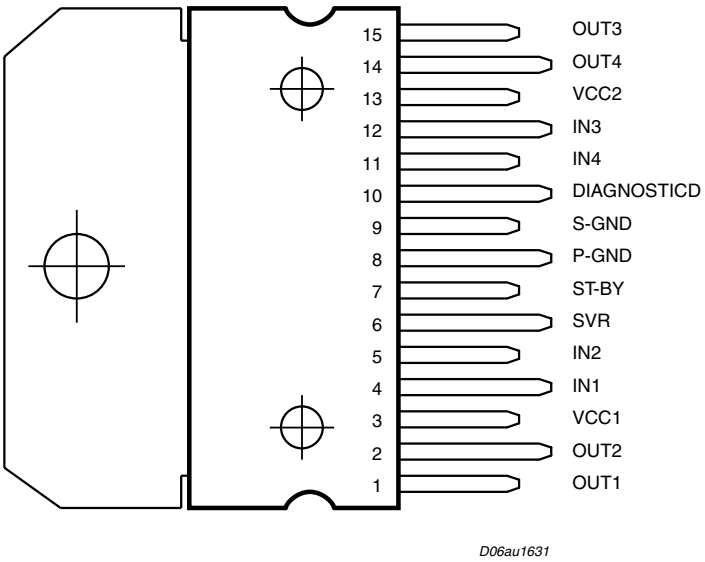



**Table 2. Pin description**

| N° | Name | Type | Function |
|---|---|---|---|
| 1 | OUT1 | OUT | Channel 1 output |
| 2 | OUT2 | OUT | Channel 2 output |
| 3 | VCC1 | PWR | Power supply |
| 4 | IN1 | IN | Channel 1 input |
| 5 | IN2 | IN | Channel 2 input |
| 6 | SVR | IN | Supply voltage rejection |
| 7 | ST-BY | IN | Standby control pin |
| 8 | P-GND | PWR | Power ground |
| 9 | S-GND | PWR | Signal ground |
| 10 | DIAGNOSTICD | OUT | Diagnostics output |
| 11 | IN4 | IN | Channel 4 input |
| 12 | IN3 | IN | Channel 3 input |
| 13 | VCC2 | PWR | Power supply |
| 14 | OUT4 | OUT | Channel 4 output |
| 15 | OUT3 | OUT | Channel 3 output |

# 2 Electrical specifications

## 2.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_s$ | Supply voltage idle mode (no signal) | 24 | V |
| | Supply voltage operating | 22 | V |
| | Supply voltage AC-DC short safe | 20 | V |
| $P_{tot}$ | Total power dissipation ($T_{case}$ = 85 °C) | 36 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to150 | °C |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |

## 2.2 Thermal data

**Table 4. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction to case (max) | 1.8 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction to ambient (max) | 35 | °C/W |

## 2.3 Electrical characteristics

The test conditions are $V_S$ = 14.4 V, $R_L$ = 4 Ω, f = 1 kHz, $T_{amb}$ = 25° C unless otherwise specified.

**Table 5. Electrical characteristics**

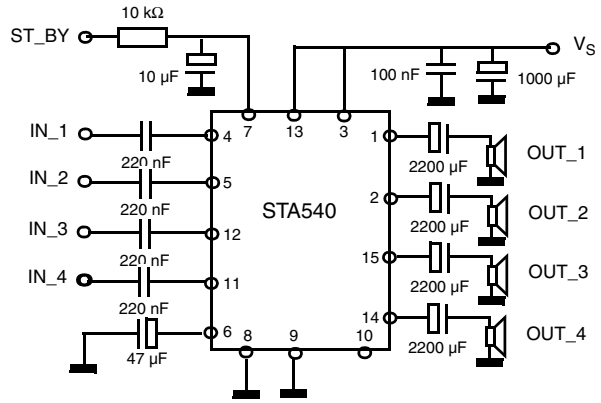
| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_S$ | Supply voltage range | | 8 | | 22 | V |
| $I_d$ | Total quiescent drain current | | | 80 | 150 | mA |
| $V_{os}$ | Output offset voltage | | -150 | | 150 | mV |
| $P_o$ | Output power, SE | THD=10%, $R_L$=4 Ω<br>THD=10%, $R_L$=2 Ω<br>THD=10%, $R_L$=4 Ω, $V_S$=22 V | 6.5 | 7<br>11.5<br>16 | | W |
| | Output power, BTL | THD=10%, $R_L$=4 Ω<br>THD=10%, $R_L$=8 Ω, $V_S$=17 V<br>THD=10%, $R_L$=8 Ω, $V_S$=22 V | 21 | 24<br>20<br>34 | | W |
| THD | Total harmonic distortion | $R_L$ = 4 Ω, $P_o$ = 0.1 to 4 W | | 0.02 | | % |
| $I_{SC}$ | Short-circuit output current | | 4.0 | | | A |

**Table 5. Electrical characteristics (continued)**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_T$ | Crosstalk | f = 1 kHz single-ended<br>f = 10 kHz single-ended<br>f = 1 kHz BTL<br>f = 10 kHz BTL | 55 | 70<br>60<br><br>60 | | dB |
| $R_{in}$ | Input impedance | Single-ended BTL | 20<br>10 | 30<br>15 | | kΩ |
| $G_v$ | Voltage gain | Single-ended BTL | 19<br>25 | 20<br>26 | 21<br>27 | dB |
| $G_v$ | Voltage gain match | | | | 0.5 | dB |
| $E_N$ | Input noise voltage | $R_{gen}$ = 0, "A" weighted, S.E.:<br>Non-inverting channels<br>Inverting channels | | <br>2<br>5 | | <br>µV<br>µV |
| | | BTL<br>$R_{gen}$ = 0, f = 22 Hz to 22 kHz | | 3.5 | | µV |
| SVR | Supply voltage rejection | $R_{gen}$ = 0, f = 300 Hz,<br>$C_{SVR}$ = 470 µF | 50 | | | dB |
| $A_{SB}$ | Standby attenuation | $P_o$ = 1 W | 80 | 90 | | dB |
| $I_{SB}$ | Current consumption in standby | $V_{ST_BY}$ = 0 to 1.5 V | | | 100 | µA |
| $V_{SB}$ | ST-BY IN threshold voltage | | | | 1.5 | V |
| | ST-BY OUT threshold voltage | | 3.5 | | | V |
| $I_{ST\text{-}BY}$ | Pin ST-BY current | Play mode, $V_{ST\text{-}BY}$ = 5 V | | | 50 | µA |
| | | Max driving current under fault | | | 5 | mA |
| $I_{cd_off}$ | Clipping detector output average current | d = 1% (*) | | 90 | | µA |
| $I_{cd_on}$ | Clipping detector output average current | d = 5% (*) | | 160 | | µA |
| $V_{DIAGNOSTICD}$ | Saturation voltage on pin DIAGNOSTICD | $I_{DIAGNOSTICD}$ = 1 mA sinking | | | 0.7 | V |
| $T_W$ | Thermal warning | | | 140 | | °C |
| $T_M$ | Thermal muting | | | 150 | | °C |
| $T_S$ | Thermal shutdown | | | 160 | | °C |

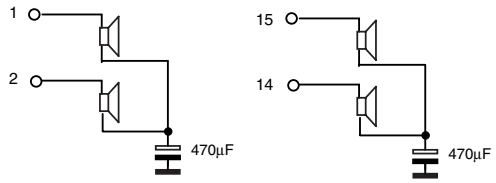
# 3 Standard application circuits

**Figure 3. Quadraphonic**



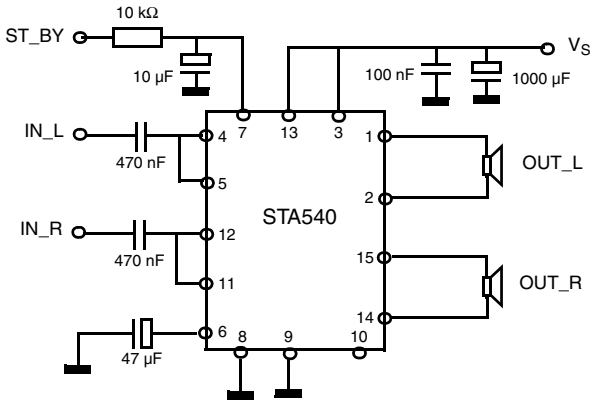

Suggested applications:
4x 13 W into 2 Ω, at 15 V
4x 11 W into 4 Ω, at 18 V
4x 9 W into 2 Ω, at 12 V
4x 8 W into 4 Ω, at 16 V
4x 5 W into 4 Ω, at 12 V

**Figure 4. Alternative single-ended speaker connection**



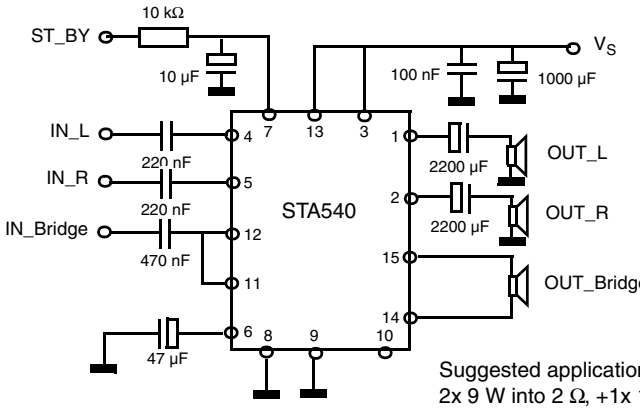

The best audio performance is obtained with the configuration where each speaker has its own DC blocking capacitor. However, if the application allows a little degradation of the spatial image it is possible to connect a couple of speakers with only one low-value DC blocking capacitor.

**Figure 5. Dual bridge**




Suggested applications:
2x 38 W into 4 Ω, at 18 V, 1 kHz, 10% THD
2x 34 W into 8 Ω, at 22 V, 1 kHz, 10% THD
2x 24 W into 4 Ω, at 14.4 V, 1 kHz, 10% THD
2x 15 W into 8 Ω, at 16 V, 1 kHz, 10% THD

**Figure 6. Stereo plus bridge drive**




Suggested applications:
2x 9 W into 2 Ω, +1x 18 W into 4 Ω, at 12 V
2x 12 W into 2 Ω, +1x 26 W into 4 Ω, at 14.4 V
2x 8 W into 4 Ω, +1x 16 W into 8 Ω, at 16 V

# 4 Electrical characteristics curves

**Figure 7. Quiescent drain current versus supply voltage (single-ended and bridge)**

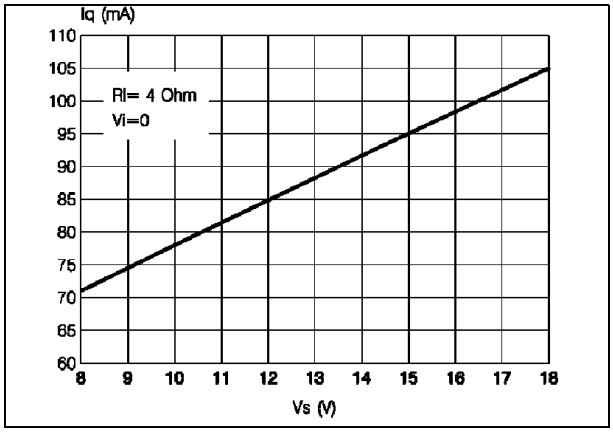



**Figure 8. Quiescent output voltage versus supply voltage (single-ended and bridge)**

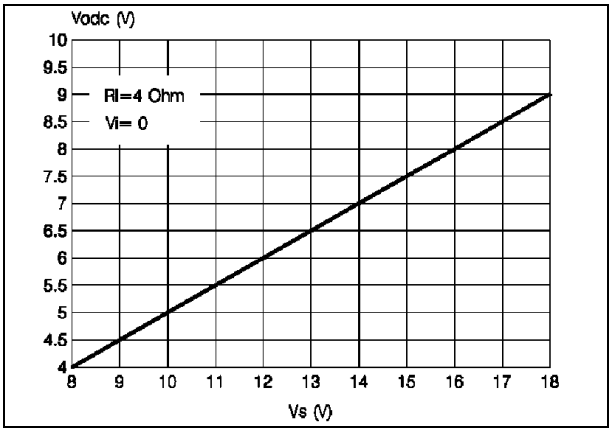



**Figure 9. Output power versus supply voltage**

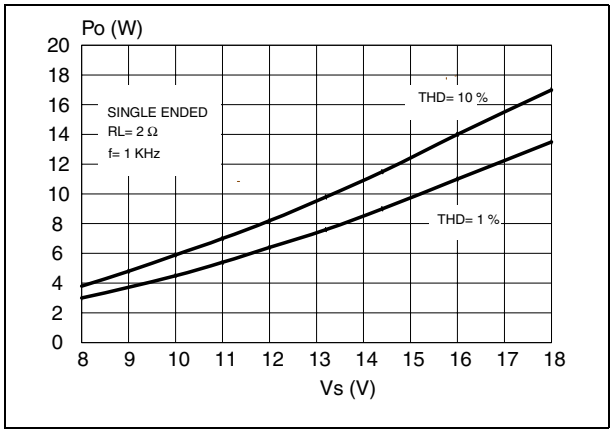



**Figure 10. Output power versus supply voltage**

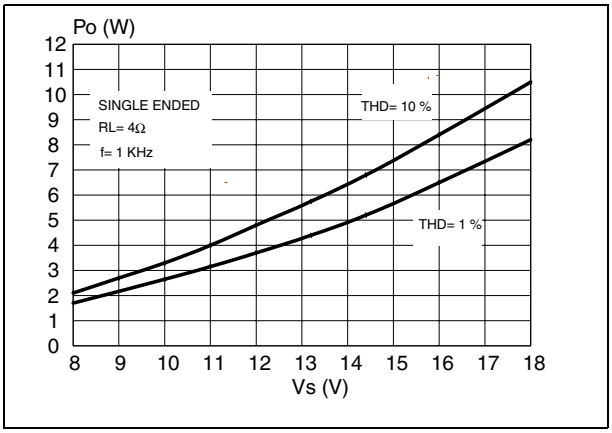



**Figure 11. Output power versus supply voltage**

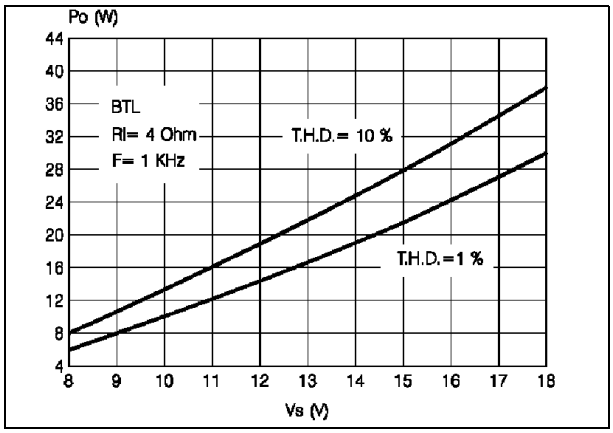



**Figure 12. Distortion versus output power**

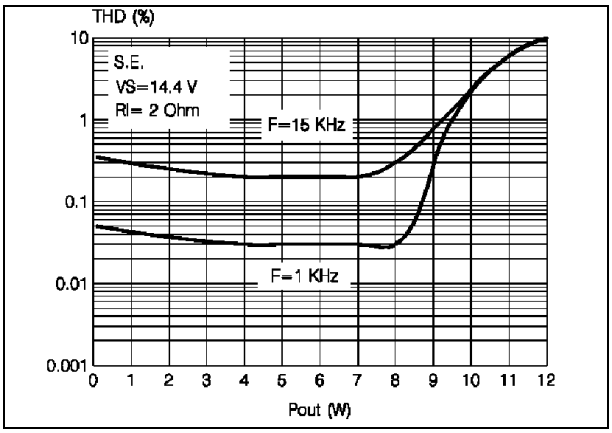


**Figure 13. Distortion versus output power**

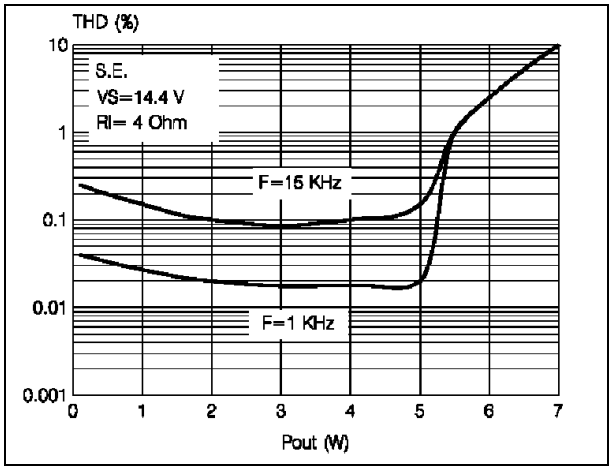



**Figure 14. Distortion versus output power**

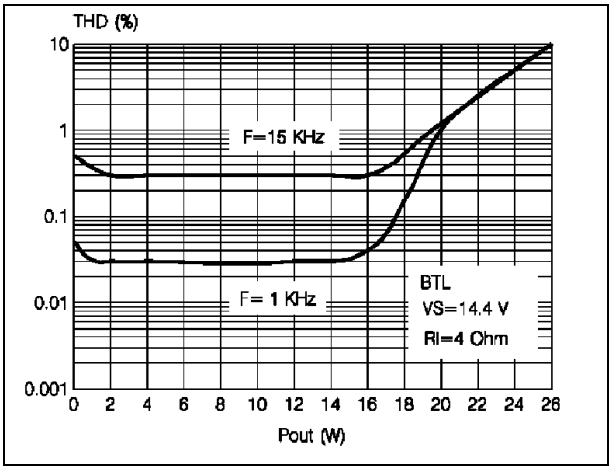



**Figure 15. Output power versus supply voltage**

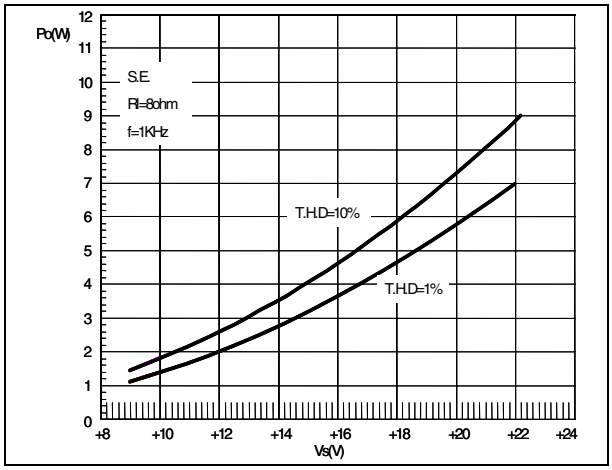



**Figure 16. Output power versus supply voltage**

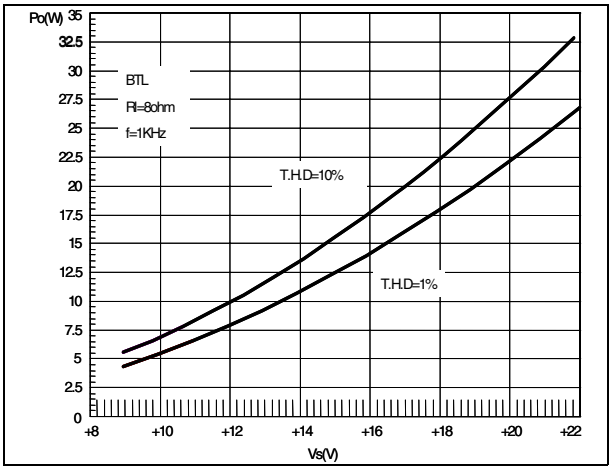



**Figure 17. Supply voltage rejection versus frequency**

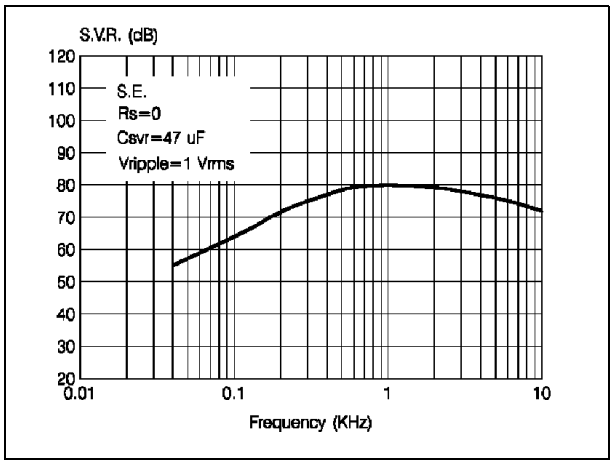



**Figure 18. Crosstalk versus frequency**

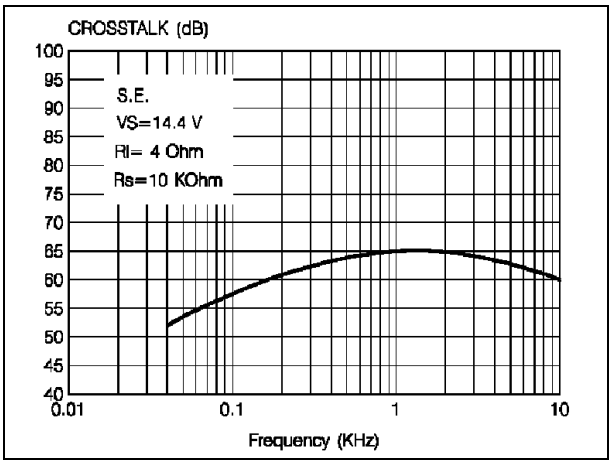


**Figure 19. Standby attenuation versus threshold voltage**

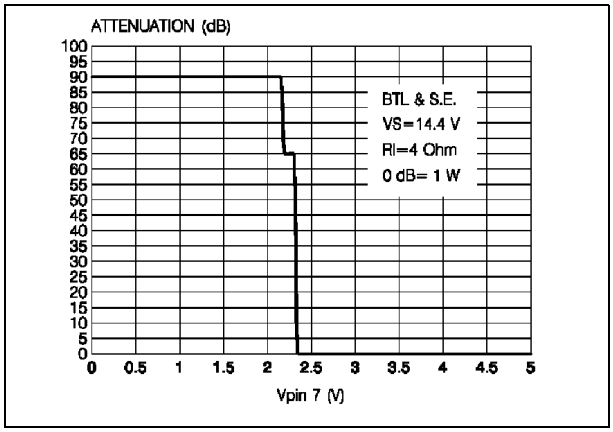



**Figure 20. Total power dissipation and efficiency versus output power**

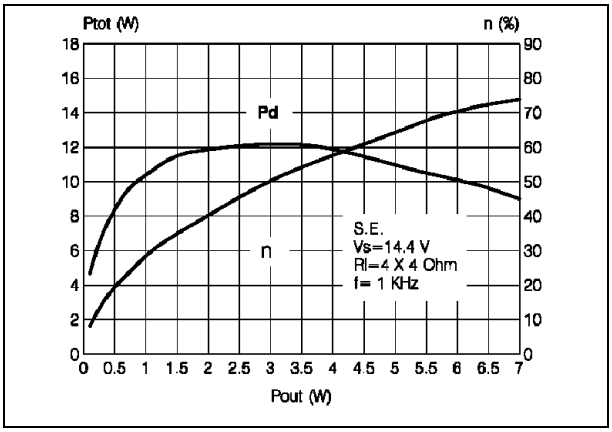
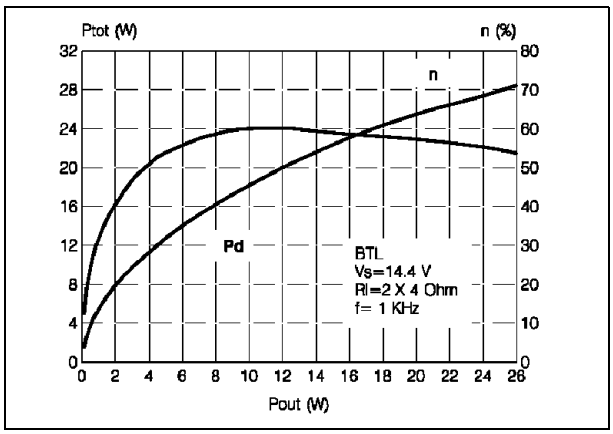



**Figure 21. Total power dissipation and efficiency versus output power**



# 5 Thermal information

In order to avoid the intervention of the thermal protection, placed at $T_j$ =150° C for thermal muting and $T_j$=160° C for thermal shutdown, it is important to calculate the heatsink thermal resistance, $R_{th_HS}$, correctly.

The parameters that influence the calculation are:

- maximum dissipated power for the device ($P_{dmax}$)
- maximum thermal resistance junction to case ($R_{th_j\text{-}case}$)
- maximum ambient temperature $T_{amb_max}$

There is also an additional term that depends on the Iq (quiescent current).

## 5.1 Heatsink specification examples

### 5.1.1 $R_{th_HS}$ calculation for 4 single-ended channels

Given $V_S$ = 14.4 V, $R_L$ = 4 Ω x 4 channels, $R_{th_j\text{-}case}$ = 1.8° C/W, $T_{amb_max}$ = 50° C and $P_{out}$ = 4 x 7 W then

the maximum power dissipated in the device is:

$$P_{dmax} = NChannel \cdot \frac{V_{CC}^2}{2\Pi^2 R_L} = 4 \cdot 2.62 = 10.5W$$

and the required thermal resistance of the heatsink is:

$$R_{th_HS} = \frac{150 - T_{amb_max}}{P_{dmax}} - R_{th_j\text{-}case} = \frac{150 - 50}{10.5} - 1.8 = 7.7°C/W$$

### 5.1.2 $R_{th_HS}$ calculation for 2 single-ended channels plus 1 BTL channel

Given $V_S$ = 14.4 V, $R_L$ = 2x 2 Ω (SE) + 1x 4 Ω (BTL), $P_{out}$ = 2 x 12 W + 1 x 26 W then

the maximum power dissipated in the device is:

$$P_{dmax} = 2 \cdot \frac{V_{CC}^2}{2\Pi^2 R_L} + \frac{2V_{CC}^2}{\Pi^2 R_L} = 2 \cdot 5.25 + 10.5 = 21W$$

and the required thermal resistance of the heatsink is:

$$R_{th_HS} = \frac{150 - T_{amb_max}}{P_{dmax}} - R_{th_j\text{-}case} = \frac{150 - 50}{21} - 1.8 = 3°C/W$$

### 5.1.3 Calculations using music power

The thermal resistance value calculated in each of the two above examples specifies a heatsink capable of sustaining the maximum dissipated power. Realistically, however, and as explained in the Application Note (AN1965), the heatsink can be smaller when the application is musical content.

When music power is considered the resulting dissipation is about 40% less than the calculated maximum. Thus, smaller or cheaper heatsinks can be employed. The heatsink thermal resistance values are modified as follows:

for example *5.1.1*: 10.5 W - 40% = 6.3 W, thus giving $R_{th_c\text{-}amb}$ = 14° C/W,

for example *5.1.2*: 21 W - 40% = 12.6 W, thus giving $R_{th_c\text{-}amb}$ = 6° C/W.

# 6 Practical information

## 6.1 Highly flexible amplifier configuration

The availability of four independent channels makes it possible to accomplish several kinds of applications ranging from four speakers stereo (F/R) to two-speaker bridge solutions.

When working with single-ended configurations, the polarity of the speakers driven by the inverting amplifier must be reversed with respect to those driven by non-inverting channels. This is to avoid phase irregularities causing sound alterations especially during the reproduction of low frequencies.

## 6.2 Easy single-ended to bridge transition

The change from single-ended to bridge configuration is made simple by connecting the two inputs together and also the speaker directly between the two outputs (no need for additional external components, in fact the output DC blocking capacitors are eliminated). However, take care to use an inverting/non-inverting amplifier pair.

## 6.3 Internally fixed gain

The advantages in internally fixing the gain (to 20 dB in single-ended configuration and to 26 dB in bridge configuration) are:

- components and space saving,
- output noise, supply voltage rejection and distortion optimization.

## 6.4 Silent turn on/off and muting/standby function

The standby mode can be easily activated by means of a CMOS logic level applied to pin ST-BY through a RC filter.

Under standby conditions, the device is turned off completely (supply current = 1 mA typical, output attenuation = 80 dB minimum).

All on/off operations are virtually pop-free. Furthermore, at turn-on the device stays in mute condition for a time determined by the value of the SVR capacitor. This prevents transients, coming from previous stages, from producing unpleasant acoustic effects at the speakers.

## 6.5 Driving circuit for standby mode

Some precautions need to be taken when designing the driving circuit for pin 7, ST-BY. For instance, the pin cannot be directly driven by a voltage source having a current capability higher than 5 mA. In practical cases a series resistance must be inserted, giving it the double purpose of limiting the current at pin 7 and to smooth down the standby on/off transitions. And, when done in combination with a capacitor, prevents output pop.

A capacitor of at least 100 nF from pin 7 to S-GND, with no resistance in between, is necessary to ensure correct turn-on.

## 6.6 Output stage

The fully complementary output stage is possible with the power ICV PNP component.

This novel design is based on the connection shown in *Figure 22* and allows the full exploitation of its capabilities. The clear advantages this new approach has over classical output stages are described in the following sections.

### 6.6.1 Rail-to-rail output voltage swing without bootstrap capacitors

The output swing is limited only by the $V_{CEsat}$ of the output transistors, which are in the range of 0.3 Ω ($R_{sat}$) each.

Classical solutions adopting composite PNP-NPN for the upper output stage have higher saturation loss on the top side of the waveform.

This unbalanced saturation causes a significant power reduction. The only way to recover power includes of the addition of expensive bootstrap capacitors.

### 6.6.2 Absolute stability without external compensation

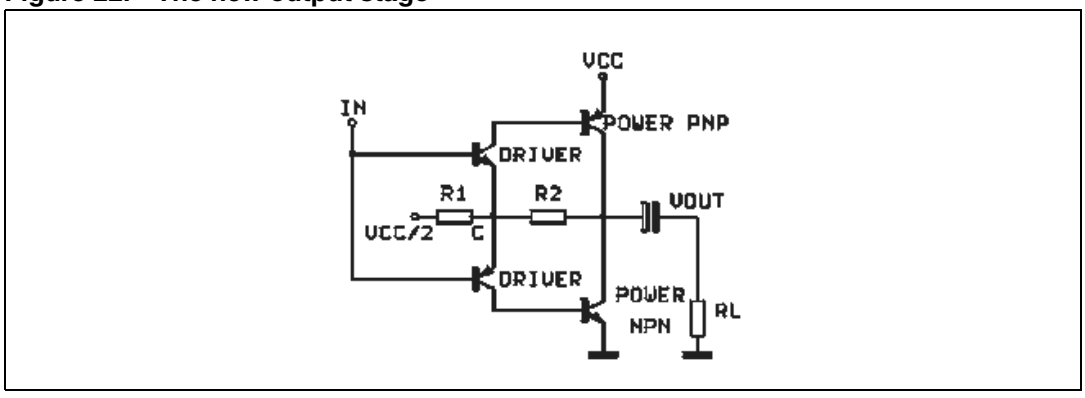
With reference to the circuit shown in *Figure 22*, the low frequency gain $V_{out}/V_{in}$ is greater than unity, that is, approximately 1 + R2/R1. The DC output level (VCC / 2) is fixed by an auxiliary amplifier common to all the channels.

By controlling the amount of this local feedback it is possible to force the loop gain (A*β) to less than unity at frequency where the phase shift is 180°. This means that the output buffer is intrinsically stable and not prone to oscillation.

The above feature has been achieved even though there is very low closed-loop gain of the amplifier.

This contrasts with the classical PNP-NPN stage which makes use of external RC networks, namely the Boucherot cells, for reducing the gain at high frequencies.

**Figure 22. The new output stage**



## 6.7 Built–in protection

### 6.7.1 Diagnostic facilities (pin 10)

The STA540 is equipped with diagnostic circuitry that is able to detect the following events:

- clipping of the output signal,
- thermal shutdown,
- output fault:
  - short circuit to GND,
  - short circuit to VS,
  - soft short circuit at turn-on.

The event is signalled when the open collector output of pin 10 begins to sink current.

### 6.7.2 Short-circuit protection

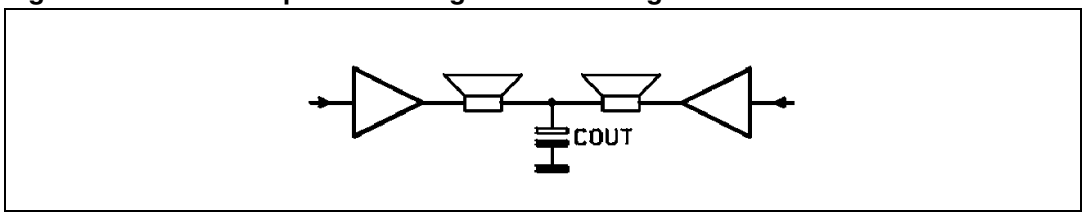
Reliable and safe operation in the presence of all kinds of output short circuit is assured by the built-in protection. As well as the AC/DC short circuit to GND and to VS, and across the speaker, there is a soft short-circuit condition, which is signalled on pin 10 (DIAGNOSTICD) during the turn-on phase, to verify output circuit integrity in order to ensure correct amplifier operation.

This particular kind of protection acts in such a way as to prevent the device being turned on (via pin ST-BY) when a resistive path (that is a DC path) less than 16 Ω exists between the output and GND. This would avoid loud speaker damage should, for example, the output coupling capacitor develop an internal short circuit.

As mentioned previously, it is important to limit the external current driving pin ST-BY to 5 mA. The reason is that the associated circuitry is normally disabled with currents greater than 5 mA.

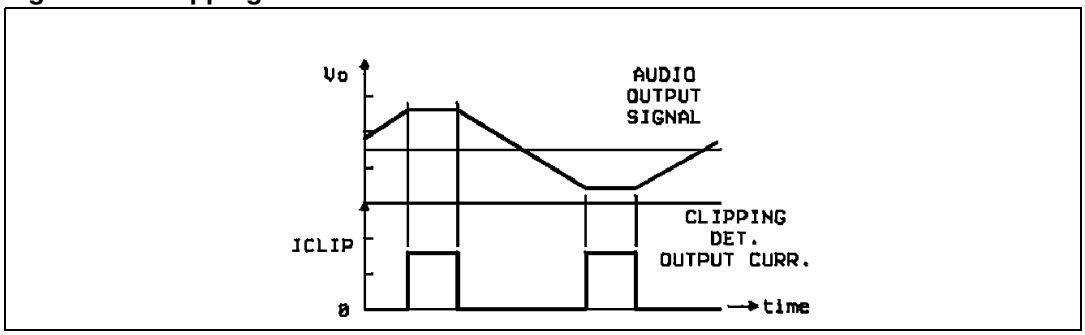
The soft short-circuit protection is particularly attractive when, in the single-ended configuration, one capacitor is shared between two outputs (see *Figure 23*).

**Figure 23. Shared capacitor in single-ended configuration**



### 6.7.3 Clipping detection

**Figure 24. Clipping detection waveforms**




Current sinking at pin 10 occurs when a certain distortion level is reached at each output. This function initiates a gain-compression facility whenever the amplifier is overdriven.

### 6.7.4 Thermal shutdown

With the thermal shutdown feature, the diagnostics output (pin 10) signals the closeness of the junction temperature to the shutdown threshold. Typically, current sinking at pin 10 starts approximately 10° C before the shutdown temperature is reached.

**Figure 25. Output fault waveforms (see *Figure 26*)**

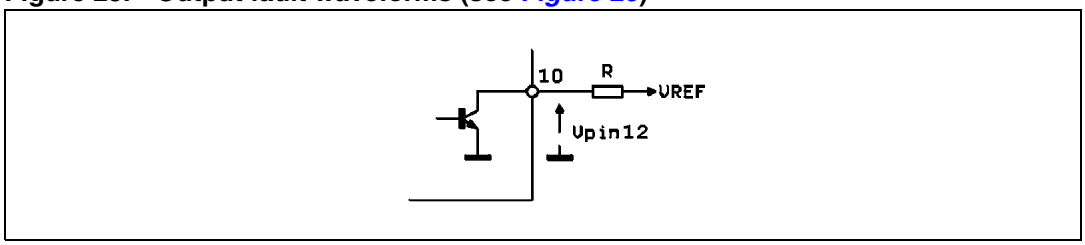
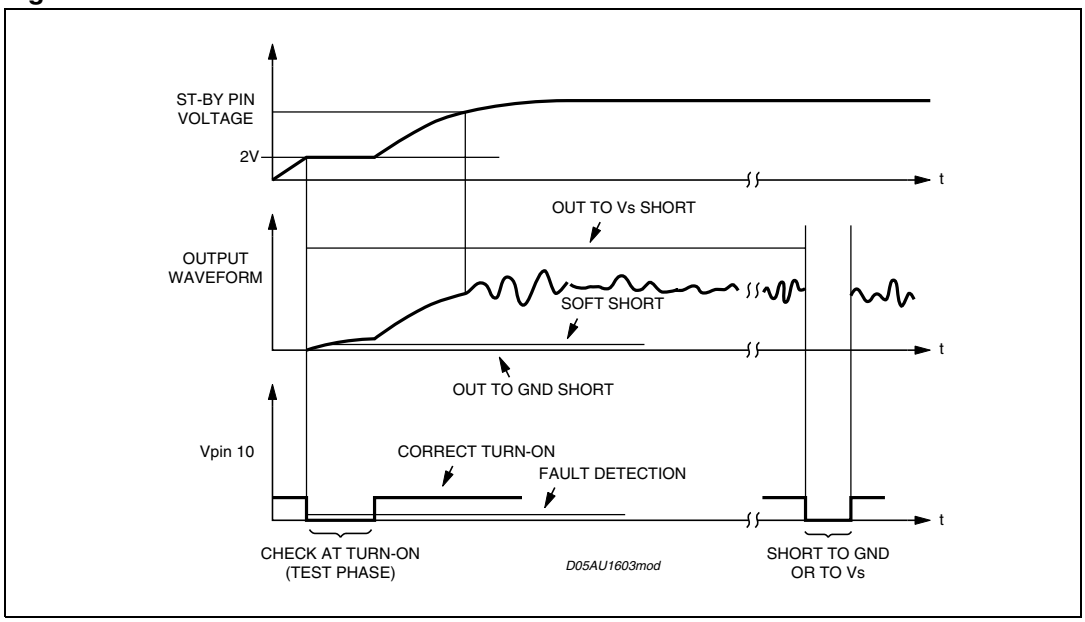



**Figure 26. Fault waveforms**



## 6.8 Handling the diagnostic information

As different diagnostic information (clipping detection, output fault, approaching thermal shutdown) becomes available at pin 10 so the behavior of the signal at this pin changes.

In order to discriminate the event, signal DIAGNOSTICD, pin 10, must be interpreted correctly. *Figure 27* shows a combination of events on the output waveform and the corresponding output on pin 10.

This events could be diagnosed based on the timing of the output signal on pin 10. For example, the clip-detector signalling under fault conditions could produce a low level for a short time. On the other hand, an output short circuit would probably produce a low level for a much longer time. With these assumptions, an interface circuit based on the one shown in *Figure 28* could differentiate the information and flag the appropriate circuits.

**Figure 27. Waveforms**

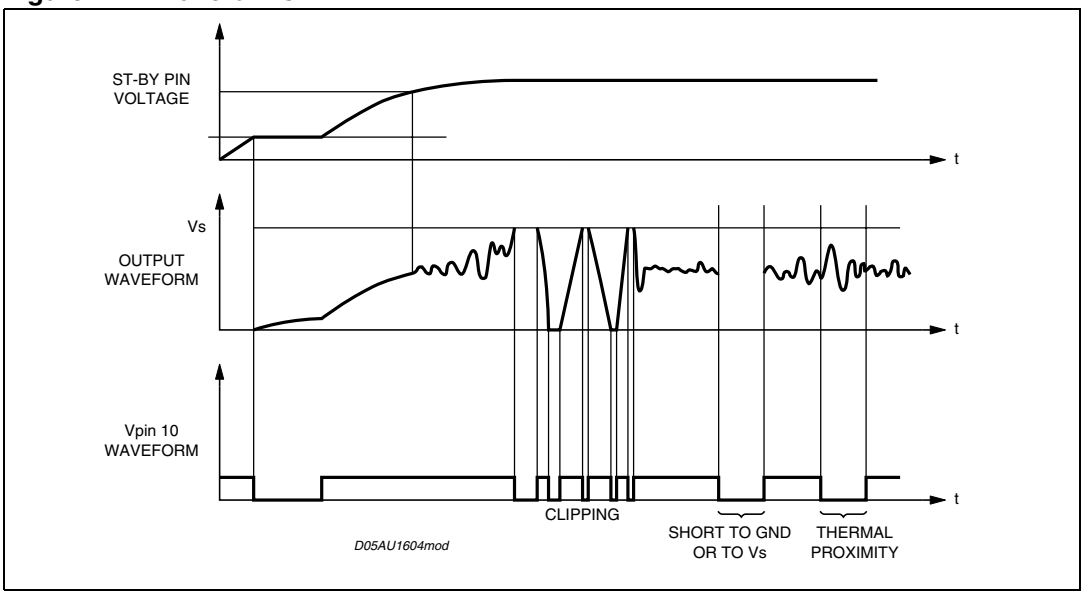
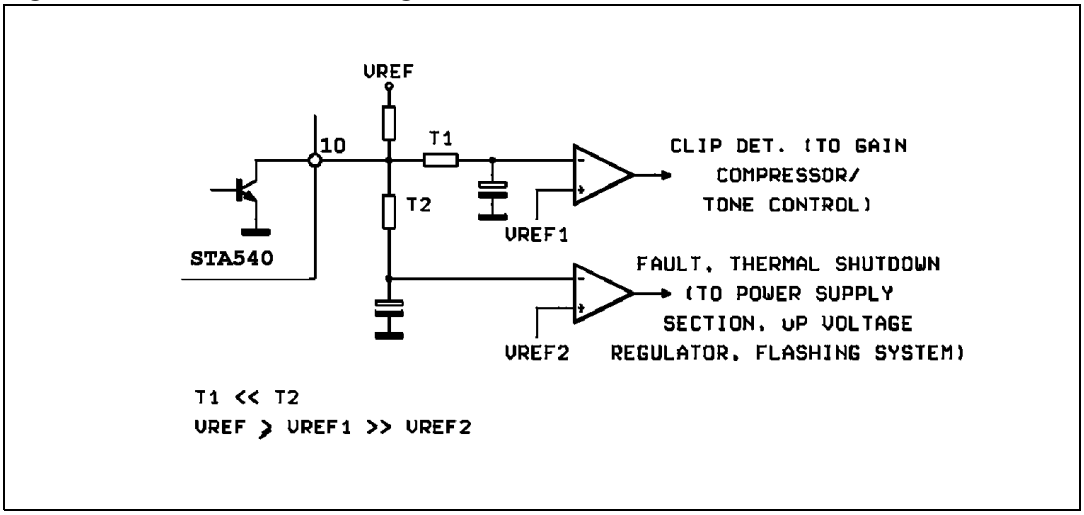



**Figure 28. Interface circuit diagram**



## 6.9 PCB ground layout

The device has two distinct ground pins, P-GND (power ground) and S-GND (signal ground) which are disconnected from each other at chip level. For superior performance the pins P-GND and S-GND must be connected together on the PCB by low-resistance tracks.

For the PCB-ground configuration, a star-like arrangement, where the center is represented by the supply-filtering electrolytic capacitor ground, is recommended. In an arrangement such as this, at least two separate paths must be provided, one for P-GND and one for S-GND.

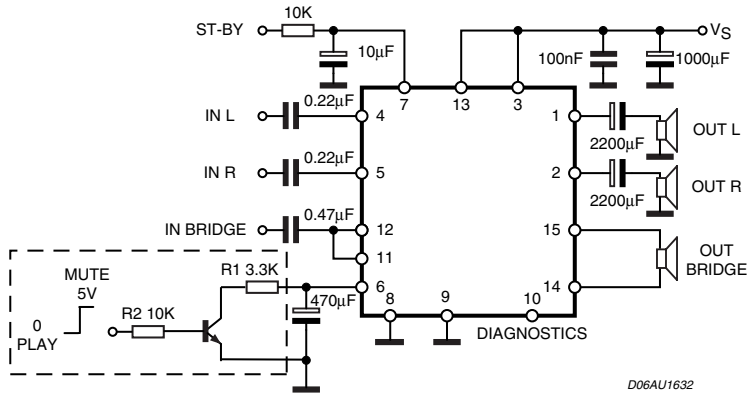
The correct ground assignments are as follows:

- on S-GND:
  - standby capacitor (pin 7, or any other standby driving networks),
  - SVR capacitor (pin 6), to be placed as close as possible to the device,
  - input signal ground (from active/passive signal processor stages)
- on P-GND:
  - power supply filtering capacitors for pins 3 and 13. The negative terminal of the electrolytic capacitor(s) must be directly tied to the battery negative line and this should represent the starting point for all the ground paths.

## 6.10 Mute function

If the mute function is desired, it can be implemented on pin 6, SVR, as shown in *Figure 29*.

**Figure 29. Optional mute function circuit**




$V_S$ = 10 to 16 V,
mute off: $V_{SVR} \geq 0.6$ to 0.8 V,
mute on: $V_{SVR} \geq 0.2$ V

Using a different value for R1 than the suggested 3.3 kΩ, results in two different situations:

- R1 > 3.3 kΩ:
  - pop noise improvement,
  - lower mute attenuation;
- R1 < 3.3 kΩ:
  - pop noise degradation,
  - higher mute attenuation.

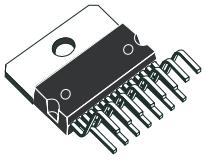
# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

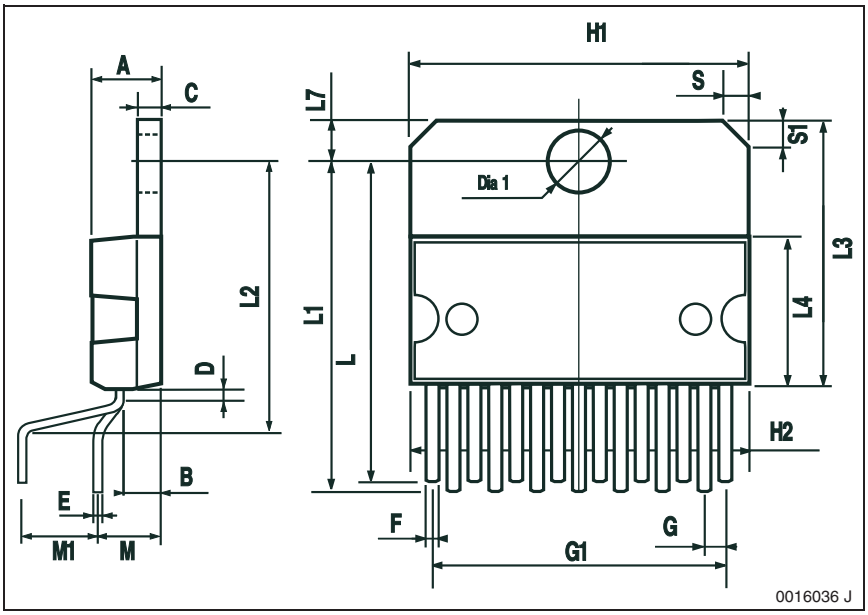
**Figure 30. Mechanical data and package dimensions (Multiwatt15)**

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 5 | | | 0.197 |
| B | | | 2.65 | | | 0.104 |
| C | | | 1.6 | | | 0.063 |
| D | | 1 | | | 0.039 | |
| E | 0.49 | | 0.55 | 0.019 | | 0.022 |
| F | 0.66 | | 0.75 | 0.026 | | 0.030 |
| G | 1.02 | 1.27 | 1.52 | 0.040 | 0.050 | 0.060 |
| G1 | 17.53 | 17.78 | 18.03 | 0.690 | 0.700 | 0.710 |
| H1 | 19.6 | | | 0.772 | | |
| H2 | | | 20.2 | | | 0.795 |
| L | 21.9 | 22.2 | 22.5 | 0.862 | 0.874 | 0.886 |
| L1 | 21.7 | 22.1 | 22.5 | 0.854 | 0.87 | 0.886 |
| L2 | 17.65 | | 18.1 | 0.695 | | 0.713 |
| L3 | 17.25 | 17.5 | 17.75 | 0.679 | 0.689 | 0.699 |
| L4 | 10.3 | 10.7 | 10.9 | 0.406 | 0.421 | 0.429 |
| L7 | 2.65 | | 2.9 | 0.104 | | 0.114 |
| M | 4.25 | 4.55 | 4.85 | 0.167 | 0.179 | 0.191 |
| M1 | 4.73 | 5.08 | 5.43 | 0.186 | 0.200 | 0.214 |
| S | 1.9 | | 2.6 | 0.075 | | 0.102 |
| S1 | 1.9 | | 2.6 | 0.075 | | 0.102 |
| Dia1 | 3.65 | | 3.85 | 0.144 | | 0.152 |

OUTLINE AND MECHANICAL DATA



Multiwatt15 (Vertical)



# 8 Revision history

**Table 6. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| May-2006 | 1 | Initial release |
| Sep-2006 | 2 | Minor non-technical edits |
| Oct-2007 | 3 | Updated description on page 1<br>Updated pin naming, numbering in all relevant figures<br>Minor non-technical edits |
| 21-Jan-2008 | 4 | Updated power specifications on pages 1, 6 and 8<br>Updated short-circuit output current in Table 5 |
| 02-Apr-2012 | 5 | Modified $V_{ST-BY}$ to $V_{SB}$ and updated parameters in *Table 5: Electrical characteristics*<br>Updated ECOPACK® text in *Section 7: Package information* |
| 24-Apr-2012 | 6 | Updated dimension A in *Figure 30: Mechanical data and package dimensions (Multiwatt15)* |

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