STW3040

High voltage fast-switching NPN power transistor

Features

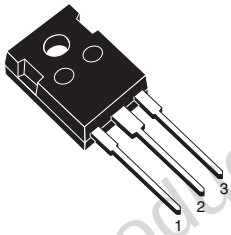
- High voltage capability
- High DC current gain
- Minimum lot-to-lot spread for reliable operation
- Wide safe operating areas (forward and reverse biased)

Applications

- Switching mode power supplies

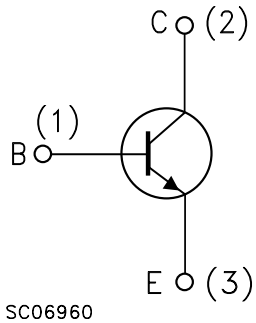
Description

The STW3040 is manufactured using diffused collector in planar technology adopting base island layout. The device is designed for use in SMPS and desktop power supply.



TO-247

Figure 1. Internal schematic diagram



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Table 1. Device summary

Order code	Marking	Package	Packaging
STW3040	W3040	TO-247	Tube

1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{CE} = 0)	700	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	400	V
V_{EBO}	Emitter-base voltage (I_C = 0)	9	V
I_C	Collector current	30	A
I_{CM}	Collector peak current	50	A
I_B	Base current	10	A
I_{BM}	Base peak current	15	A
P_{TOT}	Total dissipation at T_c = 25°C	160	W
T_{stg}	Storage temperature	-65 to 150	°C
T_J	Max. operating junction temperature	150	°C

Table 3. Thermal data

Symbol	Parameters		Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	max	0.78	°C/W

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2 Electrical characteristics

(T_{case} = 25°C; unless otherwise specified)

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector cut-off current (V_{BE} = 0)	V_{CE} = 700 V			1	mA
I_{EBO}	Emitter cut-off current (I_C = 0)	V_{EB} = 9 V			1	mA
$V_{(BR)CEO}$	Collector-emitter breakdown (I_B = 0)	I_C = 10 mA	400			V
$V_{CE(sat)}$ (1)	Collector-emitter saturation voltage	I_C = 6 A I_B = 1.2 A I_C = 20 A I_B = 4 A		0.1 0.4	 0.8	V V
$V_{BE(sat)}$ (1)	Base-emitter saturation voltage	I_C = 6 A I_B = 1.2 A I_C = 20 A I_B = 4 A			1.2 1.5	V V
h_{FE} (1)	DC current gain	I_C = 10 mA V_{CE} = 5 V I_C = 6 A V_{CE} = 5 V I_C = 20 A V_{CE} = 5 V	10 18 10	30	40	
t_{on} t_s t_f	Resistive load Turn-on time Storage time Fall time	I_C = 20 A V_{CC} = 200 V $I_{b(on)}$ = 4 A $I_{b(off)}$ = -8 A			0.5 2.5 0.3	µs µs µs

1. Pulse duration = 300 ms, duty cycle ≤1.5 %

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2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

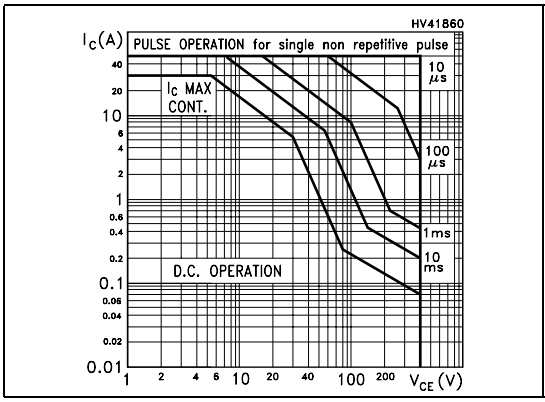


Figure 3. Derating curve

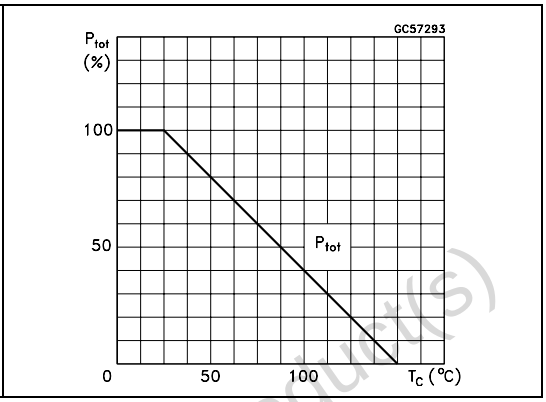


Figure 4. Reverse biased safe operating area

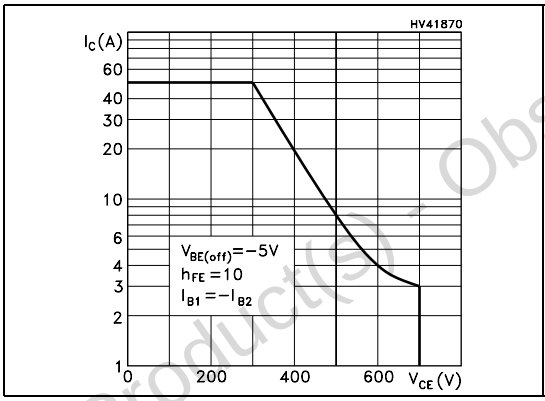


Figure 5. Output characteristics

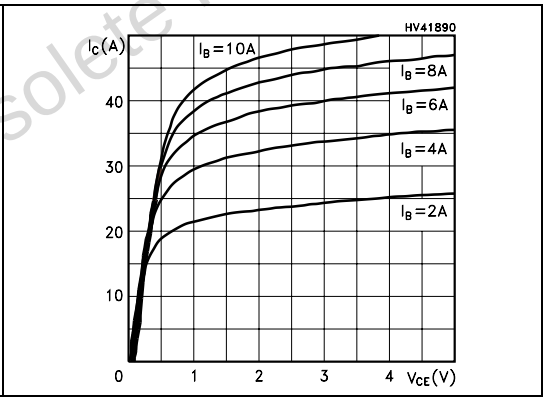


Figure 6. DC current gain

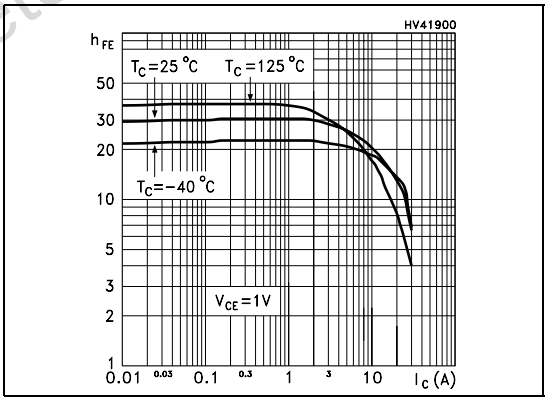
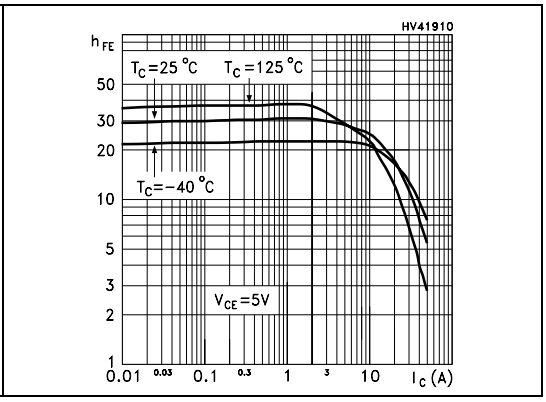


Figure 7. DC current gain



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Figure 8. Collector-emitter saturation voltage

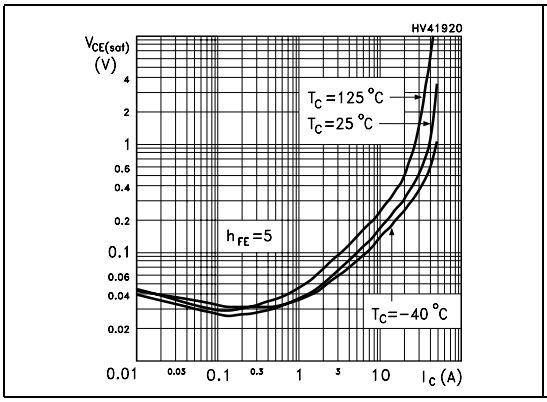


Figure 9. Base-emitter saturation voltage

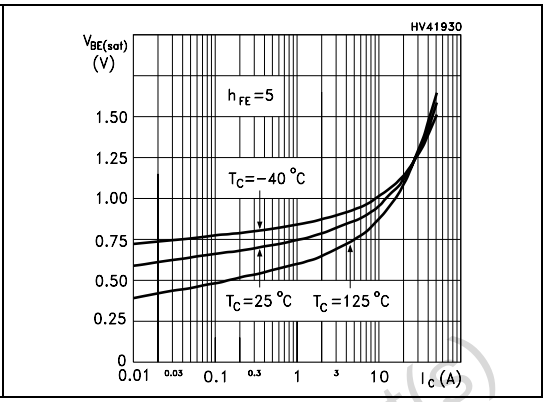


Figure 10. Resistive load switching on time

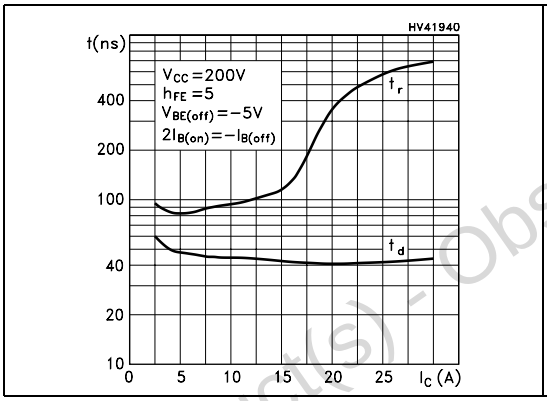
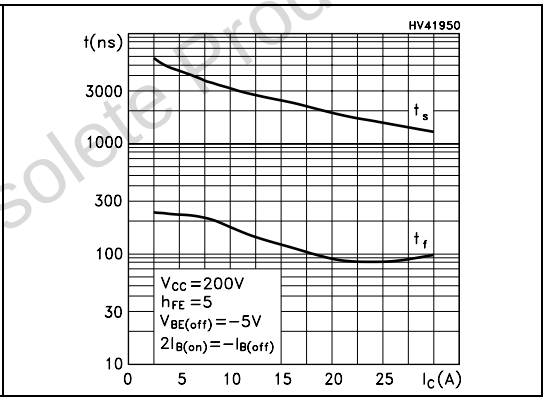


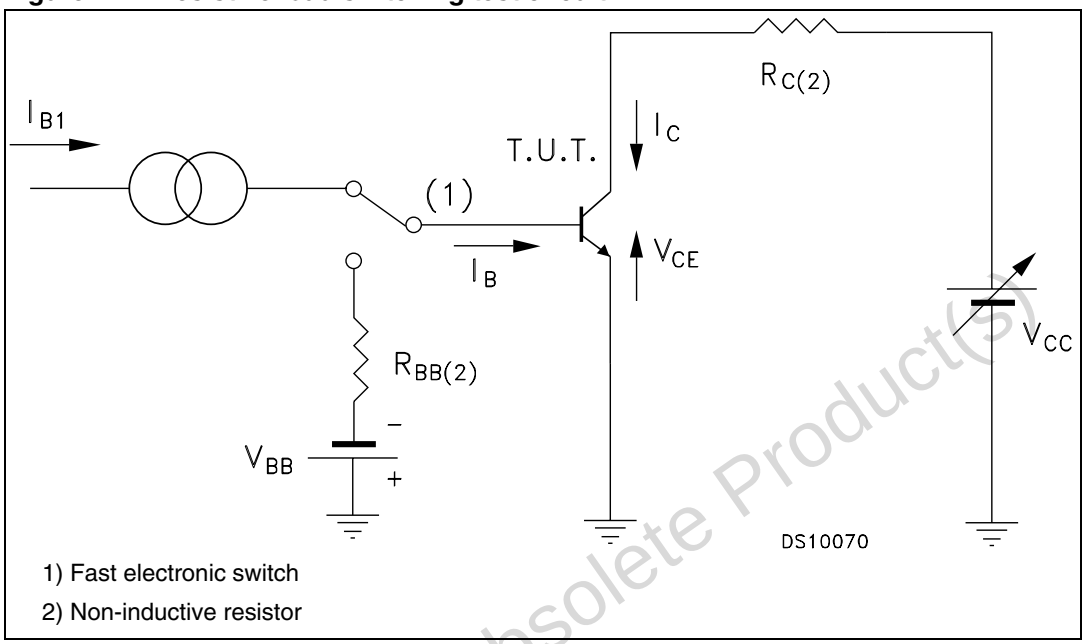
Figure 11. Resistive load switching off time



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3 Test circuit

Figure 12. Resistive load switching test circuit



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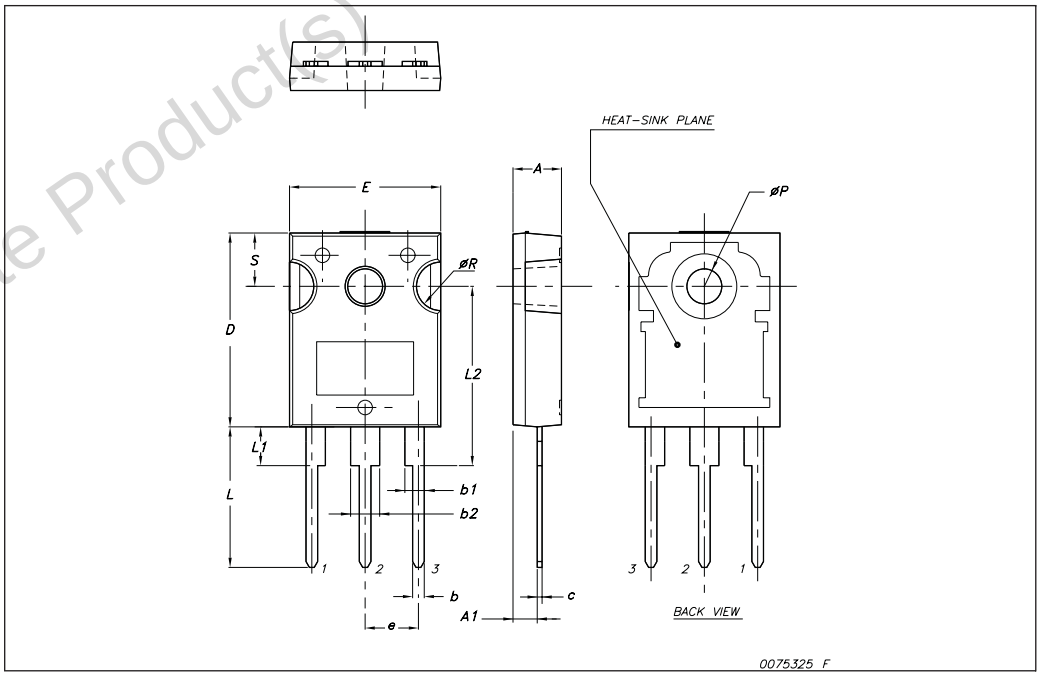
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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TO-247 Mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



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5 Revision history

Table 5. Document revision history

Date	Revision	Changes
12-Dec-2007	1	Initial release
09-Oct-2008	2	Document status promoted from preliminary data to datasheet
23-Oct-2008	3	Test conditions changed for $V_{CE(sat)}$ in *Table 4*

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