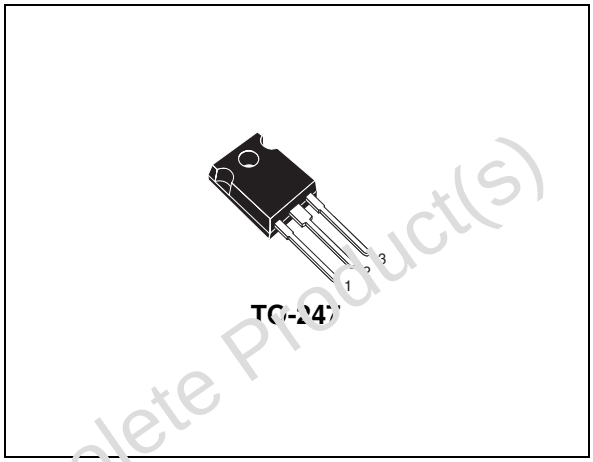
STW55NM50N

N-channel 500 V, 0.040 Ω, 54 A, MDmesh™ II Power MOSFET TO-247

Features

Type	V_{DSS} (@Tjmax)	$R_{DS(on)}$ max	I_D
STW55NM50N	550 V	<0.054 Ω	54 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Application

- Switching applications

Description

This series of devices implements second generation MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

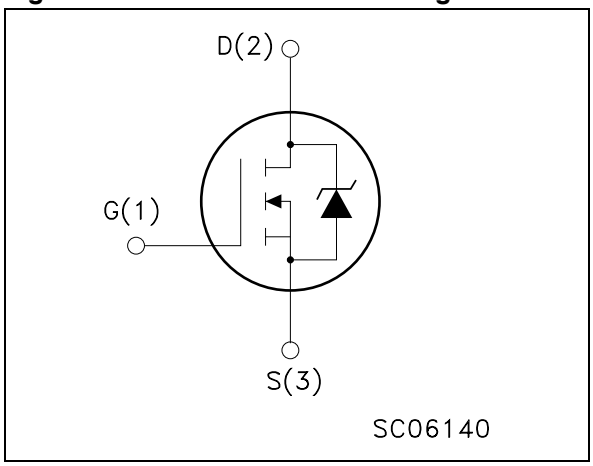


Table 1. Device summary

Order code	Marking	Package	Packaging
STW55NM50N	55NM50N	TO-247	Tube

Obsolete Product(s) - Obsolete Product(s)

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2 Electrical characteristics 4

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4 Package mechanical data 9

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Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	500	V
V_{GS}	Gate- source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	54	A
I_D	Drain current (continuous) at T_C = 100 °C	35	A
I_{DM} (1)	Drain current (pulsed)	216	A
P_{TOT}	Total dissipation at T_C = 25 °C	350	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 54$ A, di/dt ≤ 400 A/µs, V_{DD} =80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.36	°C/W
Rthj-amb	Thermal resistance junction-ambient max	50	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	15	A
E_{AS}	Single pulse avalanche energy (starting Tj=25 °C, I_D=I_{AS}, V_{DD}=50 V)	1600	mJ

Obsolete Product(s) - Obsolete Product(s)

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	500			V
dv/dt (1)	Drain source voltage slope	V_{DD}=400 V, I_D = 54 A, V_{GS}=10 V		30		V/ns
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, @125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 27 A		0.040	0.054	Ω

1. Characteristic value at turn off on inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS}=15 V, I_D = 27 A		42		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0		5800 370 30		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{GS} = 0V, V_{DS} = 0V to 400V		750		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400 V, I_D = 54 A, V_{GS} = 10 V *(see Figure 15)*		180 23 90		nC nC nC
R_g	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level = 20 mV open drain		2		Ω

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Obsolete Product(s) - Obsolete Product(s)

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} =250 V, I_D = 27 A		40		ns
t_r	Rise time	R_G = 4.7 Ω V_{GS} = 10 V		40		ns
$t_{d(off)}$	Turn-off delay time	*(see Figure 14)*		250		ns
t_f	Fall time			70		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				54	A
I_{SDM} (1)	Source-drain current (pulsed)				216	A
V_{SD} (2)	Forward on voltage	I_{SD} = 54 A, V_{GS} = 0			1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 54 A, di/dt = 100 A/µs		630		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V		13		µC
I_{RRM}	Reverse recovery current	*(see Figure 16)*		40		A
t_{rr}	Reverse recovery time	I_{SD} = 54 A, di/dt = 100 A/µs		750		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_j = 150 °C		16		µC
I_{RRM}	Reverse recovery current	*(see Figure 16)*		42		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Obsolete Product(s) - Obsolete Product(s)

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

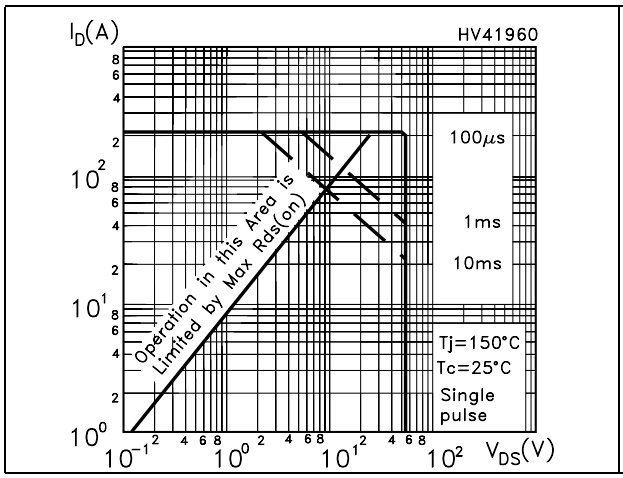


Figure 3. Thermal impedance

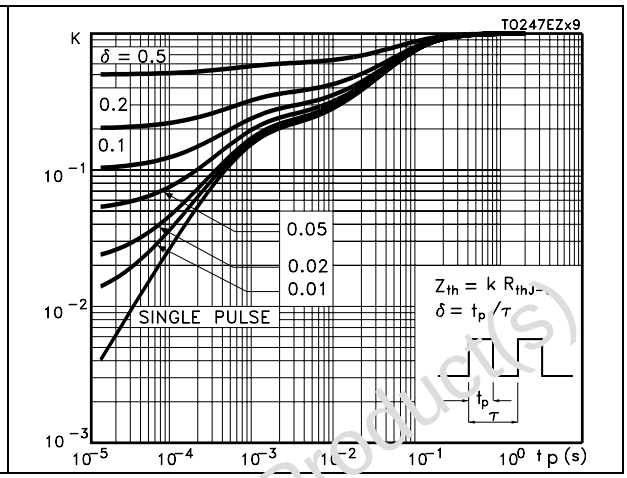


Figure 4. Output characteristics

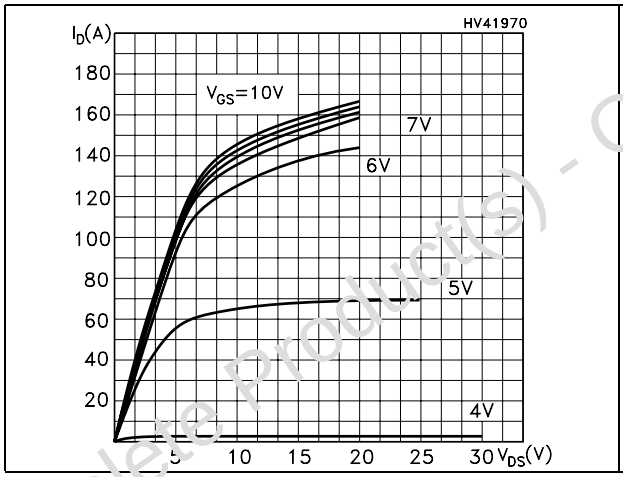


Figure 5. Transfer characteristics

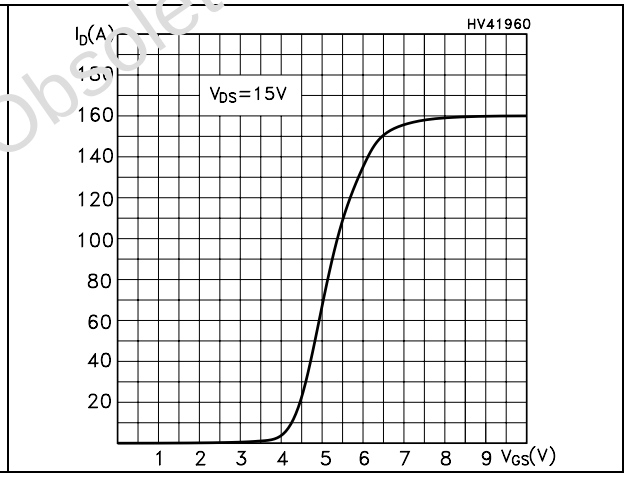


Figure 6. Transconductance

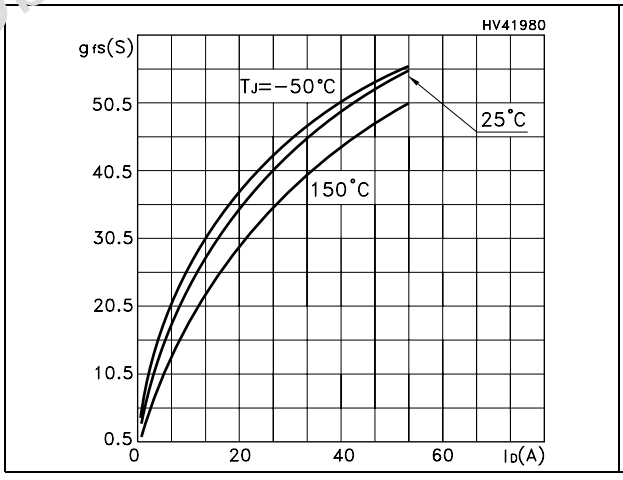
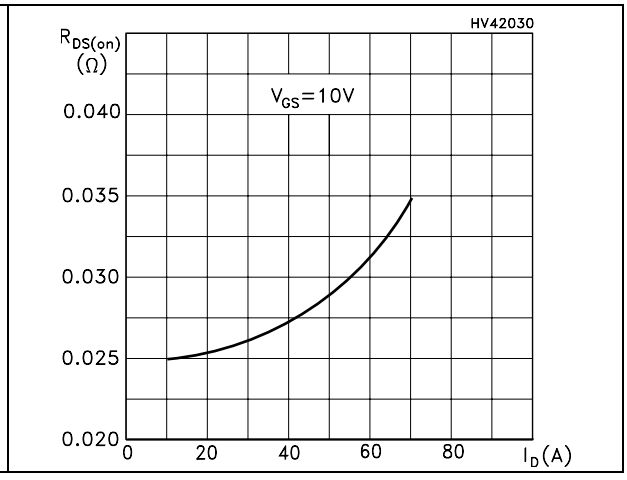


Figure 7. Static drain-source on resistance



Obsolete Product(s) - Obsolete Product(s)

Figure 8. Gate charge vs gate-source voltage

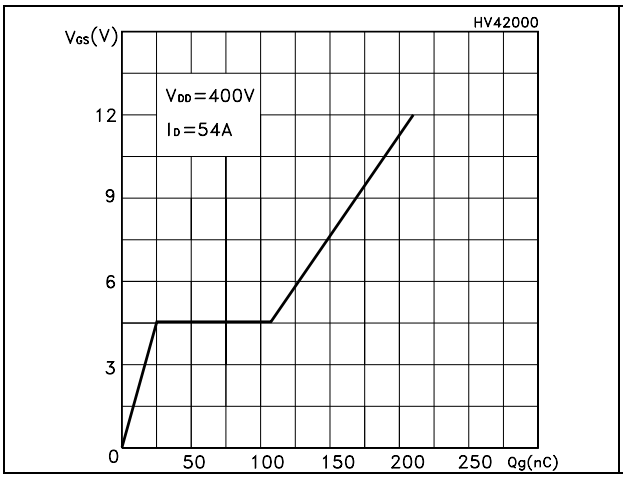


Figure 9. Capacitance variations

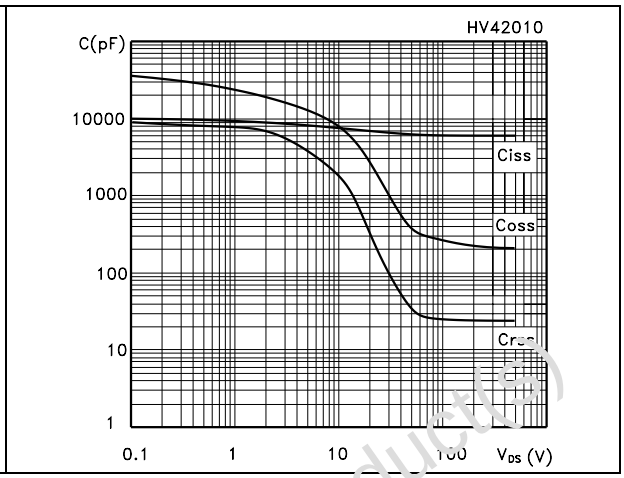


Figure 10. Normalized gate threshold voltage vs temperature

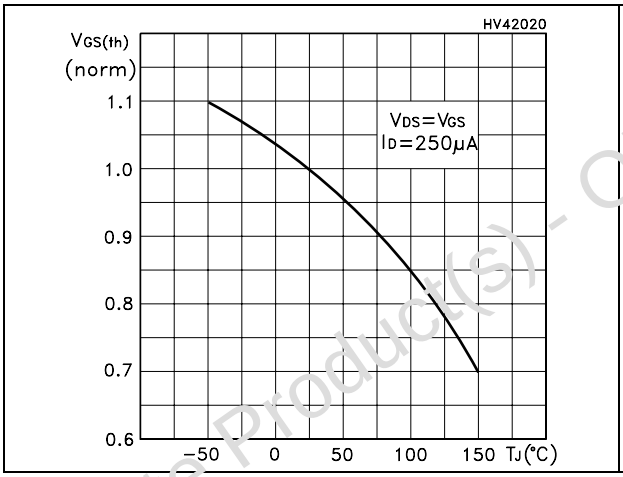


Figure 11. Normalized on resistance vs temperature

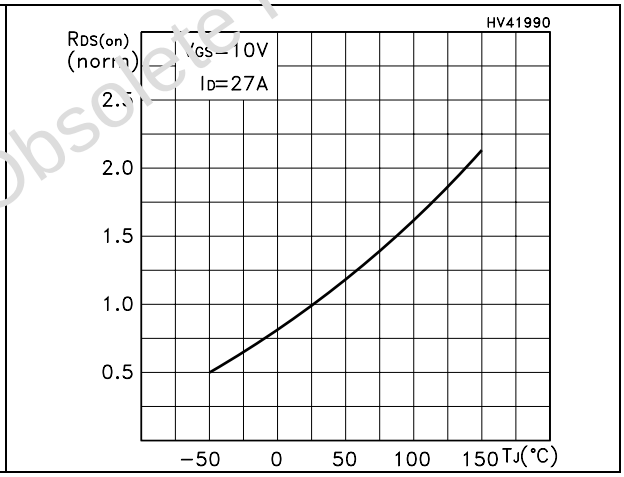


Figure 12. Normalized BV_{DSS} vs temperature

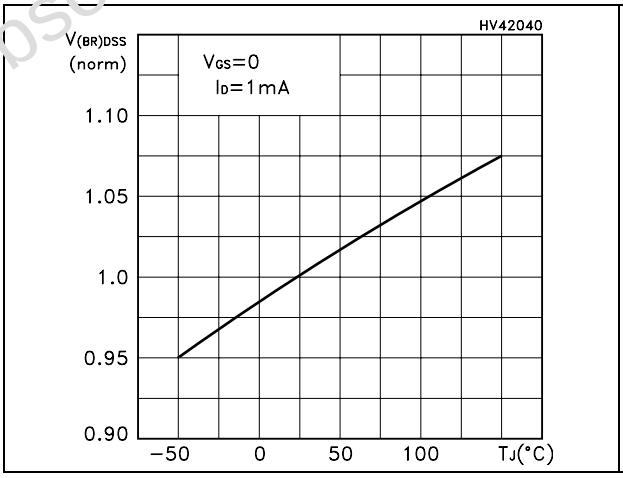
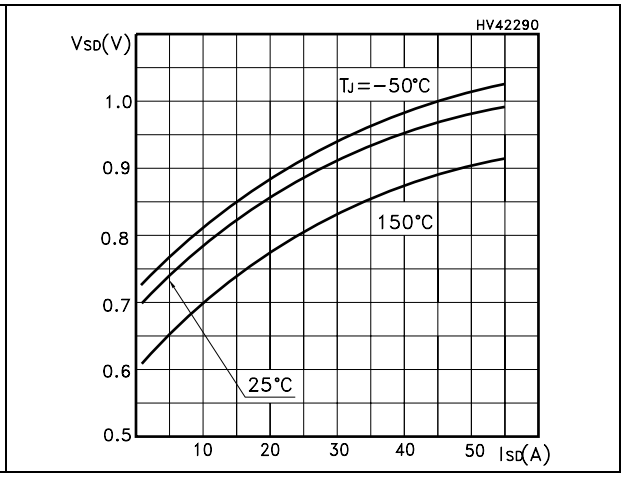


Figure 13. Source-drain diode forward characteristics



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3 Test circuits

Figure 14. Switching times test circuit for resistive load

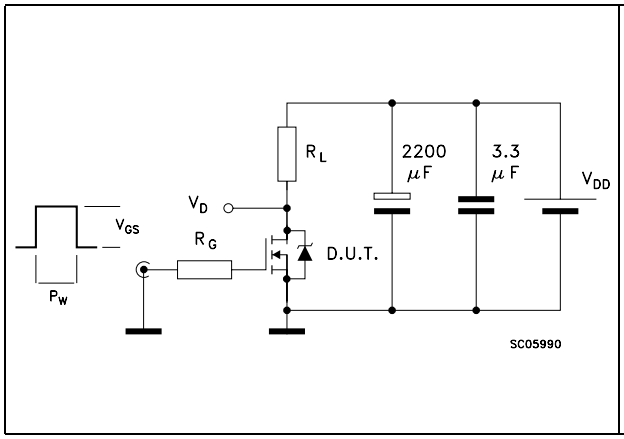


Figure 15. Gate charge test circuit

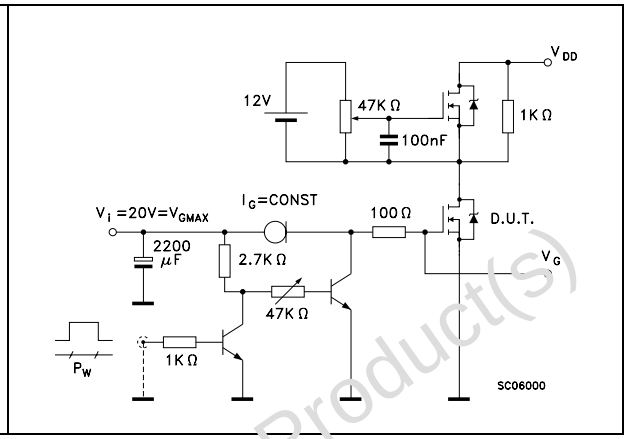


Figure 16. Test circuit for inductive load switching and diode recovery times

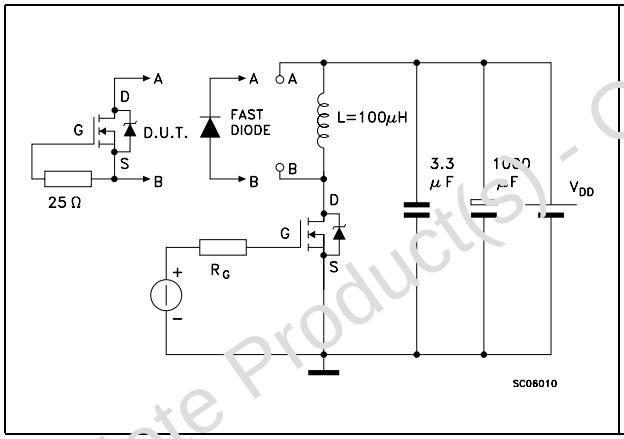


Figure 17. Unclamped Inductive load test circuit

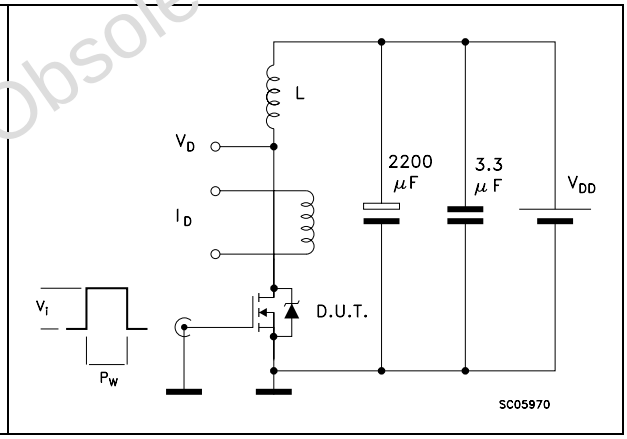


Figure 18. Unclamped inductive waveform

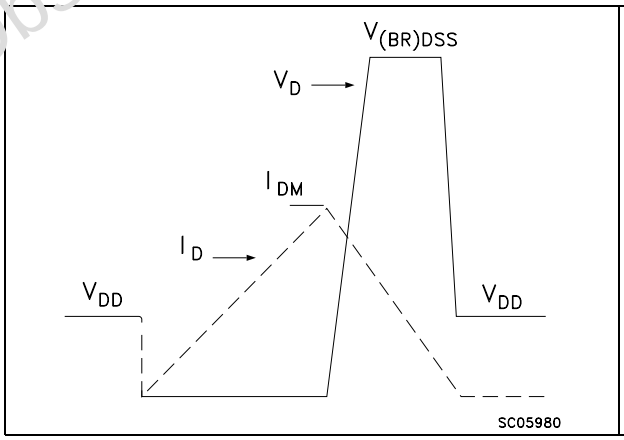
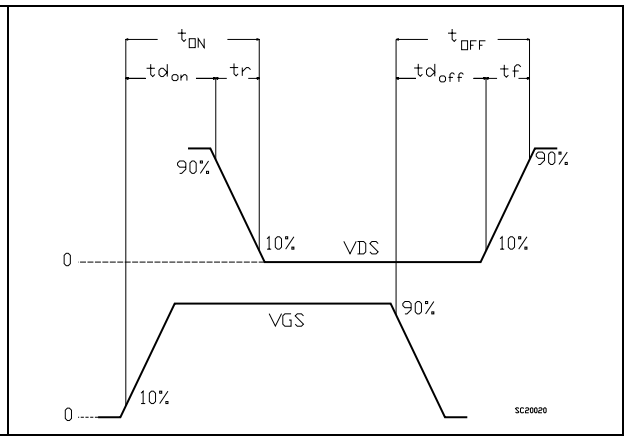


Figure 19. Switching time waveform



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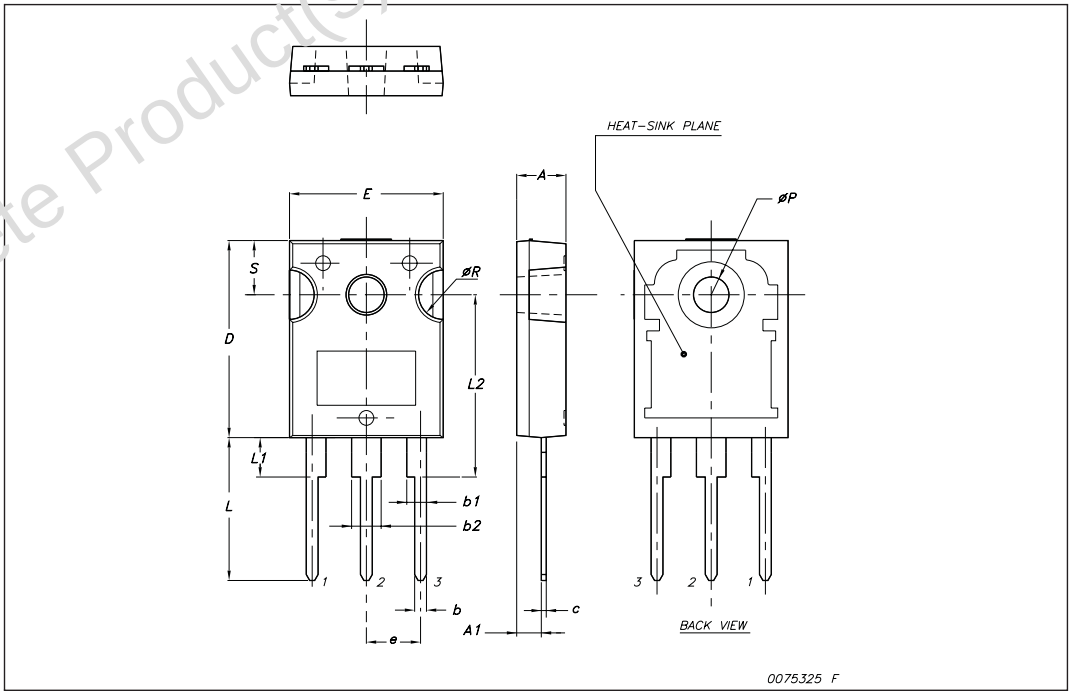
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

Obsolete Product(s) - Obsolete Product(s)

TO-247 mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



Obsolete Product(s) - Obsolete Product(s)

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
22-Apr-2008	1	First release
29-Jul-2008	2	E_{AS} value has been updated in *Table 4*

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