STF17N62K3
STP17N62K3, STW17N62K3

N-channel 620 V, 0.28 Ω, 15.5 A, TO-220FP, TO-220, TO-247 SuperMESH3™ Power MOSFET

Features

Order codes	V_{DSS}	$R_{DS(on)}$ max.	I_D	Pw
STF17N62K3	620 V	< 0.34 Ω	15.5 A	40 W
STP17N62K3	620 V	< 0.34 Ω	15.5 A	190 W
STW17N62K3	620 V	< 0.34 Ω	15.5 A	190 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

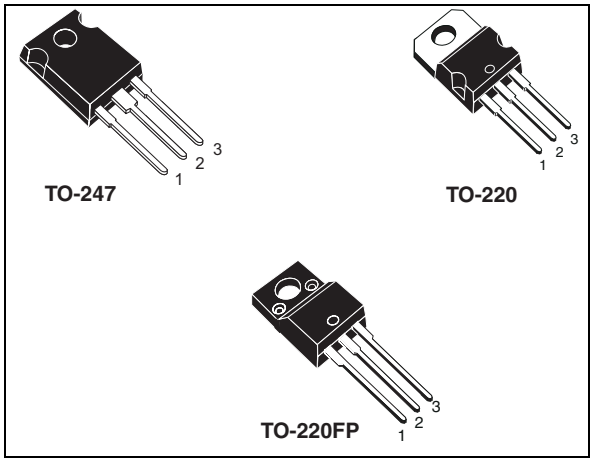
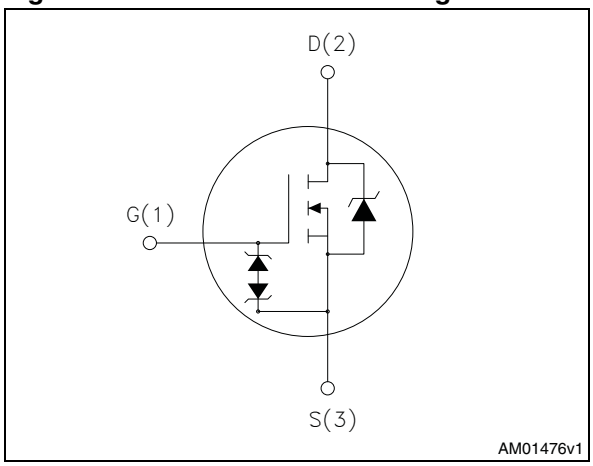


Figure 1. Internal schematic diagram



Applications

- Switching applications

Description

This SuperMESH3™ Power MOSFET is the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STF17N62K3	17N62K3	TO-220FP	Tube
STP17N62K3	17N62K3	TO-220	Tube
STW17N62K3	17N62K3	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220 TO-247	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	620		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	15.5	15.5 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	10	10 (1)	A
I_{DM} (2)	Drain current (pulsed)	62	62 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	190	40	W
I_{AR} (3)	Avalanche current, repetitive or not-repetitive	15.5		A
E_{AS} (4)	Single pulse avalanche energy	260		mJ
	Derating factor	1.52	0.32	W/°C
dv/dt (5)	Peak diode recovery voltage slope	9		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; Tc = 25 °C)		2500	V
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Limited only by temperature allowed.
2. Pulse width limited by safe operating area.
3. Pulse width limited by Tj max.
4. Starting Tj = 25°C, $I_D = I_{AR}$, V_{DD} = 50V.
5. $I_{SD} \leq 15.5$ A, di/dt $\leq$ 400 A/µs, V_{DD} = 80% $V_{(BR)DSS}$, V_{DS} peak < $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	TO-220FP	TO-220	TO-247	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	3.13	0.66		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5		50	°C/W
T_l	Maximum lead temperature for soldering purpose	300			°C

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA	620			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 620 V V_{DS} = 620 V, T_C=125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 7.5 A		0.28	0.34	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	3100 200 35	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 496 V, V_{GS} = 0	-	140	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	200	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	2.3	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 496 V, I_D = 15.5 A, V_{GS} = 10 V (see *Figure 20*)	-	105 16 62	-	nC nC nC

1. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 310 V, I_D = 7.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 19*)	-	22 29 110 62	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		15.5 62	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 15.5 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 15.5 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 24*)	-	380 5000 26		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 15.5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 24*)	-	450 6500 29		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30			V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

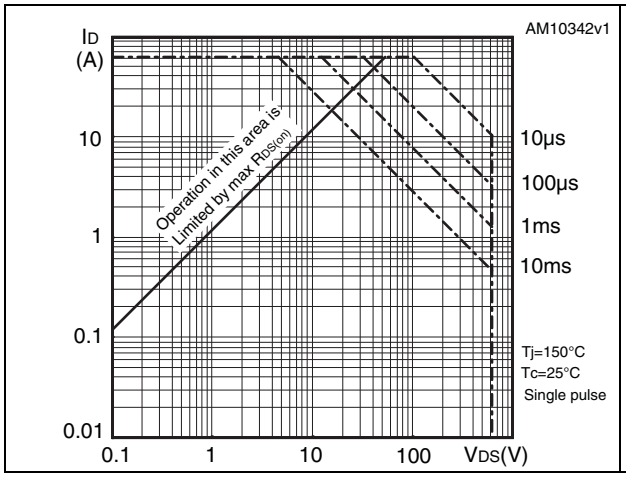


Figure 3. Thermal impedance for TO-220FP

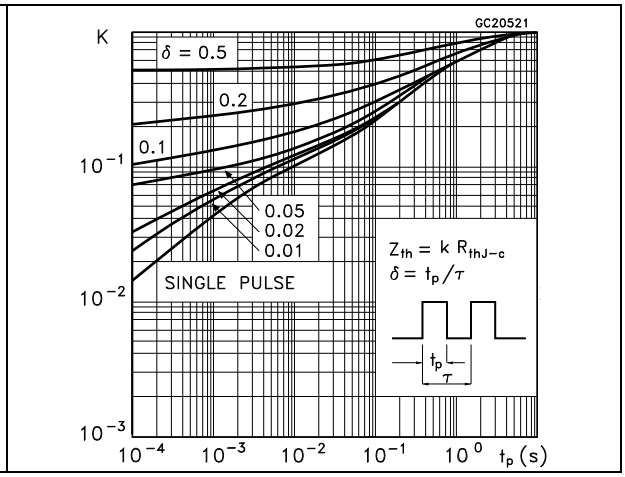


Figure 4. Safe operating area for TO-220

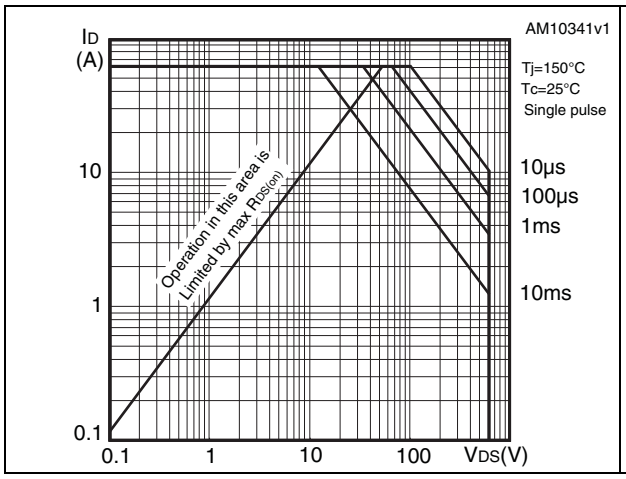


Figure 5. Thermal impedance for TO-220

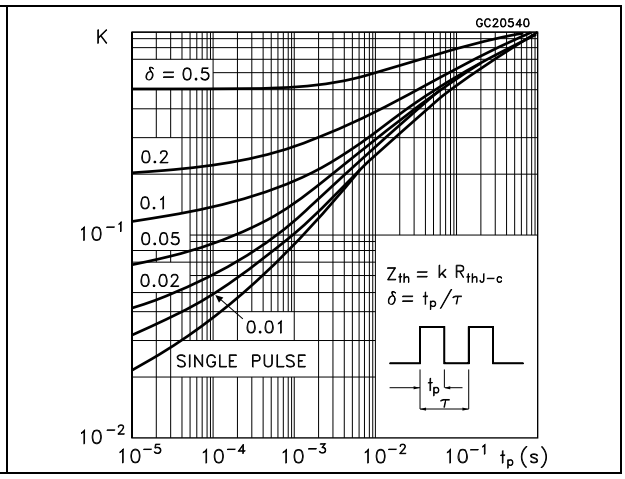


Figure 6. Safe operating area for TO-247

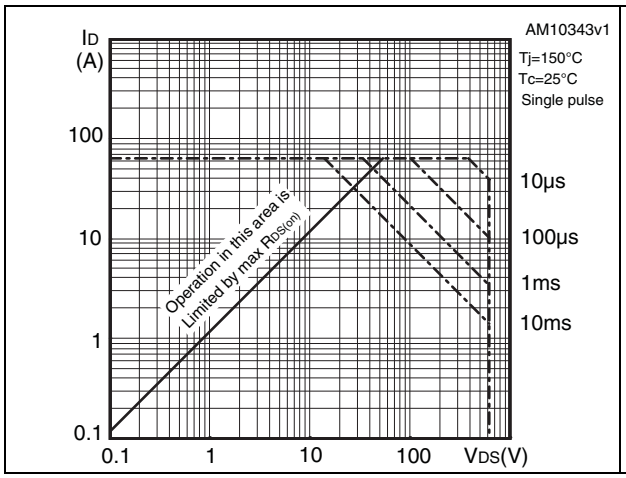


Figure 7. Thermal impedance for TO-247

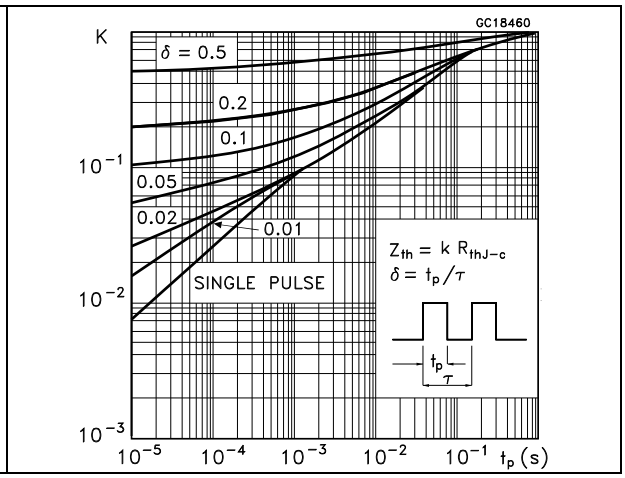


Figure 8. Output characteristics

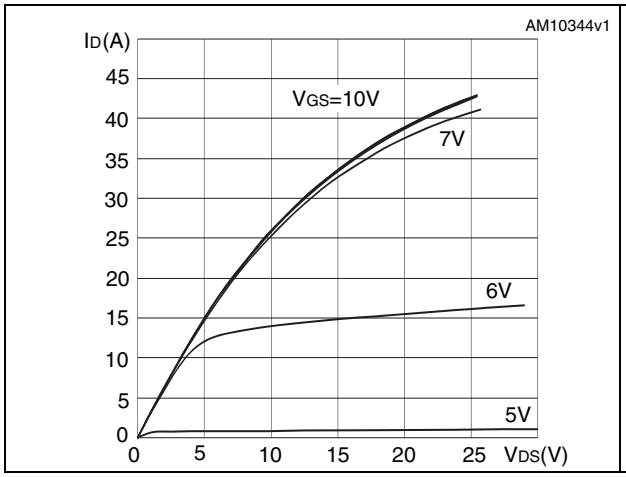


Figure 9. Transfer characteristics

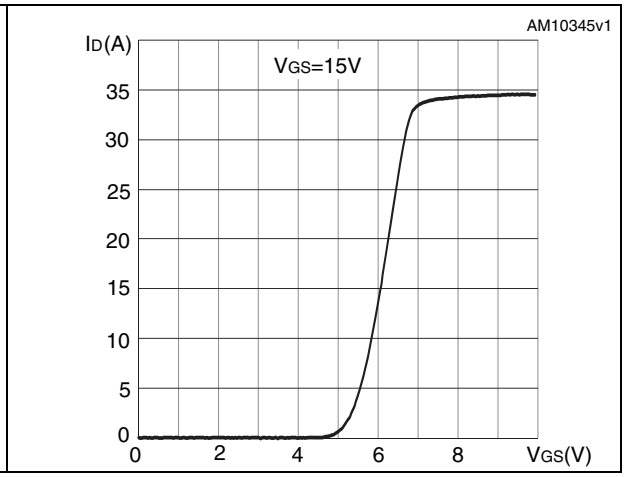


Figure 10. Gate charge vs gate-source voltage

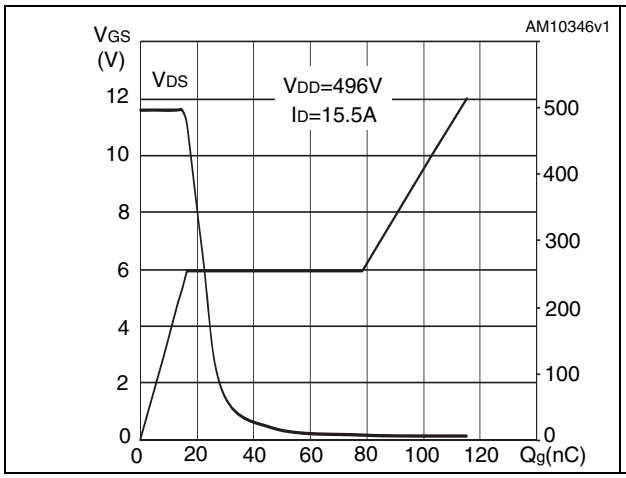


Figure 11. Static drain-source on resistance

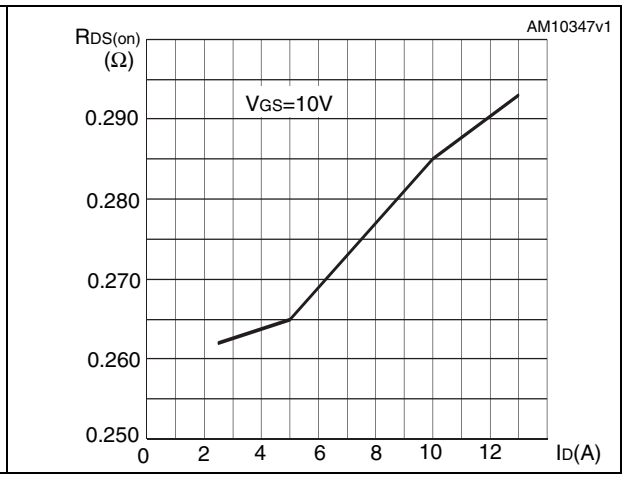


Figure 12. Capacitance variations

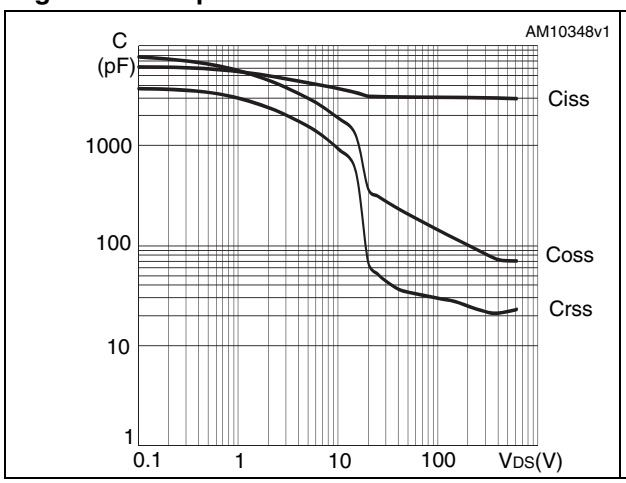


Figure 13. Output capacitance stored energy

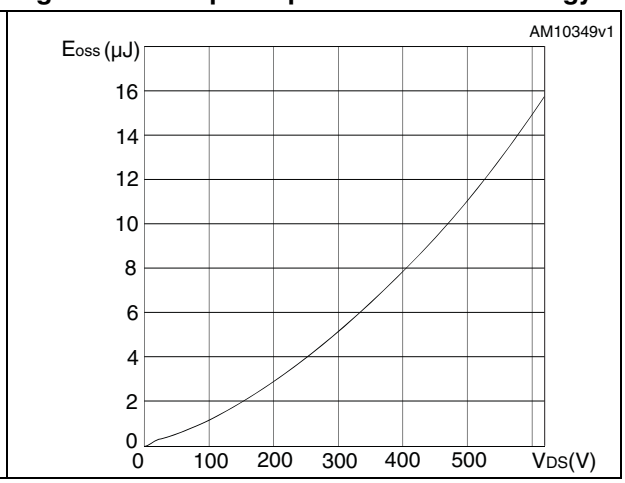


Figure 14. Normalized gate threshold voltage vs temperature

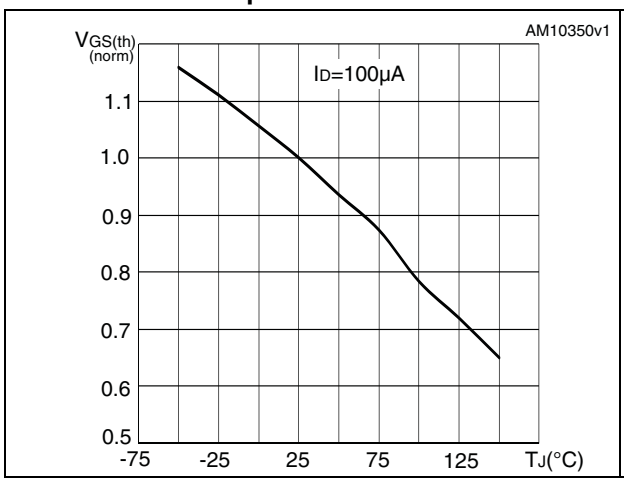


Figure 15. Normalized on resistance vs temperature

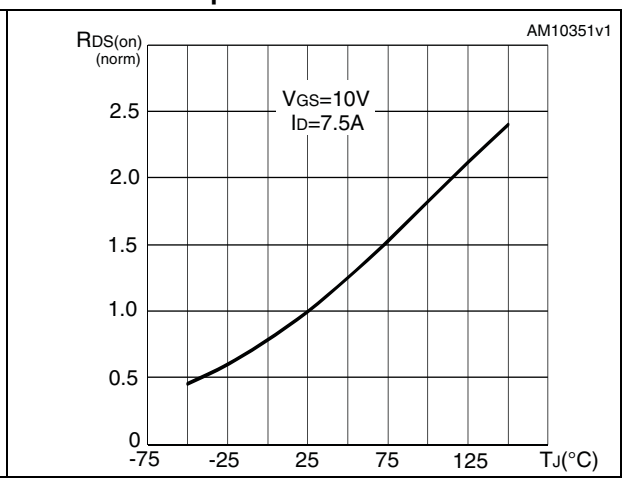


Figure 16. Source-drain diode forward characteristics

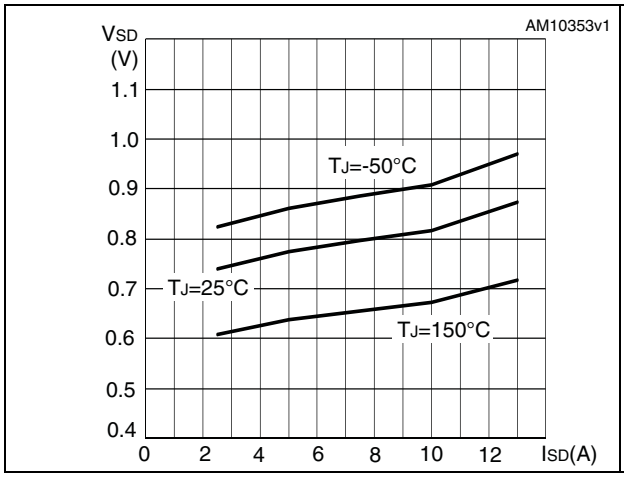


Figure 17. Normalized B_{VDSS} vs temperature

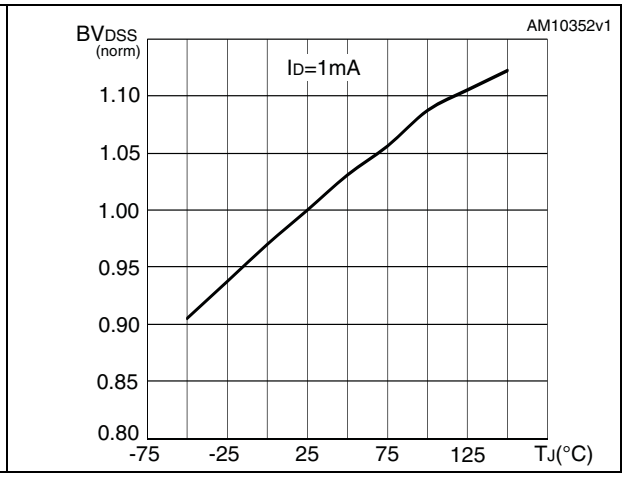
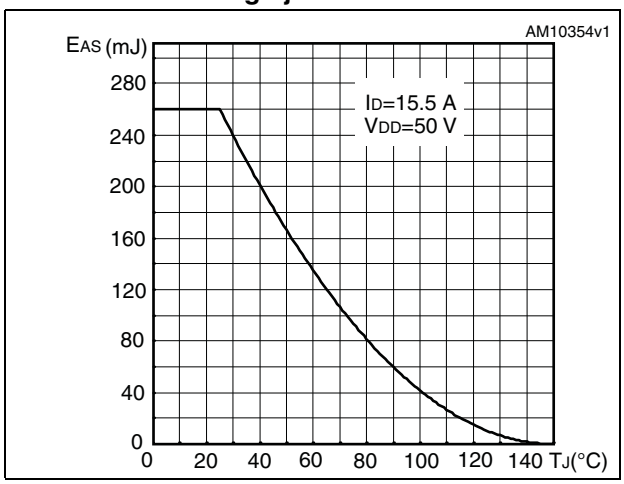


Figure 18. Maximum avalanche energy vs starting Tj



3 Test circuits

Figure 19. Switching times test circuit for resistive load

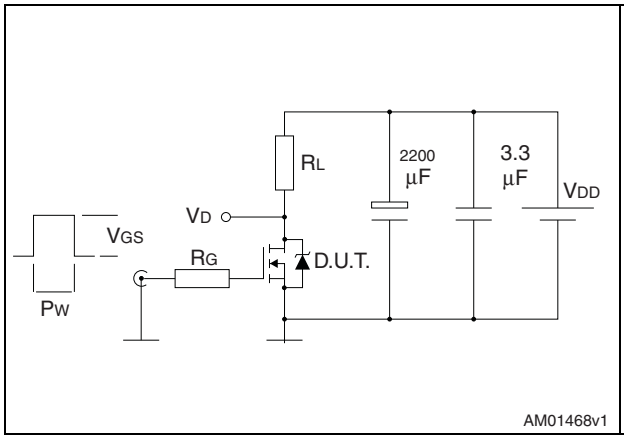


Figure 20. Gate charge test circuit

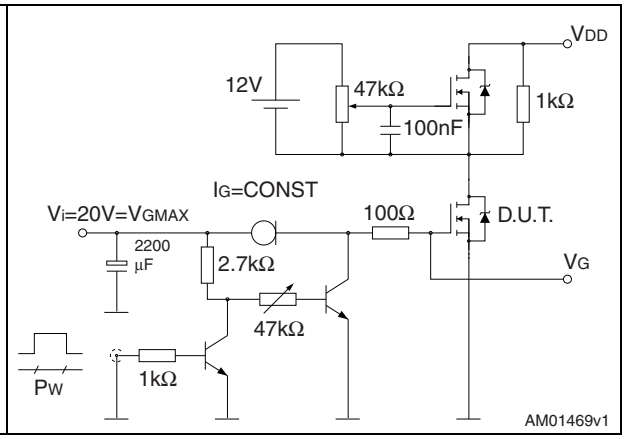


Figure 21. Test circuit for inductive load switching and diode recovery times

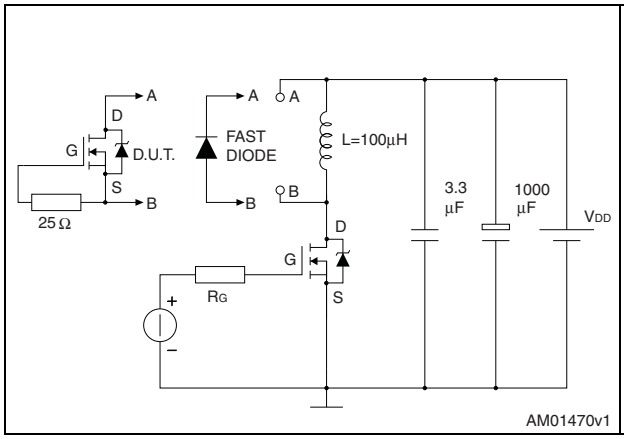


Figure 22. Unclamped Inductive load test circuit

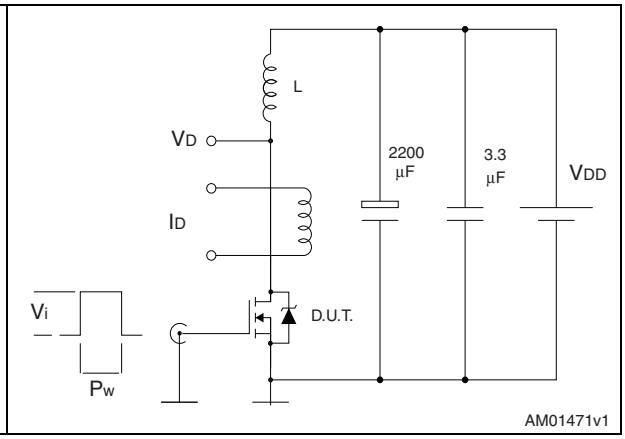


Figure 23. Unclamped inductive waveform

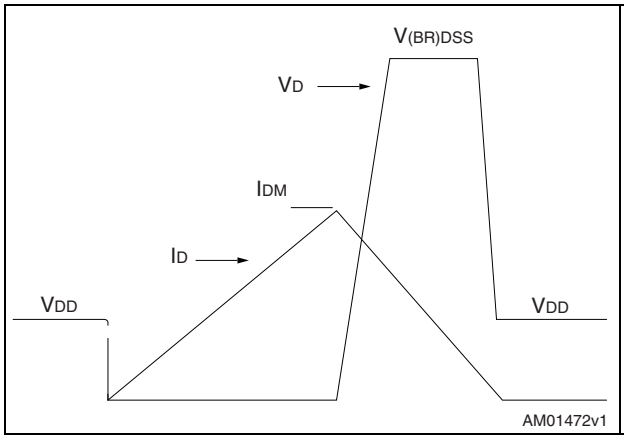
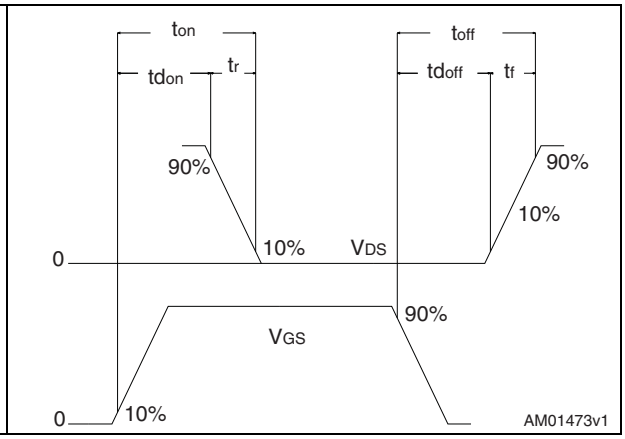


Figure 24. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 25. TO-220FP drawing

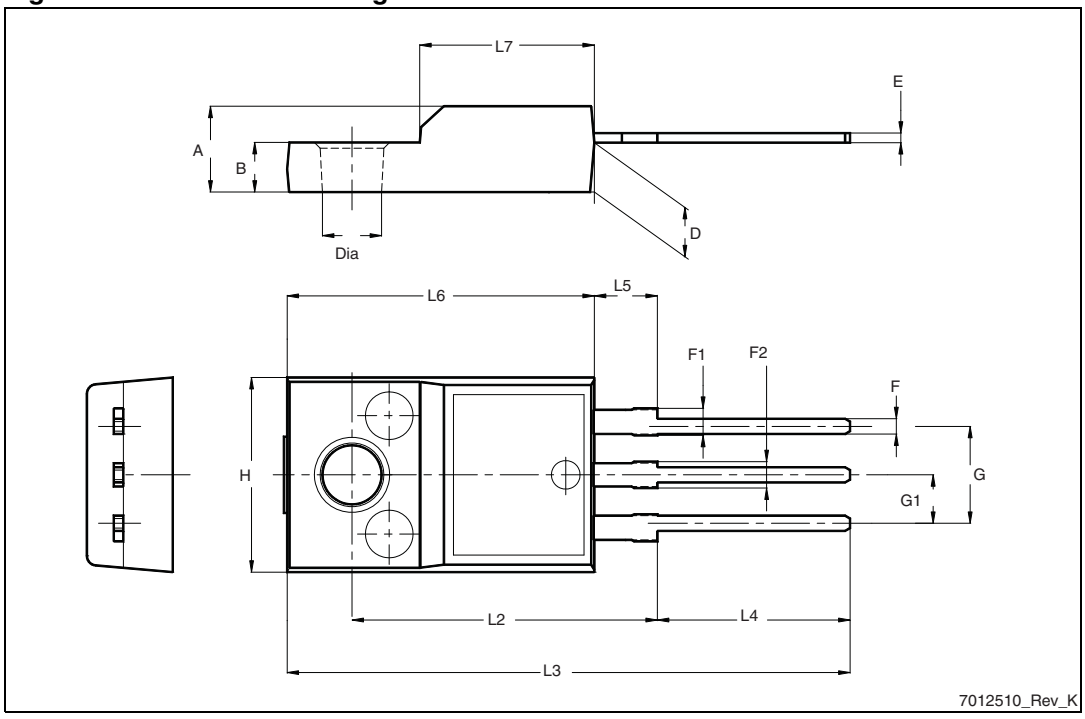


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 26. TO-220 type A drawing

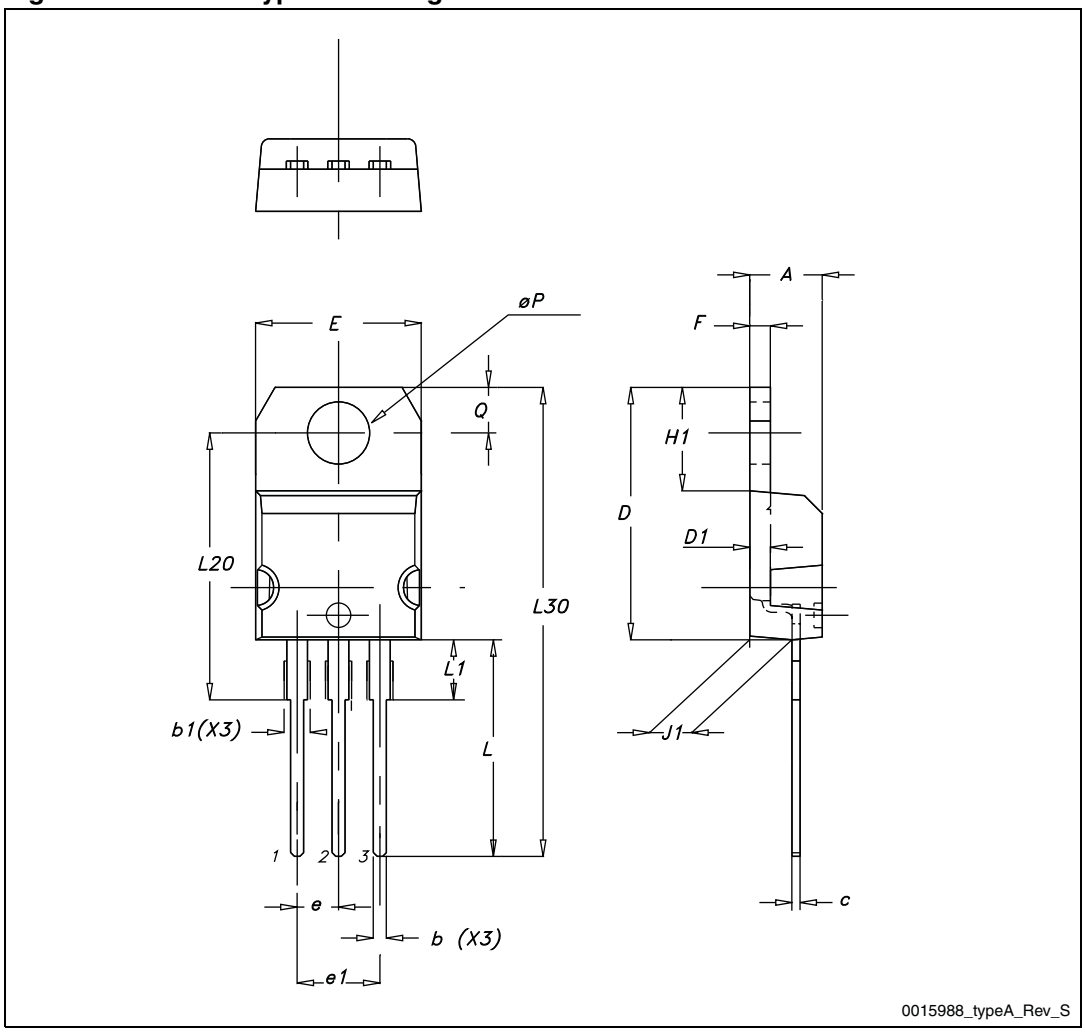
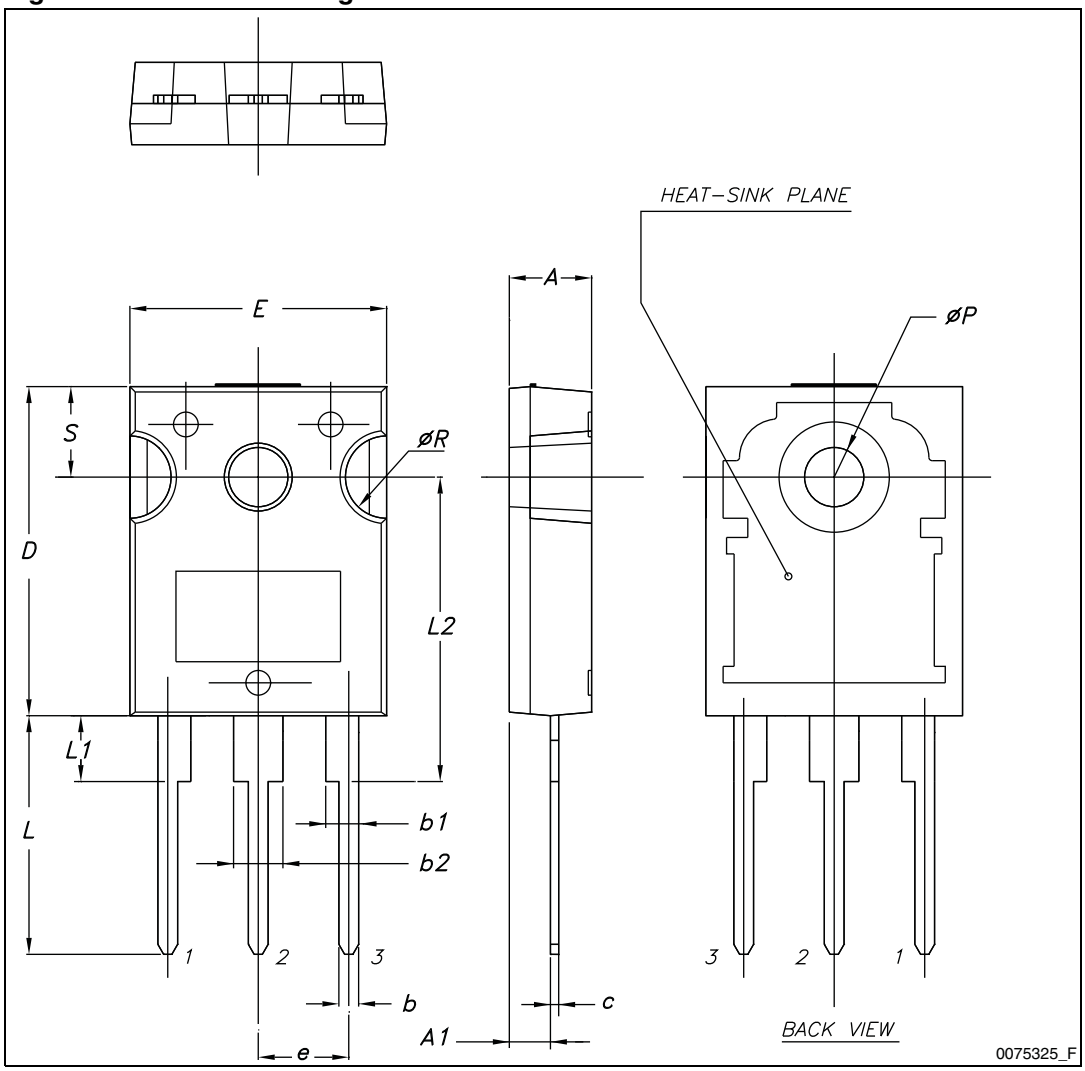


Table 11. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S		5.50	

Figure 27. TO-247 drawing



5 Revision history

Table 12. Document revision history

Date	Revision	Changes
11-Nov-2008	1	First release.
27-Jul-2011	2	*Section 2.1: Electrical characteristics (curves)* has been updated. Minor text changes.

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