ESDALC14V2-1U2

Single-line low capacitance Transil™ for ESD protection

Features

- Breakdown voltage V_{BR} = 14.2 V min.
- Unidirectional device
- Multiple ESD strike sustainability
- Very low diode capacitance: 6 pF typ. at 0 V
- Low leakage current
- 0201 SMD package size compatible
- Ultra small PCB area: 0.18 mm^2
- RoHS compliant

Benefits

- High ESD protection level
- High integration
- Suitable for high density boards
- MSL1

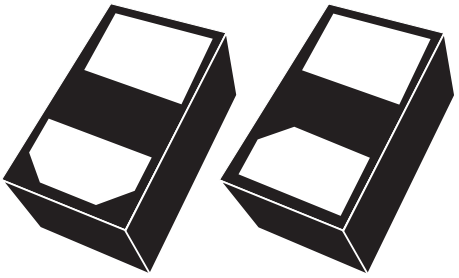
Complies with the following standards:

- IEC 61000-4-2 level 4

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

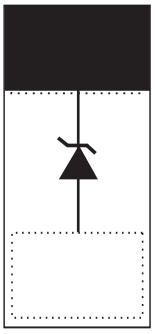
- Portable multimedia players and accessories
- Notebooks
- Digital cameras and camcorders
- Communication systems
- Cellular phone handsets and accessories



Pin 1 available in different forms

ST0201 package

Figure 1. Functional diagram (top view)



Description

The ESDALC14V2-1U2 is a unidirectional single line TVS diode designed to protect the data lines or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage: IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge		 ±8 ±15	kV
P_{PP}	Peak pulse power dissipation (8/20 µs) (1)	$T_{j\ initial}$ = T_{amb}	30	W
I_{PP}	Peak pulse current (8/20 µs)		1.5	A
T_j	Junction temperature		125	°C
T_{stg}	Storage temperature range		- 55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C
T_{op}	Operating junction temperature range		-40 to +125	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit

Figure 2. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
V_{CL}	=	Clamping voltage
I_{RM}	=	Leakage current @ V_{RM}
V_{RM}	=	Stand-off voltage
I_F	=	Forward current
I_{PP}	=	Peak pulse current
I_R	=	Breakdown current
V_F	=	Forward voltage drop
R_d	=	Dynamic impedance
αT	=	Voltage temperature

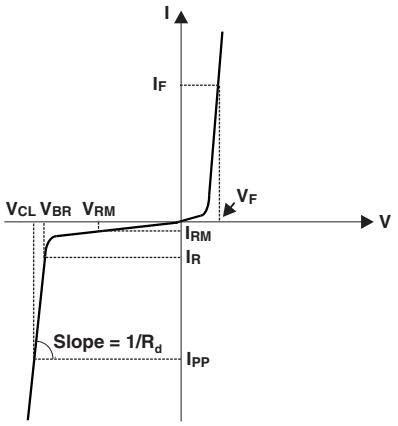


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	14.2	-	17.0	V
I_{RM}	V_{RM} = 3 V	-	-	100	nA
R_d	Square pulse, I_{PP} = 1 A t_p = 2.5 µs	-	2.6	-	Ω
αT	$\Delta V_{BR} = \alpha T(T_{amb}$ - 25 °C) x V_{BR} (25 °C)	-	-	7.2	10^{-4}/°C
C_{line}	V_R = 0 V, F_{osc} = 1 MHz, V_{osc} = 30 mV	-	6.0	-	pF

Figure 3. Relative variation of peak pulse power versus initial junction temperature

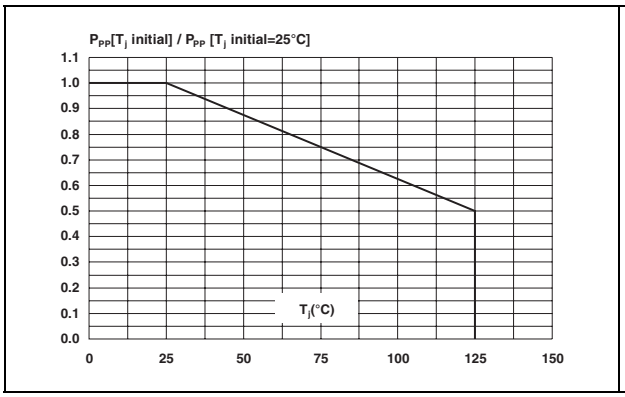


Figure 4. Peak pulse power versus exponential pulse duration

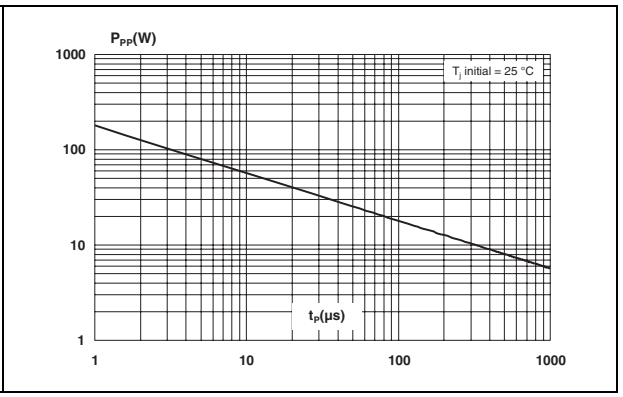


Figure 5. Clamping voltage versus peak pulse current (square pulse, typical values)

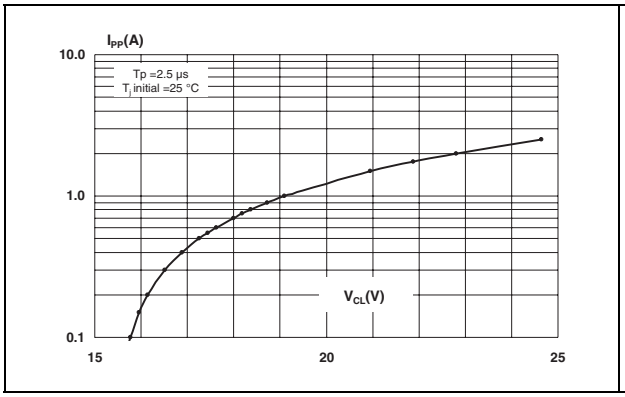


Figure 6. Junction capacitance versus reverse applied voltage (typical values)

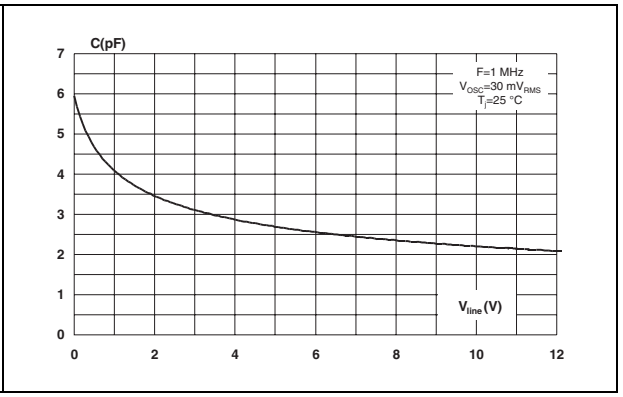


Figure 7. Relative variation of leakage current versus junction temperature (typical values)

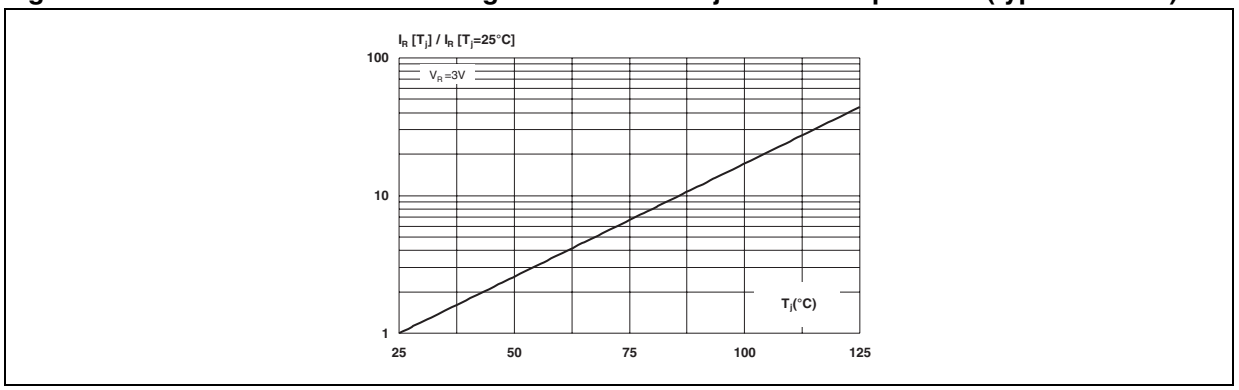


Figure 8. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

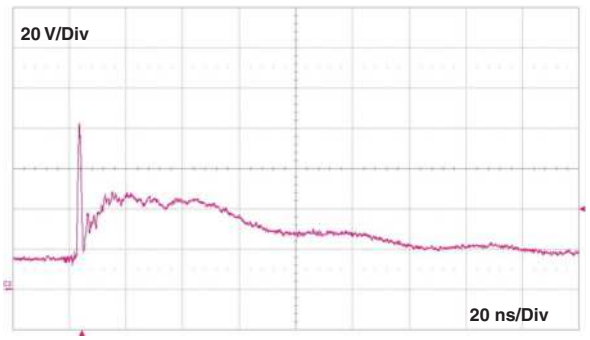


Figure 9. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

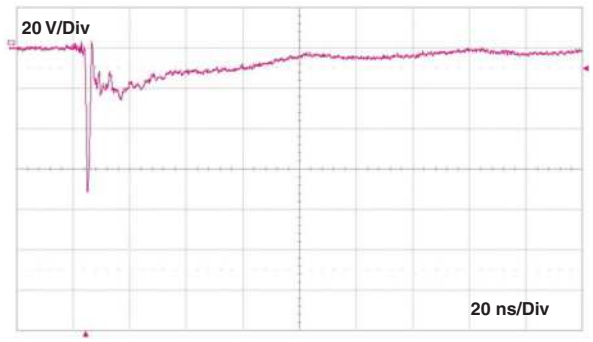


Figure 10. ESD response to IEC 61000-4-2 (+15 kV air discharge)

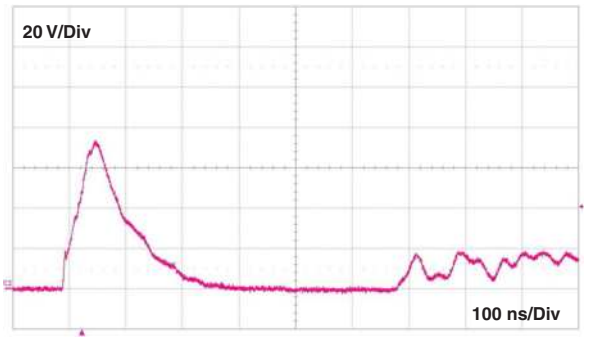


Figure 11. ESD response to IEC 61000-4-2 (-15 kV air discharge)

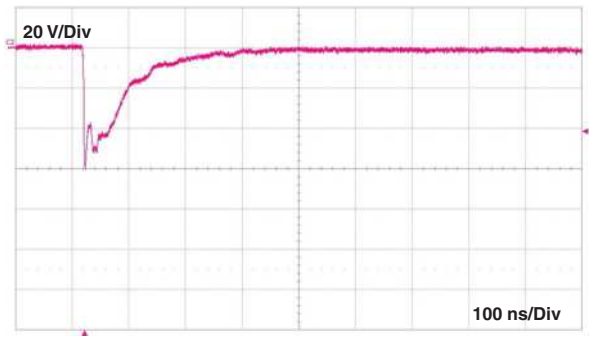
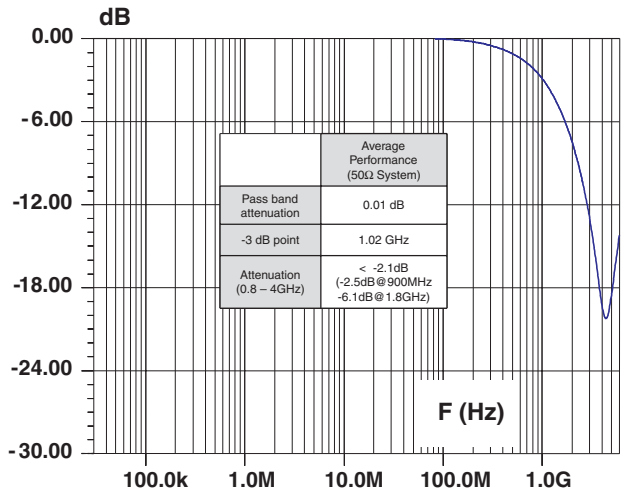
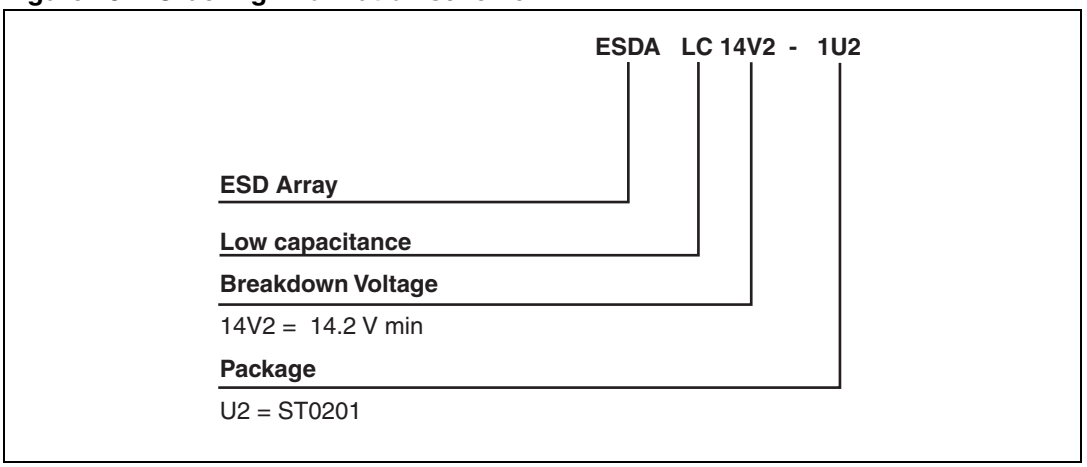


Figure 12. S21 attenuation measurement results



2 Ordering information scheme

Figure 13. Ordering information scheme

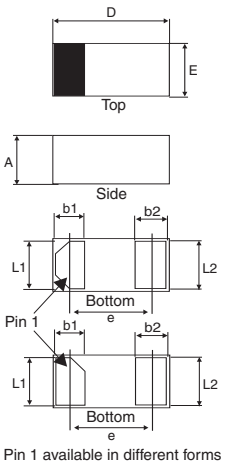


3 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

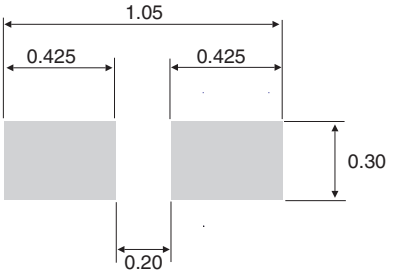
Table 3. ST0201 dimensions



Pin 1 available in different forms

Ref	Dimensions					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.23	0.28	0.33	0.009	0.011	0.013
b1	0.13	0.18	0.23	0.005	0.007	0.009
b2	0.14	0.19	0.24	0.006	0.007	0.009
D	0.55	0.60	0.65	0.022	0.024	0.026
E	0.25	0.30	0.35	0.010	0.012	0.014
e	-	0.35	-	-	0.014	-
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012

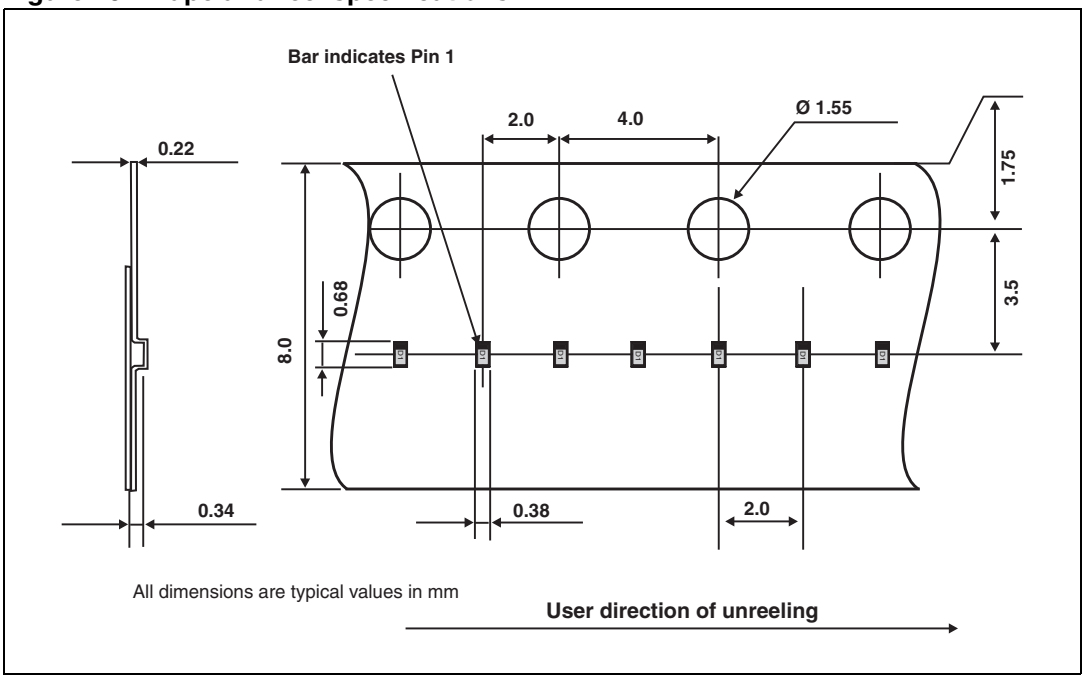
Figure 14. Footprint (dimensions in mm) **Figure 15. Marking**





Note: Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

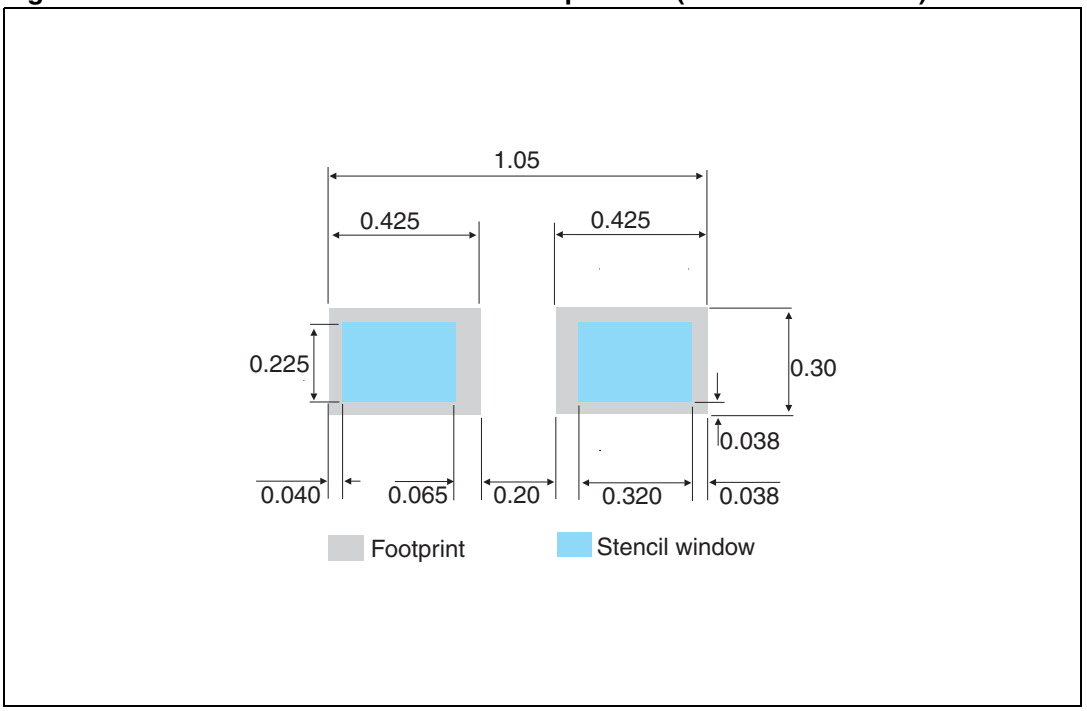
Figure 16. Tape and reel specifications



4 Recommendation on PCB assembly

4.1 Stencil opening design

Figure 17. Recommended stencil windows position (dimensions in mm)



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

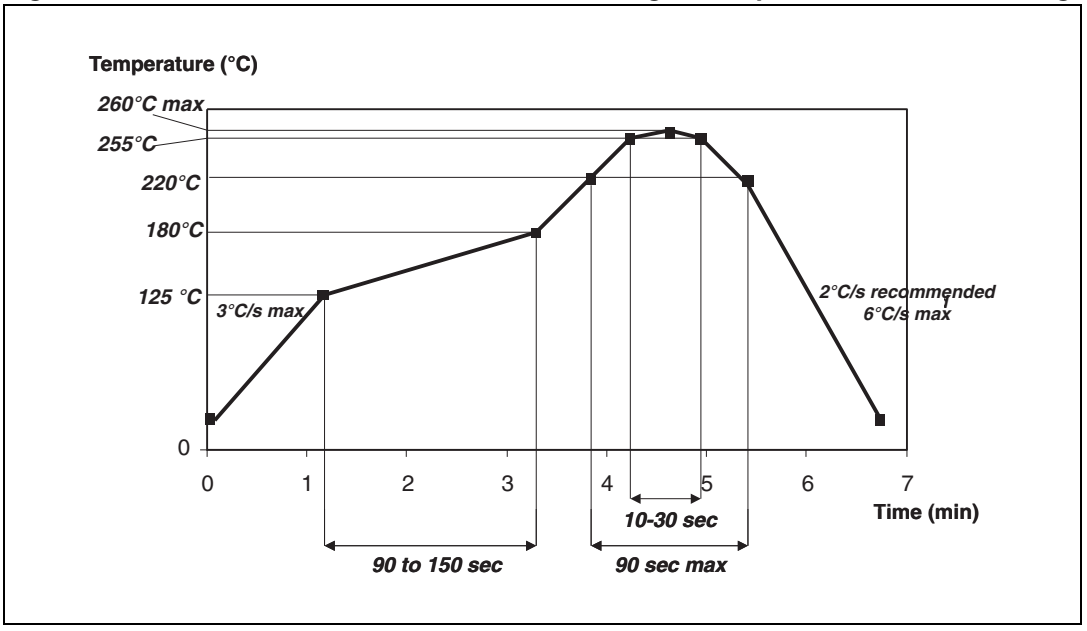
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 18. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Weight	Base qty	Delivery mode
ESDALC14V2-1U2	L2(1)	0.124 mg	15000	Tape and reel

1. The marking can be rotated by multiples of 90° to differentiate assembly location

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
07-Oct-2008	1	Initial release.
25-Jan-2010	2	Modified pin 1 form in package illustration *on page 1*, and package dimension illustration in *Table 3*. Updated base qty *Table 4.*
23-Sep-2011	3	Addional pin 1 form included in package illustration *on page 1*, and package dimension illustration in *Table 3*.

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