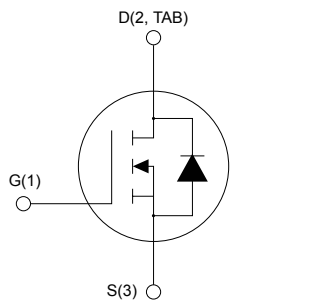
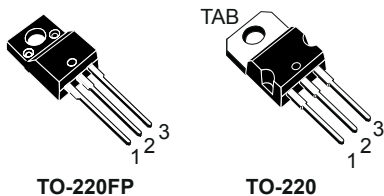


N-channel 650 V, 230 mΩ typ., 12 A MDmesh M5 Power MOSFETs in a TO-220FP and TO-220 packages



AM01475v1_noZen



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF16N65M5	650 V	279 mΩ	12 A
STP16N65M5			

- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Extremely low $R_{DS(on)}$
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Product status links

[STF16N65M5](#)

[STP16N65M5](#)

Product summary

Order code	STF16N65M5
Marking	16N65M5
Package	TO-220FP
Packing	Tube
Order code	STP16N65M5
Marking	16N65M5
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	TO-220	
V _{DS}	Drain-source voltage	650		V
V _{GS}	Gate-source voltage	±25		V
I _D	Drain current (continuous) at T _C = 25 °C	12		A
	Drain current (continuous) at T _C = 100 °C	7.3		
I _{DM} ⁽¹⁾	Drain current (pulsed)	48		A
P _{TOT}	Total power dissipation at T _C = 25 °C	90	25	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2.5	-	kV
T _{stg}	Storage temperature range	-55 to 150		°C
T _J	Maximum operating junction temperature	150		°C

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 12\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220FP	TO-220	
R_{thJC}	Thermal resistance, junction-to-case	5	1.38	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	62.5		$^{\circ}\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	200	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$	-	-	100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$	-	-	± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 6\text{ A}$	-	230	279	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1250	-	pF
C_{oss}	Output capacitance		-	30	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0\text{ V}$	-	100	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	30	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	2	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 6\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 17. Test circuit for gate charge behavior)	-	31	-	nC
Q_{gs}	Gate-source charge		-	8	-	nC
Q_{gd}	Gate-drain charge		-	12	-	nC

1. $C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.

2. $C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 8\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	25	-	ns
$t_{r(v)}$	Voltage rise time		-	7	-	ns
$t_{f(i)}$	Current fall time	(see the Figure 18. Test circuit for inductive load switching and diode recovery times and Figure 21. Switching time waveform)	-	6	-	ns
$t_{c(off)}$	Crossing time		-	8	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 12\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$	-	300	-	ns
Q_{rr}	Reverse recovery charge		-	3.5	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 18. Test circuit for inductive load switching and diode recovery times)	-	23	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	350	-	ns
Q_{rr}	Reverse recovery charge		-	4	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 18. Test circuit for inductive load switching and diode recovery times)	-	24	-	A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220FP

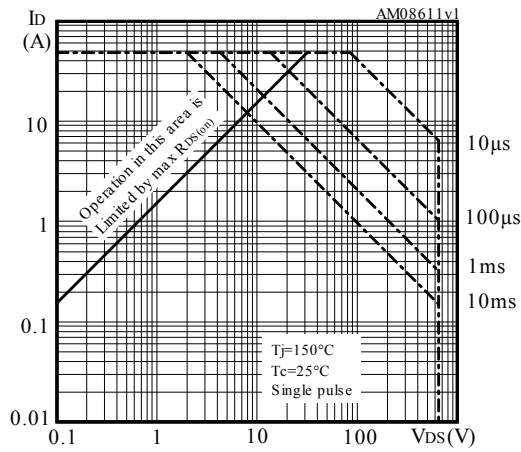


Figure 2. Normalized transient thermal impedance for TO-220FP

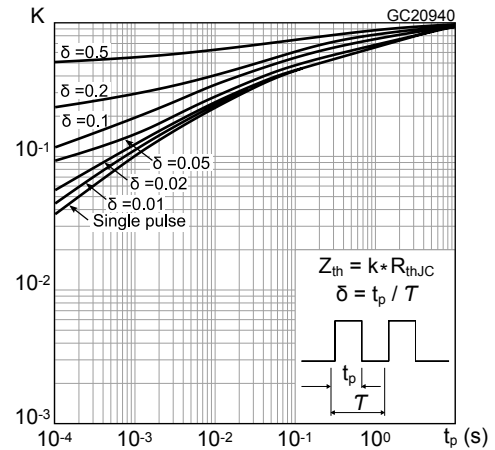


Figure 3. Safe operating area for TO-220

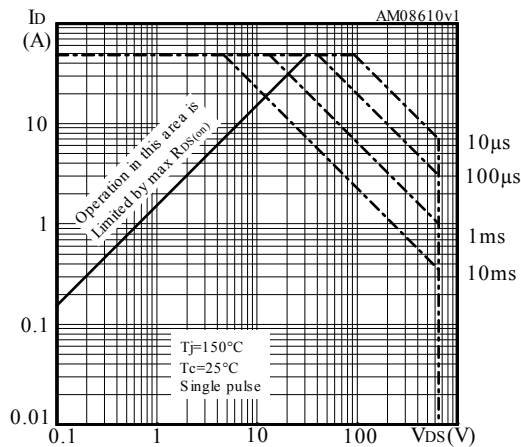


Figure 4. Normalized transient thermal impedance for TO-220

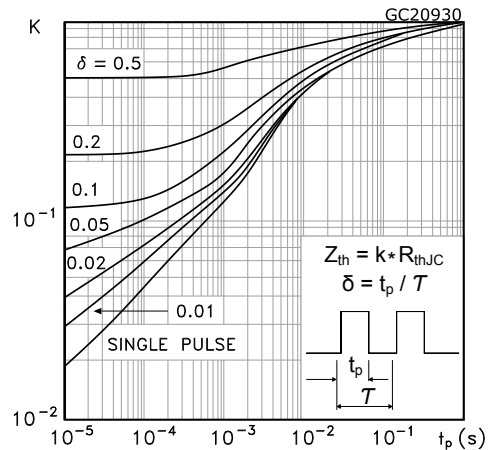


Figure 5. Typical output characteristics

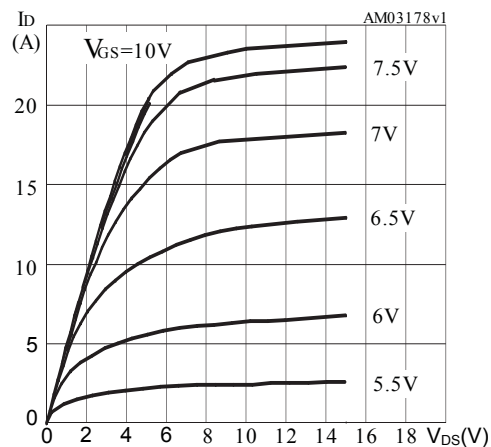


Figure 6. Typical transfer characteristics

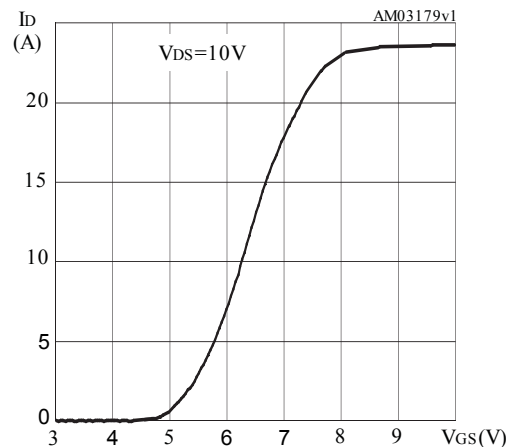


Figure 7. Typical gate charge characteristics

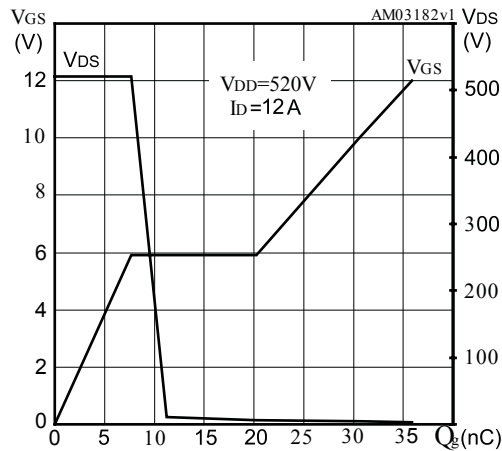


Figure 8. Typical drain-source on-resistance

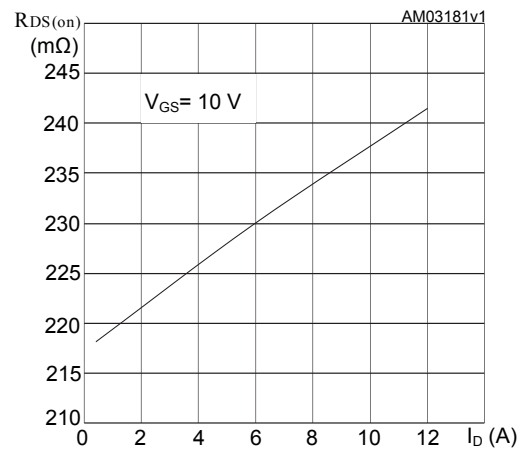


Figure 9. Typical capacitance characteristics

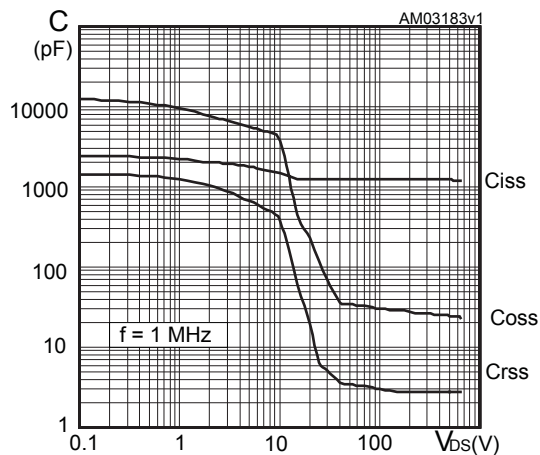


Figure 10. Typical output capacitance stored energy

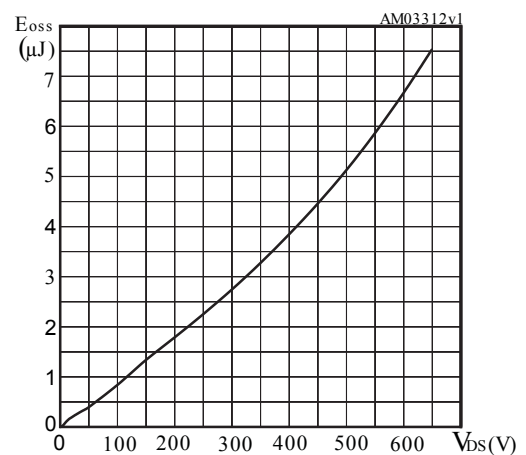


Figure 11. Normalized gate threshold vs temperature

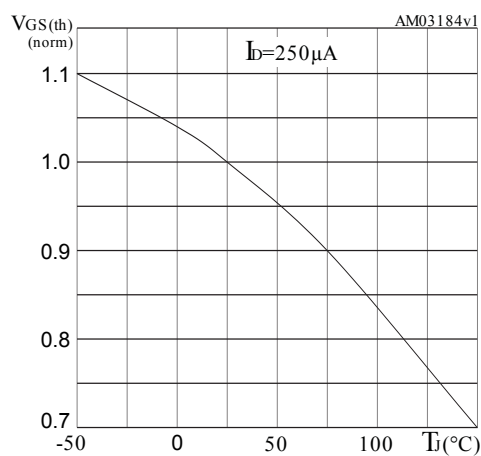


Figure 12. Normalized on-resistance vs temperature

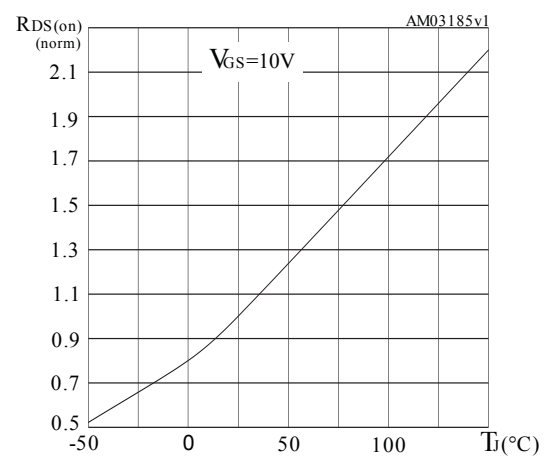


Figure 13. Typical reverse diode forward characteristics

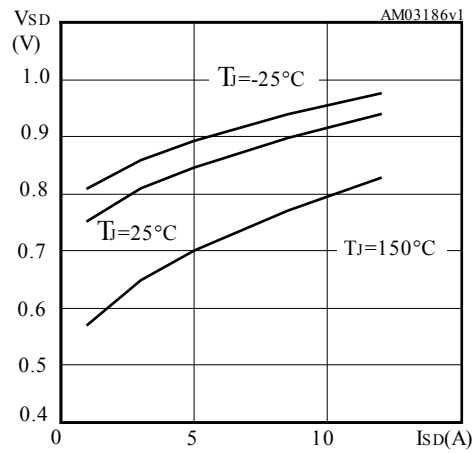


Figure 14. Normalized breakdown voltage vs temperature

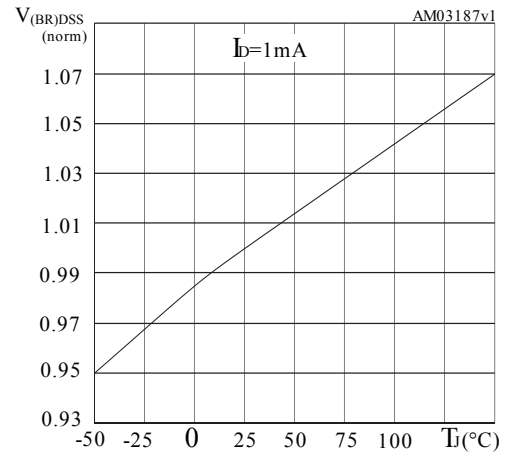
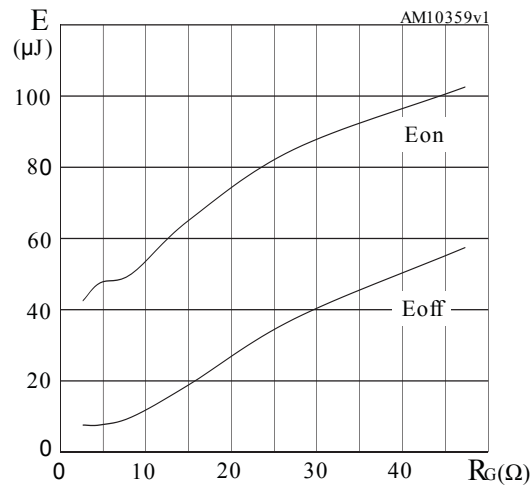
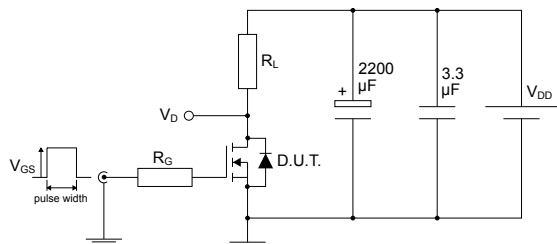


Figure 15. Typical switching energy vs gate resistance

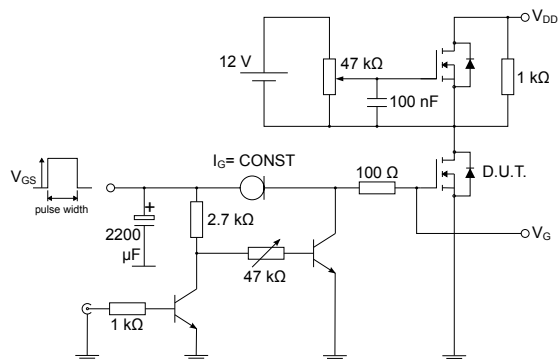


Note: E_{on} including reverse recovery of a SiC diode.

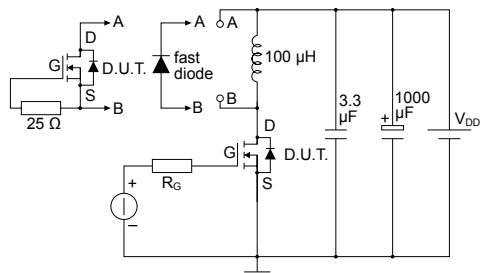
3 Test circuits

Figure 16. Test circuit for resistive load switching times


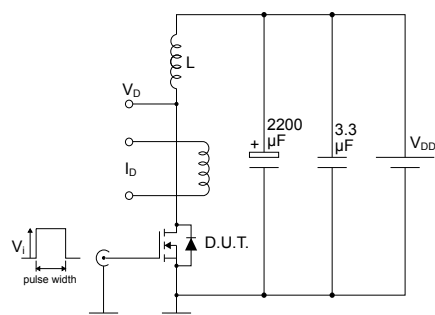
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Figure 17. Test circuit for gate charge behavior


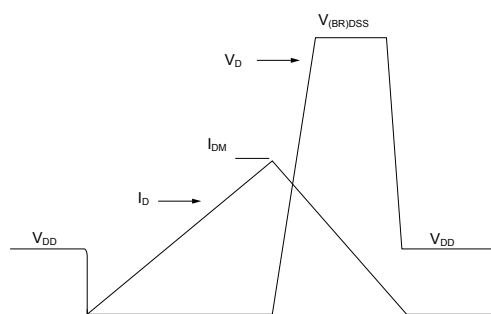
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Figure 18. Test circuit for inductive load switching and diode recovery times


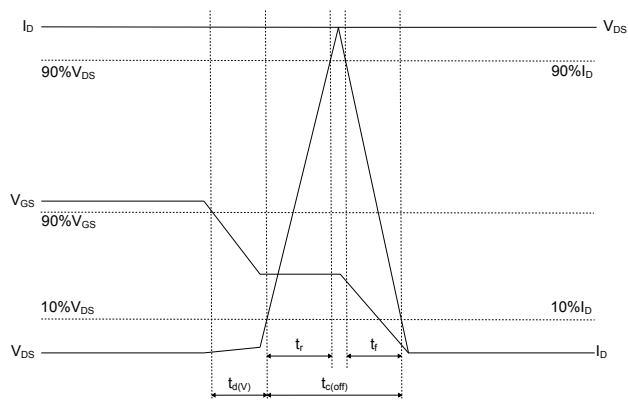
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Figure 19. Unclamped inductive load test circuit


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Figure 20. Unclamped inductive waveform


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Figure 21. Switching time waveform


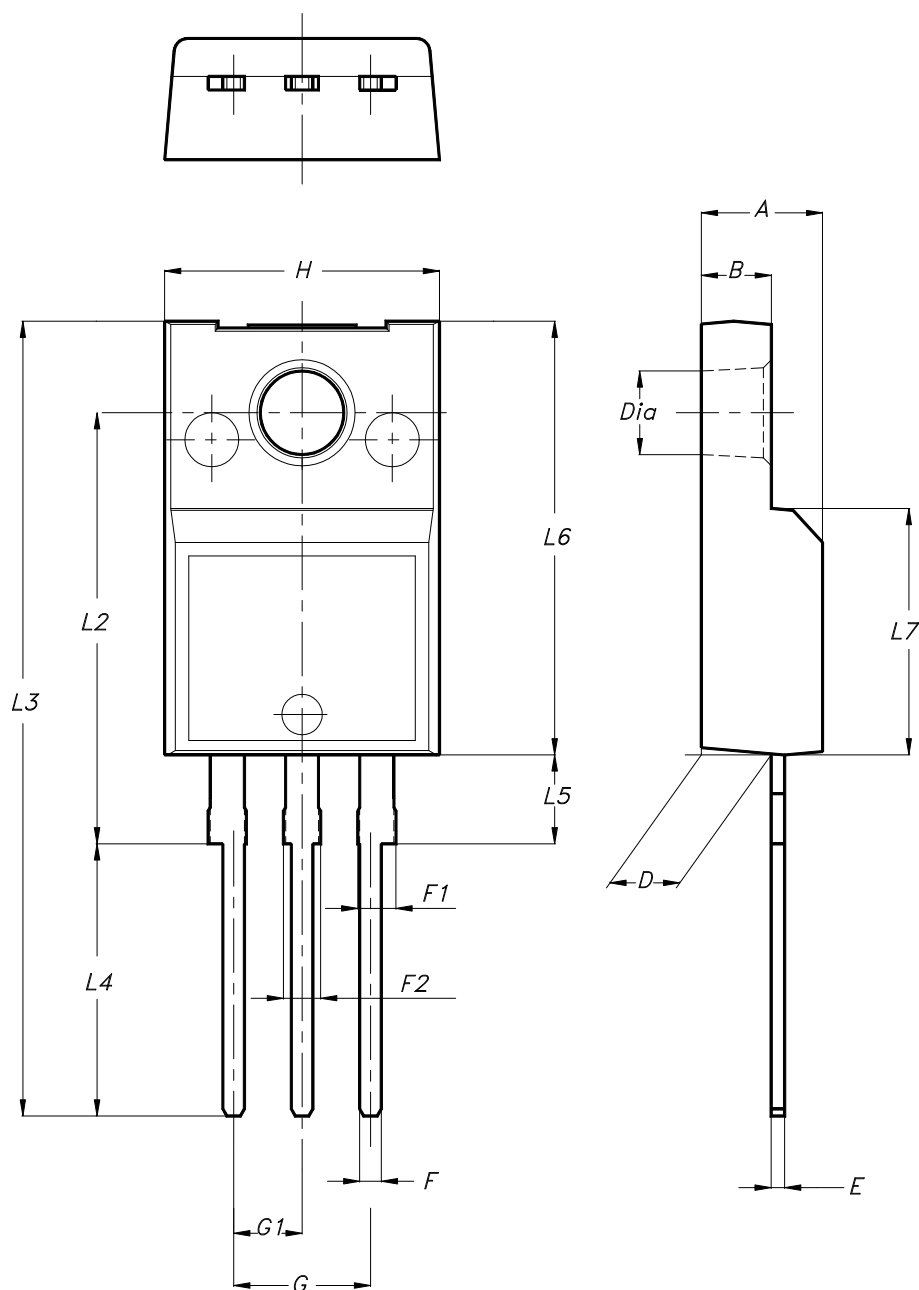
AM05540v2

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 22. TO-220FP type B package outline



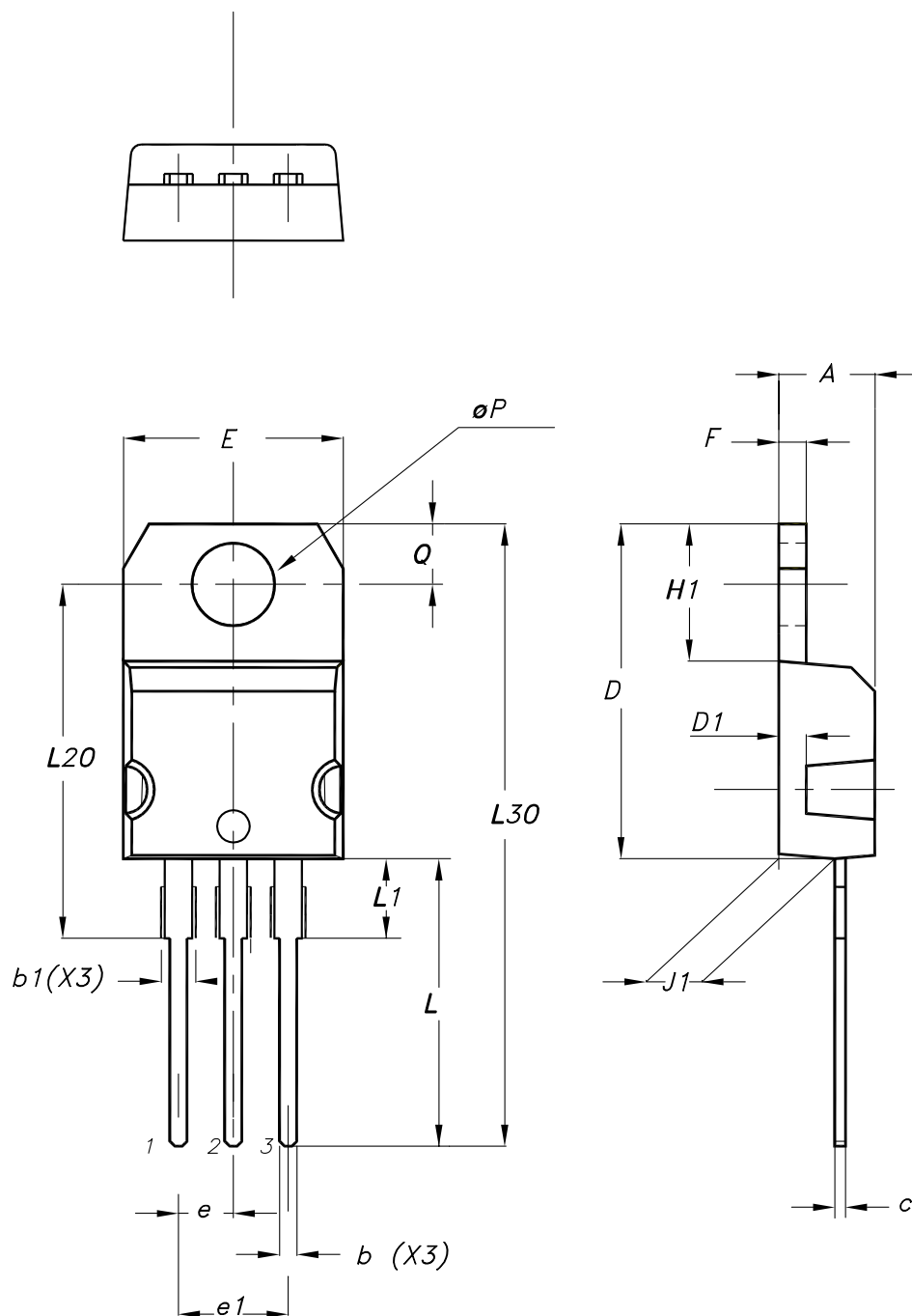
7012510_B_rev.14

Table 8. TO-220FP type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.2 TO-220 type A package information

Figure 23. TO-220 type A package outline



0015988_typeA_Rev_24

Table 9. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 10. Document revision history

Date	Revision	Changes
12-Feb-2009	1	First release.
21-Oct-2010	2	Document status promoted from preliminary data to datasheet. Added new package, mechanical data: I ² PAK. Removed DPAK, D ² PAK packages and mechanical data.
10-Feb-2011	3	Modified R _{DS(on)} value (see <i>Table 4</i> and <i>Figure 11</i>).
13-Oct-2011	4	Modified <i>Section 2.1: Electrical characteristics (curves)</i> : <i>Figure 8, Figure 9, Figure 10, Figure 11, Figure 15 and Figure 16</i> . Added <i>Figure 18</i> . Updated R _{DS(on)} value in <i>Table 4</i> . Updated values in <i>Table 6</i> . Minor text changes.
03-Feb-2026	5	Removed order code STI16N65M5, STU16N65M5 and STW16N65M5. Updated Section 4: Package information . Minor text changes.

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