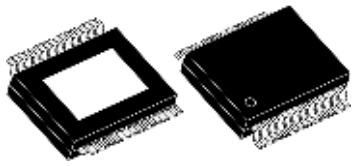
STA339BW

2.1-channel high-efficiency digital audio system

Datasheet - production data



PowerSSO-36 (slug down)

Features

- Wide voltage supply range
  - 5 V to 26 V (operating range)
  - 30 V (absolute maximum rating)
- 3 power output configurations
  - 2 channels of ternary PWM (stereo mode) (2 x 20 W into 8 Ω at 18 V)
  - 3 channels - left, right using binary and LFE using ternary PWM (2.1 mode) (2 x 9 W + 1 x 20 W into 2 x 4 Ω, 1 x 8 Ω at 18 V)
  - 2 channels of ternary PWM (2 x 20 W) + stereo lineout ternary
- 2.1 channels of 24-bit FFX® 100 dB SNR and dynamic range
- Selectable 32 to 192 kHz input sample rates
- I^2C control with selectable device address
- Digital gain/attenuation +48 dB to -80 dB with 0.5 dB/step resolution
- Soft volume update with programmable ratio
- Individual channel and master gain/attenuation
- Two independent DRC configurable as a dual-band anti-clipper (B^2DRC) or as independent limiters/compressors
- EQ-DRC for DRC based on filtered signals
- Dedicated LFE processing for bass boosting with 0.5 dB/step resolution
- Audio presets:
  - 15 preset crossover filters
  - 5 preset anti-clipping modes
  - Preset night-time listening mode
- Individual channel and master soft/hard mute
- Independent channel volume and DSP bypass
- Automatic zero-detect mute
- Automatic invalid input-detect mute
- 2-channel I^2S input data interface
- Input and output channel mapping
- Up to 8 user-programmable biquads per channel with 28-bit resolution
- 3 coefficient banks for EQ presets storing with fast recall via I^2C interface
- Bass/treble tones and de-emphasis control
- Selectable high-pass filter for DC blocking
- Advanced AM interference frequency switching and noise suppression modes
- Selectable high- or low-bandwidth noise-shaping topologies
- Variable max power correction for lower full-power THD
- Selectable clock input ratio
- 96 kHz internal processing sample rate, 24 to 28-bit precision
- Thermal overload and short-circuit protection embedded
- Video apps: 576 * f_S input mode supported
- Fully compatible with STA339BWS.

Table 1. Device summary

Order code	Package	Packaging
STA339BWTR	PowerSSO-36 slug down	Tape and reel

This is information on a product in full production. www.st.com

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1 Description

The STA339BW is an integrated solution of digital audio processing, digital amplifier control, and FFX-power output stage, thereby creating a high-power single-chip FFX® solution comprising high-quality, high-efficiency, all digital amplification.

STA339BW is based on FFX (fully flexible amplification) processor, an STMicroelectronics proprietary technology. FFX is the evolution and the enlargement of the ST ternary technology: the new processor can be configured to work in ternary, binary, binary differential and phase shift PWM modulation schemes.

STA339BW contains the ternary, binary and binary differential implementations, a subset of the full capability of the FFX processor.

The STA339BW is part of the Sound Terminal® family that provides full digital audio streaming to the speaker, offering cost effectiveness, low power dissipation and sound enrichment.

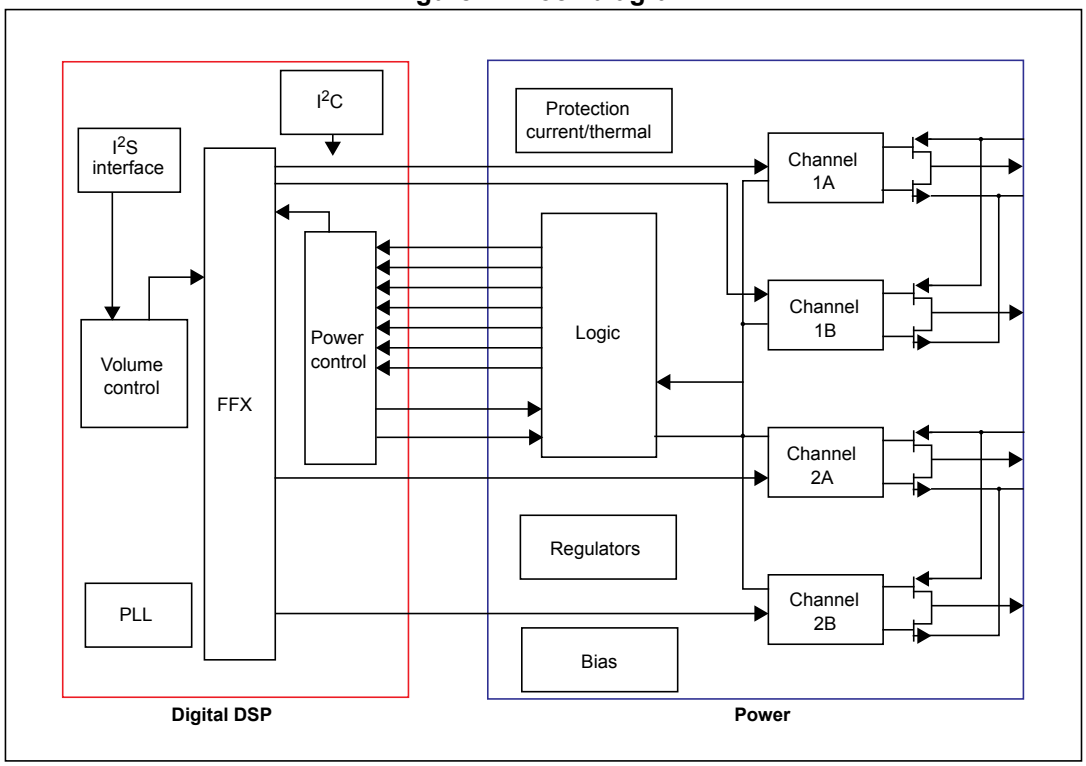
The STA339BW power section consists of four independent half bridges. These can be configured via digital control to operate in different modes. 2.1 channels can be provided by two half bridges and a single full bridge, providing up to 2 x 9 W + 1 x 20 W of power output. Two channels can be provided by two full bridges, providing up to 2 x 20 W of power. The IC can also be configured as 2.1 channels with 2 x 20 W provided by the device and external power for FFX power drive.

Also provided in the STA339BW are a full assortment of digital processing features. This includes up to 8 programmable 28-bit biquads (EQ) per channel and bass/treble tone control. Available presets enable a time-to-market advantage by substantially reducing the amount of software development needed for certain functions. This includes audio preset volume loudness, preset volume curves and preset EQ settings. There are also new advanced AM radio interference reduction modes. Dual-band DRC dynamically equalizes the system to provide speaker linear frequency response regardless of the output power level. This feature independently processes the two bands, controlling dynamically the output power level in each band and so providing better sound quality.

The serial audio data input interface accepts all possible formats, including the popular I^2S format. Three channels of FFX processing are provided. This high-quality conversion from PCM audio to FFX PWM switching waveform provides over 100 dB SNR and dynamic range.

1.1 Block diagram

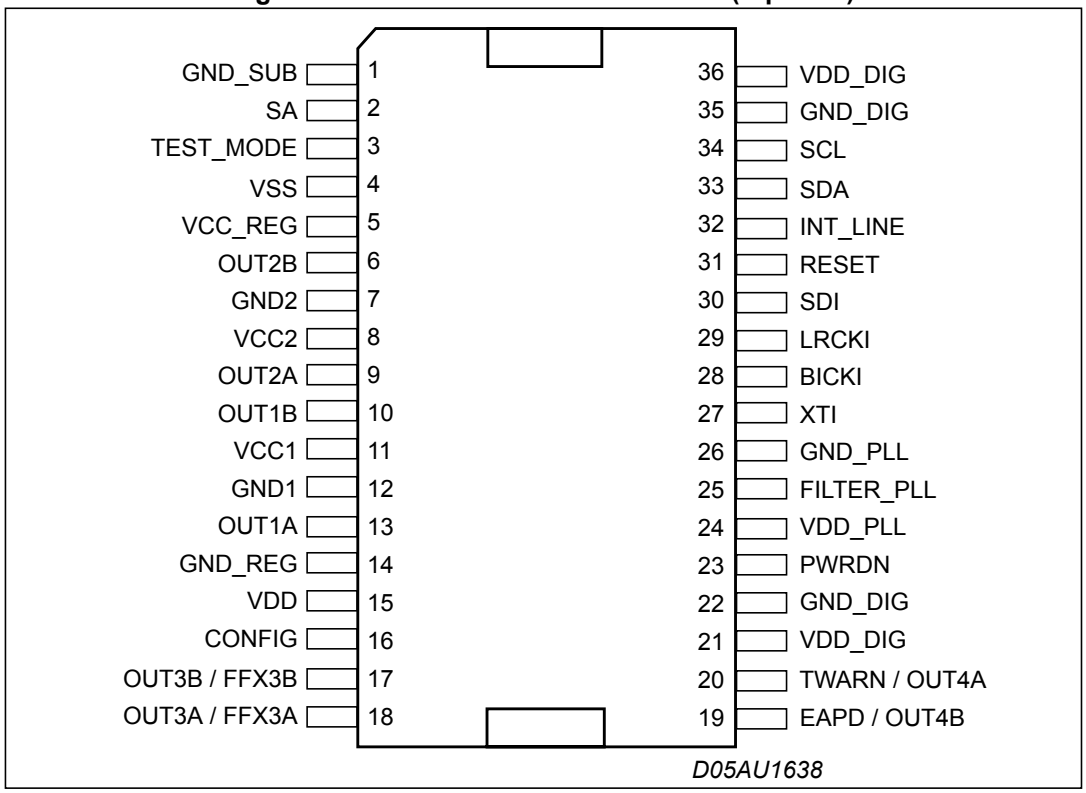
Figure 1. Block diagram



2 Pin connections

2.1 Connection diagram

Figure 2. Pin connection PowerSSO-36 (top view)



2.2 Pin description

Table 2. Pin description

Pin	Type	Name	Description
1	GND	GND_SUB	Substrate ground
2	I	SA	I^2C select address (pull-down)
3	I	TEST_MODE	This pin must be connected to ground (pull-down)
4	I/O	VSS	Internal reference at V_{CC} - 3.3 V
5	I/O	VCC_REG	Internal V_{CC} reference
6	O	OUT2B	Output half bridge 2B
7	GND	GND2	Power negative supply
8	Power	VCC2	Power positive supply
9	O	OUT2A	Output half bridge 2A
10	O	OUT1B	Output half bridge 1B

Table 2. Pin description (continued)

Pin	Type	Name	Description
11	Power	VCC1	Power positive supply
12	GND	GND1	Power negative supply
13	O	OUT1A	Output half bridge 1A
14	GND	GND_REG	Internal ground reference
15	Power	VDD	Internal 3.3 V reference voltage
16	I	CONFIG	Paralleled mode command
17	O	OUT3B / FFX3B	PWM out Ch3B / external bridge driver
18	O	OUT3A / FFX3A	PWM out Ch3A / external bridge driver
19	O	EAPD / OUT4B	Power down for external bridge / PWM out Ch4B
20	I/O	TWARN / OUT4A	Thermal warning from external bridge (pull-up when input) / PWM out Ch4A
21	Power	VDD_DIG	Digital supply voltage
22	GND	GND_DIG	Digital ground
23	I	PWRDN	Power down (pull-up)
24	Power	VDD_PLL	Positive supply for PLL
25	I	FILTER_PLL	Connection to PLL filter
26	GND	GND_PLL	Negative supply for PLL
27	I	XTI	PLL input clock
28	I	BICKI	I^2S serial clock
29	I	LRCKI	I^2S left/right clock
30	I	SDI	I^2S serial data channels 1 and 2
31	I	RESET	Reset (pull-up)
32	O	INT_LINE	Fault interrupt
33	I/O	SDA	I^2C serial data
34	I	SCL	I^2C serial clock
35	GND	GND_DIG	Digital ground
36	Power	VDD_DIG	Digital supply voltage

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power supply voltage (VCCxA, VCCxB)	-0.3	-	30	V
VDD_DIG	Digital supply voltage	-0.3	-	4	V
VDD_PLL	PLL supply voltage	-0.3	-	4	V
T_{op}	Operating junction temperature	-20	-	150	°C
T_{stg}	Storage temperature	-40	-	150	°C

Warning: **Stresses beyond those listed in *Table 3* above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended operating conditions" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. In the real application, power supplies with nominal values rated within the recommended operating conditions, may experience some rising beyond the maximum operating conditions for a short time when no or very low current is sinked (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum ratings are not exceeded.**

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-case (thermal pad)	-	-	1.5	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient (1)	-	-	-	°C/W
$T_{th\text{-}sdj}$	Thermal shut-down junction temperature	-	150	-	°C
$T_{th\text{-}w}$	Thermal warning temperature	-	130	-	°C
$T_{th\text{-}sdh}$	Thermal shut-down hysteresis	-	20	-	°C

1. See *Section 9: Package thermal characteristics on page 74* for details.

3.3 Recommended operating conditions

Table 5. Recommended operating condition

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power supply voltage (VCCxA, VCCxB)	5	-	26	V
VDD_DIG	Digital supply voltage	2.7	3.3	3.6	V
VDD_PLL	PLL supply voltage	2.7	3.3	3.6	V
T_{amb}	Ambient temperature	-20	-	70	°C

3.4 Electrical specifications for the digital section

Table 6. Electrical specifications - digital section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Low-level input current without pull-up/down device	Vi = 0 V	-10	1	10	µA
I_{ih}	High-level input current without pull-up/down device	Vi = VDD_DIG = 3.6 V	-10	1	10	µA
V_{il}	Low-level input voltage	-	-	-	0.2 * VDD_DIG	V
V_{ih}	High-level input voltage	-	0.8 * VDD_DIG	-	-	V
V_{ol}	Low-level output voltage	Iol = 2 mA	-	-	0.4 * VDD_DIG	V
V_{oh}	High-level output voltage	Ioh = 2 mA	0.8 * VDD_DIG	-	-	V
I_{pu}	Pull-up/down current	-	25	66	125	µA
R_{pu}	Equivalent pull-up/down resistance	-	-	50	-	kΩ

3.5 Electrical specifications for the power section

The specifications given in this section are valid for the operating conditions: V_{CC} = 18 V, f = 1 kHz, f_{sw} = 384 kHz, T_{amb} = 25° C and R_L = 8 Ω, unless otherwise specified.

Table 7. Electrical specifications - power section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Po	Output power BTL	THD = 1%	-	16	-	W
		THD = 10%	-	20	-	
	Output power SE	THD = 1%	-	4	-	W
		THD = 10%	-	5	-	
R_{dsON}	Power Pchannel/Nchannel MOSFET (total bridge)	I_d = 1.5 A	-	180	250	mΩ
gP	Power Pchannel RdsON matching	I_d = 1.5 A	95	-	-	%
gN	Power Nchannel RdsON matching	I_d = 1.5 A	95	-	-	%
Idss	Power Pchannel/Nchannel leakage	V_{CC} = 20 V	-	-	10	µA
I_{LDT}	Low current dead time (static)	Resistive load(1)	-	8	15	ns
I_{HDT}	High current dead time (dynamic)	Iload = 1.5 A(1)	-	15	30	ns
t_r	Rise time	Resistive load(1)	-	10	18	ns
t_f	Fall time	Resistive load(1)	-	10	18	ns
V_{CC}	Supply voltage operating voltage	-	5	-	26	V
I_{vcc}	Supply current from V_{CC} in power down	PWRDN = 0	-	0.1	1	mA
	Supply current from V_{CC} in operation	PCM input signal = -60 dBfs, Switching frequency = 384 kHz, No LC filters	-	52	60	mA
I_{vdd}	Supply current FFX processing (reference only)	Internal clock = 49.152 MHz	-	55	70	mA
I_{lim}	Overcurrent limit	(2)	3.0	3.8(3)	-	A
I_{sc}	Short-circuit protection	Hi-Z output	3.8	4.8	-	A
UVL	Undervoltage protection	-	-	3.5	4.3	V
t_{min}	Output minimum pulse width	No load	20	30	60	ns
DR	Dynamic range	-	-	100	-	dB
SNR	Signal-to-noise ratio, ternary mode	A-weighted	-	100	-	dB
	Signal-to-noise ratio binary mode	-	-	90	-	dB
PSSR	Power supply rejection ratio	FFX stereo mode, <5 kHz V_{RIPPLE} = 1 V RMS Audio input = dither only	-	80	-	dB

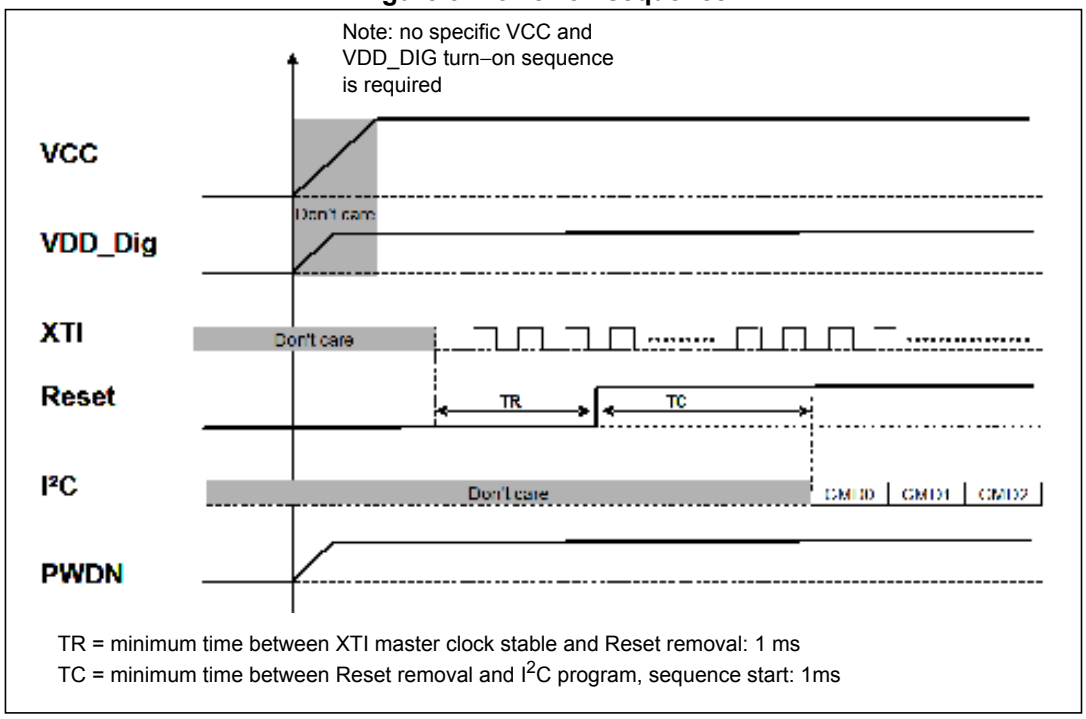
Table 7. Electrical specifications - power section (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD+N	Total harmonic distortion + noise	FFX stereo mode, Po = 1 W f = 1 kHz	-	0.2	-	%
X_{TALK}	Crosstalk	FFX stereo mode, <5 kHz One channel driven at 1 W Other channel measured	-	80	-	dB
η	Peak efficiency, FFX mode	Po = 2 x 20 W into 8 Ω	-	90	-	%
	Peak efficiency,binary modes	Po = 2 x 9 W into 4 Ω + 1 x 20 W into 8 Ω	-	87	-	

1. Refer to *Figure 5: Test circuit 1*.
2. Limit current if the register (OCRB par 6.1.3.3) overcurrent warning detect adjustment bypass is enabled. When disabled, refer to I_{sc}.
3. I_{lim} typical value is $0.8*I_{sc}$.

3.6 Power on/off sequence

Figure 3. Power-on sequence

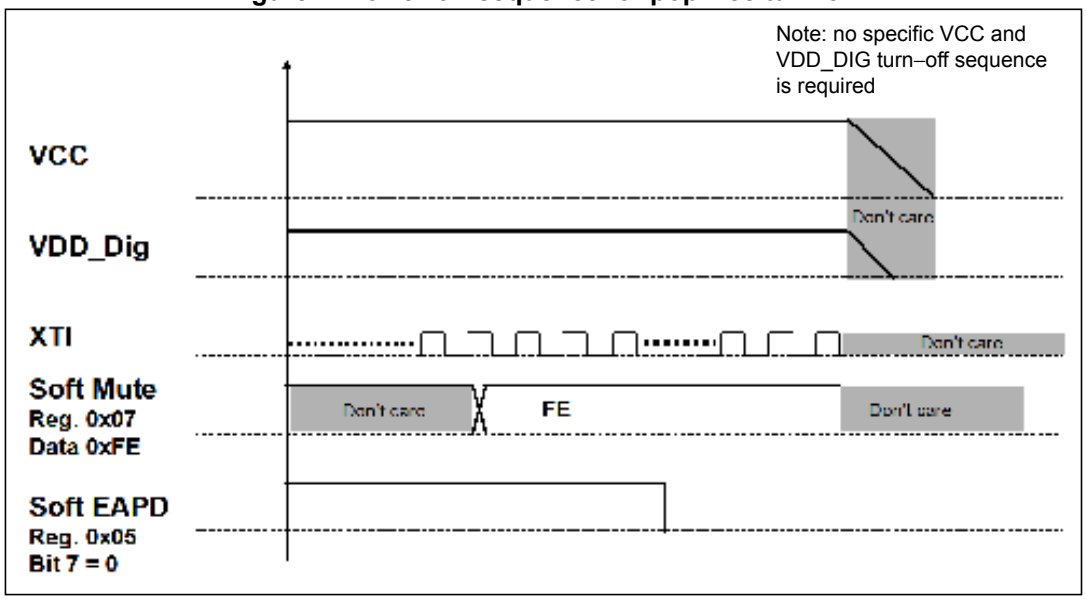


TR = minimum time between XTI master clock stable and Reset removal: 1 ms
TC = minimum time between Reset removal and I^2C program, sequence start: 1ms

Note: The definition of a stable clock is when $f_{max} - f_{min} < 1$ MHz.

Section 7.2.3 on page 31 gives information on setting up the I^2S interface.

Figure 4. Power-off sequence for pop-free turn-off



3.7 Testing

3.7.1 Functional pin definition

Table 8. Functional pin definition

Pin name	Number	Logic value	IC status
PWRDN	23	0	Low consumption
		1	Normal operation
TWARN	20	0	A temperature warning is indicated by the external power stage
		1	Normal operation
EAPD	19	0	Low consumption for power stage All internal regulators are switched off
		1	Normal operation

Figure 5. Test circuit 1

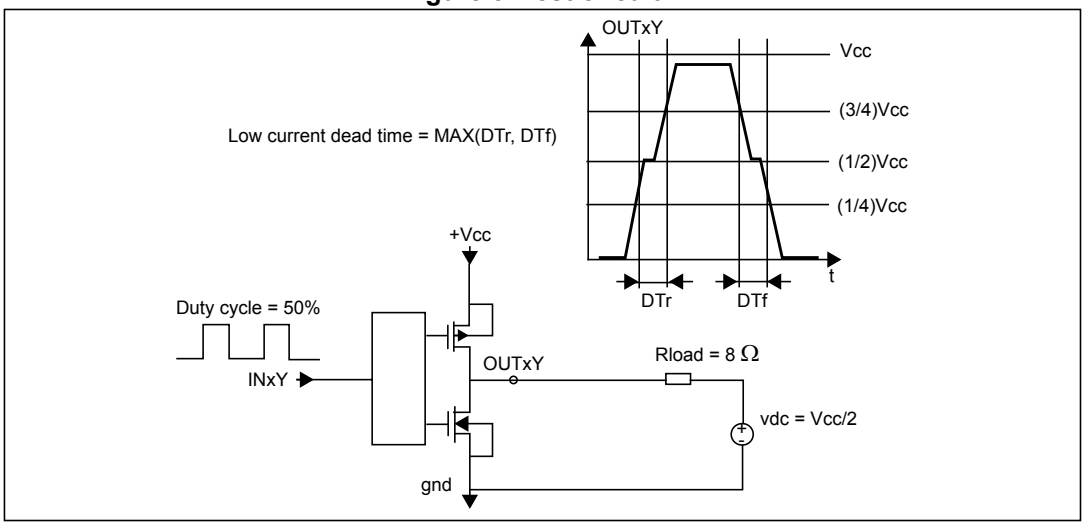
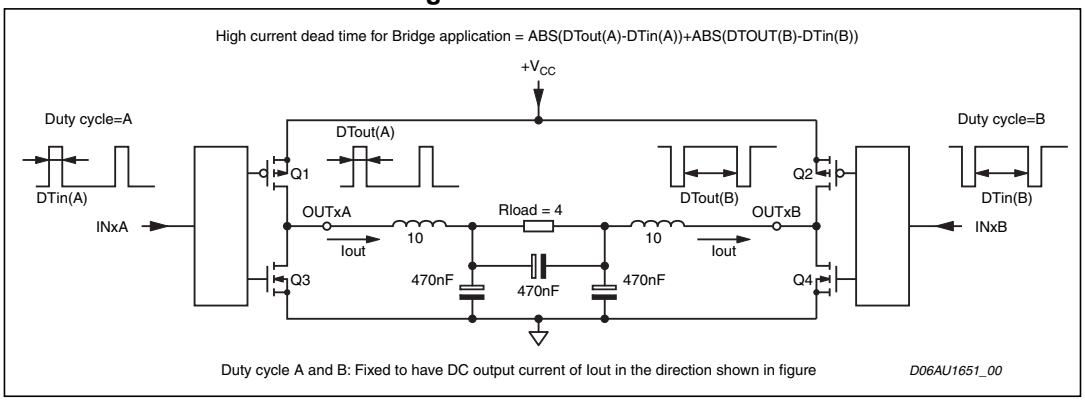


Figure 6. Test circuit 2



4 Serial audio interface

The STA339BW audio serial input interface was designed to interface with standard digital audio components and to accept a number of serial data formats. The STA339BW always acts as the slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using three inputs: left/right clock LRCKI, serial clock BICKI, and serial data SDI12.

The SAI bit and the SAIFB bit are used to specify the serial data format. The default serial data format is I^2S, MSB-first.

4.0.1 Timings

In the STA339BW the BICKI and LRCKI pins are configured as inputs and they must be supplied by the external peripheral.

Figure 7. Timing diagram for SAI interface

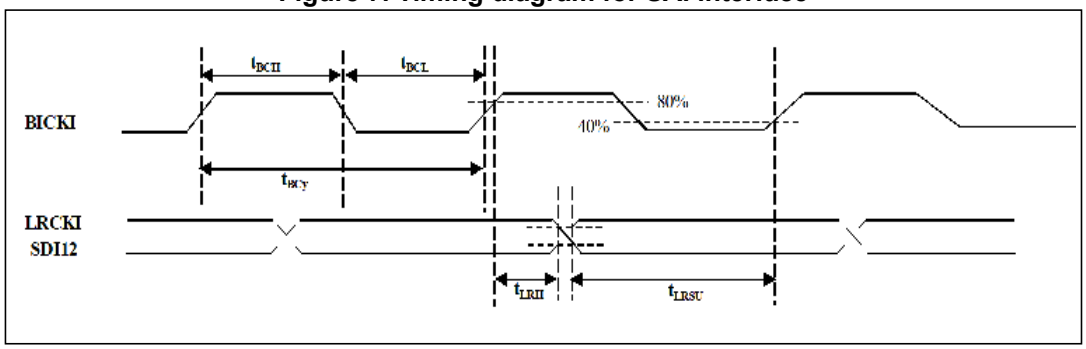


Table 9. Timing parameters for slave mode

Symbol	Parameter	Min	Typ	Max	Unit
t_{BCy}	BICK cycle time	80	-	-	ns
t_{BCH}	BICK pulse width high	40	-	-	ns
t_{BCL}	BICK pulse width low	40	-	-	ns
t_{LRSU}	LRCKI setup time to BICKI strobing edge	40	-	-	ns
t_{LRH}	LRCKI hold time to BICKI strobing edge	40	-	-	ns
t_{LRJT}	LRCKI Jitter Tolerance			40	ns

4.0.2 Delay serial clock enable

To tolerate anomalies in some I^2S master devices, a PLL clock cycle delay can be added to the BICKI signal before the SAI interface.

4.0.3 Channel input mapping

Each channel received via I^2S can be mapped to any internal processing channel via the channel input mapping registers. This allows for flexibility in processing. The default settings of these registers map each I^2S input channel to its corresponding processing channel.

5 Processing data paths

The whole processing chain is composed of two consecutive sections. In the first one dual-channel processing is implemented, as described below. Then each channel is fed into the post-mixing block where there is a choice of processing, either the dual-band DRC is disabled or it is enabled. When B^{2}DRC is disabled a third channel, typically used in 2.1 output configuration and with cross-over filters enabled, is used. When B^{2}DRC is enabled the 2.0 output configuration with cross-over filters for defining the cutoff frequency of the two bands is used.

The first section, *Figure 8*, begins with a 2x oversampling FIR filter allowing a 2 * fs audio processing. Then a selectable high-pass filter removes the DC level (enabled if HFB = 0).

The channel 1 and 2 processing chain can include up to 8 filters, depending on the selected configuration (bits BQL, BQ5, BQ6, BQ7 and XO[3:0]).

By default, four independent filters per channel are enabled, plus the preconfigured de-emphasis, bass and treble controls (BQL = 0, BQ5 = 0, BQ6 = 0, BQ7 = 0).

If the coefficient sets are linked (BQL = 1) then it is possible to use the de-emphasis, bass and treble filter in a user defined configuration (provided the relevant BQx bits are set to 1). In other words both channels use the same processing coefficients and can have up to 7 filters each. Note that if BQL = 0 the BQx bits are ignored and the 5th, 6th and 7th filters are configured as de-emphasis, bass and treble controls, respectively.

Moreover the common 8th filter, from the subsequent processing section, can be available on both channels (provided the pre-defined cross-over frequencies are not used, XO[3:0] = 0, and the dual-band DRC is not used).

In the second section, mixing and crossover filters are available. If B^{2}DRC is not enabled (lower schematic in *Figure 9*) they are fully user-programmable and allow a third channel (2.1 outputs) to be generated. Alternatively, in B^{2}DRC mode (upper schematic in *Figure 9*), those blocks will be used to split the sub-band and define the cutoff frequencies of the two bands. A prescaler and a final post scaler allow full control over the signal dynamics before and after, respectively, the filtering stages. A mixer function is also available.

Figure 8. Left and right processing part 1

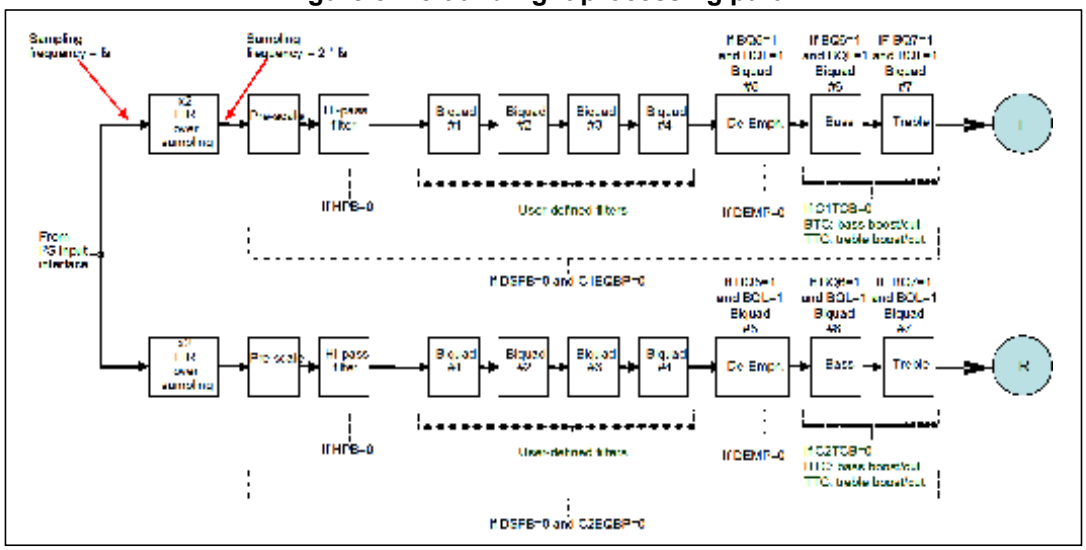
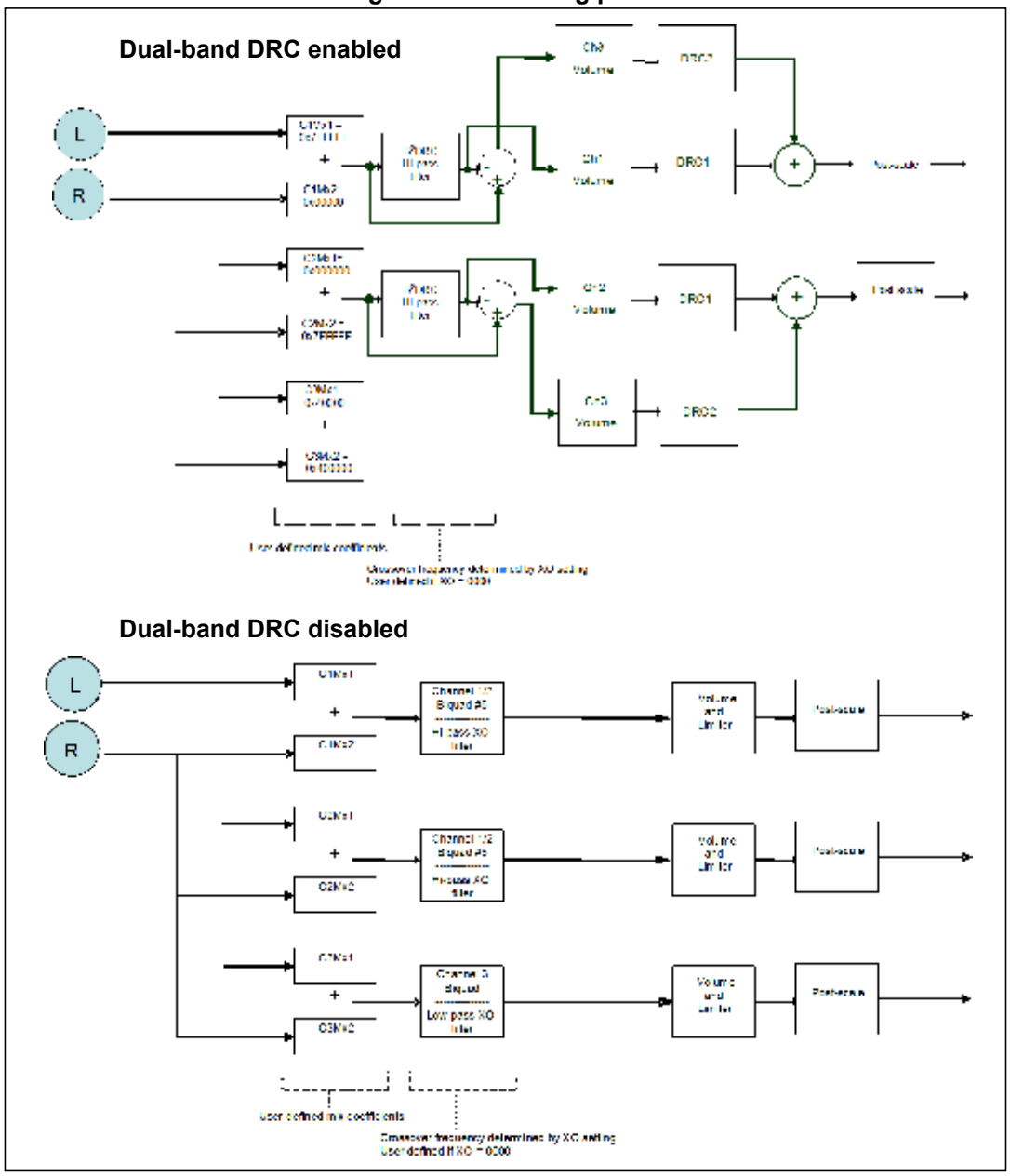


Figure 9. Processing part 2



6 I²C bus specification

The STA339BW supports the I²C protocol via the input ports SCL and SDA_IN (master to slave) and the output port SDA_OUT (slave to master). This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA339BW is always a slave device in all of its communications. It can operate at up to 400 kb/s (fast-mode bit rate). The STA339BW I²C interface is a slave only interface.

6.1 Communication protocol

6.1.1 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a START or STOP condition.

6.1.2 Start condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

6.1.3 Stop condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between STA339BW and the bus master.

6.1.4 Data input

During the data input the STA339BW samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

6.2 Device addressing

To start communication between the master and the STA339BW, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8-bits (MSB first) corresponding to the device select address and read or write mode.

The seven most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA339BW the I²C interface has two device addresses depending on the SA port configuration, 0x38 when SA = 0, and 0x3A when SA = 1.

The eighth bit (LSB) identifies read or write operation RW, this bit is set to 1 in read mode and to 0 for write mode. After a START condition the STA339BW identifies on the bus the device address and if a match is found, acknowledges the identification on the SDA bus during the 9th bit time. The byte following the device identification byte is the internal space address.

6.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA339BW acknowledges this and the writes for the byte of internal address. After receiving the internal byte address the STA339BW again responds with an acknowledgement.

6.3.1 Byte write

In the byte write mode the master sends one data byte, this is acknowledged by the STA339BW. The master then terminates the transfer by generating a STOP condition.

6.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

6.4 Read operation

6.4.1 Current address byte read

Following the START condition the master sends a device select code with the RW bit set to 1. The STA339BW acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

6.4.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA339BW. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

6.4.3 Random address byte read

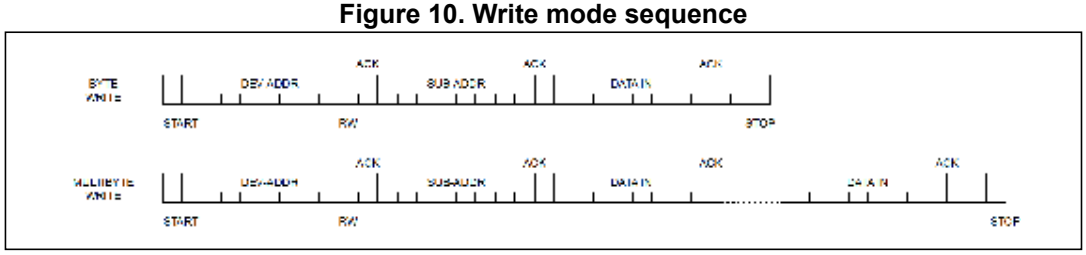
Following the START condition the master sends a device select code with the RW bit set to 0. The STA339BW acknowledges this and then the master writes the internal address byte. After receiving, the internal byte address the STA339BW again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The STA339BW acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

6.4.4 Random address multi-byte read

The multi-byte read modes could start from any internal address. Sequential data bytes are read from sequential addresses within the STA339BW. The master acknowledges each data byte read and then generates a STOP condition terminating the transfer.

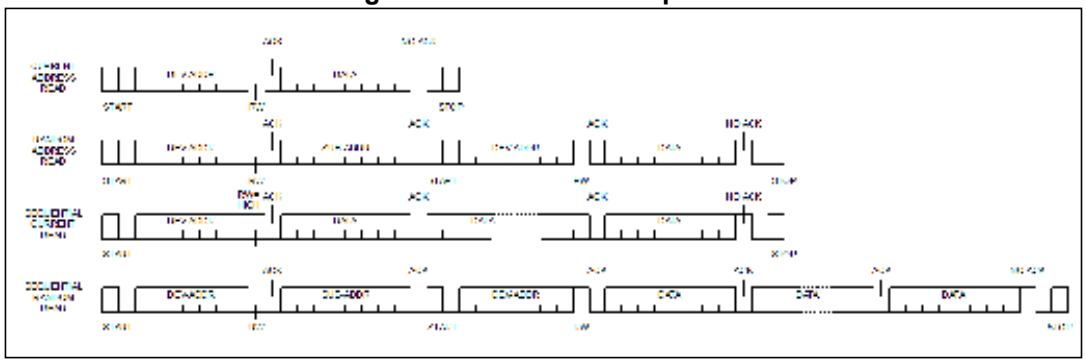
6.4.5 Write mode sequence

Figure 10. Write mode sequence



6.4.6 Read mode sequence

Figure 11. Read mode sequence



7 Register description

Table 10. Register summary

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	CONFA	FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0x01	CONFB	C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
0x02	CONFC	OCRB	Reserved	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
0x03	CONFD	SME	ZDE	DRC	BQL	PSL	DSPB	DEMP	HPB
0x04	CONFE	SVE	ZCE	DCCV	PWMS	AME	NSBW	MPC	MPCV
0x05	CONFF	EAPD	PWDN	ECLE	LDTE	BCLE	IDE	OCFG1	OCFG0
0x06	MUTE/LOC	LOC1	LOC0	Reserved		C3M	C2M	C1M	MMUTE
0x07	MVOL	MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
0x08	C1VOL	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0x09	C2VOL	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0x0A	C3VOL	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0x0B	AUTO1	Reserved		AMGC1	AMGC0	Reserved			
0x0C	AUTO2	XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0x0D	AUTO3	Reserved							
0x0E	C1CFG	C1OM1	C1OM0	C1LS1	C1LS0	C1BO	C1VBP	C1EQBP	C1TCB
0x0F	C2CFG	C2OM1	C2OM0	C2LS1	C2LS0	C2BO	C2VBP	C2EQBP	C2TCB
0x10	C3CFG	C3OM1	C3OM0	C3LS1	C3LS0	C3BO	C3VBP	Reserved	
0x11	TONE	TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0x12	L1AR	L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0x13	L1ATRT	L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0x14	L2AR	L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0x15	L2ATRT	L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0x16	CFADDR	Reserved		CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0x17	B1CF1	C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0x18	B1CF2	C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0x19	B1CF3	C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0x1A	B2CF1	C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0x1B	B2CF2	C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0x1C	B2CF3	C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0x1D	A1CF1	C3B23	C3B22	C3B21	C3B20	C3B19	C3B18	C3B17	C3B16
0x1E	A1CF2	C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0x1F	A1CF3	C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0

Table 10. Register summary (continued)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x20	A2CF1	C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0x21	A2CF2	C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0x22	A2CF3	C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0x23	B0CF1	C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0x24	B0CF2	C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0x25	B0CF3	C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0x26	CFUD	Reserved				RA	R1	WA	W1
0x27	MPCC1	MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0x28	MPCC2	MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
0x29	DCC1	DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
0x2A	DCC2	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0x2B	FDRC1	FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0x2C	FDRC2	FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0x2D	STATUS	PLLUL	FAULT	UVFAULT	OVFAULT	OCFAULT	OCWARN	TFAULT	TWARN
0x2E	Reserved	Reserved		RO1BACT	R5BACT	R4BACT	R3BACT	R2BACT	R1BACT
0x2F	Reserved	Reserved		R01BEND	R5BEND	R4BEND	R3BEND	R2BEND	R1BEND
0x30	Reserved	Reserved			R5BBAD	R4BBAD	R3BBAD	R2BBAD	R1BBAD
0x31	EQCFG	XOB	Reserved		AMGC3	AMGC2	Reserved	SEL1	SEL0
0x32	EATH1	EATHEN1	EATH1[6]	EATH1[5]	EATH1[4]	EATH1[3]	EATH1[2]	EATH1[1]	EATH1[0]
0x33	ERTH1	ERTHEN1	ERTH1[6]	ERTH1[5]	ERTH1[4]	ERTH1[3]	ERTH1[2]	ERTH1[1]	ERTH1[0]
0x34	EATH2	EATHEN2	EATH2[6]	EATH2[5]	EATH2[4]	EATH2[3]	EATH2[2]	EATH2[1]	EATH2[0]
0x35	ERTH2	ERTHEN2	ERTH2[6]	ERTH2[5]	ERTH2[4]	ERTH2[3]	ERTH2[2]	ERTH2[1]	ERTH2[0]
0x36	CONFX	MDRC[1]	MDRC[0]	PS48DB	XAR1	XAR2	BQ5	BQ6	BQ7
0x37	SVCA	Reserved		SVUPE	SVUP[4]	SVUP[3]	SVUP[2]	SVUP[1]	SVUP[0]
0x38	SVCB	Reserved		SVDWE	SVDW[4]	SVDW[3]	SVDW[2]	SVDW[1]	SVDW[0]
0x39	RMS0A	R_C0[23]	R_C0[22]	R_C0[21]	R_C0[20]	R_C0[19]	R_C0[18]	R_C0[17]	R_C0[16]
0x3A	RMS0B	R_C0[15]	R_C0[14]	R_C0[13]	R_C0[12]	R_C0[11]	R_C0[10]	R_C0[9]	R_C0[8]
0x3B	RMS0C	R_C0[7]	R_C0[6]	R_C0[5]	R_C0[4]	R_C0[3]	R_C0[2]	R_C0[1]	R_C0[0]
0x3C	RMS1A	R_C1[23]	R_C1[22]	R_C1[21]	R_C1[20]	R_C1[19]	R_C1[18]	R_C1[17]	R_C1[16]
0x3D	RMS1B	R_C1[15]	R_C1[14]	R_C1[13]	R_C1[12]	R_C1[11]	R_C1[10]	R_C1[9]	R_C1[8]
0x3E	RMS1C	R_C1[7]	R_C1[6]	R_C1[5]	R_C1[4]	R_C1[3]	R_C1[2]	R_C1[1]	R_C1[0]

7.1 Configuration register A (addr 0x00)

D7	D6	D5	D4	D3	D2	D1	D0
FDRB	TWAB	TWRB	IR1	IR0	MCS2	MCS1	MCS0
0	1	1	0	0	0	1	1

7.1.1 Master clock select

Table 11. Master clock select

Bit	R/W	RST	Name	Description
0	R/W	1	MCS0	Selects the ratio between the input I^2S sample frequency and the input clock.
1	R/W	1	MCS1	
2	R/W	0	MCS2	

The STA339BW supports sample rates of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz. Therefore the internal clock is:

- 32.768 MHz for 32 kHz
- 45.1584 MHz for 44.1 kHz, 88.2 kHz, and 176.4 kHz
- 49.152 MHz for 48 kHz, 96 kHz, and 192 kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sample frequency (f_S).

The relationship between the input clock and the input sample rate is determined by both the MCSx and the IR (input rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IR bit determines the oversampling ratio used internally.

Table 12. Input sampling rates

Input sample rate *fs* (kHz)	IR	MCS[2:0]					
-	-	101	100	011	010	001	000
32, 44.1, 48	00	576 * fs	128 * fs	256 * fs	384 * fs	512 * fs	768 * fs
88.2, 96	01	NA	64 * fs	128 * fs	192 * fs	256 * fs	384 * fs
176.4, 192	1X	NA	32 * fs	64 * fs	96 * fs	128 * fs	192 * fs

7.1.2 Interpolation ratio select

Table 13. Internal interpolation ratio

Bit	R/W	RST	Name	Description
4:3	R/W	00	IR [1:0]	Selects internal interpolation ratio based on input I^2S sample frequency

The STA339BW has variable interpolation (oversampling) settings such that internal processing and FFX output rates remain consistent. The first processing block interpolates by either 2-times or 1-time (pass-through) or provides a 2-times downsample. The oversampling ratio of this interpolation is determined by the IR bits.

Table 14. IR bit settings as a function of input sample rate

Input sample rate fs (kHz)	IR	1st stage interpolation ratio
32	00	2 times oversampling
44.1	00	2 times oversampling
48	00	2 times oversampling
88.2	01	Pass-through
96	01	Pass-through
176.4	10	2 times downsampling
192	10	2 times downsampling

7.1.3 Thermal warning recovery bypass

Table 15. Thermal warning recovery bypass

Bit	R/W	RST	Name	Description
5	R/W	1	TWRB	0: Thermal warning recovery enabled 1: Thermal warning recovery disabled

If the thermal warning adjustment is enabled (TWAB = 0), then the thermal warning recovery determines if the -3 dB output limit is removed when thermal warning is negative.

If TWRB = 0 and TWAB = 0, then when a thermal warning disappears the -3 dB output limit is removed and the gain is added back to the system. If TWRB = 1 and TWAB = 0, then when a thermal warning disappears the -3 dB output limit remains until TWRB is changed to zero or the device is reset.

7.1.4 Thermal warning adjustment bypass

Table 16. Thermal warning adjustment bypass

Bit	R/W	RST	Name	Description
6	R/W	1	TWAB	0: Thermal warning adjustment enabled 1: Thermal warning adjustment disabled

The on-chip STA339BW power output block provides feedback to the digital controller using inputs to the power control block. Input TWARN is used to indicate a thermal warning condition. When TWARN is asserted (set to 0) for a period of time greater than 400 ms, the power control block forces a -3 dB output limit (determined by TWOCL in the coefficient RAM) to the modulation limit in an attempt to eliminate the thermal warning condition. Once the thermal warning output limit adjustment is applied, it remains in this state until reset, unless FDRB = 0.

7.1.5 Fault detect recovery bypass

Table 17. Fault detect recovery bypass

Bit	R/W	RST	Name	Description
7	R/W	0	FDRB	0: fault detect recovery enabled 1: fault detect recovery disabled

The on-chip STA339BW power output block provides feedback to the digital controller using inputs to the power control block. The FAULT input is used to indicate a fault condition (either overcurrent or thermal). When FAULT is asserted (set to 0), the power control block attempts a recovery from the fault by asserting the tri-state output (setting it to 0 which directs the power output block to begin recovery), holds it at 0 for period of time in the range of 0.1 ms to 1 second as defined by the fault-detect recovery constant register (FDRC registers 0x2B-0x2C), then toggles it back to 1. This sequence is repeated as log as the fault indication exists. This feature is enabled by default but can be bypassed by setting the FDRB control bit to 1.

7.2 Configuration register B (addr 0x01)

D7	D6	D5	D4	D3	D2	D1	D0
C2IM	C1IM	DSCKE	SAIFB	SAI3	SAI2	SAI1	SAI0
1	0	0	0	0	0	0	0

7.2.1 Serial audio input interface format

Table 18. Serial audio input interface

Bit	R/W	RST	Name	Description
0	R/W	0	SAI0	Determines the interface format of the input serial digital audio interface.
1	R/W	0	SAI1	
2	R/W	0	SAI2	
3	R/W	0	SAI3	

7.2.2 Serial data interface

The STA339BW audio serial input was designed to interface with standard digital audio components and to accept a number of serial data formats. STA339BW always acts as slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using three inputs: left/right clock LRCKI, serial clock BICKI, and serial data 1 and 2 SDI12.

The SAI bits (D3 to D0) and the SAIFB bit (D4) are used to specify the serial data format. The default serial data format is I^2S, MSB-first. Available formats are shown in the tables and figure that follow.

7.2.3 Serial data first bit

Table 19. Serial data first bit

SAIFB	Format
0	MSB-first
1	LSB-first

Table 20. Supported serial audio input formats for MSB-first (SAIFB = 0)

BICKI	SAI [3:0]	SAIFB	Interface format
32 * fs	0000	0	I^2S 15-bit data
	0001	0	Left/right-justified 16-bit data
48 * fs	0000	0	I^2S 16 to 23-bit data
	0001	0	Left-justified 16 to 24-bit data
	0010	0	Right-justified 24-bit data
	0110	0	Right-justified 20-bit data
	1010	0	Right-justified 18-bit data
	1110	0	Right-justified 16-bit data
64 * fs	0000	0	I^2S 16 to 24-bit data
	0001	0	Left-justified 16 to 24-bit data
	0010	0	Right-justified 24-bit data
	0110	0	Right-justified 20-bit data
	1010	0	Right-justified 18-bit data
	1110	0	Right-justified 16-bit data

Table 21. Supported serial audio input formats for LSB-first (SAIFB = 1)

BICKI	SAI [3:0]	SAIFB	Interface format
32 * fs	1100	1	I^2S 15-bit data
	1110	1	Left/right-justified 16-bit data
48 * fs	0100	1	I^2S 23-bit data
	0100	1	I^2S 20-bit data
	1000	1	I^2S 18-bit data
	1100	1	LSB first I^2S 16-bit data
	0001	1	Left-justified 24-bit data
	0101	1	Left-justified 20-bit data
	1001	1	Left-justified 18-bit data
	1101	1	Left-justified 16-bit data
	0010	1	Right-justified 24-bit data
	0110	1	Right-justified 20-bit data
	1010	1	Right-justified 18-bit data
	1110	1	Right-justified 16-bit data
64 * fs	0000	1	I^2S 24-bit data
	0100	1	I^2S 20-bit data
	1000	1	I^2S 18-bit data
	1100	1	LSB first I^2S 16-bit data
	0001	1	Left-justified 24-bit data
	0101	1	Left-justified 20-bit data
	1001	1	Left-justified 18-bit data
	1101	1	Left-justified 16-bit data
	0010	1	Right-justified 24-bit data
	0110	1	Right-justified 20-bit data
	1010	1	Right-justified 18-bit data
	1110	1	Right-justified 16-bit data

To make the STA339BW work properly, the serial audio interface LRCKI clock must be synchronous to the PLL output clock. It means that:

- the frequency of PLL clock / frequency of LRCKI = N ±4 cycles, where N depends on the settings in *Table 14 on page 29*
- the PLL must be locked.

If these two conditions are not met, and bit IDE of register address 0x05 is set to 1, the STA339BW immediately mutes the I^2S PCM data out (provided to the processing block) and it freezes any active processing task.

To avoid any audio side effects (like pop noise), it is strongly recommended to soft mute any audio streams flowing into STA339BW data path before the desynchronization event happens. At the same time any processing related to the I^2C configuration should be issued only after the serial audio interface and the internal PLL are synchronous again.

Note: Any mute or volume change causes some delay in the completion of the I^2C operation due to the soft volume feature. The soft volume phase change must be finished before any clock desynchronization.

7.2.4 Delay serial clock enable

Table 22. Delay serial clock enable

Bit	R/W	RST	Name	Description
5	R/W	0	DSCKE	0: No serial clock delay 1: Serial clock delay by 1 core clock cycle to tolerate anomalies in some I^2S master devices

7.2.5 Channel input mapping

Table 23. Channel input mapping

Bit	R/W	RST	Name	Description
6	R/W	0	C1IM	0: Processing channel 1 receives Left I^2S Input 1: Processing channel 1 receives Right I^2S Input
7	R/W	1	C2IM	0: Processing channel 2 receives Left I^2S Input 1: Processing channel 2 receives Right I^2S Input

Each channel received via I^2S can be mapped to any internal processing channel via the Channel Input Mapping registers. This allows for flexibility in processing. The default settings of these registers map each I^2S input channel to its corresponding processing channel.

7.3 Configuration register C (addr 0x02)

D7	D6	D5	D4	D3	D2	D1	D0
OCRB	Reserved	CSZ3	CSZ2	CSZ1	CSZ0	OM1	OM0
1	0	0	1	1	1	1	1

7.3.1 FFX power output mode

Table 24. FFX power output mode

Bit	R/W	RST	Name	Description
0	R/W	1	OM0	Selects configuration of FFX output.
1	R/W	1	OM1	

The FFX power output mode selects how the FFX output timing is configured.

Different power devices use different output modes.

Table 25. Output modes

OM[1,0]	Output stage mode
00	Drop compensation
01	Discrete output stage - tapered compensation
10	Full power mode
11	Variable drop compensation (CSZx bits)

7.3.2 FFX compensating pulse size register

Table 26. FFX compensating pulse size bits

Bit	R/W	RST	Name	Description
2	R/W	1	CSZ0	When OM[1,0] = 11, this register determines the size of the FFX compensating pulse from 0 clock ticks to 15 clock periods.
3	R/W	1	CSZ1	
4	R/W	1	CSZ2	
5	R/W	0	CSZ3	

Table 27. Compensating pulse size

CSZ[3:0]	Compensating pulse size
0000	0 ns (0 tick) compensating pulse size
0001	20 ns (1 tick) clock period compensating pulse size
…	…
1111	300 ns (15 tick) clock period compensating pulse size

7.3.3 Overcurrent warning detect adjustment bypass

Table 28. Overcurrent warning bypass

Bit	R/W	RST	Name	Description
7	R/W	1	OCRB	0: overcurrent warning adjustment enabled 1: overcurrent warning adjustment disabled

The OCWARN input is used to indicate an overcurrent warning condition. When OCWARN is asserted (set to 0), the power control block forces an adjustment to the modulation limit (default is -3 dB) in an attempt to eliminate the overcurrent warning condition. Once the overcurrent warning volume adjustment is applied, it remains in this state until reset is applied. The level of adjustment can be changed via the TWOCL (thermal warning / overcurrent limit) setting which is address 0x37 of the user defined coefficient RAM.

7.4 Configuration register D (addr 0x03)

D7	D6	D5	D4	D3	D2	D1	D0
SME	ZDE	DRC	BQL	PSL	DSPB	DEMP	HPB
0	1	0	0	0	0	0	0

7.4.1 High-pass filter bypass

Table 29. High-pass filter bypass

Bit	R/W	RST	Name	Description
0	R/W	0	HPB	Setting of one bypasses internal AC coupling digital high-pass filter

The STA339BW features an internal digital high-pass filter for the purpose of AC coupling. The purpose of this filter is to prevent DC signals from passing through a FFX amplifier. DC signals can cause speaker damage. When HPB = 0, this filter is enabled.

7.4.2 De-emphasis

Table 30. De-emphasis

Bit	R/W	RST	Name	Description
1	R/W	0	DEMP	0: No de-emphasis 1: Enable de-emphasis on all channels

7.4.3 DSP bypass

Table 31. DSP bypass

Bit	R/W	RST	Name	Description
2	R/W	0	DSPB	0: Normal operation 1: Bypass of biquad and bass/treble functions

Setting the DSPB bit bypasses the EQ function of the STA339BW.

7.4.4 Post-scale link

Table 32. Post-scale link

Bit	R/W	RST	Name	Description
3	R/W	0	PSL	0: Each channel uses individual post-scale value 1: Each channel uses channel 1 post-scale value

Post-scale functionality can be used for power-supply error correction. For multi-channel applications running off the same power-supply, the post-scale values can be linked to the value of channel 1 for ease of use and update the values faster.

7.4.5 Biquad coefficient link

Table 33. Biquad coefficient link

Bit	R/W	RST	Name	Description
4	R/W	0	BQL	0: Each channel uses coefficient values 1: Each channel uses channel 1 coefficient values

For ease of use, all channels can use the biquad coefficients loaded into the Channel-1 coefficient RAM space by setting the BQL bit to 1. Therefore, any EQ updates only have to be performed once.

7.4.6 Dynamic range compression/anti-clipping bit

Table 34. Dynamic range compression/anti-clipping bit

Bit	R/W	RST	Name	Description
5	R/W	0	DRC	0: Limiters act in anti-clipping mode 1: Limiters act in dynamic range compression mode

Both limiters can be used in one of two ways, anti-clipping or dynamic range compression. When used in anti-clipping mode the limiter threshold values are constant and dependent on the limiter settings. In dynamic range compression mode the limiter threshold values vary with the volume settings allowing a nighttime listening mode that provides a reduction in the dynamic range regardless of the volume level.

7.4.7 Zero-detect mute enable

Table 35. Zero-detect mute enable

Bit	R/W	RST	Name	Description
6	R/W	1	ZDE	Setting of 1 enables the automatic zero-detect mute

Setting the ZDE bit enables the zero-detect automatic mute. The zero-detect circuit looks at the data for each processing channel at the output of the crossover (bass management) filter. If any channel receives 2048 consecutive zero value samples (regardless of fs) then that individual channel is muted if this function is enabled.

7.4.8 Submix mode enable

Table 36. Submix mode enable

Bit	R/W	RST	Name	Description
7	R/W	0	SME	0: Sub Mix into Left/Right disabled 1: Sub Mix into Left/Right enabled

7.5 Configuration register E (addr 0x04)

D7	D6	D5	D4	D3	D2	D1	D0
SVE	ZCE	DCCV	PWMS	AME	NSBW	MPC	MPCV
1	1	0	0	0	0	1	0

7.5.1 Max power correction variable

Table 37. Max power correction variable

Bit	R/W	RST	Name	Description
0	R/W	0	MPCV	0: Use standard MPC coefficient 1: Use MPCC bits for MPC coefficient

7.5.2 Max power correction

Table 38. Max power correction

Bit	R/W	RST	Name	Description
1	R/W	1	MPC	Setting of 1 enables Power Bridge correction for THD reduction near maximum power output.

Setting the MPC bit turns on special processing that corrects the STA339BW power device at high power. This mode should lower the THD+N of a full FFX system at maximum power output and slightly below. If enabled, MPC is operational in all output modes except tapered (OM[1,0] = 01) and binary. When OCFG = 00, MPC will not effect channels 3 and 4, the line-out channels.

7.5.3 Noise-shaper bandwidth selection

Table 39. Noise-shaper bandwidth selection

Bit	R/W	RST	Name	Description
2	R/W	0	NSBW	1: Third order NS 0: Fourth order NS

7.5.4 AM mode enable

Table 40. AM mode enable

Bit	R/W	RST	Name	Description
3	R/W	0	AME	0: Normal FFX operation. 1: AM reduction mode FFX operation

STA339BW features aFFX processing mode that minimizes the amount of noise generated in frequency range of AM radio. This mode is intended for use when FFX is operating in a device with an AM tuner active. The SNR of the FFX processing is reduced to approximately 83 dB in this mode, which is still greater than the SNR of AM radio.

7.5.5 PWM speed mode

Table 41. PWM speed mode

Bit	R/W	RST	Name	Description
4	R/W	0	PWMS	0: Normal speed (384 kHz) all channels 1: Odd speed (341.3 kHz) all channels

7.5.6 Distortion compensation variable enable

Table 42. Distortion compensation variable enable

Bit	R/W	RST	Name	Description
5	R/W	0	DCCV	0: Use preset DC coefficient 1: Use DCC coefficient

7.5.7 Zero-crossing volume enable

Table 43. Zero-crossing volume enable

Bit	R/W	RST	Name	Description
6	R/W	1	ZCE	1: Volume adjustments only occur at digital zero-crossings 0: Volume adjustments occur immediately

The ZCE bit enables zero-crossing volume adjustments. When volume is adjusted on digital zero-crossings no clicks are audible.

7.5.8 Soft volume update enable

Table 44. Soft volume update enable

Bit	R/W	RST	Name	Description
7	R/W	1	SVE	1: Volume adjustments ramp according to SVR settings 0: Volume adjustments occur immediately

7.6 Configuration register F (addr 0x05)

D7	D6	D5	D4	D3	D2	D1	D0
EAPD	PWDN	ECLE	LDTE	BCLE	IDE	OCFG1	OCFG0
0	1	0	1	1	1	0	0

7.6.1 Output configuration

Table 45. Output configuration

Bit	R/W	RST	Name	Description
0	R/W	0	OCFG0	Selects the output configuration
1	R/W	0	OCFG1	

Table 46. Output configuration engine selection

OCFG[1:0]	Output configuration	Config pin
00	2 channel (full-bridge) power, 2 channel data-out: 1A/1B → 1A/1B 2A/2B → 2A/2B LineOut1 → 3A/3B LineOut2 → 4A/4B Line Out Configuration determined by LOC register	0
01	2(Half-Bridge).1(Full-Bridge) On-Board Power: 1A → 1A Binary 0 ° 2A → 1B Binary 90° 3A/3B → 2A/2B Binary 45° 1A/B → 3A/B Binary 0° 2A/B → 4A/B Binary 90°	0
10	2 Channel (Full-Bridge) Power, 1 Channel FFX: 1A/1B → 1A/1B 2A/2B → 2A/2B 3A/3B → 3A/3B EAPDEXT and TWARNEXT Active	0
11	1 Channel Mono-Parallel: 3A → 1A/1B w/ C3BO 45° 3B → 2A/2B w/ C3BO 45° 1A/1B → 3A/3B 2A/2B → 4A/4B	1

Note: To the left of the arrow is the processing channel. When using channel output mapping, any of the three processing channel outputs can be used for any of the three inputs.

Figure 12. OCFG = 00 (default value)

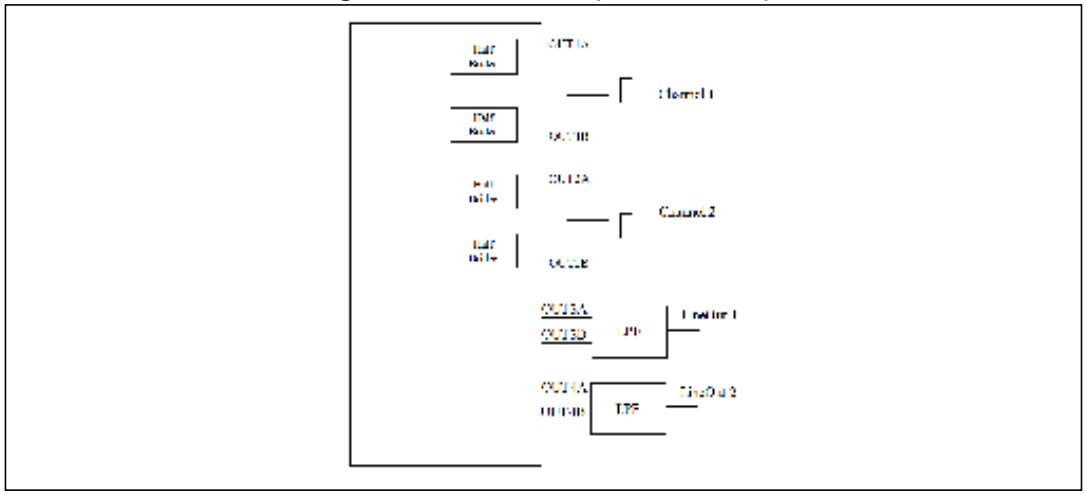


Figure 13. OCFG = 01

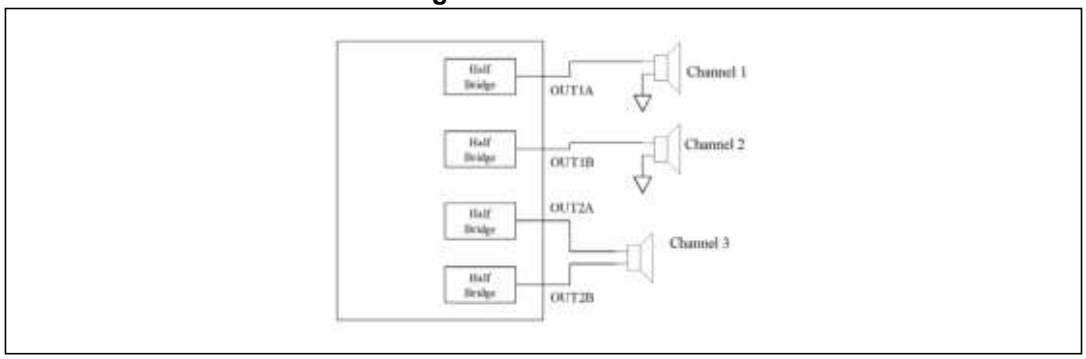


Figure 14. OCFG = 10

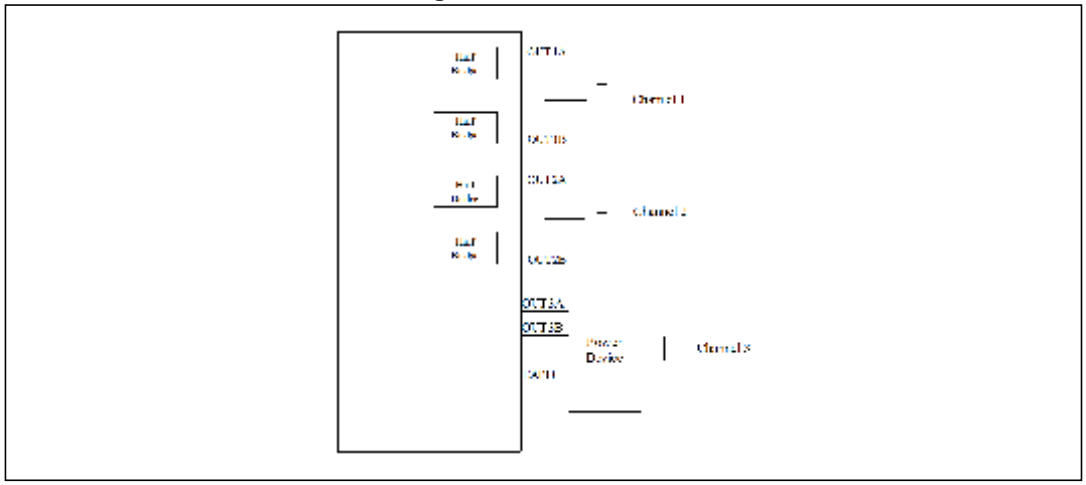
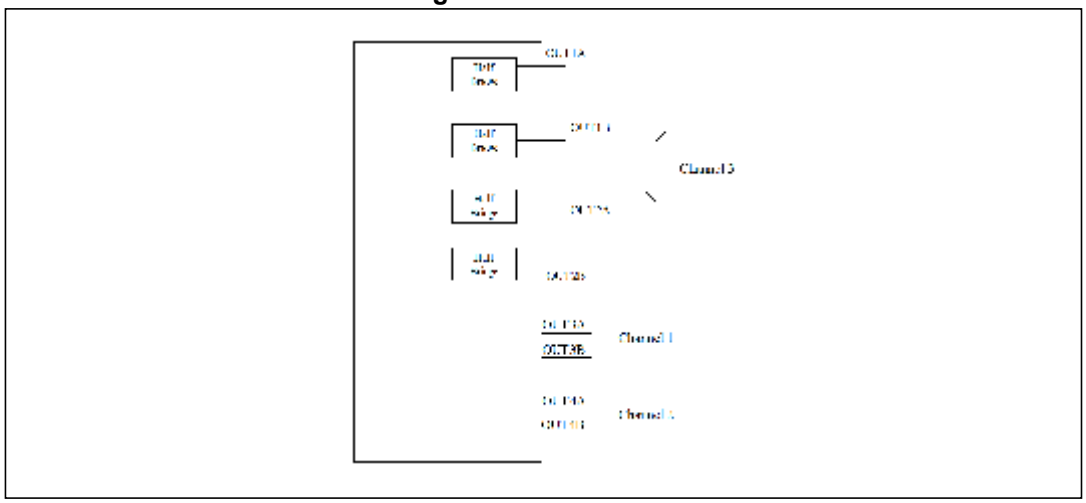
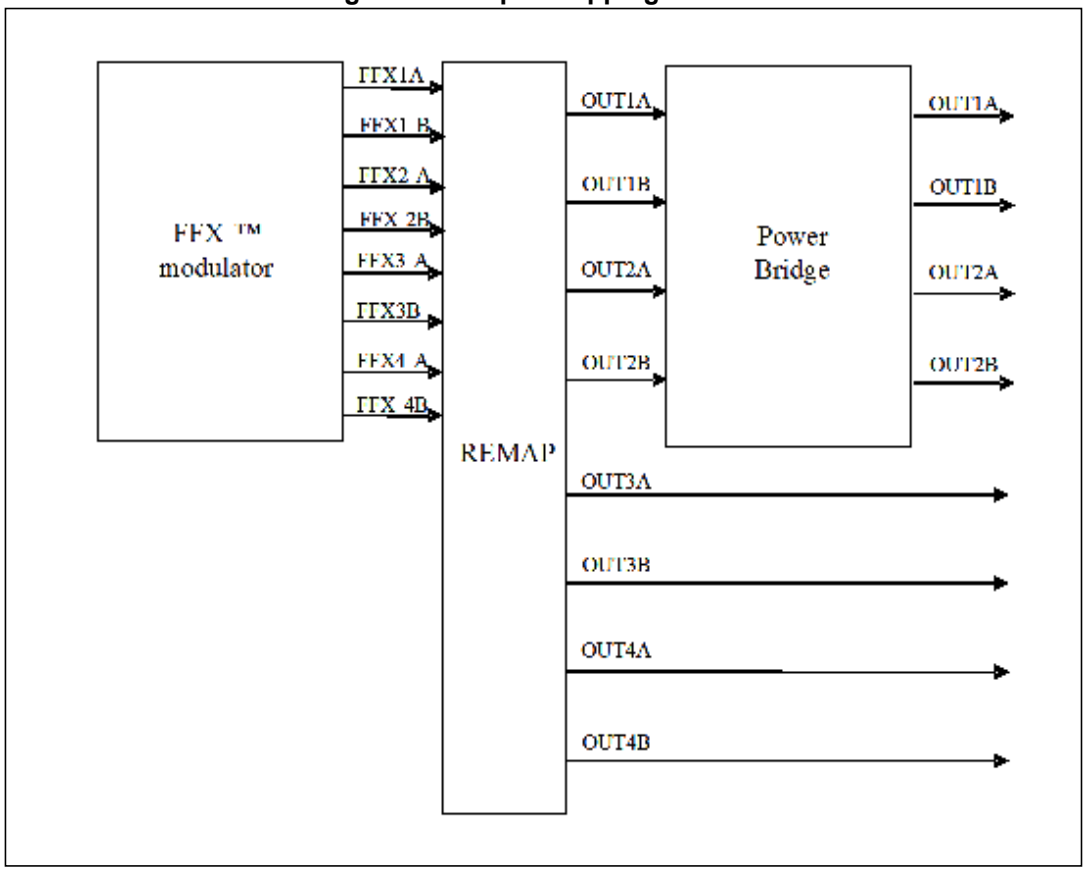


Figure 15. OCFG = 11



The STA339BW can be configured to support different output configurations. For each PWM output channel a PWM slot is defined. A PWM slot is always 1 / (8 * fs) seconds length. The PWM slot define the maximum extension for PWM rise and fall edge, that is, rising edge as far as the falling edge cannot range outside PWM slot boundaries.

Figure 16. Output mapping scheme



For each configuration the PWM signals from the digital driver are mapped in different ways to the power stage:

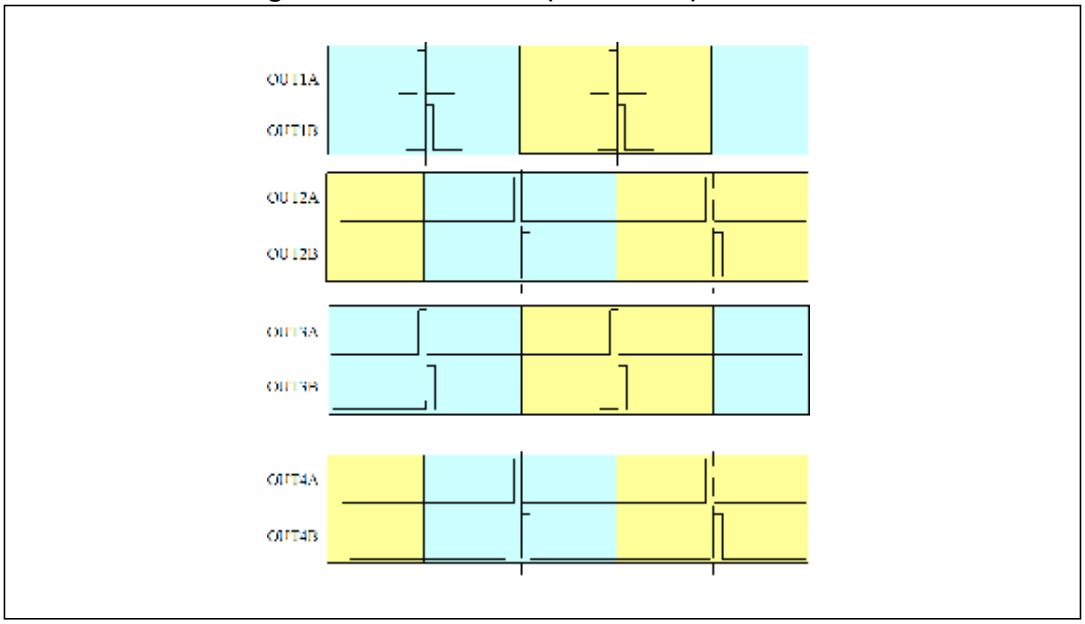
2.0 channels, two full bridges (OCFG = 00)

- FFX1A -> OUT1A
- FFX1B -> OUT1B
- FFX2A -> OUT2A
- FFX2B -> OUT2B
- FFX3A -> OUT3A
- FFX3B -> OUT3B
- FFX4A -> OUT4A
- FFX4B -> OUT4B
- FFX1A/1B configured as ternary
- FFX2A/2B configured as ternary
- FFX3A/3B configured as lineout ternary
- FFX4A/4B configured as lineout ternary

On channel 3 line out (LOC bits = 00) the same data as channel 1 processing is sent. On channel 4 line out (LOC bits = 00) the same data as channel 2 processing is sent. In this configuration, volume control or EQ have no effect on channels 3 and 4.

In this configuration the PWM slot phase is the following as shown in *Figure 17*.

Figure 17. 2.0 channels (OCFG = 00) PWM slots



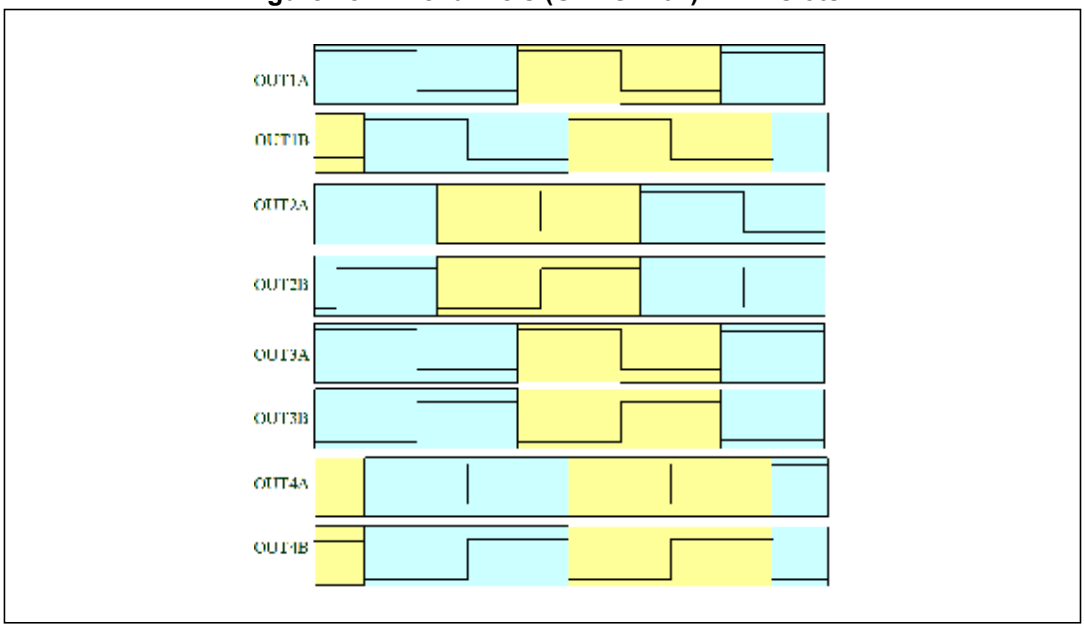
2.1 channels, two half bridges + one full bridge (OCFG = 01)

- FFX1A -> OUT1A
- FFX2A -> OUT1B
- FFX3A -> OUT2A
- FFX3B -> OUT2B
- FFX1A -> OUT3A
- FFX1B -> OUT3B
- FFX2A -> OUT4A
- FFX2B -> OUT4B
- FFX1A/1B configured as binary
- FFX2A/2B configured as binary
- FFX3A/3B configured as binary
- FFX4A/4B is not used

In this configuration, channel 3 has full control (volume, EQ, etc…). On OUT3/OUT4 channels the channel 1 and channel 2 PWM are replicated.

In this configuration the PWM slot phase is the following as shown in *Figure 18*.

Figure 18. 2.1 channels (OCFG = 01) PWM slots



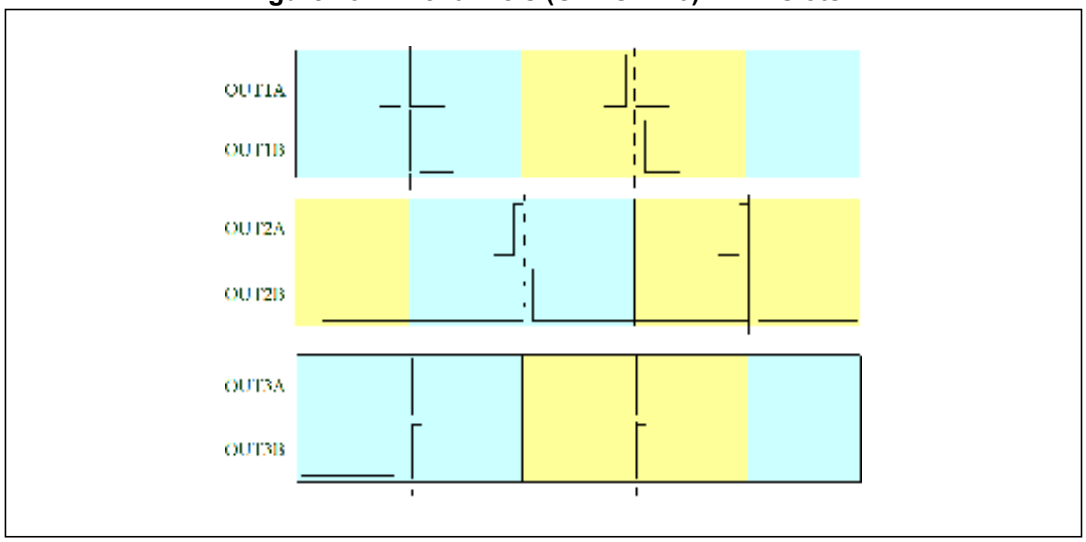
2.1 channels, two fullbridge + one external full bridge (OCFG = 10)

- FFX1A -> OUT1A
- FFX1B -> OUT1B
- FFX2A -> OUT2A
- FFX2B -> OUT2B
- FFX3A -> OUT3A
- FFX3B -> OUT3B
- EAPD -> OUT4A
- TWARN -> OUT4B
- FFX1A/1B configured as ternary
- FFX2A/2B configured as ternary
- FFX3A/3B configured as ternary
- FFX4A/4B is not used

In this configuration, channel 3 has full control (volume, EQ, etc…). On OUT4 channel the external bridge control signals are muxed.

In this configuration the PWM slot phase is the following as shown in *Figure 19*.

Figure 19. 2.1 channels (OCFG = 10) PWM slots



7.6.2 Invalid input detect mute enable

Table 47. Invalid input detect mute enable

Bit	R/W	RST	Name	Description
2	R/W	1	IDE	Setting of 1 enables the automatic invalid input detect mute

Setting the IDE bit enables this function, which looks at the input I^2S data and automatically mutes if the signals are perceived as invalid.

7.6.3 Binary output mode clock loss detection

Table 48. Binary output mode clock loss detection

Bit	R/W	RST	Name	Description
3	R/W	1	BCLE	Binary output mode clock loss detection enable

Detects loss of input MCLK in binary mode and will output 50% duty cycle.

7.6.4 LRCK double trigger protection

Table 49. LRCK double trigger protection

Bit	R/W	RST	Name	Description
4	R/W	1	LDTE	LRCLK double trigger protection enable

Actively prevents double trigger of LRCLK.

7.6.5 Auto EAPD on clock loss

Table 50. Auto EAPD on clock loss

Bit	R/W	RST	Name	Description
5	R/W	0	ECLE	Auto EAPD on clock loss

When active, issues a power device power down signal (EAPD) on clock loss detection.

7.6.6 IC power down

Table 51. IC power down

Bit	R/W	RST	Name	Description
7	R/W	1	PWDN	0: IC power down low-power condition 1: IC normal operation

The PWDN register is used to place the IC in a low-power state. When PWDN is written as 0, the output begins a soft-mute. After the mute condition is reached, EAPD is asserted

to power down the power-stage, then the master clock to all internal hardware expect the I^2C block is gated. This places the IC in a very low power consumption state.

7.6.7 External amplifier power down

Table 52. External amplifier power down

Bit	R/W	RST	Name	Description
7	R/W	0	EAPD	0: External power stage power down active 1: Normal operation

The EAPD register directly disables/enables the internal power circuitry.

When EAPD = 0, the internal power section is placed on a low-power state (disabled). This register also controls the FFX4B/EAPD output pin when OCFG = 10.

7.7 Volume control registers (addr 0x06 - 0x0A)

7.7.1 Mute/line output configuration register

D7	D6	D5	D4	D3	D2	D1	D0
LOC1	LOC0	Reserved		C3M	C2M	C1M	MMUTE
0	0	0	0	0	0	0	0

Table 53. Line output configuration

LOC[1:0]	Line output configuration
00	Line output fixed - no volume, no EQ
01	Line output variable - CH3 volume effects line output, no EQ
10	Line output variable with EQ - CH3 volume effects line output

Line output is only active when OCFG = 00. In this case LOC determines the line output configuration. The source of the line output is always the channel 1 and 2 inputs.

7.7.2 Master volume register

D7	D6	D5	D4	D3	D2	D1	D0
MV7	MV6	MV5	MV4	MV3	MV2	MV1	MV0
1	1	1	1	1	1	1	1

7.7.3 Channel 1 volume

D7	D6	D5	D4	D3	D2	D1	D0
C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
0	1	1	0	0	0	0	0

7.7.4 Channel 2 volume

D7	D6	D5	D4	D3	D2	D1	D0
C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
0	1	1	0	0	0	0	0

7.7.5 Channel 3 / line output volume

D7	D6	D5	D4	D3	D2	D1	D0
C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
0	1	1	0	0	0	0	0

The Volume structure of the STA339BW consists of individual volume registers for each channel and a master volume register that provides an offset to each channels volume setting. The individual channel volumes are adjustable in 0.5 dB steps from +48 dB to -80 dB.

As an example if C3V = 0x00 or +48 dB and MV = 0x18 or -12 dB, then the total gain for channel 3 = +36 dB.

The master mute, when set to 1, mutes all channels at once, whereas the individual channel mutes (CxM) mutes only that channel. Both the master mute and the channel mutes provide a “soft mute” with the volume ramping down to mute in 4096 samples from the maximum volume setting at the internal processing rate (approximately 96 kHz).

A “hard (instantaneous) mute” can be obtained by programming a value of 0xFF (255) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register any channel whose total volume is less than -80 dB is muted.

All changes in volume take place at zero-crossings when ZCE = 1 (*Configuration register E (addr 0x04) on page 37*) on a per channel basis as this creates the smoothest possible volume transitions. When ZCE = 0, volume updates occur immediately.

Table 54. Master volume offset as a function of MV[7:0]

MV[7:0]	Volume offset from channel value
00000000 (0x00)	0 dB
00000001 (0x01)	-0.5 dB
00000010 (0x02)	-1 dB
…	…
01001100 (0x4C)	-38 dB
…	…
11111110 (0xFE)	-127.5 dB
11111111 (0xFF)	Hard master mute

Table 55. Channel volume as a function of CxV[7:0]

CxV[7:0]	Volume
00000000 (0x00)	+48 dB
00000001 (0x01)	+47.5 dB
00000010 (0x02)	+47 dB
…	…
01011111 (0x5F)	+0.5 dB
01100000 (0x60)	0 dB
01100001 (0x61)	-0.5 dB
…	…
11010111 (0xD7)	-59.5 dB
11011000 (0xD8)	-60 dB
11011001 (0xD9)	-61 dB
11011010 (0xDA)	-62 dB
…	…
11101100 (0xEC)	-80 dB
11101101 (0xED)	Hard channel mute
…	…
11111111 (0xFF)	Hard channel mute

7.8 Audio preset registers (addr 0x0B and 0x0C)

7.8.1 Audio preset register 1 (addr 0x0B)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		AMGC[1]	AMGC[0]	Reserved			
0	0	0	0	0	0	0	0

Using AMGC[3:0] bits, attack and release thresholds and rates are automatically configured to properly fit application specific configurations. AMGC[3:2] is defined in register *EQ coefficients and DRC configuration register (addr 0x31) on page 66*.

The AMGC[1:0] bits behave in two different ways depending on the value of AMGC[3:2]. When this value is 00 then bits AMGC[1:0] are defined below in *Table 56*.

Table 56. Audio preset gain compression/limiters selection for AMGC[3:2] = 00

AMGC[1:0]	Mode
00	User programmable GC
01	AC no clipping 2.1
10	AC limited clipping (10%) 2.1
11	DRC night-time listening mode 2.1

7.8.2 Audio preset register 2 (addr 0x0C)

D7	D6	D5	D4	D3	D2	D1	D0
XO3	XO2	XO1	XO0	AMAM2	AMAM1	AMAM0	AMAME
0	0	0	0	0	0	0	0

7.8.3 AM interference frequency switching

Table 57. AM interference frequency switching bits

Bit	R/W	RST	Name	Description
0	R/W	0	AMAME	Audio preset AM enable 0: switching frequency determined by PWMS setting 1: switching frequency determined by AMAM settings

Table 58. Audio preset AM switching frequency selection

AMAM[2:0]	48 kHz/96 kHz input fs	44.1 kHz/88.2 kHz input fs
000	0.535 MHz - 0.720 MHz	0.535 MHz - 0.670 MHz
001	0.721 MHz - 0.900 MHz	0.671 MHz - 0.800 MHz
010	0.901 MHz - 1.100 MHz	0.801 MHz - 1.000 MHz
011	1.101 MHz - 1.300 MHz	1.001 MHz - 1.180 MHz
100	1.301 MHz - 1.480 MHz	1.181 MHz - 1.340 MHz
101	1.481 MHz - 1.600 MHz	1.341 MHz - 1.500 MHz
110	1.601 MHz - 1.700 MHz	1.501 MHz - 1.700 MHz

7.8.4 Bass management crossover

Table 59. Bass management crossover

Bit	R/W	RST	Name	Description
4	R/W	0	XO0	Selects the bass-management crossover frequency. A 1st-order hign-pass filter (channels 1 and 2) or a 2nd-order low-pass filter (channel 3) at the selected frequency is performed.
5	R/W	0	XO1	
6	R/W	0	XO2	
7	R/W	0	XO3	

Table 60. Bass management crossover frequency

XO[3:0]	Crossover frequency
0000	User-defined
0001	80 Hz
0010	100 Hz
0011	120 Hz

Table 60. Bass management crossover frequency (continued)

XO[3:0]	Crossover frequency
0100	140 Hz
0101	160 Hz
0110	180 Hz
0111	200 Hz
1000	220 Hz
1001	240 Hz
1010	260 Hz
1011	280 Hz
1100	300 Hz
1101	320 Hz
1110	340 Hz
1111	360 Hz

7.9 Channel configuration registers (addr 0x0E - 0x10)

D7	D6	D5	D4	D3	D2	D1	D0
C1OM1	C1OM0	C1LS1	C1LS0	C1BO	C1VPB	C1EQBP	C1TCB
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
C2OM1	C2OM0	C2LS1	C2LS0	C2BO	C2VPB	C2EQBP	C2TCB
0	1	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
C3OM1	C3OM0	C3LS1	C3LS0	C3BO	C3VPB	Reserved	
1	0	0	0	0	0	0	0

7.9.1 Tone control bypass

Tone control (bass/treble) can be bypassed on a per channel basis for channels 1 and 2.

Table 61. Tone control bypass

CxTCB	Mode
0	Perform tone control on channel x - normal operation
1	Bypass tone control on channel x

7.9.2 EQ bypass

EQ control can be bypassed on a per channel basis for channels 1 and 2. If EQ control is bypassed on a given channel the prescale and all filters (high-pass, biquads, de-emphasis, bass, treble in any combination) are bypassed for that channel.

Table 62. EQ bypass

CxEQBP	Mode
0	Perform EQ on channel x - normal operation
1	Bypass EQ on channel x

7.9.3 Volume bypass

Each channel contains an individual channel volume bypass. If a particular channel has volume bypassed via the CxVBP = 1 register then only the channel volume setting for that particular channel affects the volume setting, the master volume setting will not affect that channel.

7.9.4 Binary output enable registers

Each individual channel output can be set to output a binary PWM stream. In this mode output A of a channel is considered the positive output and output B is negative inverse.

Table 63. Binary output enable registers

CxBO	Mode
0	FFX 3-state output - normal operation
1	Binary output

7.9.5 Limiter select

Limiter selection can be made on a per-channel basis according to the channel limiter select bits.

Table 64. Channel limiter mapping as a function of CxLS bits

CxLS[1:0]	Channel limiter mapping
00	Channel has limiting disabled
01	Channel is mapped to limiter #1
10	Channel is mapped to limiter #2

7.9.6 Output mapping

Output mapping can be performed on a per channel basis according to the CxOM channel output mapping bits. Each input into the output configuration engine can receive data from any of the three processing channel outputs.

Table 65. Channel output mapping as a function of CxOM bits

CxOM[1:0]	Channel x output source from
00	Channel1
01	Channel 2
10	Channel 3

7.10 Tone control register (addr 0x11)

D7	D6	D5	D4	D3	D2	D1	D0
TTC3	TTC2	TTC1	TTC0	BTC3	BTC2	BTC1	BTC0
0	1	1	1	0	1	1	1

7.10.1 Tone control

Table 66. Tone control boost/cut as a function of BTC and TTC bits

BTC[3:0]/TTC[3:0]	Boost/Cut
0000	-12 dB
0001	-12 dB
…	…
0111	-4 dB
0110	-2 dB
0111	0 dB
1000	+2 dB
1001	+4 dB
…	…
1101	+12 dB
1110	+12 dB
1111	+12 dB

7.11 Dynamic control registers (addr 0x12 - 0x15)

7.11.1 Limiter 1 attack/release rate

D7	D6	D5	D4	D3	D2	D1	D0
L1A3	L1A2	L1A1	L1A0	L1R3	L1R2	L1R1	L1R0
0	1	1	0	1	0	1	0

7.11.2 Limiter 1 attack/release threshold

D7	D6	D5	D4	D3	D2	D1	D0
L1AT3	L1AT2	L1AT1	L1AT0	L1RT3	L1RT2	L1RT1	L1RT0
0	1	1	0	1	0	0	1

7.11.3 Limiter 2 attack/release rate

D7	D6	D5	D4	D3	D2	D1	D0
L2A3	L2A2	L2A1	L2A0	L2R3	L2R2	L2R1	L2R0
0	1	1	0	1	0	1	0

7.11.4 Limiter 2 attack/release threshold

D7	D6	D5	D4	D3	D2	D1	D0
L2AT3	L2AT2	L2AT1	L2AT0	L2RT3	L2RT2	L2RT1	L2RT0
0	1	1	0	1	0	0	1

The STA339BW includes two independent limiter blocks. The purpose of the limiters is to automatically reduce the dynamic range of a recording to prevent the outputs from clipping in anti-clipping mode or to actively reduce the dynamic range for a better listening environment such as a night-time listening mode which is often needed for DVDs. The two modes are selected via the DRC bit in *Configuration register E (addr 0x04) on page 37*. Each channel can be mapped to either limiter or not mapped, meaning that channel will clip when 0 dBfs is exceeded. Each limiter looks at the present value of each channel that is mapped to it, selects the maximum absolute value of all these channels, performs the limiting algorithm on that value, and then if needed adjusts the gain of the mapped channels in unison.

The limiter attack thresholds are determined by the LxAT registers if EATHx[7] bits are set to 0 else the thresholds are determined by EATHx[6:0] . It is recommended in anti-clipping mode to set this to 0 dBfs, which corresponds to the maximum unclipped output power of a FFX amplifier. Since gain can be added digitally within the STA339BW it is possible to exceed 0 dBfs or any other LxAT setting, when this occurs, the limiter, when active, automatically starts reducing the gain. The rate at which the gain is reduced when the attack threshold is exceeded is dependent upon the attack rate register setting for that limiter. Gain reduction occurs on a peak-detect algorithm. Setting EATHx[7] bits to 1 selects the anti-clipping mode.

The limiter release thresholds are determined by the LxRT registers if ERTHx[7] bits are set to 0 else the thresholds are determined by ERTHx[6:0]. Settings to 1 ERTHx[7] bits the anti-clipping mode is selected automatically. The release of limiter, when the gain is again increased, is dependent on a RMS-detect algorithm. The output of the volume/limiter block is passed through a RMS filter. The output of this filter is compared to the release threshold, determined by the Release Threshold register. When the RMS filter output falls below the release threshold, the gain is again increased at a rate dependent upon the Release Rate register. The gain can never be increased past its set value and, therefore, the release only occurs if the limiter has already reduced the gain. The release threshold value can be used to set what is effectively a minimum dynamic range, this is helpful as over-limiting can reduce the dynamic range to virtually zero and cause program material to sound “lifeless”.

In AC mode, the attack and release thresholds are set relative to full-scale. In DRC mode, the attack threshold is set relative to the maximum volume setting of the channels mapped to that limiter and the release threshold is set relative to the maximum volume setting plus the attack threshold.

Figure 20. Basic limiter and volume flow diagram

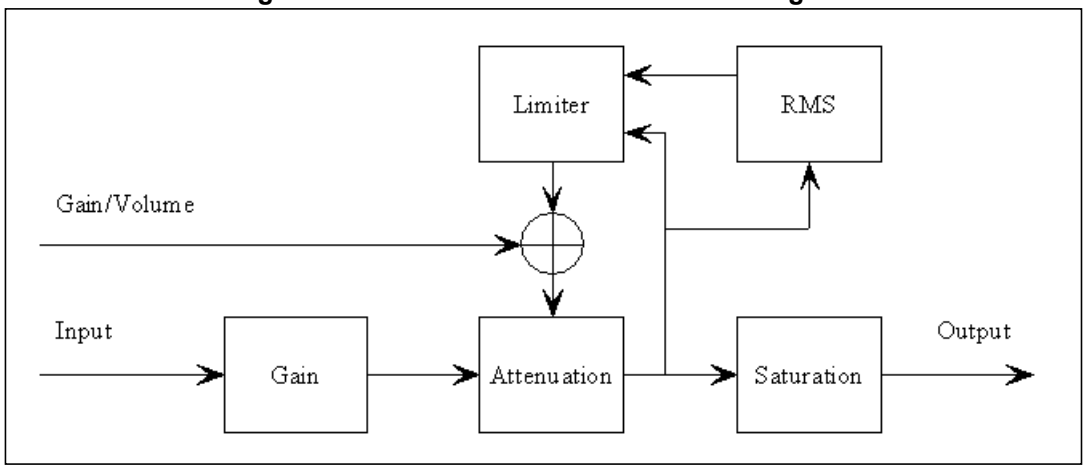


Table 67. Limiter attack rate as a function of LxA bits

LxA[3:0]	Attack Rate dB/ms	
0000	3.1584	Fast
0001	2.7072	
0010	2.2560	
0011	1.8048	
0100	1.3536	
0101	0.9024	
0110	0.4512	
0111	0.2256	
1000	0.1504	
1001	0.1123	
1010	0.0902	
1011	0.0752	
1100	0.0645	
1101	0.0564	
1110	0.0501	Slow
1111	0.0451	

Table 68. Limiter release rate as a function of LxR bits

LxR[3:0]	Release Rate dB/ms	
0000	0.5116	Fast
0001	0.1370	
0010	0.0744	
0011	0.0499	
0100	0.0360	
0101	0.0299	
0110	0.0264	
0111	0.0208	
1000	0.0198	
1001	0.0172	
1010	0.0147	
1011	0.0137	
1100	0.0134	
1101	0.0117	
1110	0.0110	Slow
1111	0.0104	

Anti-clipping mode

Table 69. Limiter attack threshold as a function of LxAT bits (AC mode)

LxAT[3:0]	AC (dB relative to fs)
0000	-12
0001	-10
0010	-8
0011	-6
0100	-4
0101	-2
0110	0
0111	+2
1000	+3
1001	+4
1010	+5
1011	+6
1100	+7
1101	+8
1110	+9
1111	+10

Table 70. Limiter release threshold as a function of LxRT bits (AC mode)

LxRT[3:0]	AC (dB relative to fs)
0000	-∞
0001	-29 dB
0010	-20 dB
0011	-16 dB
0100	-14 dB
0101	-12 dB
0110	-10 dB
0111	-8 dB
1000	-7 dB
1001	-6 dB
1010	-5 dB
1011	-4 dB
1100	-3 dB
1101	-2 dB
1110	-1 dB
1111	-0 dB

Dynamic range compression mode

Table 71. Limiter attack threshold as a function of LxAT bits (DRC mode)

LxAT[3:0]	DRC (dB relative to Volume)
0000	-31
0001	-29
0010	-27
0011	-25
0100	-23
0101	-21
0110	-19
0111	-17
1000	-16
1001	-15
1010	-14
1011	-13
1100	-12
1101	-10
1110	-7
1111	-4

Table 72. Limiter release threshold as a as a function of LxRT bits (DRC mode)

LxRT[3:0]	DRC (db relative to Volume + LxAT)
0000	-∞
0001	-38 dB
0010	-36 dB
0011	-33 dB
0100	-31 dB
0101	-30 dB
0110	-28 dB
0111	-26 dB
1000	-24 dB
1001	-22 dB
1010	-20 dB
1011	-18 dB
1100	-15 dB
1101	-12 dB
1110	-9 dB
1111	-6 dB

7.11.5 Limiter 1 Extended attack threshold (addr 0x32)

D7	D6	D5	D4	D3	D2	D1	D0
EATHEN1	EATH1[6]	EATH1[5]	EATH1[4]	EATH1[3]	EATH1[2]	EATH1[1]	EATH1[0]
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

The extended attack threshold value is determined as follows:

attack threshold = -12 + EATH1 / 4

7.11.6 Limiter 1 Extended release threshold (addr 0x33)

D7	D6	D5	D4	D3	D2	D1	D0
ERTHEN1	ERTH1[6]	ERTH1[5]	ERTH1[4]	ERTH1[3]	ERTH1[2]	ERTH1[1]	ERTH1[0]
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

The extended release threshold value is determined as follows:

release threshold = -12 + ERTH1 / 4

7.11.7 Limiter 2 Extended attack threshold (addr 0x34)

D7	D6	D5	D4	D3	D2	D1	D0
EATHEN2	EATH2[6]	EATH2[5]	EATH2[4]	EATH2[3]	EATH2[2]	EATH2[1]	EATH2[0]
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

The extended attack threshold value is determined as follows:

attack threshold = -12 + EATH2 / 4

7.11.8 Limiter 2 Extended release threshold (addr 0x35)

D7	D6	D5	D4	D3	D2	D1	D0
ERTHEN2	ERTH2[6]	ERTH2[5]	ERTH2[4]	ERTH2[3]	ERTH2[2]	ERTH2[1]	ERTH2[0]
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

The extended release threshold value is determined as follows:

release threshold = -12 + ERTH2 / 4

Note: Attack/release threshold step is 0.125 dB in the range -12 dB and 0 dB.

7.12 User-defined coefficient control registers (addr 0x16 - 0x26)

7.12.1 Coefficient address register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		CFA5	CFA4	CFA3	CFA2	CFA1	CFA0
0		0	0	0	0	0	0

7.12.2 Coefficient b1 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

7.12.3 Coefficient b1 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C1B15	C1B14	C1B13	C1B12	C1B11	C1B10	C1B9	C1B8
0	0	0	0	0	0	0	0

7.12.4 Coefficient b1 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C1B7	C1B6	C1B5	C1B4	C1B3	C1B2	C1B1	C1B0
0	0	0	0	0	0	0	0

7.12.5 Coefficient b2 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C2B23	C2B22	C2B21	C2B20	C2B19	C2B18	C2B17	C2B16
0	0	0	0	0	0	0	0

7.12.6 Coefficient b2 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C2B15	C2B14	C2B13	C2B12	C2B11	C2B10	C2B9	C2B8
0	0	0	0	0	0	0	0

7.12.7 Coefficient b2 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C2B7	C2B6	C2B5	C2B4	C2B3	C2B2	C2B1	C2B0
0	0	0	0	0	0	0	0

7.12.8 Coefficient a1 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C1B23	C1B22	C1B21	C1B20	C1B19	C1B18	C1B17	C1B16
0	0	0	0	0	0	0	0

7.12.9 Coefficient a1 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C3B15	C3B14	C3B13	C3B12	C3B11	C3B10	C3B9	C3B8
0	0	0	0	0	0	0	0

7.12.10 Coefficient a1 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C3B7	C3B6	C3B5	C3B4	C3B3	C3B2	C3B1	C3B0
0	0	0	0	0	0	0	0

7.12.11 Coefficient a2 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C4B23	C4B22	C4B21	C4B20	C4B19	C4B18	C4B17	C4B16
0	0	0	0	0	0	0	0

7.12.12 Coefficient a2 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C4B15	C4B14	C4B13	C4B12	C4B11	C4B10	C4B9	C4B8
0	0	0	0	0	0	0	0

7.12.13 Coefficient a2 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C4B7	C4B6	C4B5	C4B4	C4B3	C4B2	C4B1	C4B0
0	0	0	0	0	0	0	0

7.12.14 Coefficient b0 data register bits 23:16

D7	D6	D5	D4	D3	D2	D1	D0
C5B23	C5B22	C5B21	C5B20	C5B19	C5B18	C5B17	C5B16
0	0	0	0	0	0	0	0

7.12.15 Coefficient b0 data register bits 15:8

D7	D6	D5	D4	D3	D2	D1	D0
C5B15	C5B14	C5B13	C5B12	C5B11	C5B10	C5B9	C5B8
0	0	0	0	0	0	0	0

7.12.16 Coefficient b0 data register bits 7:0

D7	D6	D5	D4	D3	D2	D1	D0
C5B7	C5B6	C5B5	C5B4	C5B3	C5B2	C5B1	C5B0
0	0	0	0	0	0	0	0

7.12.17 Coefficient write/read control register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				RA	R1	WA	W1
0				0	0	0	0

Coefficients for user-defined EQ, mixing, scaling, and bass management are handled internally in the STA339BW via RAM. Access to this RAM is available to the user via an I^2C register interface. A collection of I^2C registers are dedicated to this function. One contains a coefficient base address, five sets of three store the values of the 24-bit coefficients to be written or that were read, and one contains bits used to control the write/read of the coefficient(s) to/from RAM.

Three different RAM banks are embedded in STA339BW. The three banks are managed in paging mode using EQCFG register bits. They can be used to store different EQ settings. For speaker frequency compensation, a sampling frequency independent EQ must be implemented. Computing three different coefficients set for 32 kHz, 44.1kHz, 48 kHz and downloading them into the three RAM banks, it is possible to select the suitable RAM block depending from the incoming frequency with a simple I^2C write operation on register 0x31.

For example, in case of different input sources (different sampling rates), the three different sets of coefficients can be downloaded once at the start up, and during the normal play it is possible to switch among the three RAM blocks allowing a faster operation, without any additional download from the microcontroller.

To write the coefficients in a particular RAM bank, this bank must be selected first writing bit 0 and bit 1 in register 0x31. Then the write procedure below can be used.

Note that as soon as a RAM bank is selected, the EQ settings are automatically switched to the coefficients stored in the active RAM block.

Note: The read write operation on RAM coefficients works only if RLCKI (pin29) is switching and stable (ref. Table 9, tLRJT timing) and PLL must be locked (ref bit D7 reg 0x2D).

Reading a coefficient from RAM

1. Select the RAM block with register 0x31 bit1, bit0.
2. Write 6 bits of address to I^2C register 0x16.
3. Write 1 to R1 bit in I^2C address 0x26.
4. Read top 8 bits of coefficient in I^2C address 0x17.
5. Read middle 8 bits of coefficient in I^2C address 0x18.
6. Read bottom 8 bits of coefficient in I^2C address 0x19.

Reading a set of coefficients from RAM

1. Select the RAM block with register 0x31 bit1, bit0.
2. Write 6 bits of address to I^2C register 0x16.
3. Write 1 to RA bit in I^2C address 0x26.
4. Read top 8 bits of coefficient in I^2C address 0x17.
5. Read middle 8 bits of coefficient in I^2C address 0x18.
6. Read bottom 8 bits of coefficient in I^2C address 0x19.
7. Read top 8 bits of coefficient b2 in I^2C address 0x1A.
8. Read middle 8 bits of coefficient b2 in I^2C address 0x1B.
9. Read bottom 8 bits of coefficient b2 in I^2C address 0x1C.
10. Read top 8 bits of coefficient a1 in I^2C address 0x1D.
11. Read middle 8 bits of coefficient a1 in I^2C address 0x1E.
12. Read bottom 8 bits of coefficient a1 in I^2C address 0x1F.
13. Read top 8 bits of coefficient a2 in I^2C address 0x20.
14. Read middle 8 bits of coefficient a2 in I^2C address 0x21.
15. Read bottom 8 bits of coefficient a2 in I^2C address 0x22.
16. Read top 8 bits of coefficient b0 in I^2C address 0x23.
17. Read middle 8 bits of coefficient b0 in I^2C address 0x24.
18. Read bottom 8 bits of coefficient b0 in I^2C address 0x25.

Writing a single coefficient to RAM

1. Select the RAM block with register 0x31 bit1, bit0.
2. Write 6 bits of address to I^2C register 0x16.
3. Write top 8 bits of coefficient in I^2C address 0x17.
4. Write middle 8 bits of coefficient in I^2C address 0x18.
5. Write bottom 8 bits of coefficient in I^2C address 0x19.
6. Write 1 to W1 bit in I^2C address 0x26.

Writing a set of coefficients to RAM

1. Select the RAM block with register 0x31 bit1, bit0.
2. Write 6 bits of starting address to I^2C register 0x16.
3. Write top 8 bits of coefficient b1 in I^2C address 0x17.
4. Write middle 8 bits of coefficient b1 in I^2C address 0x18.
5. Write bottom 8 bits of coefficient b1 in I^2C address 0x19.
6. Write top 8 bits of coefficient b2 in I^2C address 0x1A.
7. Write middle 8 bits of coefficient b2 in I^2C address 0x1B.
8. Write bottom 8 bits of coefficient b2 in I^2C address 0x1C.
9. Write top 8 bits of coefficient a1 in I^2C address 0x1D.
10. Write middle 8 bits of coefficient a1 in I^2C address 0x1E.
11. Write bottom 8 bits of coefficient a1 in I^2C address 0x1F.
12. Write top 8 bits of coefficient a2 in I^2C address 0x20.
13. Write middle 8 bits of coefficient a2 in I^2C address 0x21.
14. Write bottom 8 bits of coefficient a2 in I^2C address 0x22.
15. Write top 8 bits of coefficient b0 in I^2C address 0x23.
16. Write middle 8 bits of coefficient b0 in I^2C address 0x24.
17. Write bottom 8 bits of coefficient b0 in I^2C address 0x25.
18. Write 1 to WA bit in I^2C address 0x26.

The mechanism for writing a set of coefficients to RAM provides a method of updating the five coefficients corresponding to a given biquad (filter) simultaneously to avoid possible unpleasant acoustic side-effects. When using this technique, the 6-bit address specifies the address of the biquad b1 coefficient (for example, 0, 5, 10, 20, 35 decimal), and the STA339BW generates the RAM addresses as offsets from this base value to write the complete set of coefficient data.

7.12.18 User-defined EQ

The STA339BW can be programmed for four EQ filters (biquads) per each of the two input channels. The biquads use the following equation:

$Y[n] = 2 * (b_0 / 2) * X[n] + 2 * (b_1 / 2) * X[n-1] + b_2 * X[n-2] - 2 * (a_1 / 2) * Y[n-1] - a_2 * Y[n-2]$

$= b_0 * X[n] + b_1 * X[n-1] + b_2 * X[n-2] - a_1 * Y[n-1] - a_2 * Y[n-2]$

where Y[n] represents the output and X[n] represents the input. Multipliers are 24-bit signed fractional multipliers, with coefficient values in the range of 0x800000 (-1) to 0x7FFFFF (0.9999998808).

Coefficients stored in the user defined coefficient RAM are referenced in the following manner:

$CxHy0 = b_1 / 2$

$CxHy1 = b_2$

$CxHy2 = -a_1 / 2$

$CxHy3 = -a_2$

$CxHy4 = b_0 / 2$

where x represents the channel and the y the biquad number. For example, C2H41 is the b_2 coefficient in the fourth biquad for channel 2.

Additionally, the STA339BW can be programmed for a high-pass filter (processing channels 1 and 2) and a low-pass filter (processing channel 3) to be used for bass-management crossover when the XO setting is 000 (user-defined). Both of these filters when defined by the user (rather than using the preset crossover filters) are second order filters that use the biquad equation given above. They are loaded into the C12H0-4 and C3Hy0-4 areas of RAM noted in *Table 73*.

By default, all user-defined filters are pass-through where all coefficients are set to 0, except the $b_0/2$ coefficient which is set to 0x400000 (representing 0.5)

7.12.19 Prescale

The STA339BW provides a multiplication for each input channel for the purpose of scaling the input prior to EQ. This pre-EQ scaling is accomplished by using a 24-bit signed fractional multiplier, with 0x800000 = -1 and 0x7FFFFF = 0.9999998808. The scale factor for this multiplication is loaded into RAM using the same I^2C registers as the biquad coefficients and the bass management. All channels can use the channel-1 prescale factor by setting the Biquad link bit. By default, all prescale factors are set to 0x7FFFFF.

7.12.20 Postscale

The STA339BW provides one additional multiplication after the last interpolation stage and the distortion compensation on each channel. This postscaling is accomplished by using a 24-bit signed fractional multiplier, with 0x800000 = -1 and 0x7FFFFF = 0.9999998808. The scale factor for this multiply is loaded into RAM using the same I^2C registers as the biquad coefficients and the bass management. This postscale factor can be used in conjunction with an ADC equipped microcontroller to perform power-supply error correction. All channels can use the channel-1 postscale factor by setting the postscale link bit. By default, all postscale factors are set to 0x7FFFFF. When line output is being used, channel-3 postscale will affect both channels 3 and 4.

7.12.21 Overcurrent postscale

The STA339BW provides a simple mechanism for reacting to overcurrent detection in the power block. When the ocwarn input is asserted, the overcurrent postscale value is used in place of the normal postscale value to provide output attenuation on all channels. The default setting provides 3 dB of output attenuation when ocwarn is asserted.

The amount of attenuation to be applied in this situation can be adjusted by modifying the Overcurrent postscale value. As with the normal postscale, this scaling value is a 24-bit signed fractional multiplier, with 0x800000 = -1 and 0x7FFFFF = 0.9999998808. By default, the overcurrent postscale factor is set to 0x5A9DF7. Once the overcurrent attenuation is applied, it remains until the device is reset.

Table 73. RAM block for biquads, mixing, scaling and bass management

Index (decimal)	Index (hex)	RAM block setting	Coefficient	Default
0	0x00	Channel 1 - Biquad 1	C1H10(b1/2)	0x000000
1	0x01		C1H11(b2)	0x000000
2	0x02		C1H12(a1/2)	0x000000
3	0x03		C1H13(a2)	0x000000
4	0x04		C1H14(b0/2)	0x400000
5	0x05	Channel 1 - Biquad 2	C1H20	0x000000
…	…	…	…	…
19	0x13	Channel 1 - Biquad 4	C1H44	0x400000
20	0x14	Channel 2 - Biquad 1	C2H10	0x000000
21	0x15		C2H11	0x000000
…	…	…	…	…
39	0x27	Channel 2 - Biquad 4	C2H44	0x400000
40	0x28	Channel 1/2 - Biquad 5 for XO = 000 High-pass 2nd order filter for XO≠000	C12H0(b1/2)	0x000000
41	0x29		C12H1(b2)	0x000000
42	0x2A		C12H2(a1/2)	0x000000
43	0x2B		C12H3(a2)	0x000000
44	0x2C		C12H4(b0/2)	0x400000
45	0x2D	Channel 3 - Biquad for XO = 000 Low-pass 2nd order filter for XO≠000	C3H0(b1/2)	0x000000
46	0x2E		C3H1(b2)	0x000000
47	0x2F		C3H2(a1/2)	0x000000
48	0x30		C3H3(a2)	0x000000
49	0x31		C3H4(b0/2)	0x400000
50	0x32	Channel 1 - Prescale	C1PreS	0x7FFFFF
51	0x33	Channel 2 - Prescale	C2PreS	0x7FFFFF
52	0x34	Channel 1 - Postscale	C1PstS	0x7FFFFF
53	0x35	Channel 2 - Postscale	C2PstS	0x7FFFFF
54	0x36	Channel 3 - Postscale	C3PstS	0x7FFFFF

Table 73. RAM block for biquads, mixing, scaling and bass management (continued)

Index (decimal)	Index (hex)	RAM block setting	Coefficient	Default
55	0x37	TWARN/OC - Limit	TWOCL	0x5A9DF7
56	0x38	Channel 1 - Mix 1	C1MX1	0x7FFFFF
57	0x39	Channel 1 - Mix 2	C1MX2	0x000000
58	0x3A	Channel 2 - Mix 1	C2MX1	0x000000
59	0x3B	Channel 2 - Mix 2	C2MX2	0x7FFFFF
60	0x3C	Channel 3 - Mix 1	C3MX1	0x400000
61	0x3D	Channel 3 - Mix 2	C3MX2	0x400000
62	0x3E	Unused	-	-
63	0x3F	Unused	-	-

7.13 Variable max power correction registers (addr 0x27 - 0x28)

D7	D6	D5	D4	D3	D2	D1	D0
MPCC15	MPCC14	MPCC13	MPCC12	MPCC11	MPCC10	MPCC9	MPCC8
0	0	0	1	1	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
MPCC7	MPCC6	MPCC5	MPCC4	MPCC3	MPCC2	MPCC1	MPCC0
1	1	0	0	0	0	0	0

MPCC bits determine the 16 MSBs of the MPC compensation coefficient. This coefficient is used in place of the default coefficient when MPCV = 1.

7.14 Variable distortion compensation registers (addr 0x29 - 0x2A)

D7	D6	D5	D4	D3	D2	D1	D0
DCC15	DCC14	DCC13	DCC12	DCC11	DCC10	DCC9	DCC8
1	1	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0
0	0	1	1	0	0	1	1

DCC bits determine the 16 MSBs of the Distortion compensation coefficient. This coefficient is used in place of the default coefficient when DCCV = 1.

7.15 Fault detect recovery constant registers (addr 0x2B - 0x2C)

D7	D6	D5	D4	D3	D2	D1	D0
FDRC15	FDRC14	FDRC13	FDRC12	FDRC11	FDRC10	FDRC9	FDRC8
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
FDRC7	FDRC6	FDRC5	FDRC4	FDRC3	FDRC2	FDRC1	FDRC0
0	0	0	0	1	1	0	0

FDRC bits specify the 16-bit fault detect recovery time delay. When FAULT is asserted, the TRISTATE output is immediately asserted low and held low for the time period specified by this constant. A constant value of 0x0001 in this register is approximately 0.083 ms. The default value of 0x000C gives approximately 0.1 ms.

7.16 Device status register (addr 0x2D)

D7	D6	D5	D4	D3	D2	D1	D0
PLLUL	FAULT	UVFAULT	OVFAULT	OCFAULT	OCWARN	TFAULT	TWARN

This read-only register provides fault- and thermal-warning status information from the power control block. Logic value 1 for faults or warning means normal state. Logic 0 means a fault or warning has been detected on the power bridge. The PLLUL = 1 means that the PLL is not locked.

Table 74. Status register bits

Bit	R/W	RST	Name	Description
7	R	-	PLLUL	0: PLL locked 1: PLL not locked
6	R	-	FAULT	0: fault detected on power bridge 1: normal operation
5	R	-	UVFAULT	0: VCCxX internally detected 1: undervoltage threshold
4	R	-	OVFAULT	0: VCCxX internally detected 1: overvoltage threshold
3	R	-	OCFAULT	0: overcurrent fault detected
2	R	-	OCWARN	0: overcurrent warning
1	R	-	TFAULT	0: thermal fault, junction temperature over limit
0	R	-	TWARN	0: thermal warning, junction temperature is close to fault condition

7.17 EQ coefficients and DRC configuration register (addr 0x31)

D7	D6	D5	D4	D3	D2	D1	D0
XOB	Reserved		AMGC[3]	AMGC[2]	Reserved	SEL[1]	SEL[0]
0	0	0	0	0	0	0	0

Table 75. EQ RAM select

SEL[1:0]	EQ RAM bank selected
00/11	Bank 0 activated
01	Bank 1 activated
10	Bank 2 activated

Bits AMGC[3:2] change the behavior of the bits AMGC[1:0] as given in *Table 76* below.

Table 76. Anti-clipping and DRC preset

AMGC[3:2]	Anti-clipping and DRC preset selected
00	DRC/Anti-clipping behavior described in *Table 56 on page 48* (default).
01	DRC/Anti-clipping behavior is described in *Table 77* below
10/11	Reserved, do not use

When AMGC[3:2] = 01 then the bits 1:0 are defined as given here in *Table 77*.

Table 77. Anti-clipping selection for AMGC[3:2] = 01

AMGC[1:0]	Mode
00	AC0, stereo anticlipping 0 dB limiter
01	AC1, stereo anticlipping +1.25 dB limiter
10	AC2, stereo anticlipping +2 dB limiter
11	Reserved do not use

AC0, AC1, AC2 settings are designed for the loudspeaker protection function, limiting at the minimum any audio artefacts introduced by typical anti-clipping/DRC algorithms. More detailed information is available in the applications notes “Configurable output power rate using STA335BW” and “STA335BWS vs STA335BW”.

Bit XOB can be used to bypass the crossover filters. Logic 1 means that the function is not active. In this case, high pass crossover filter works as a passtrough on the data path (b0 = 1, all the other coefficients at logic 0) while the low pass filter is configured to have zero signal on channel-3 data processing (all the coefficients are at logic 0).

7.18 Extended configuration register (addr 0x36)

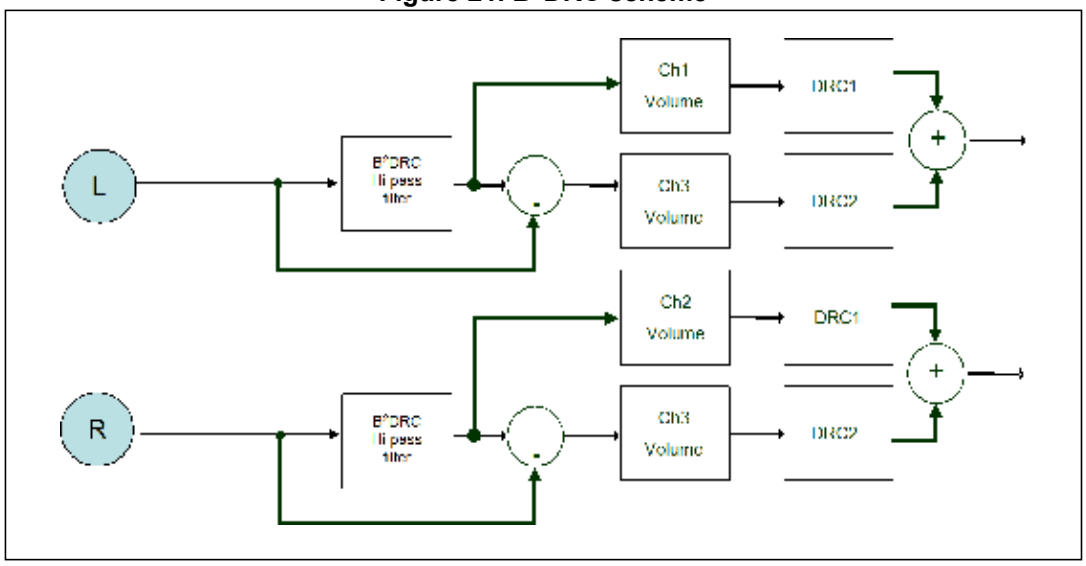
D7	D6	D5	D4	D3	D2	D1	D0
Mdrc[1]	Mdrc[0]	PS48DB	XAR1	XAR2	BQ5	BQ6	BQ7
0	0	0	0	0	0	0	0

Extended configuration register provides access to B^{2}DRC and biquads 5, 6 and 7.

7.18.1 Dual-band DRC

The STA339BW provides a dual-band DRC (B^{2}DRC) on the left- and right-channel data path, as depicted in *Figure 21*. Dual-band DRC is activated by setting MDRC[1:0] = 1x.

Figure 21. B^{2}DRC scheme



The low-frequency information (LFE) is extracted from the left and right channels by removing the high frequencies with a programmable Biquad filter, so that, using the original signal, the difference signal can be computed. Limiter 1 (DRC1) is then used to control the left and right high-frequency component amplitudes while limiter 2 (DRC2) is used to control the low-frequency components (see *Chapter 7.11*).

The cutoff frequency of the high-pass filters can be user defined, XO[3:0] = 0, or selected from the pre-defined values.

DRC1 and DRC2 are then used to independently limit the left- and right-channel high frequencies and the LFE-channel amplitude (see *Chapter 7.11*) as well as their volume control. Note that, in this configuration, the dedicated channel-3 volume control can actually be used as a bass boost enhancer as well (0.5 dB/step resolution).

The processed LFE channel is then recombined with the L and R channels in order to reconstruct the 2.0 output signal.

Sub band decomposition

The sub band decomposition for B^{2}DRC can be configured specifying the cutoff frequency. The cut off frequency can be programmed in two ways, using XO bits in register 0x0C, or using “user programmable” mode (coefficients stored in RAM adresses 0x28 to 0x31).

For the user programmable mode, use the formulae below to compute the high pass filters:

b0 = (1 + alpha) / 2 a0 = 1

b1 = -(1 + alpha) / 2 a1 = -alpha

b2 = 0 a2 = 0

where alpha = (1-sin(ω_0))/cos(ω_0), and ω_0 is the cutoff frequency.

A first-order filter is suggested to guarantee that for every ω_0 the corresponding low-pass filter obtained as difference (as shown in *Figure 21*) will have a symmetric (relative to HP filter) frequency response, and the corresponding recombination after the DRC has low ripple. Second-order filters can be used as well, but in this case the filter shape must be carefully choosen to provide good low pass response and minimum ripple recombination. For second-order is not possible to give a closed formula to get the best coefficients, but empirical adjustment should be done.

DRC settings

The DRC blocks used by B^2DRC are the same as those described in *Chapter 7.11*. B^2DRC configure automatically the DRC blocks in anticlipping mode. Attack and release thresholds can be selected using registers 0x32, 0x33, 0x34, 0x35, while attack and release rates are configured by registers 0x12 and 0x14.

Band downmixing

The low-frequency band is down-mixed to the left and right channels at the B^2DRC output. Channel volume can be used to weight the bands recombination to fine tune the overall frequency response.

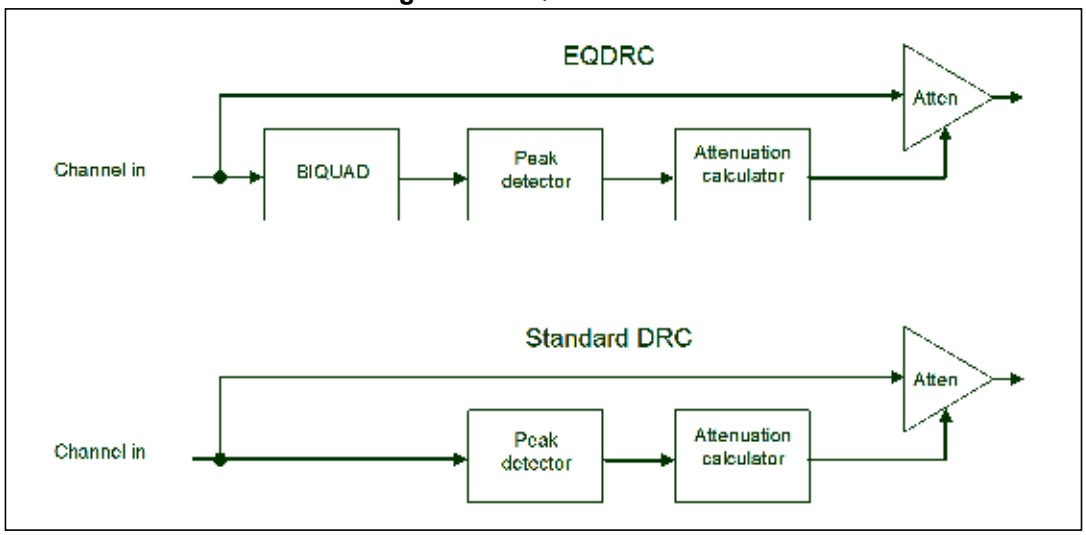
7.18.2 EQ DRC mode

Setting MDRC = 01, it is possible to add a programmable biquad (the XO biquad at RAM addresses 0x28 to 0x2C is used for this purpose) to the Limiter/compressor measure path (side chain). Using EQDRC the peak detector input can be shaped in frequency using the programmable biquad. For example if a +2 dB bass boost is applied (using a low shelf filter for example), the effect is that the EQDRC out will limit bass frequencies to -2 dB below the selected attack treshold.

Generally speaking, if the biquad boosts frequency f with an amount of X dB, the level of a compressed sinusoid at the output will be TH - X, where TH is the selected attack threshold.

Note: EQDRC works only if the biquad frequency response magnitude is >= 0 dB for every frequency.

Figure 22. EQDRC scheme



7.18.3 Extended post scale range

Table 78. Post scale setup

PS48DB	Mode
0	Postscale value is applied as defined in coefficient RAM
1	Postscale value is applied with +48-dB offset with respect to the coefficient RAM value

Post scale is an attenuation by default. When PS48DB is set to 1, a 48-dB offset is applied to the configured word, so postscale can act as a gain too.

7.18.4 Extended attack rate

The attack rate shown in *Table 67* can be extended to provide up to 8 dB/ms attack rate on both limiters.

Table 79. Extended attack rate setup for limiter 1

XAR1	Mode
0	Limiter1 attack rate is configured using *Table 67*
1	Limiter1 attack rate is 8 dB/ms

Table 80. Extended attack rate setup for limiter 2

XAR2	Mode
0	Limiter2 attack rate is configured using *Table 67*
1	Limiter2 attack rate is 8 dB/ms

7.18.5 Extended BIQUAD selector

De-ephasis filter as well as bass and treble controls can be configured as user defined filters when equalization coefficients link is activated (BQL = 1) and the corresponding BQx bit is set to 1.

Table 81. De-emphasis filter setup

BQ5	Mode
0	Preset de-emphasis filter selected
1	User defined biquad 5 coefficients are selected

Table 82. Bass filter setup

BQ6	Mode
0	Preset bass filter selected as per *Table 66*
1	User defined biquad 6 coefficients are selected

Table 83. Treble filter setup

BQ7	Mode
0	Preset treble filter selected as per *Table 66*
1	User defined biquad 7 coefficients are selected

When filters from 5th to 7th are configured as user-programmable, the corresponding coefficients are stored respectively in addresses 0x20-0x24 (BQ5), 0x25-0x29 (BQ6), 0x2A-0x2E (BQ7) as in *Table 73*.

Note: BQx bits are ignored if BQL = 0 or if DEMP = 1 (relevant for BQ5) or CxTCB = 1 (relevant for BQ6 and BQ7).

7.19 EQ soft volume configuration registers (addr 0x37 - 0x38)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		SVUPE	SVUP[4]	SVUP[3]	SVUP[2]	SVUP[1]	SVUP[0]
0	0	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		SVDWE	SVDW4]	SVDW[3]	SVDW[2]	SVDW[1]	SVDW[0]
0	0	0	0	0	0	0	0

Soft volume update has a fixed rate by default. Using register 0x37 and 0x38 it is possible to override the default behavior allowing different volume change rates.

It is also possible to independently define the fade-in (volume is increased) and fade-out (volume is decreased) rates according to the desired behavior.

Table 84. Soft volume (increasing) setup

SVUPE	Mode
0	When volume is increased, use the default rate
1	When volume is increased, use the rates defined by SVUP[4:0] .

When SVUPE = 1 the fade-in rate is defined by the SVUP[4:0] bits according to the formula:

Fade-in rate = 48 / (SVUP[4:0] + 1) dB/ms.

Table 85. Soft volume (decreasing) setup

SVDWE	Mode
0	When volume is decreased, use the default rate
1	When volume is decreased, use the rates defined by SVDW[4:0] .

When SVDWE = 1 the fade-out rate is defined by the SVDW[4:0] bits according to the formula:

Fade-in rate = 48 / (SVDW[4:0] + 1) dB/ms.

7.20 DRC RMS filter coefficients (addr 0x39 - 0x3E)

D7	D6	D5	D4	D3	D2	D1	D0
R_C0[23]	R_C0[22]	R_C0[21]	R_C0[20]	R_C0[19]	R_C0[18]	R_C0[17]	R_C0[16]
0	0	0	0	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
R_C0[15]	R_C0[14]	R_C0[13]	R_C0[12]	R_C0[11]	R_C0[10]	R_C0[9]	R_C0[8]
1	1	1	0	1	1	1	0

D7	D6	D5	D4	D3	D2	D1	D0
R_C0[7]	R_C0[6]	R_C0[5]	R_C0[4]	R_C0[3]	R_C0[2]	R_C0[1]	R_C0[0]
1	1	1	1	1	1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
R_C1[23]	R_C1[22]	R_C1[21]	R_C1[20]	R_C1[19]	R_C1[18]	R_C1[17]	R_C1[16]
0	1	1	1	1	1	1	0

D7	D6	D5	D4	D3	D2	D1	D0
R_C1[15]	R_C1[14]	R_C1[13]	R_C1[12]	R_C1[11]	R_C1[10]	R_C1[9]	R_C1[8]
1	1	0	0	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
R_C1[7]	R_C1[6]	R_C1[5]	R_C1[4]	R_C1[3]	R_C1[2]	R_C1[1]	R_C1[0]
0	0	1	0	0	1	1	0

Signal level detection in DRC algorithm is computed usign the following formula:

y(t) = c0 * abs(x(t)) + c1 * y(t-1)

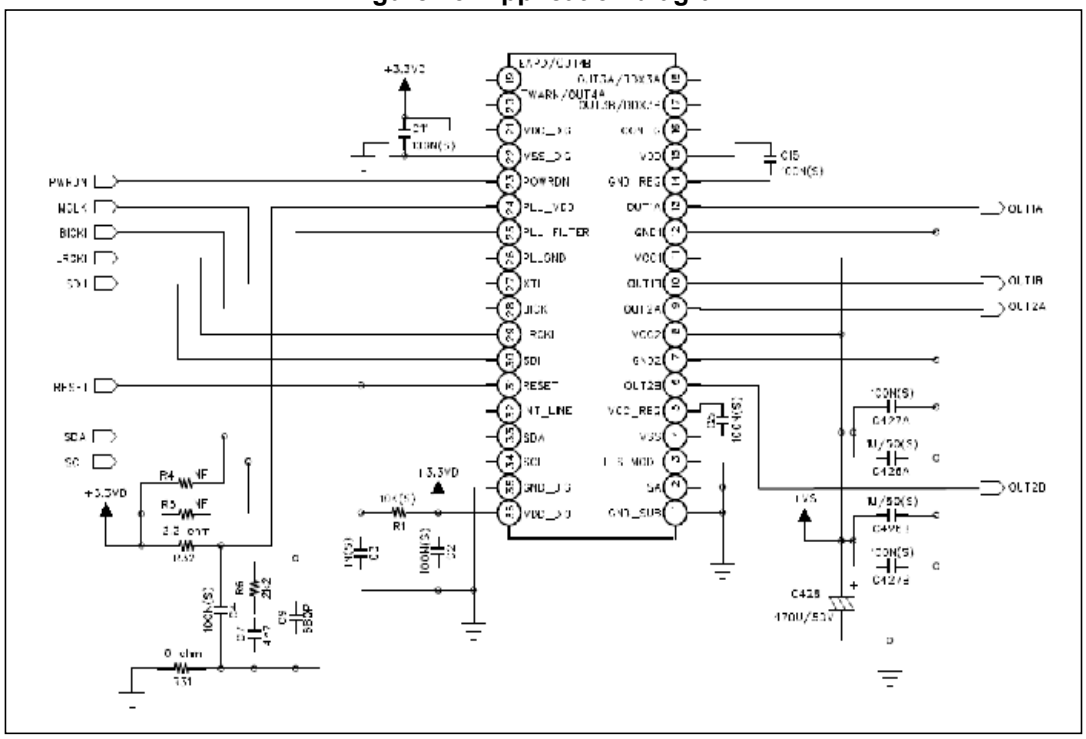
where x(t) represents the audio signal applied to the limiter, and y(t) the measured level.

8 Application

8.1 Application scheme for power supplies

Here in *Figure 23* below is the typical application diagram for STA339BW showing the power supply decoupling. Particular care has to be taken with the layout of the PCB. In particular the 3.3 Ω resistors on the digital supplies (VDD_DIG) have to be placed as close as possible to the device. This helps to prevent unwanted oscillation in the digital part of the device due to the inductive tracks of the PCB. The same rule also applies to all the decoulpling capacitors in order to limit spikes on all the supplies.

Figure 23. Application diagram



8.2 PLL filter

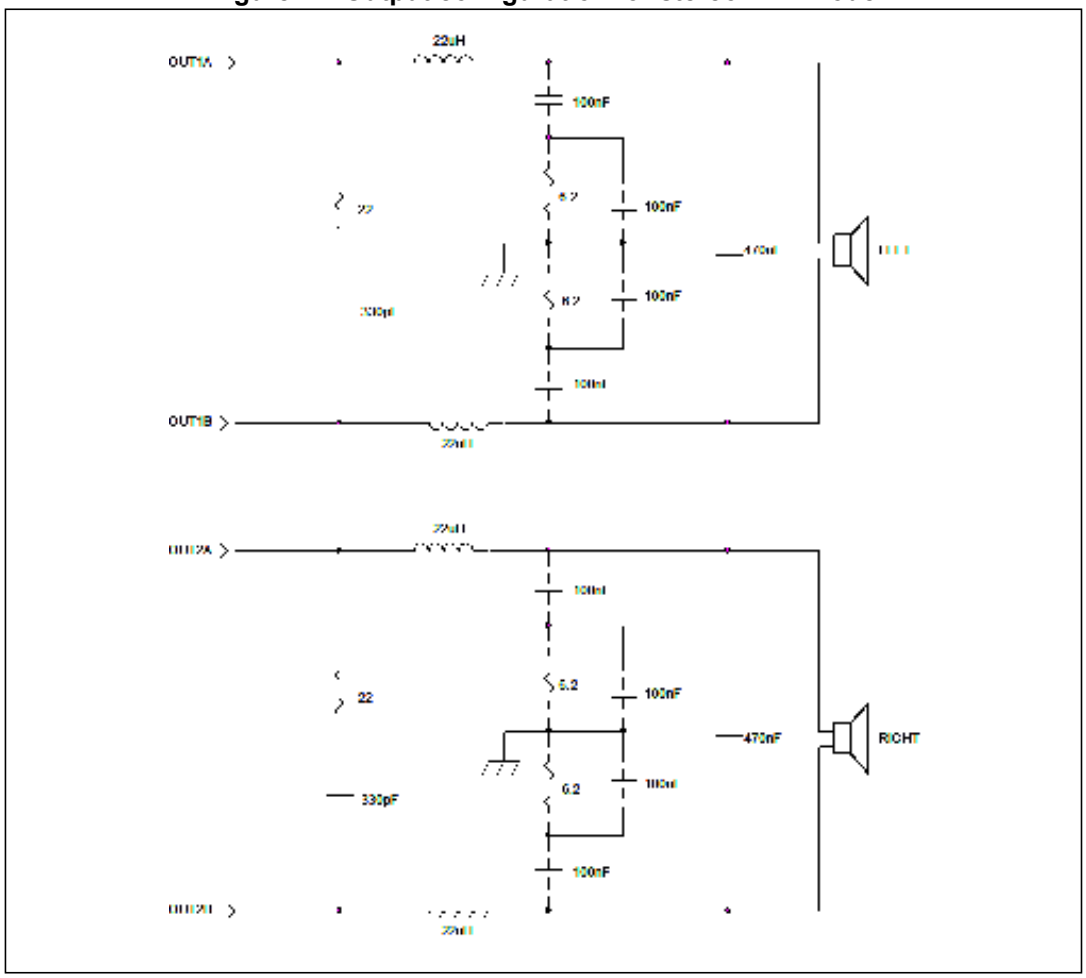
It is recommended to use the above scheme and values for the PLL filter to achieve the best performance from the device in general applications. Note that the ground of this filter circuit has to be connected to the ground of the PLL without any resistive path.

Concerning the component values, remember that the greater is the filter bandwidth, the less is the lock time but the higher is the PLL output jitter.

8.3 Typical output configuration

Here after the typical output configuration used for BTL stereo mode. Please refer to the application note for all the other possible output configuration recommended schematics.

Figure 24. Output configuration for stereo BTL mode



9 Package thermal characteristics

Using a double-layer PCB the thermal resistance junction to ambient with 2 copper ground areas of 3 x 3 cm^2 and with 16 via holes (see *Figure 25*) is 24 °C/W in natural air convection.

The dissipated power within the device depends primarily on the supply voltage, load impedance and output modulation level.

Thus, the maximum estimated dissipated power for the STA339BW is:

2 x 20 W @ 8 Ω, 18 V	Pd max ~ 4 W
2 x 10 W + 1 x 20 W @ 4 Ω, 8 Ω, 18 V	Pd max < 5 W

Figure 25. Double-layer PCB with 2 copper ground areas and 16 via holes

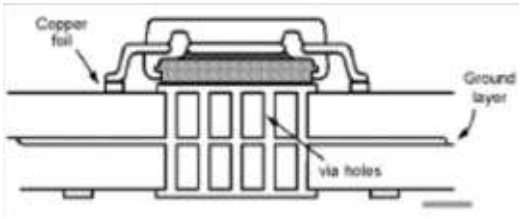
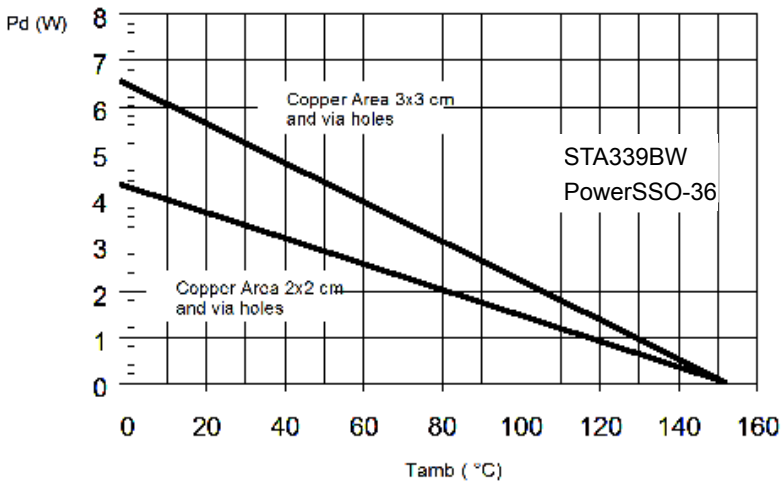


Figure 26 shows the power derating curve for the PowerSSO-36 slug-down package on PCBs with copper areas of 2 x 2 cm^2 and 3 x 3 cm^2.

Figure 26. PowerSSO-36 power derating curve



10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 27 shows the package outline and *Table 86* gives the dimensions of the PowerSSO-36 package with exposed pad (slug) down (EPD).

Table 86. PowerSSO-36 EPD dimensions

Symbol	Dimensions in mm			Dimensions in inches		
	Min	Typ	Max	Min	Typ	Max
A	2.15	-	2.47	0.085	-	0.097
A2	2.15	-	2.40	0.085	-	0.094
a1	0	-	0.10	0	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	-
e3	-	8.5	-	-	0.335	-
F	-	2.3	-	-	0.091	-
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398	-	0.413
h	-	-	0.40	-	-	0.016
k	0	-	8 degrees	-	-	8 degrees
L	0.60	-	1.00	0.024	-	0.039
M	-	4.30	-	-	0.169	-
N	-	-	10 degrees	-		10 degrees
O	-	1.20	-	-	0.047	-
Q	-	0.80	-	-	0.031	-
S	-	2.90	-	-	0.114	-
T	-	3.65	-	-	0.144	-
U	-	1.00	-	-	0.039	-
X	4.10	-	4.70	0.161	-	0.185
Y	4.90	-	7.10	0.193	-	0.280

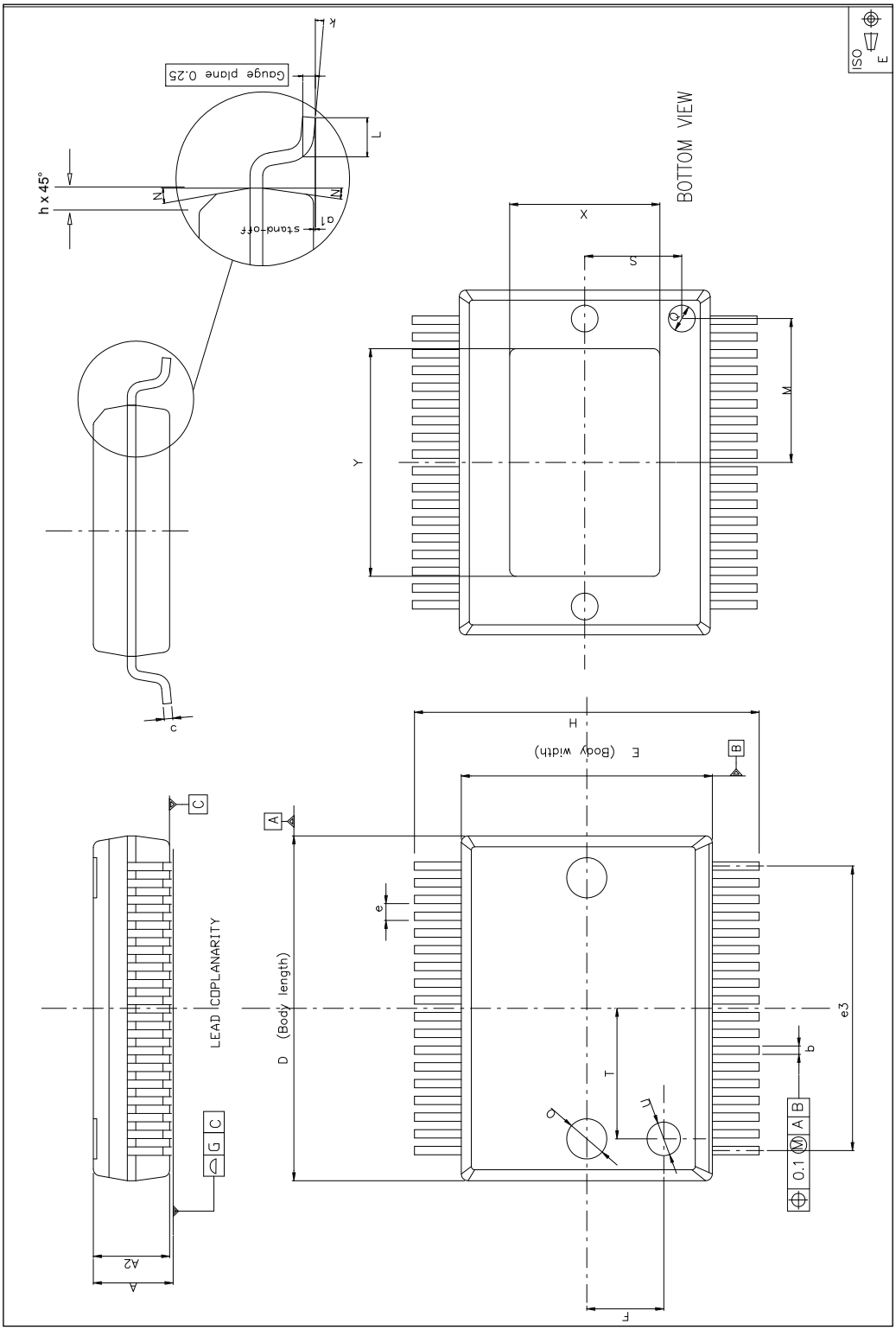


Figure 27. PowerSSO-36 EPD outline drawing

11 Revision history

Table 87. Document revision history

Date	Revision	Changes
09-Dec-2008	1	Initial release
16-Feb-2009	2	Updated names/descriptions for pins 17-20 in *Chapter 2 on page 12* Added cross reference to I^2S interface setup in *Section 3.6: Power on/off sequence on page 18* Updated text and *Figure 23: Application diagram on page 72* Updated *Section 8.2: PLL filter on page 72*
01-Apr-2009	3	Updated Y dimension in *Table 86: PowerSSO-36 EPD dimensions on page 75*
15-May-2009	4	Updated *Chapter 1 on page 10* to “8 programmable 28-bit biquads” Updated I_{il} and I_{ih} in *Table 6: Electrical specifications - digital section on page 15* Updated I_{lim} and I_{sc} in *Table 7: Electrical specifications - power section on page 16* Updated register FDRC addresses in *Section 7.1.5: Fault detect recovery bypass on page 30* Updated bits 4 and 5 in *Table 74: Status register bits on page 65*.
04-Aug-2010	5	Updated order code in *Table 1: Device summary on page 1* Updated name of *Chapter 10 on page 75* to *Package mechanical data*
18-Sep-2013	6	Added *Section 4 on page 20* Modified *Note:: The read write operation on RAM coefficients works only if RLCKI (pin29) is switching and stable (ref. Table 9, tLRJT timing) and PLL must be locked (ref bit D7 reg 0x2D). on page 60* Updated Company information appearing on last page of document
13-Feb-2014	7	Updated order code in *Table 1 on page 1*
05-Jan-2015	8	Updated I_{lim} in *Table 7: Electrical specifications - power section*

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