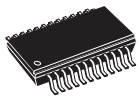
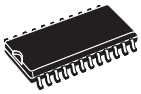
STP16CPC05

Datasheet

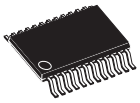
Low voltage 16-bit constant current LED sink driver with balanced output rise/fall time



QSOP-24



SO-24



TSSOP24



TSSOP24
(exposed pad)

Maturity status link
STP16CPC05

Features

- Low voltage power supply down to 3 V
- 16 constant current output channels
- Adjustable output current through external resistor
- Serial data IN/parallel data OUT
- Can be driven by a 3.3 V microcontroller
- Output current: 5 - 100 mA
- Max clock frequency 30 MHz
- ESD protection 2.5 kV HBM, 200 V MM

Description

The STP16CPC05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The STP16CPC05 contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bit, D-type storage register. In the output stage, sixteen regulated current sources provide from 5 mA to 100 mA constant current to drive the LEDs. The STP16CPC05`s output stage is designed to optimize the turn-on and turn-off time, typically 100 nS. The balanced turning ON/OFF improves the system performances reducing the bypass capacitance in applications where parasitic inductance generate ringing or noise in the system. The LEDs' brightness can be controlled by using an external resistor to adjust the STP16CPC05 output current. The STP16CPC05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, makes the device suitable for high data rate transmission. The 3.3 V voltage supply is useful in applications that interface with a 3.3 V microcontroller.

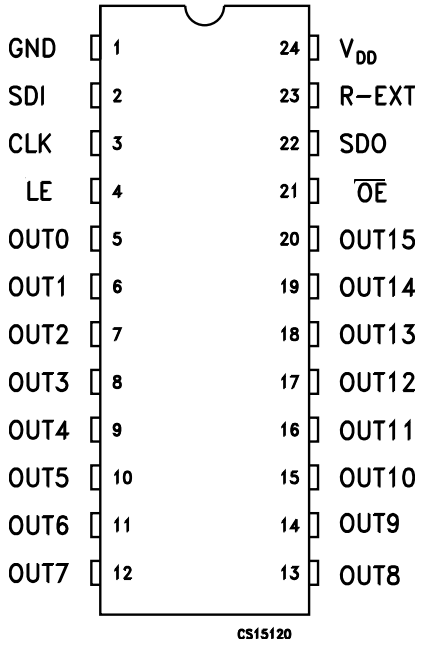
1 Summary description

Table 1. Typical current accuracy

Output voltage	Current accuracy		Output current	V_{DD}	Temperature
	Between bits	Between ICs			
≥ 1.3 V	± 1.5 %	± 5 %	≥20 to 100 mA	3.3 V to 5 V	25 °C

1.1 Pin connection and description

Figure 1. Pin connection



GIPD140320161440MT

Note: The exposed pad should be electrically connected to a metal land electrically isolated or connected to ground.

Table 2. Pin description

Pin n°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5 - 20	OUT 0 - 15	Output terminal
21	$\overline{OE}$	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal for an external resistor for constant current programming
24	V_{DD}	Supply voltage terminal

2 Electrical ratings

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	100	mA
V_I	Input voltage	-0.4 to V_{DD}+0.4	V
I_{GND}	GND terminal current	1600	mA
f_{CLK}	Clock frequency	50	MHz

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter		Value	Unit
T_{OPR}	Operating temperature range		-40 to +125	°C
T_{STG}	Storage temperature range		-55 to +150	°C
R_{thja}	Thermal resistance junction-ambient	SO-24	60	°C/W
		TSSOP24	85	°C/W
		TSSOP24 exposed pad(1)	37.5	°C/W
		QSOP-24	72	°C/W

1. *The exposed pad should be soldered directly to the PCB to realize the thermal benefits.*

2.3 Recommended operating conditions

Table 5. Recommended operating conditions T_A = 25 °C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.0	-	5.5	V
V_O	Output voltage			-	20	V
I_O	Output current	OUTn	3	-	100	mA
I_{OH}	Output current	SERIAL-OUT		-	+1	mA
I_{OL}	Output current	SERIAL-OUT		-	-1	mA
V_{IH}	Input voltage		0.7 V_{DD}	-	V_{DD}+0.3	V
V_{IL}	Input voltage		-0.3	-	0.3 V_{DD}	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{wLAT}	LE pulse width	V_{DD} = 3.0 V to 5.0 V	20	-		ns
t_{wCLK}	CLK pulse width		16	-		ns
t_{wEN}	OE pulse width		200	-		ns
$t_{SETUP(D)}$	Setup time for DATA		8	-		ns
$t_{HOLD(D)}$	Hold time for DATA		4	-		ns
$t_{SETUP(L)}$	Setup time for LATCH		5	-		ns
f_{CLK}	Clock frequency	Cascade operation V_{DD} = 5 V (1)		-	30	MHz

1. *If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please consider the timings carefully.*

3 Electrical characteristics

V_{DD} = 3.3 V to 5 V, T_A = 25 °C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input voltage high level		0.7 V_{DD}		V_{DD}	V
V_{IL}	Input voltage low level		GND		0.3 V_{DD}	V
I_{OH}	Output leakage current	V_{OH} = 20 V			10	µA
V_{OL}	Output voltage (serial-OUT)	I_{OL} = 1 mA			0.4	V
V_{OH}	Output voltage (serial-OUT)	I_{OH} = -1 mA	V_{DD}-0.4 V			V
I_{OL1}	Output current	V_O = 0.3 V, R_{ext} = 4.2 kΩ	4.25	5	5.75	mA
I_{OL2}		V_O = 0.3 V, R_{ext} = 1 kΩ	19	20	21	
I_{OL3}		V_O = 1.3 V, R_{ext} = 200 Ω	96	100	104	
ΔI_{OL1}	Output current error between bit (all output ON)	V_O = 0.3 V, R_{ext} = 4.2 kΩ		± 5	± 8	%
ΔI_{OL2}		V_O = 0.3 V, R_{ext} = 1 kΩ		± 1.5	± 3	
ΔI_{OL3}		V_O = 1.3 V, R_{ext} = 200 Ω		± 1.2	± 3	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	kΩ
$R_{SIN(down)}$	Pull-down resistor		100	200	400	kΩ
$I_{DD(OFF1)}$	Supply current (OFF)	R_{ext} = 1 kΩ, OUT 0 to 15 = OFF		4		mA
$I_{DD(OFF2)}$		R_{ext} = 250 Ω, OUT 0 to 15 = OFF		11.2		
$I_{DD(ON1)}$	Supply current (ON)	R_{ext} = 1 kΩ, OUT 0 to 15 = ON		4.5		
$I_{DD(ON2)}$		R_{ext} = 250 Ω, OUT 0 to 15 = ON		11.7		
Thermal	Thermal protection			170		°C

V_{DD} = 5 V, T_A = 25 °C, unless otherwise specified.

Table 7. Switching characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
t_{PLH1}	CLK-$\overline{OUTn}$, LE = H, $\overline{OE}$ = L Propagation delay time,	$V_{IH} = V_{DD}$ V_{IL} = GND C_L = 10 pF I_O = 20 mA V_L = 3.0 V R_{EXT} = 1 KΩ R_L = 60 Ω	V_{DD} = 3.3 V	-	175	227	ns
			V_{DD} = 5 V	-	159	206	
t_{PLH2}	LE-$\overline{OUTn}$, $\overline{OE}$ = L Propagation delay time,		V_{DD} = 3.3 V	-	176	228	ns
			V_{DD} = 5 V	-	158	205	
t_{PLH3}	$\overline{OE}$ - $\overline{OUTn}$, LE = H Propagation delay time,		V_{DD} = 3.3 V	-	235	305	ns
			V_{DD} = 5 V	-	192	250	
t_{PLH}	CLK-SDO Propagation delay time,		V_{DD} = 3.3 V	-	20	26	ns
			V_{DD} = 5 V	-	14	18	
t_{PHL1}	CLK-$\overline{OUTn}$, LE = H, $\overline{OE}$ = L Propagation delay time,		V_{DD} = 3.3 V	-	70	91	ns
			V_{DD} = 5 V	-	68	88	
t_{PHL2}	LE-$\overline{OUTn}$, $\overline{OE}$ = L Propagation delay time,		V_{DD} = 3.3 V	-	56	73	ns
			V_{DD} = 5 V	-	54	70	
t_{PHL3}	$\overline{OE}$ - $\overline{OUTn}$, LE = H Propagation delay time,		V_{DD} = 3.3 V	-	102	132	ns
			V_{DD} = 5 V	-	100	130	
t_{PHL}	CLK-SDO Propagation delay time,		V_{DD} = 3.3 V	-	25	32	ns
			V_{DD} = 5 V	-	17	22	
t_{ON}	Output rise time 10~90% of voltage waveform		V_{DD} = 3.3 V	-	116	150	ns
			V_{DD} = 5 V	-	108	140	
t_{OFF}	Output fall time 90~10% of voltage waveform		V_{DD} = 3.3 V	-	80	104	ns
			V_{DD} = 5 V	-	80	104	
t_r	CLK rise time (1)			-		5000	ns
t_f	CLK fall time (1)			-		5000	ns

1. *In order to achieve high cascade data transfer, please consider tr/tf timings carefully.*

4 Equivalent circuit and outputs

Figure 2. $\overline{OE}$ terminal

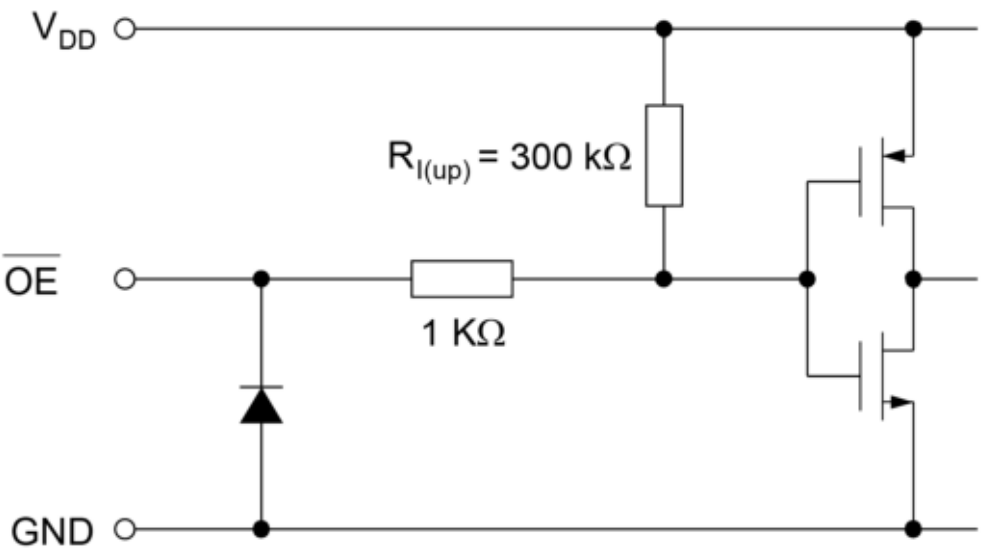


Figure 3. LE terminal

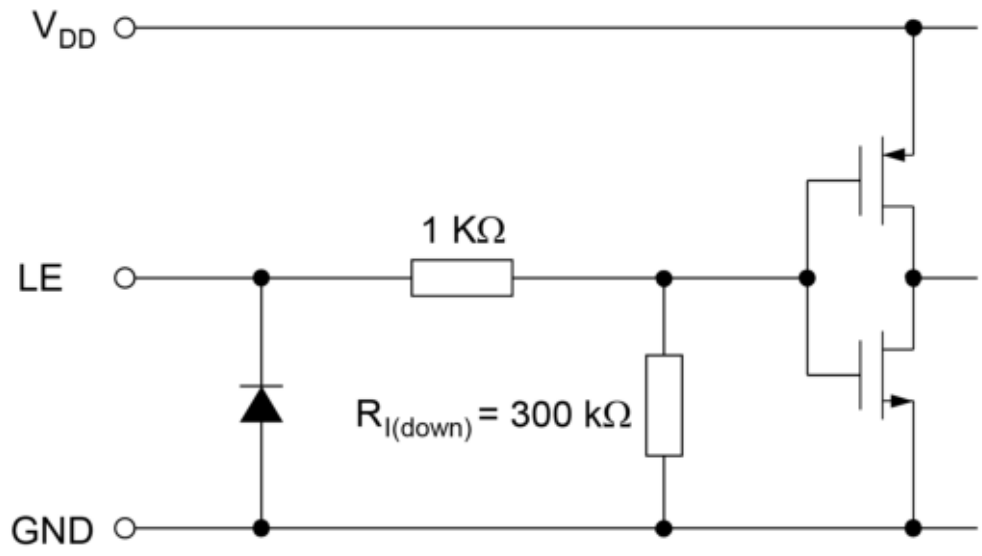


Figure 4. **CLK, SDI terminal**

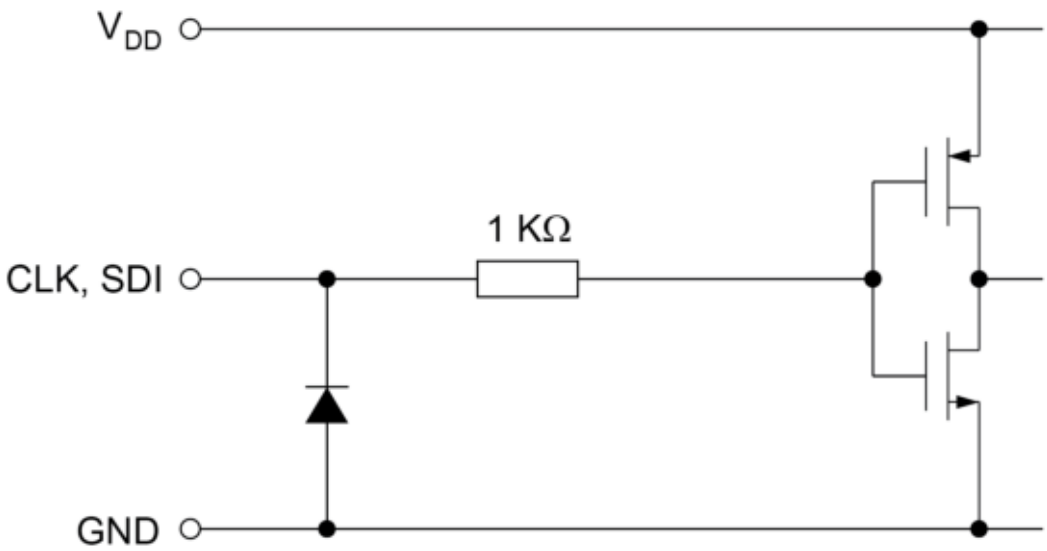
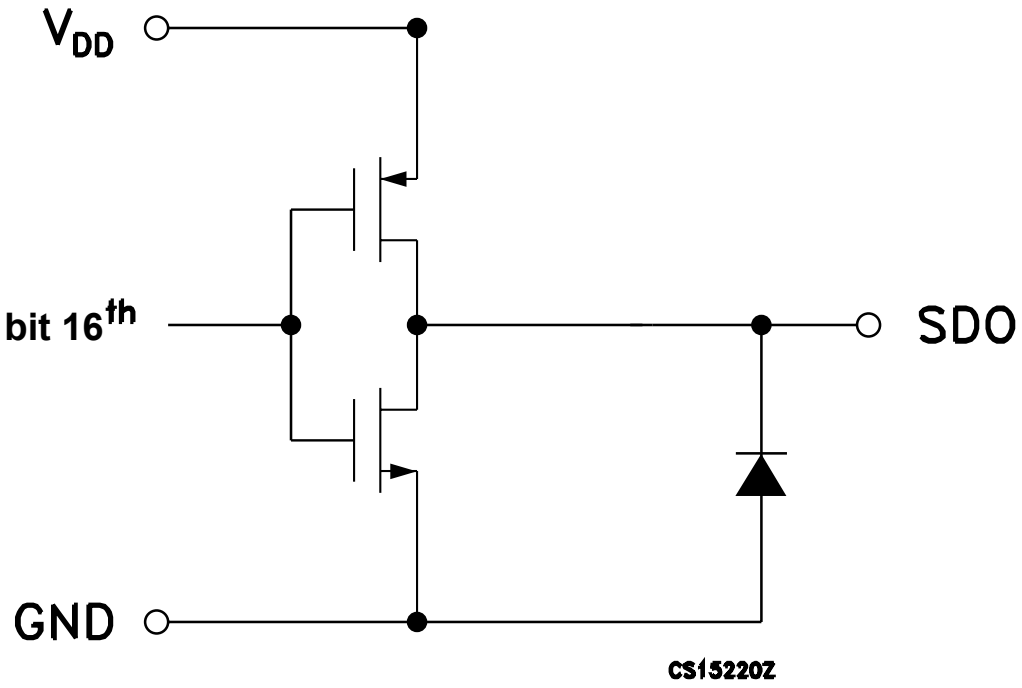
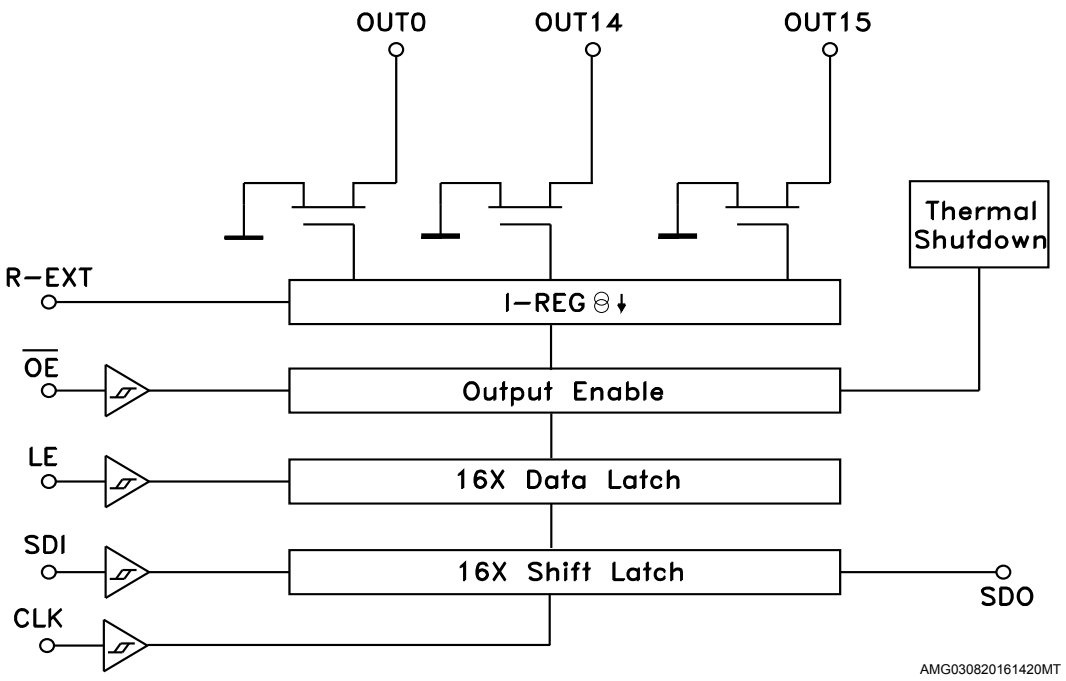


Figure 5. **SDO terminal**



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Figure 6. **Block diagram**



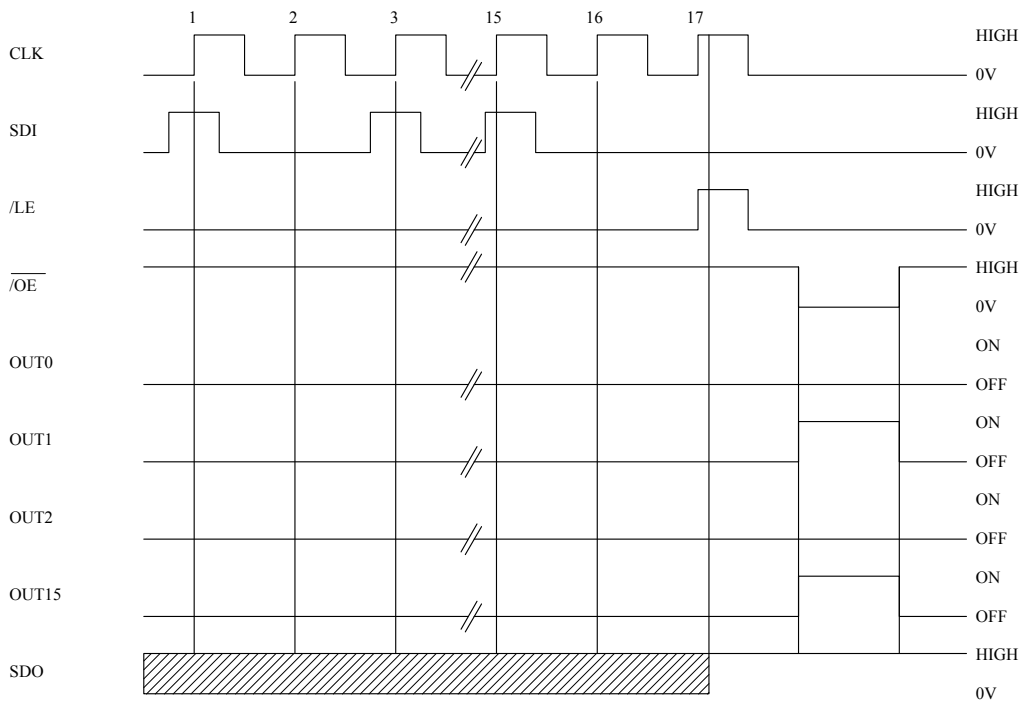
5 Timing diagrams

Table 8. Truth table

CLOCK	LE	$\overline{OE}$	Serial -IN	$\overline{OUT0}$ ..... $\overline{OUT7}$ ..... $\overline{OUT15}$	SDO
_|‾	H	L	Dn	Dn ..... Dn - 7 ..... Dn -15	Dn - 15
_|‾	L	L	Dn + 1	No change	Dn - 14
_|‾	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
‾|_	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
‾|_	X	H	Dn + 3	OFF	Dn - 13

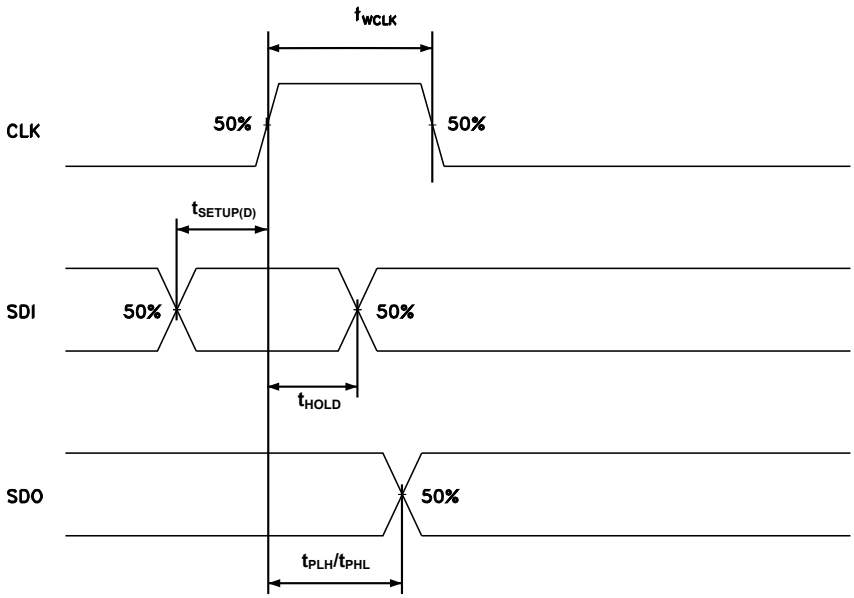
Note: OUTn = ON when Dn = H OUTn = OFF when Dn = L.

Figure 7. Timing diagram



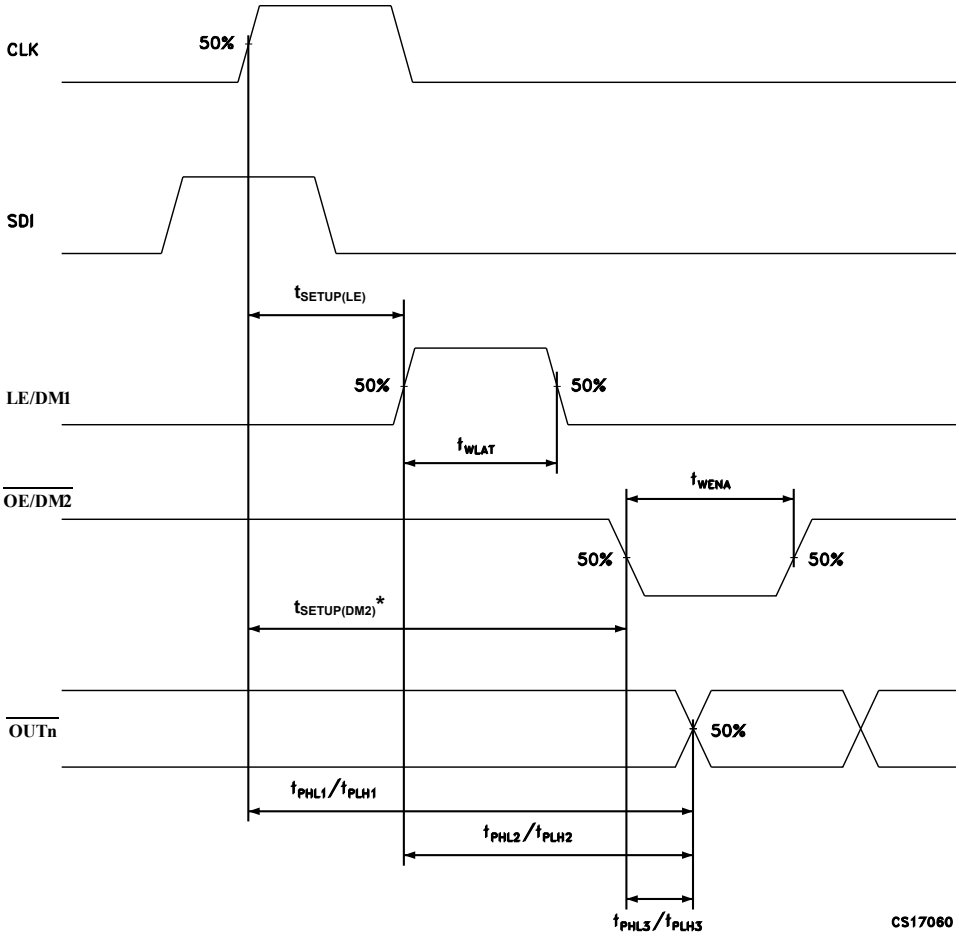
Note: 1 When LE terminal is at high level, latch circuit does not hold the data it passes from the input to the output.
2 When $\overline{OE}$ terminal is at low level, output terminals OUT0 to OUT15 respond to the data, either ON or OFF.
3 When $\overline{OE}$ terminal is at high level, it switches off all the data on the output terminal.

Figure 8. **Clock, serial-in, serial-out**



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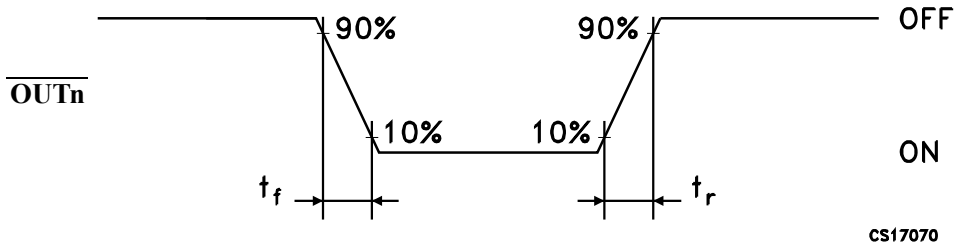
Figure 9. **Clock, serial-in, latch, enable, outputs**



* Only for detection feature.

AMG130220170702MT

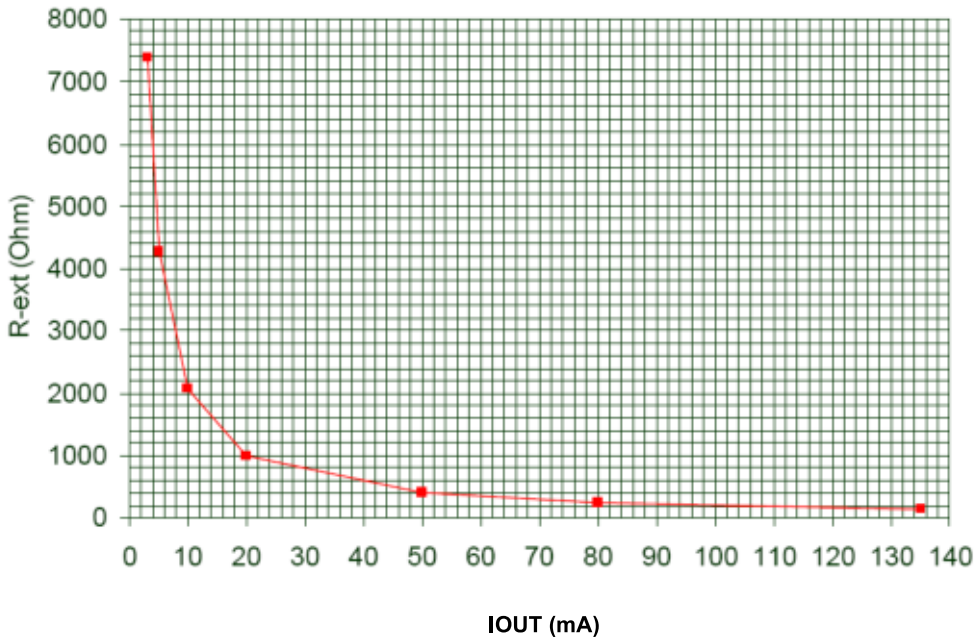
Figure 10. **Outputs**



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6 Typical characteristics

Figure 11. Output current-R_{EXT} resistor

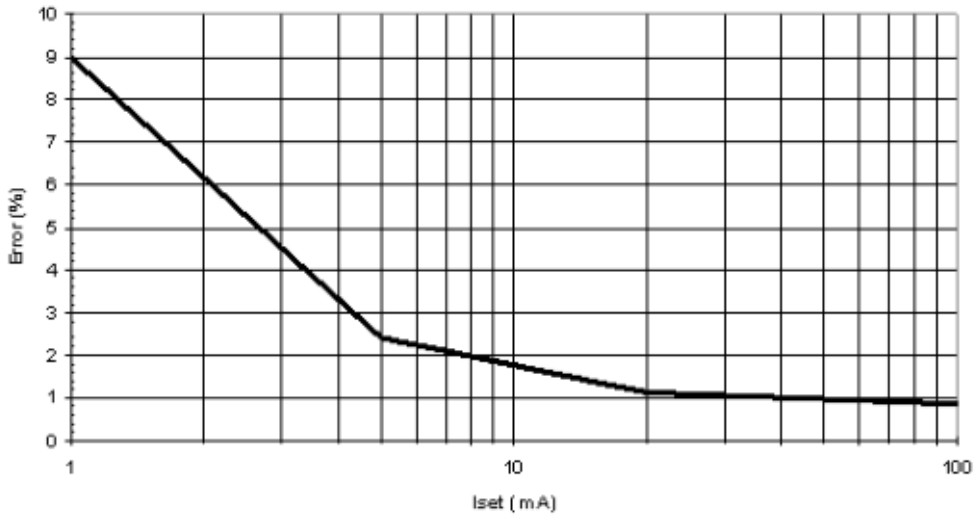


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Table 9. Output current-R_{EXT} resistor

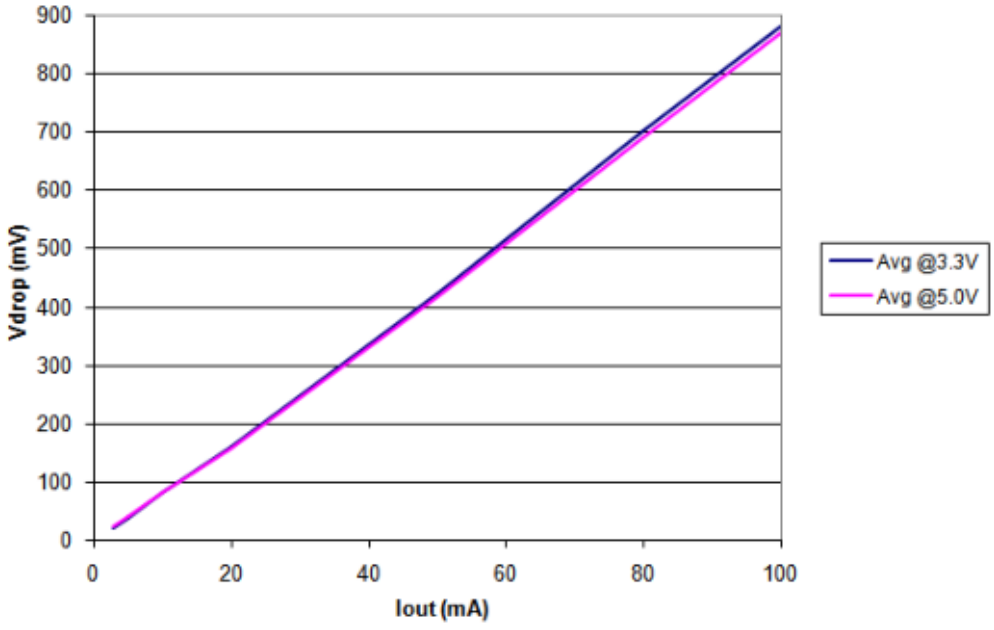
R_{EXT} (Ω)	Output current (mA)
7370	3
4270	5
2056	10
1006	20
382	50
251	80
200	100

Figure 12. Output current vs ± ΔI_{OL}(%) T_A = 25 °C



GIPD051020151346MT

Figure 13. I_{SET} vs drop out voltage (V_{drop}) T_A = 25 °C

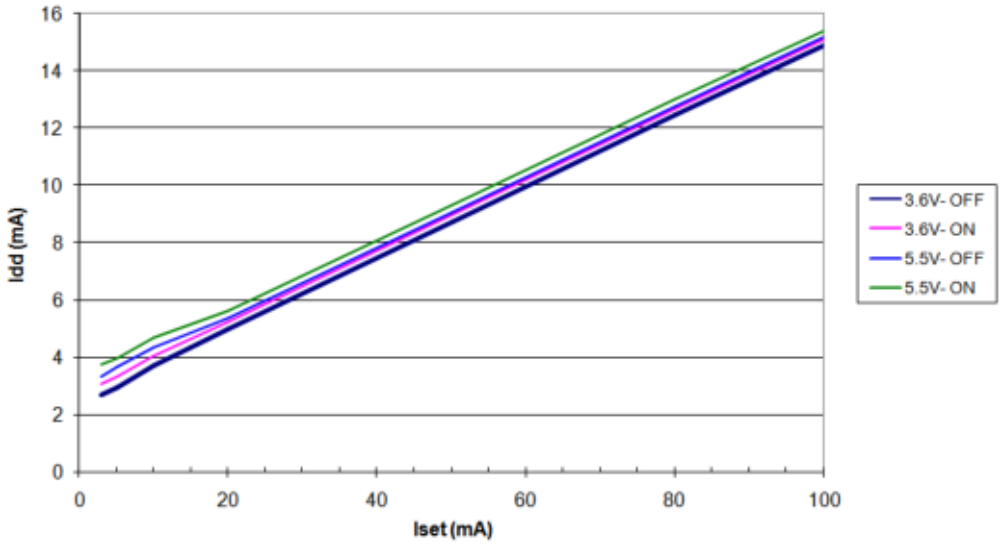


GIPD051020151348MT

Table 10. I_{SET} vs. dropout voltage (V_{drop})

Iout (mA)	Avg @ 3.3 V	Avg @ 5.0 V
3	20	22
5	37	40
10	79	79
20	160	158
50	422	415
80	700	690
100	880	870

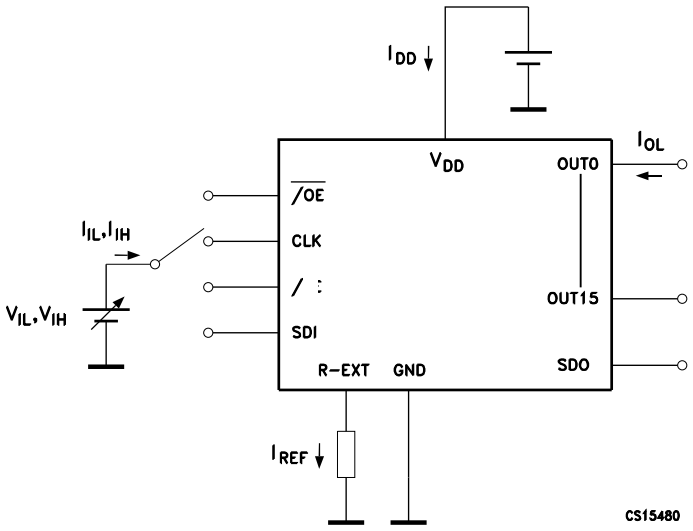
Figure 14. I_{DD} ON/OFF, T_A = 25 °C



GIPD051020151353MT

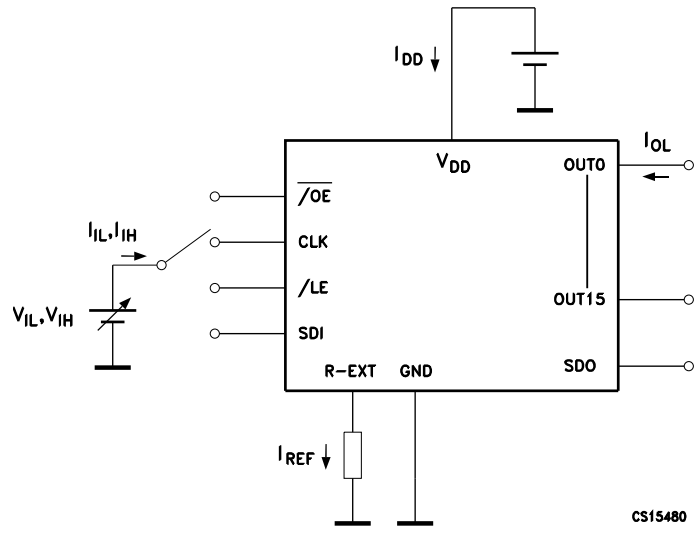
7 Test circuit

Figure 15. DC characteristic



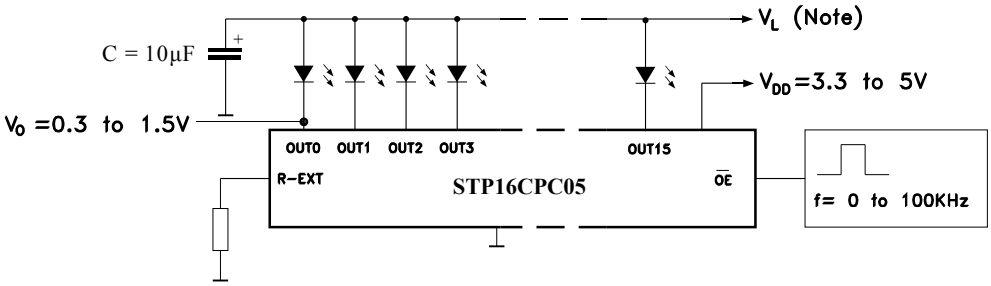
GIPD150320161338MT

Figure 16. AC characteristic



GIPD150320161339MT

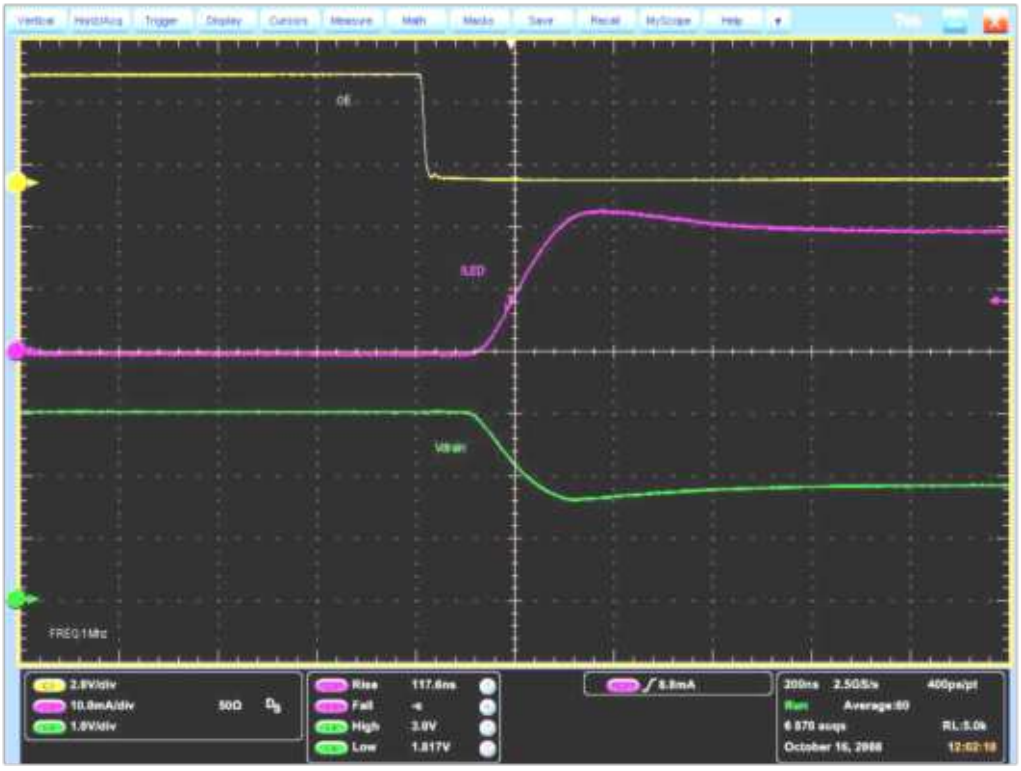
Figure 17. **Typical application schematic**



GIPD120420161338MT

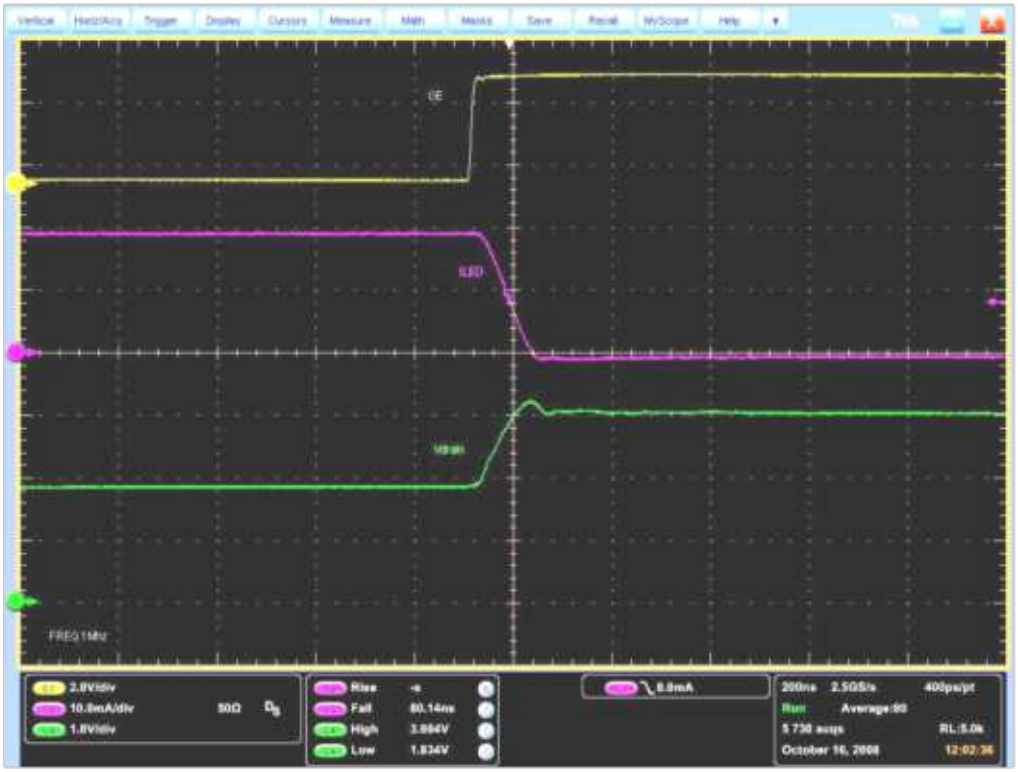
Note: V_L will be determined by the V_F of the LEDs.
Test condition: temp. = 25 °C, V_{DD} = 3.0 V, C_L = 10 pF, freq. = 1 MHz.

Figure 18. **Turn ON output current setup**



GIPD120420161350MT

Figure 19. **Turn OFF output current setup**



GIPD120420161350MT

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 QSOP-24 package information

Figure 20. **QSOP-24 package outline**

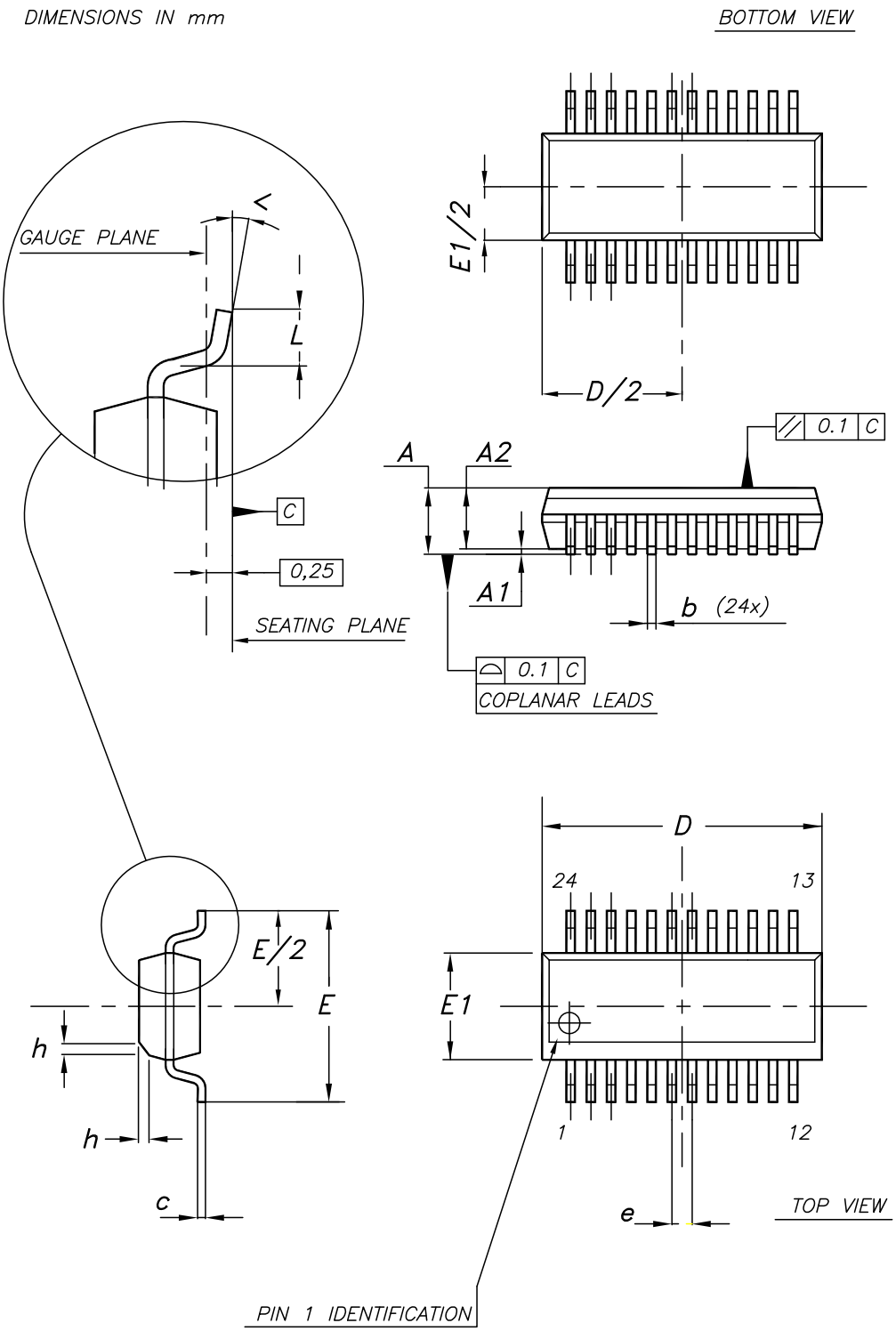


Table 11. **QSOP-24 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	1.54	1.62	1.73
A1	0.10	0.15	0.25
A2		1.47	
b	0.20		0.31
c	0.17		0.254
D	8.56	8.66	8.76
E	5.80	6.00	6.20
E1	3.80	3.91	4.01
e		0.635	
L	0.40	0.635	0.89
h	0.25	0.33	0.41
<	0°		8°

8.2 SO-24 0070769 package information

Figure 21. **SO-24 package outline**

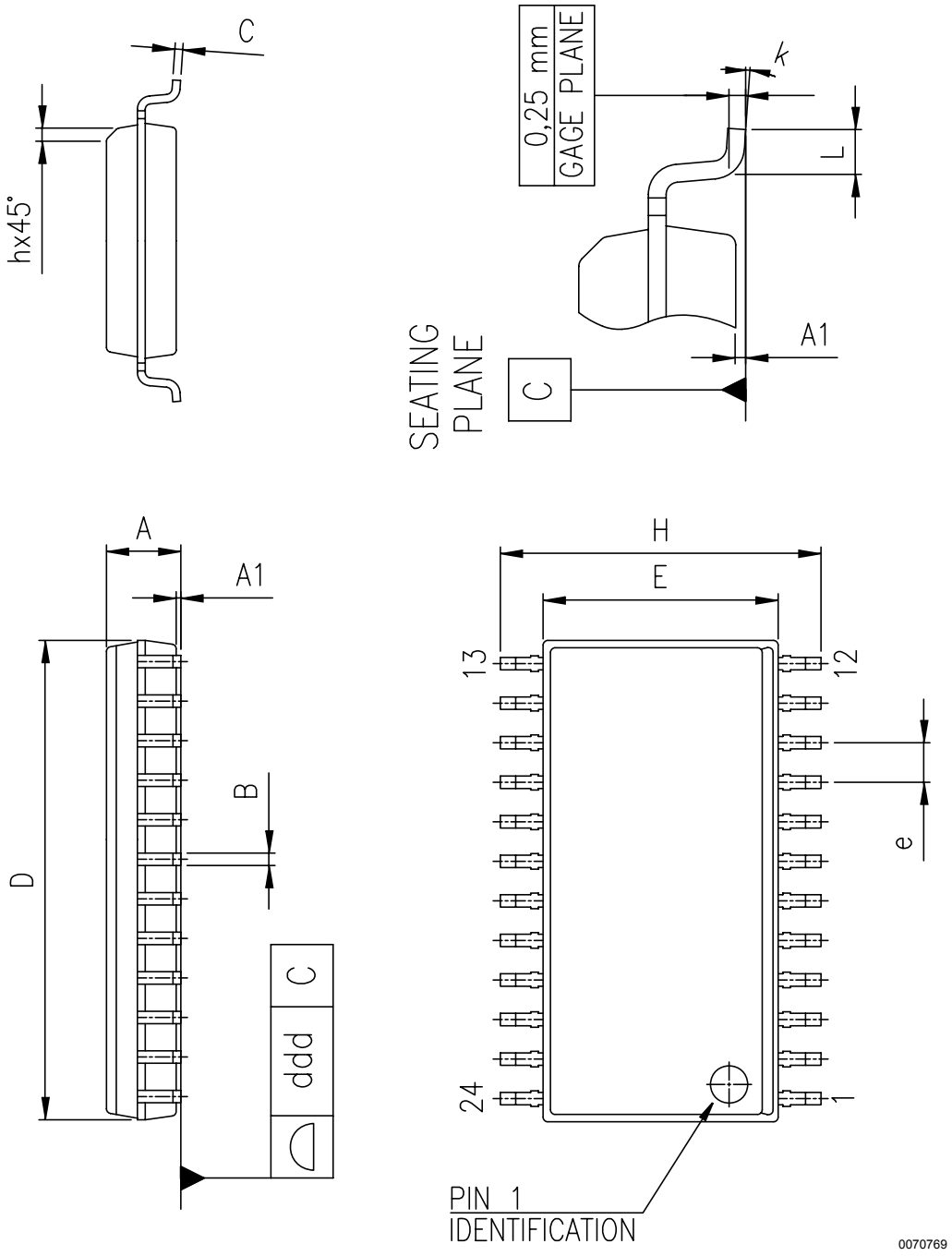


Table 12. **SO-24 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	15.20		15.60
E	7.40		7.60
e		1.27	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
k	0		8
ddd			0.10

8.3 TSSOP24 package information

Figure 22. **TSSOP24 package outline**

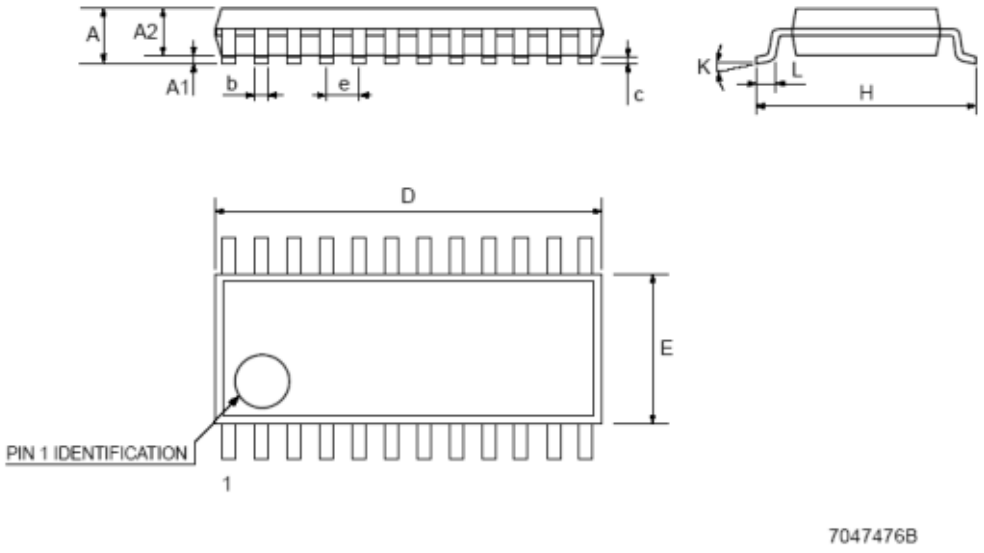


Table 13. **TSSOP24 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.1
A1	0.05		0.15
A2		0.9	
b	0.19		0.30
c	0.09		0.20
D	7.7		7.9
E	4.3		4.5
e		0.65 BSC	
H	6.25		6.5
K	0°		8°
L	0.50		0.70

8.4 TSSOP24 exposed pad package information

Figure 23. **TSSOP24 exposed pad package outline**

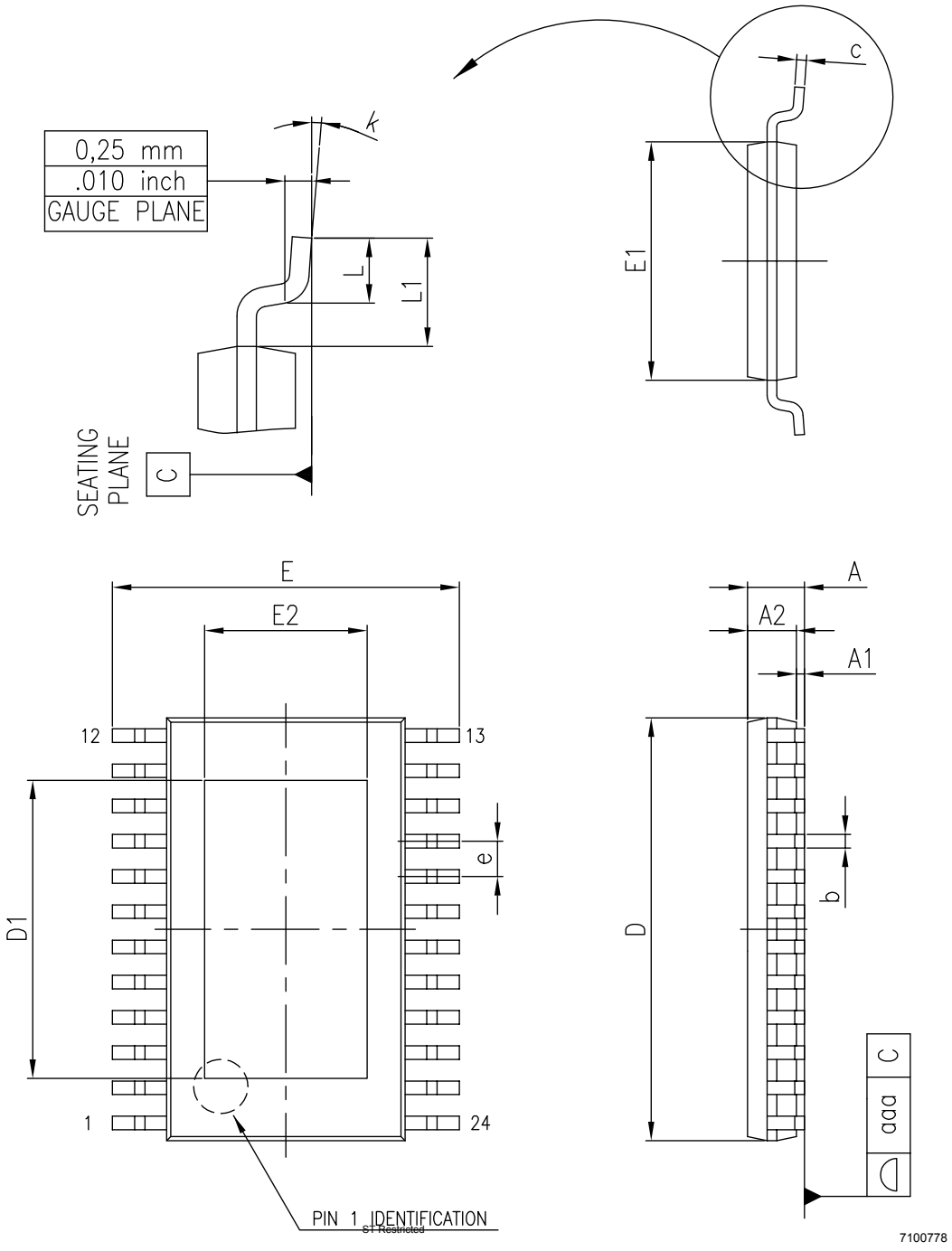


Table 14. **TSSOP24 exposed pad mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
D1	4.80	5.00	5.20
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	3.00	3.20	3.40
e			
L	0.45	0.60	0.75
L1		1.00	
K	0		8
aaa			0.10

8.5 TSSOP24, TSSOP24 exposed pad and SO-24 packing information

Figure 24. **TSSOP24, TSSOP24 exposed pad and SO-24 reel outline**

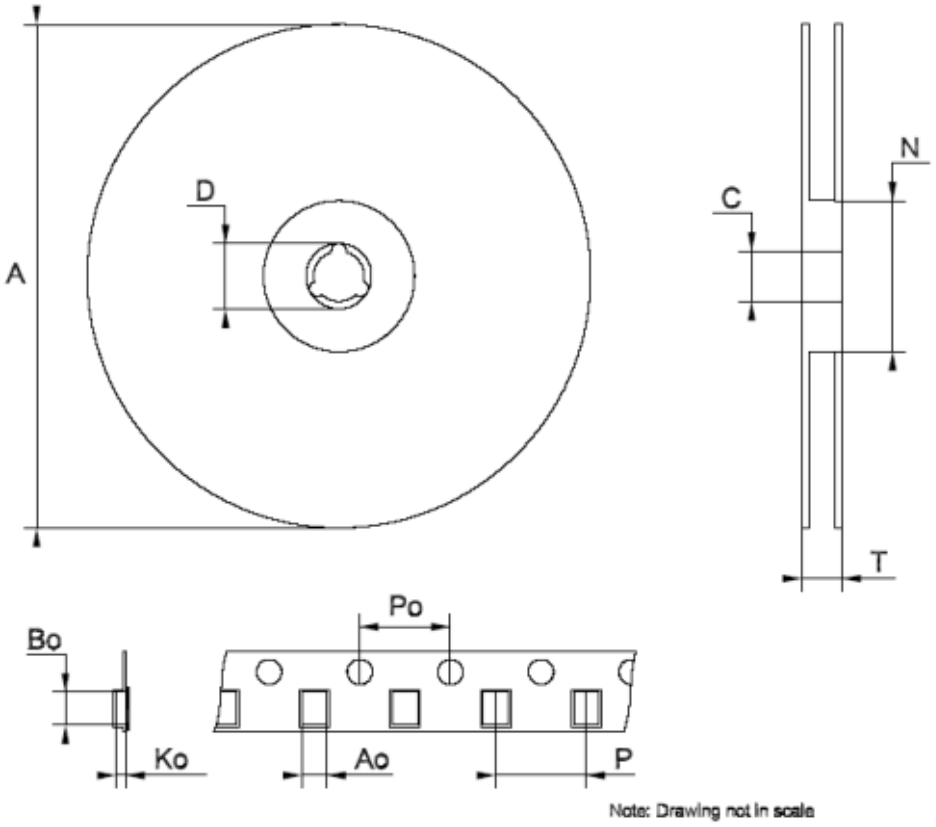


Table 15. **TSSOP24 and TSSOP24 exposed pad tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	330	-	331
C	13.0	-	14.0
D	18.7	-	
N	100	-	
T	16.5	-	18.5
Ao	6.85	-	7.05
Bo	8.20	-	8.40
Ko	1.5	-	1.7
Po	3.9	-	4.1
P	7.9	-	8.1

Table 16. **SO-24 tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	30.4
Ao	10.8	-	11.0
Bo	15.7	-	15.9
Ko	2.9	-	3.1
Po	3.9	-	4.1
P	11.9	-	12.1

9 Device summary

Table 17. **Device summary**

Order code	Package	Packing
STP16CPC05MTR	SO-24	1000 parts per reel
STP16CPC05TTR	TSSOP24	2500 parts per reel
STP16CPC05XTTR	TSSOP24 exposed pad	2500 parts per reel
STP16CPC05PTR	QSOP-24	2500 parts per reel

Revision history

Table 18. **Document revision history**

Date	Revision	Changes
30-Jan-2009	1	First release
12-May-2009	2	Updated Table 6 on page 6
29-Oct-2009	3	Updated Note: on page 3
16-Jun-2014	4	Updated Section 8: Package mechanical data. Added Section 9: Packaging mechanical data. Minor text changes.
08-Mar-2017	5	Updated Table 5: "Thermal data", Figure 5: "SDO terminal", Figure 8: "Clock, serial-in, serial-out", Figure 9: "Clock, serial-in, latch, enable, outputs" and Section 8: "Package information". Minor text changes
07-Sep-2023	6	Updated Table 15.

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