STD95N4LF3

N-channel 40 V, 5.0 mΩ typ., 80 A STripFET™ III Power MOSFET in a DPAK package

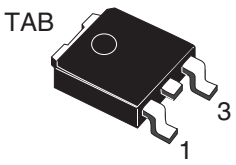
Datasheet — production data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	P_D
STD95N4LF3	40 V	< 6.0 mΩ	80 A(1)	110 W

1. Value limited by wire bonding

- 100% avalanche tested
- Logic level drive



DPAK

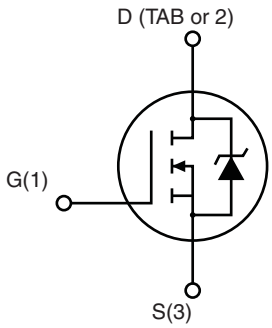
Applications

- Switching application
  - Automotive

Description

This device is an N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

Figure 1. Internal schematic diagram



AM01474v1

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD95N4LF3	95N4LF3	DPAK	Tape and reel

This is information on a product in full production. www.st.com

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 16	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	80	A
I_D	Drain current (continuous) at T_C = 100 °C	65	A
I_{DM} (2)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
	Derating factor	0.73	W/°C
dv/dt (3)	Peak diode recovery voltage slope	8	V/ns
E_{AS} (4)	Single pulse avalanche energy	400	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Value limited by wire bonding
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 80$ A, di/dt $\leq$ 40 A/µs, $V_{DS} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$
4. Starting T_J = 25 °C, I_D = 40 A, V_{DD} = 35 V *Figure 16* and *Figure 17*

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.36	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	50	°C/W

1. When mounted on 1inch² FR-4 2Oz Cu board

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} =0	40			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = 40 V, T_C= 125 °C	V_{DS} = 40 V			10 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 16 V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 40 A V_{GS} = 5 V, I_D = 40 A		5.0	6.0 9.0	mΩ mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	2500 560 50		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 20 V, I_D = 40 A R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 13* and *Figure 18*)	-	7.5 45 45 11		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 20 V, I_D = 80 A, V_{GS} = 10 V (see *Figure 14*)	-	50 7 9.5	70	nC nC nC

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		80 320	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 80 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 80 A, di/dt = 100 A/µs, V_{DD} = 20 V, T_j = 150 °C (see *Figure 15* and *Figure 19*)	-	40 55 3		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

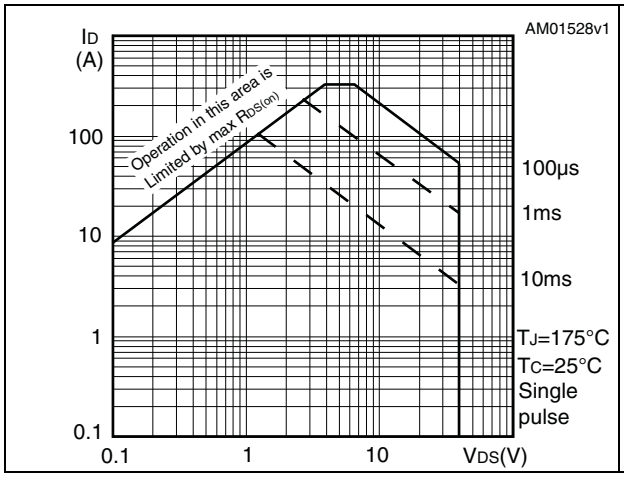


Figure 3. Thermal impedance

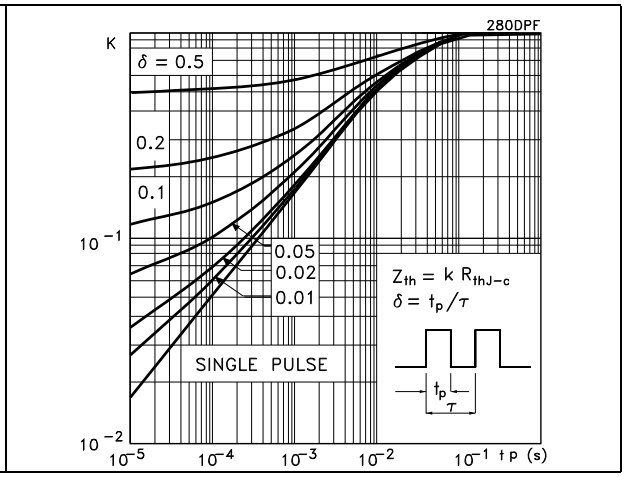


Figure 4. Output characteristics

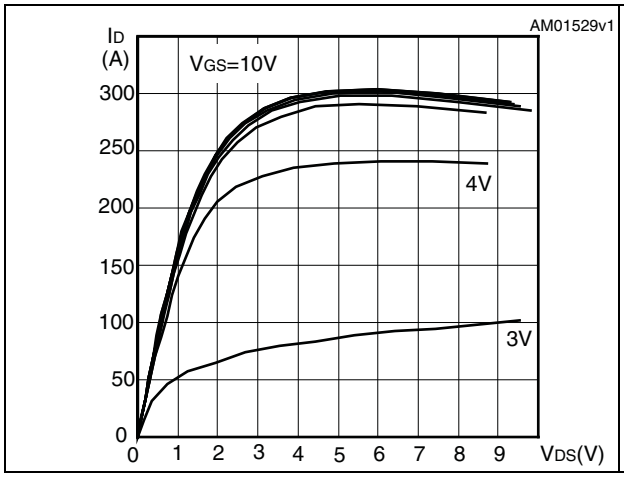


Figure 5. Transfer characteristics

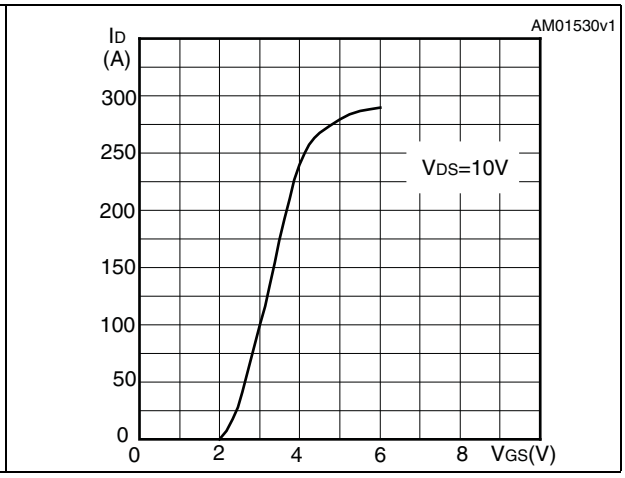


Figure 6. Static drain-source on-resistance

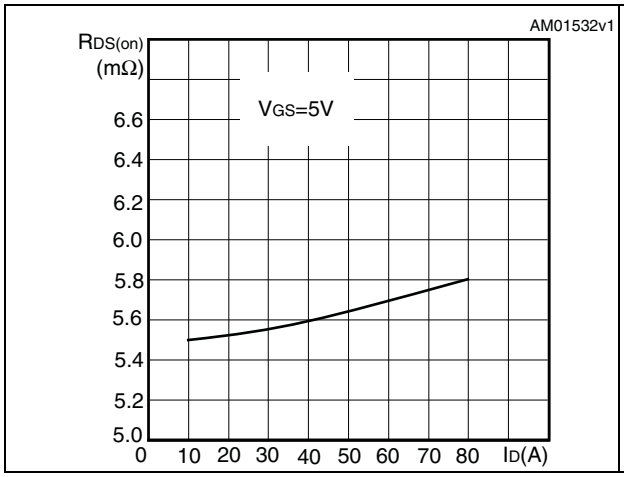


Figure 7. Normalized B_{VDSS} vs temperature

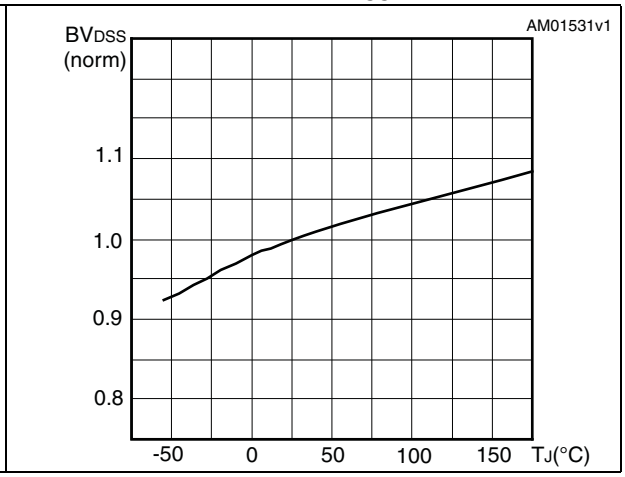


Figure 8. Gate charge vs gate-source voltage

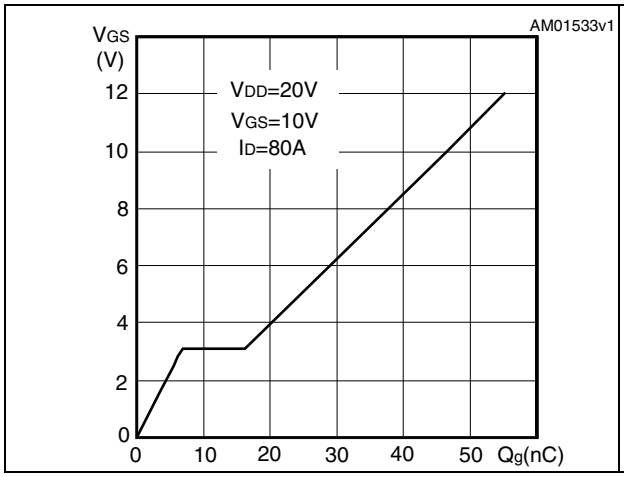


Figure 9. Capacitance variations

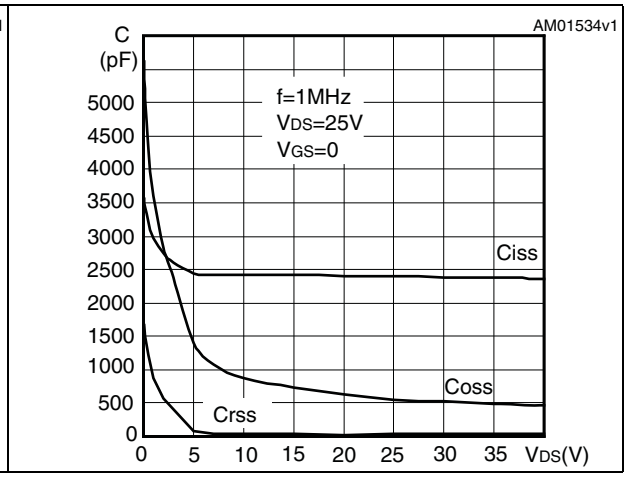


Figure 10. Normalized gate threshold voltage vs temperature

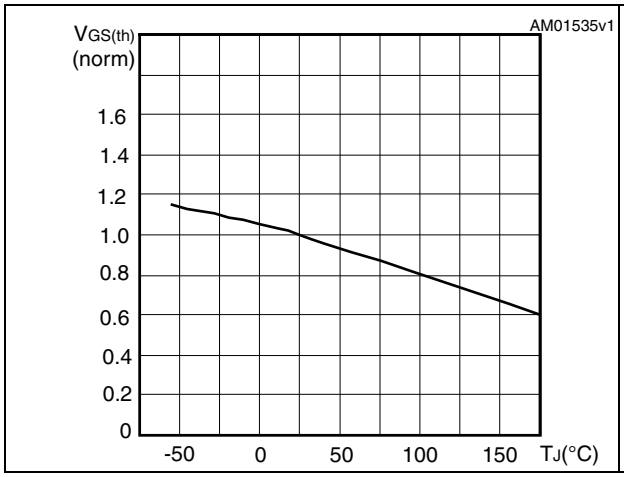


Figure 11. Normalized on resistance vs temperature

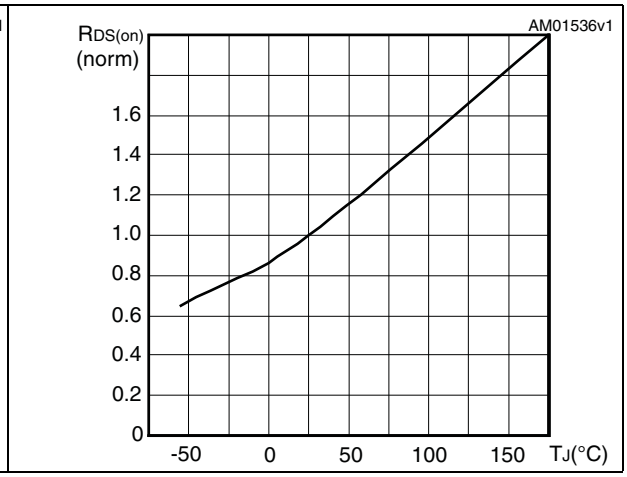
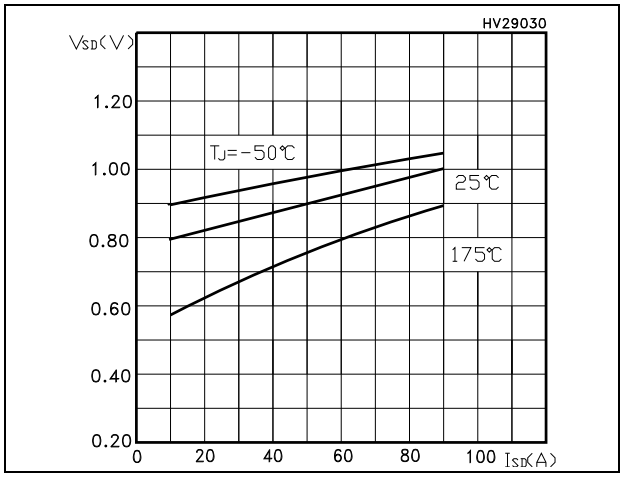


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

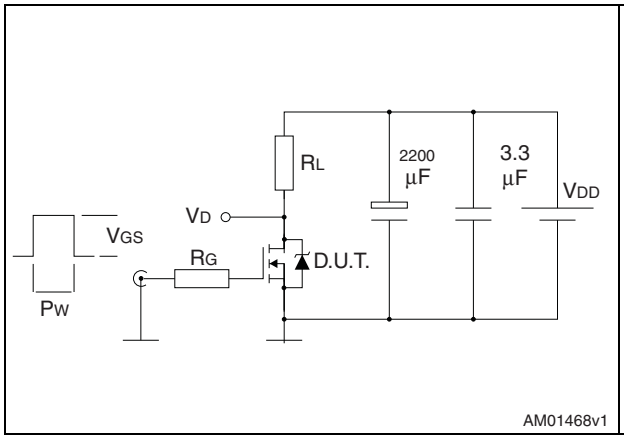


Figure 14. Gate charge test circuit

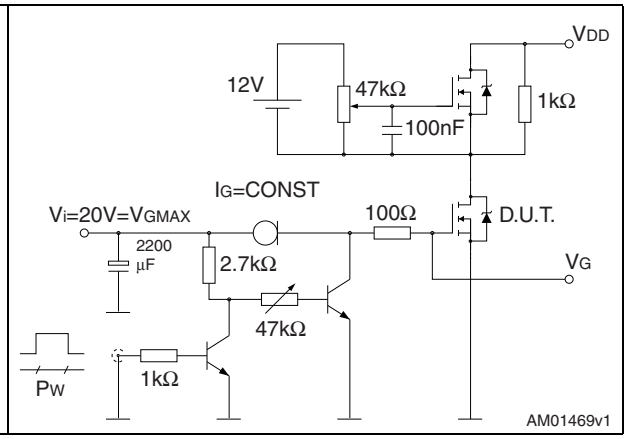


Figure 15. Test circuit for inductive load switching and diode recovery times

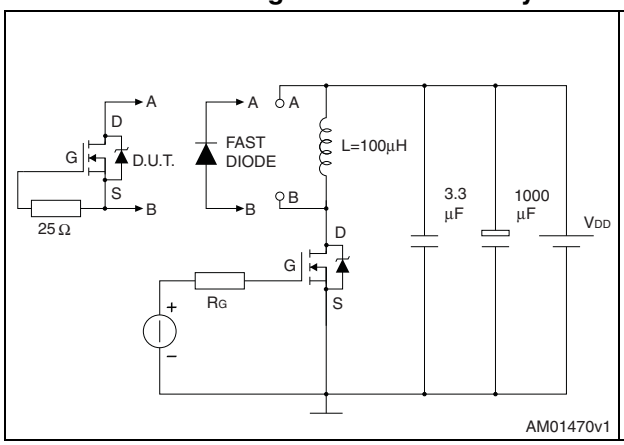


Figure 16. Unclamped inductive load test circuit

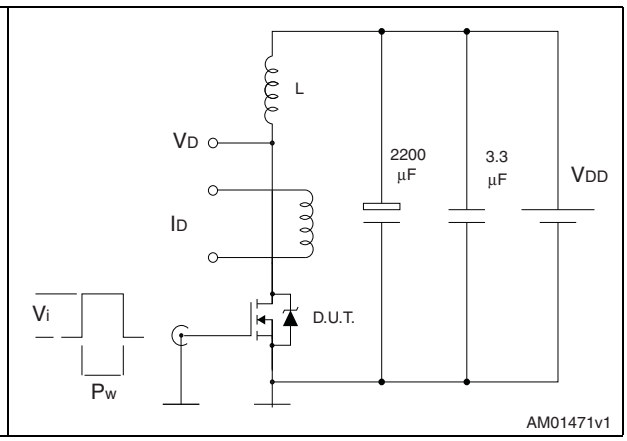


Figure 17. Unclamped inductive waveform

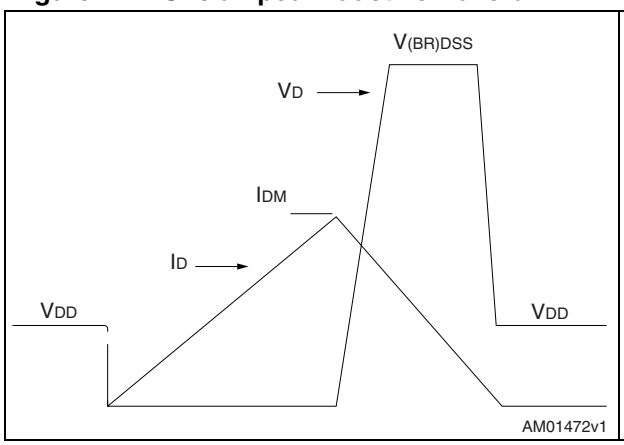


Figure 18. Switching time waveform

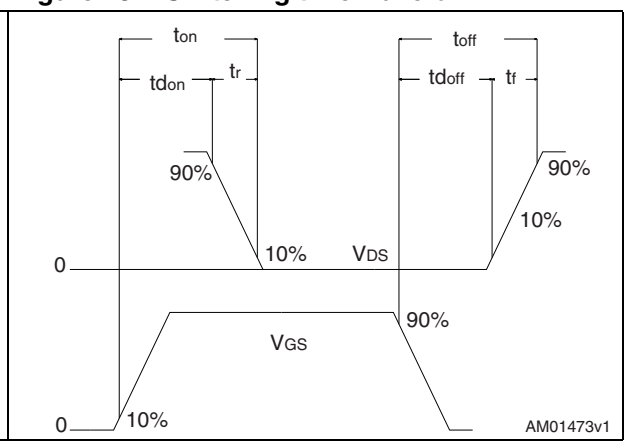
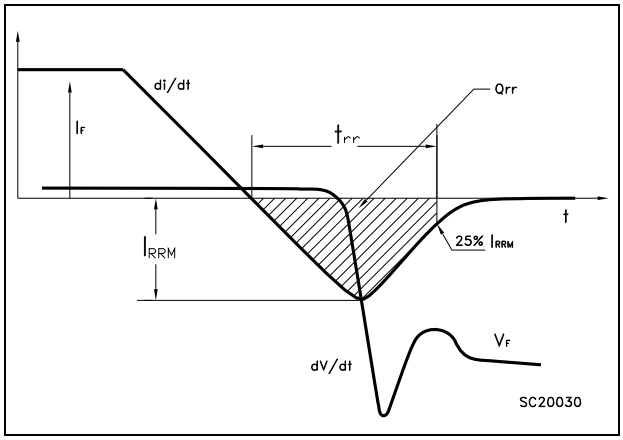


Figure 19. Diode reverse recovery waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 7. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 20. DPAK (TO-252) drawing

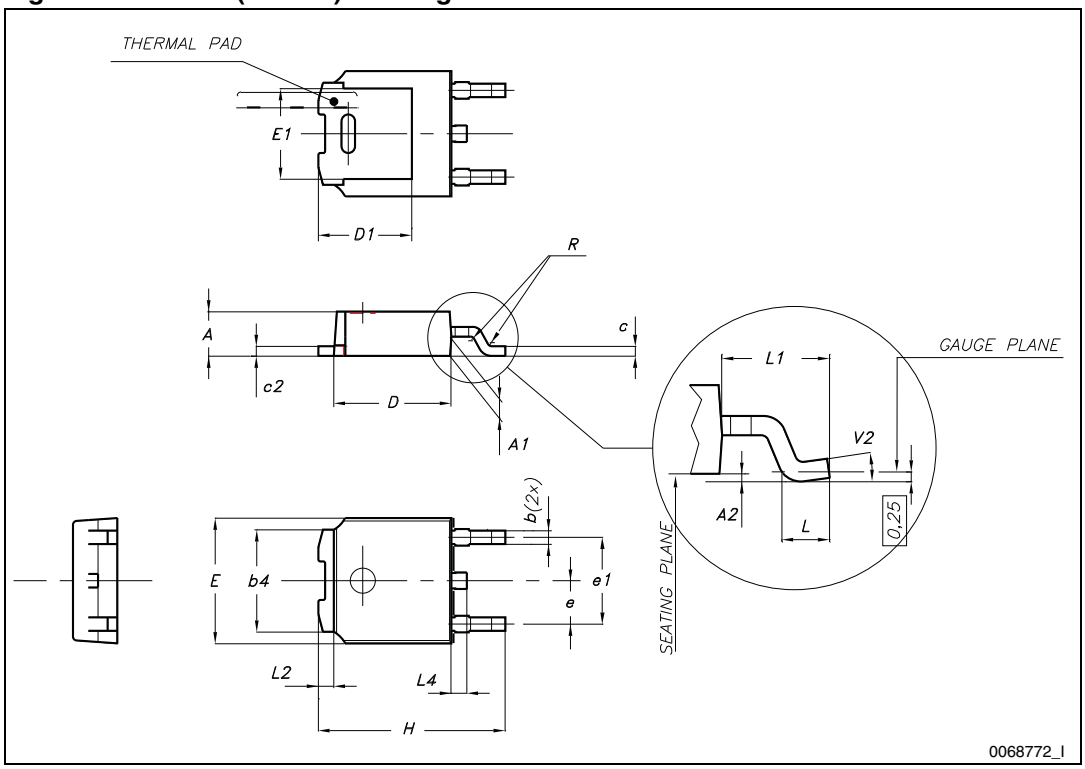
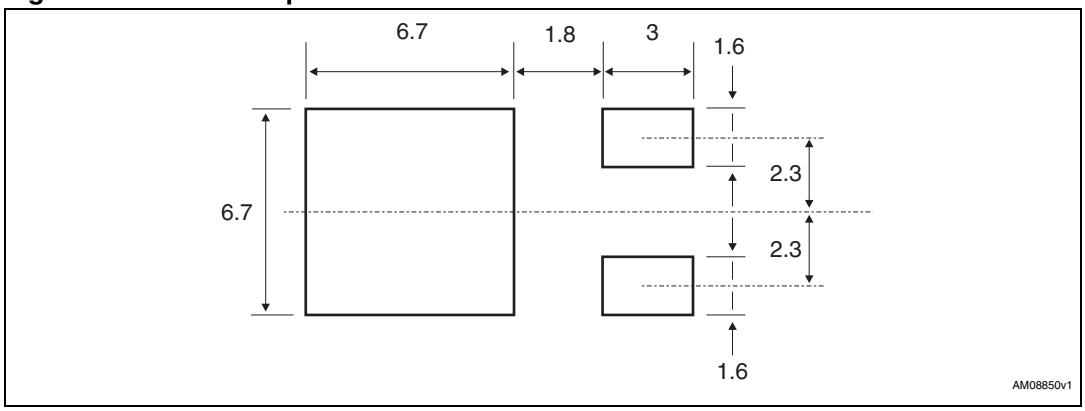


Figure 21. DPAK footprint[a]



a. All dimensions are in millimeters

5 Packing mechanical data

Table 8. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 22. Tape for DPAK (TO-252)

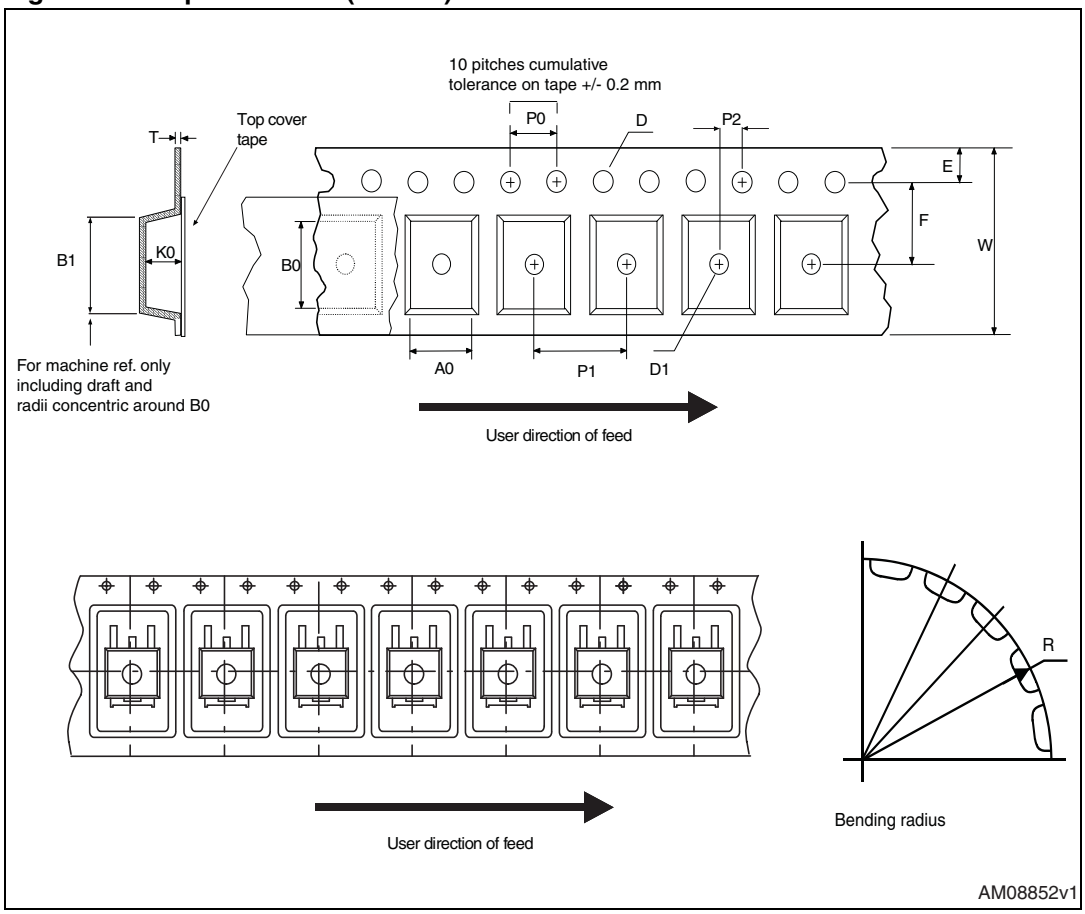
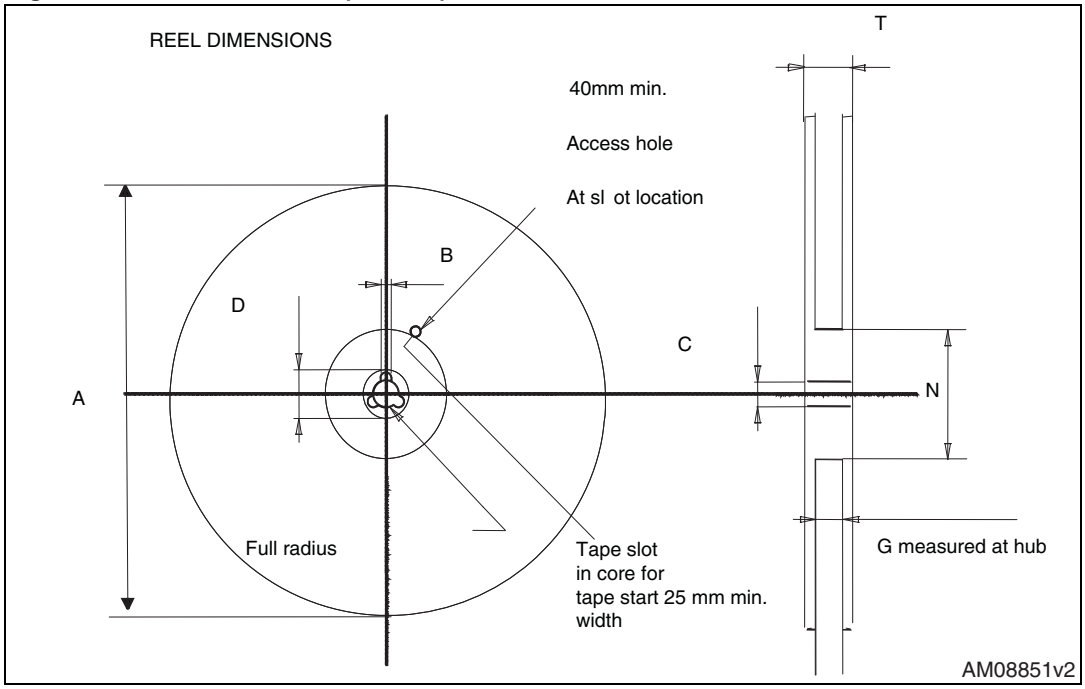


Figure 23. Reel for DPAK (TO-252)



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
11-Feb-2009	1	First release
23-Jul-2009	2	Marking on device summary has been corrected.
13-Jul-2012	3	Updated title on the cover page. Minor text changes. Updated *Section 4: Package mechanical data* and *Section 5: Packing mechanical data*.

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