HDMIULC6-2x6

Ultra large bandwidth ESD protection

Features

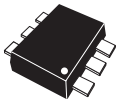
- 2-line ESD protection (at 15 kV air and contact discharge, exceeds IEC 61000-4-2)
- Ultra low capacitance: 0.6 pF @ 825 MHz
- Ultra high bandwidth - no influence on signal rise and fall times - maximised number of signal harmonics
- Very low leakage current: 0.5 µA max.
- Fast response time compared with varistors
- Protects V_{BUS} when applicable
- RoHS compliant

Benefits

- ESD standards compliance guaranteed at device level, thus greater immunity at system level
- ESD protection of V_{BUS} when applicable.
- High efficiency due to low residual voltage when confronted by an ESD surge
- Large bandwidth to minimize impact on data signal quality
- Consistent D+ / D- signal balance:
  - Ultra low impact on intra- and inter-pair skew
  - Matching high bit rate HDMI requirements and ready for future evolution
- Low PCB space occupation - 1.45 mm^2 for µQFN
- Low leakage current for longer operation of battery powered devices
- Higher reliability offered by monolithic integration
- 500 µm pitch for µQFN 6 leads



µQFN (pin view)
HDMIULC6-2M6



SOT-666
HDMIULC6-2P6

Complies with these standards

- IEC 61000-4-2 level 4
  - 15 kV air discharge
  - 8 kV contact discharge
- MIL STD883G-Method 3015-7

Applications

- HDMI ports at 1.65 Gb/s and up to 3.2 Gb/s
- IEEE 1394a, b, or c up to 3.2 Gb/s
- USB 2.0 ports up to 480 Mb/s (Hi-Speed)
- Ethernet port: 10/100/1000 Mb/s
- Video line protection

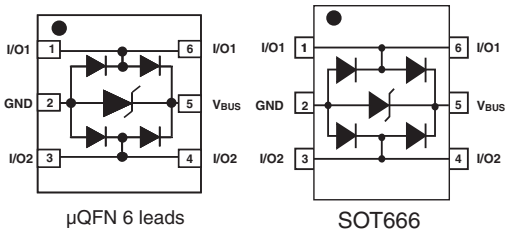
Description

The HDMIULC6-2x6 is a monolithic, application specific discrete device dedicated to ESD protection of the HDMI connection. It also offers the same high level of protection for IEEE 1394a and IEEE 1394b/c, USB 2.0, Ethernet links, and video lines.

Its ultra high cutoff frequency (5.9 GHz) secures a high level of signal integrity. The device topology provides this integrity without compromising the complete protection of ICs against the most stringent ESD strikes.

1 Characteristics

Figure 1. Functional diagram



When used with a HDMI application, Pin 5 should not be connected to protect against backdrive current flow on data lines.

Table 1. Absolute ratings

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 air discharge IEC 61000-4-2 contact discharge MIL STD883G-Method 3015-7	±15 ±15 ±25	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_j	Maximum junction temperature		125	°C
T_L	Lead solder temperature (10 seconds duration)		260	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max	
I_{RM}	Leakage current	V_{RM} = 5 V			0.5	µA
V_{BR}	Breakdown voltage between V_{BUS} and GND	I_R = 1 mA	6			V
V_{CL}	Clamping voltage	I_{PP} = 1 A, t_p = 8/20 µs Any I/O pin to GND			12	V
		I_{PP} = 5 A, t_p = 8/20 µs Any I/O pin to GND			17	V
$C_{i/o-GND}$	Capacitance between I/O and GND	V_R = 0 V, F = 825 MHz			0.85	pF
$\Delta C_{i/o-GND}$	Capacitance variation between I/O and GND	V_R = 0 V, F = 1 MHz		0.02		pF
$C_{i/o-i/o}$	Capacitance between I/O	V_R = 0 V, F = 825 MHz			0.5	pF

Figure 2. Line capacitance versus line voltage (typical values)

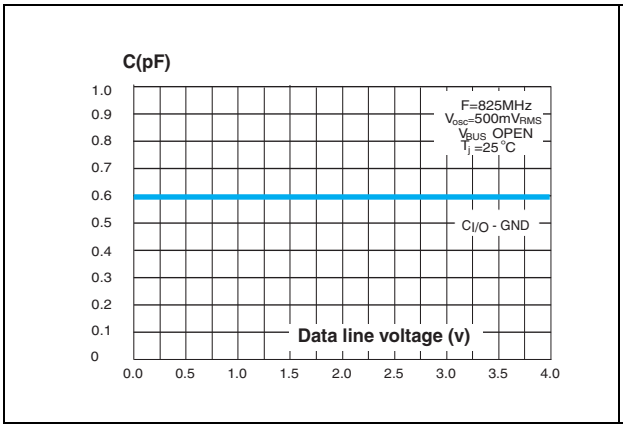


Figure 3. Line capacitance versus frequency (typical values) HDMIULC6-2M6

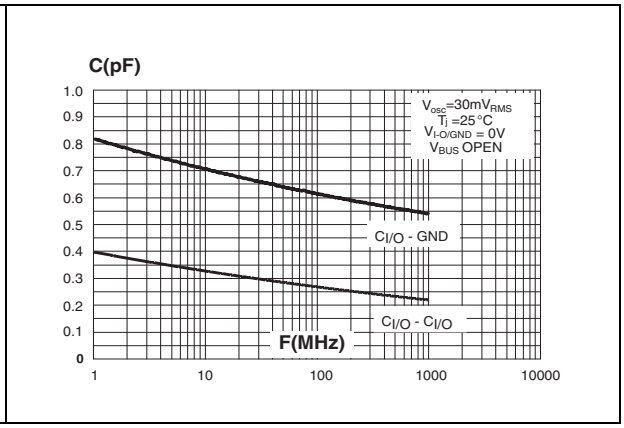


Figure 4. Line capacitance versus frequency (typical values) HDMIULC6-2P6

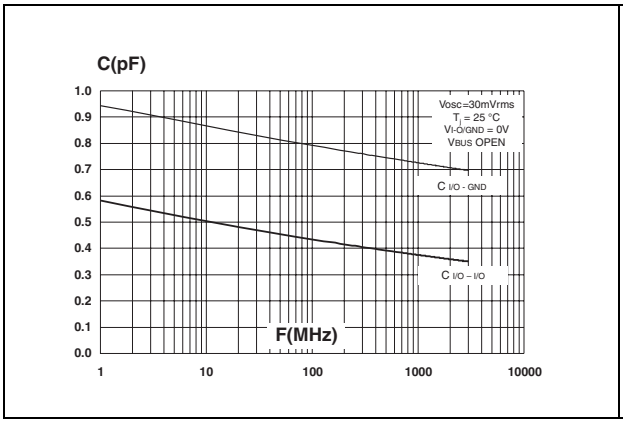


Figure 5. Frequency response (typical values) HDMIULC6-2M6

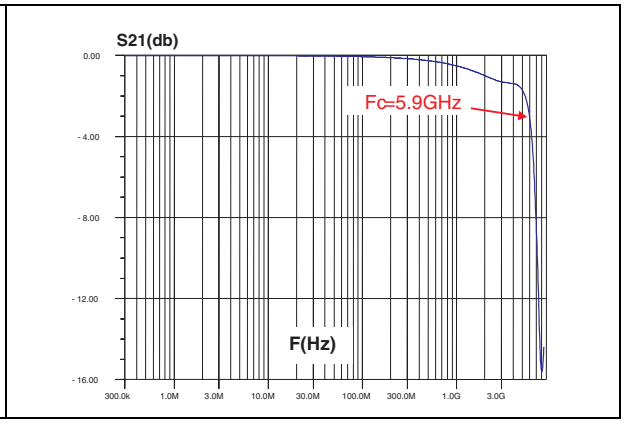


Figure 6. Frequency response (typical values) HDMIULC6-2P6

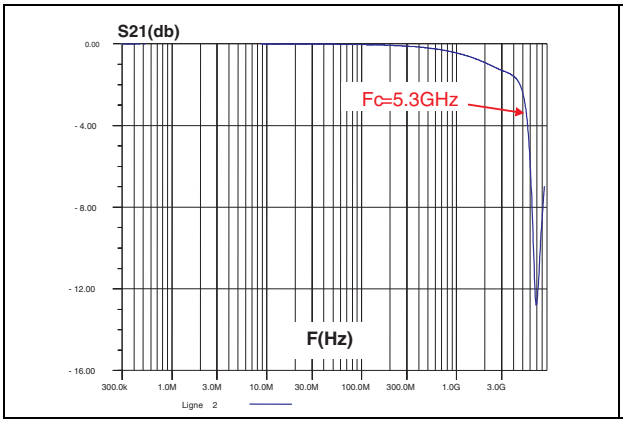


Figure 7. Relative variation of leakage current versus junction temperature (typical values)

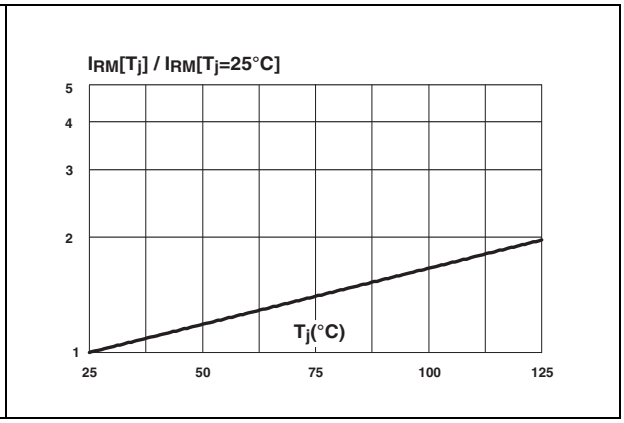


Figure 8. Eye diagram at 1.65 Gbps amplitude 500 mV PCB + HDMIULC6-2M6

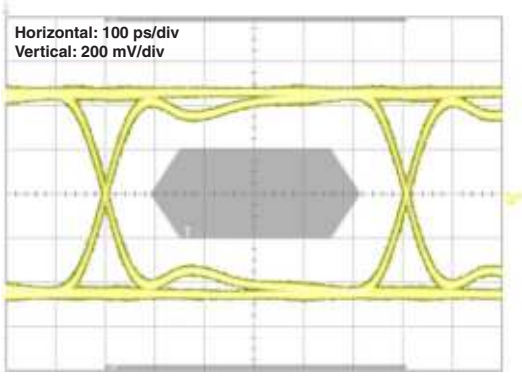


Figure 9. Eye diagram at 3.2 Gbps amplitude 500 mV PCB + HDMIULC6-2M6

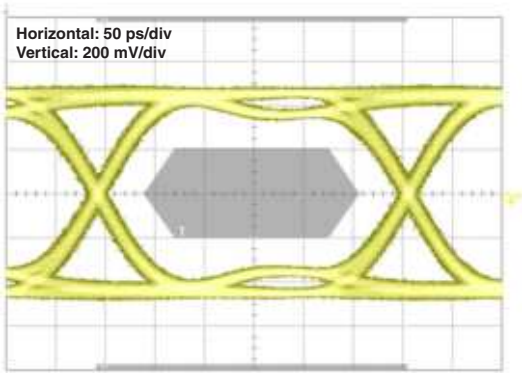


Figure 10. Eye diagram at 1.65 Gbps amplitude 500 mV PCB + HDMIULC6-2P6

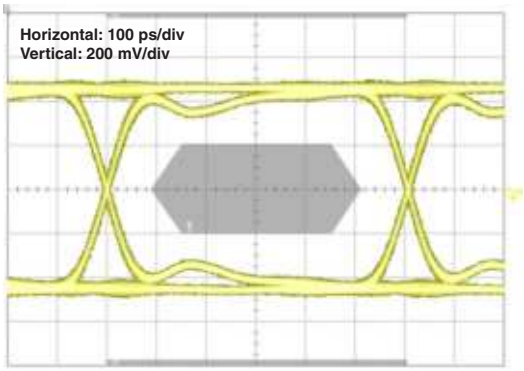
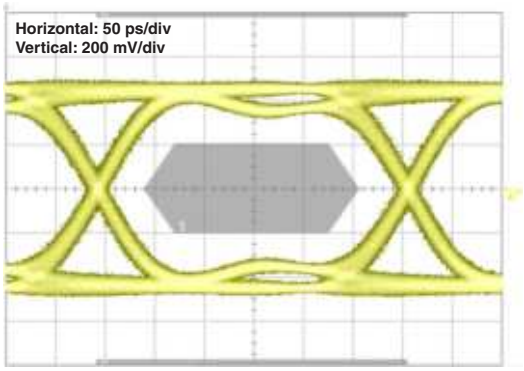


Figure 11. Eye diagram at 3.2 Gbps amplitude 500 mV PCB + HDMIULC6-2P6



2 Application examples

Figure 12. HDMI single link application

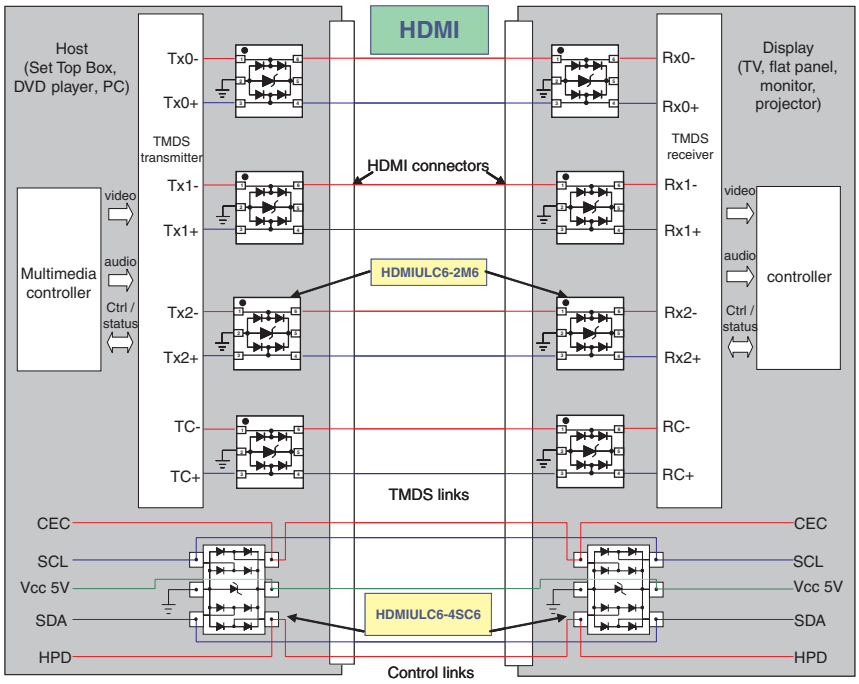
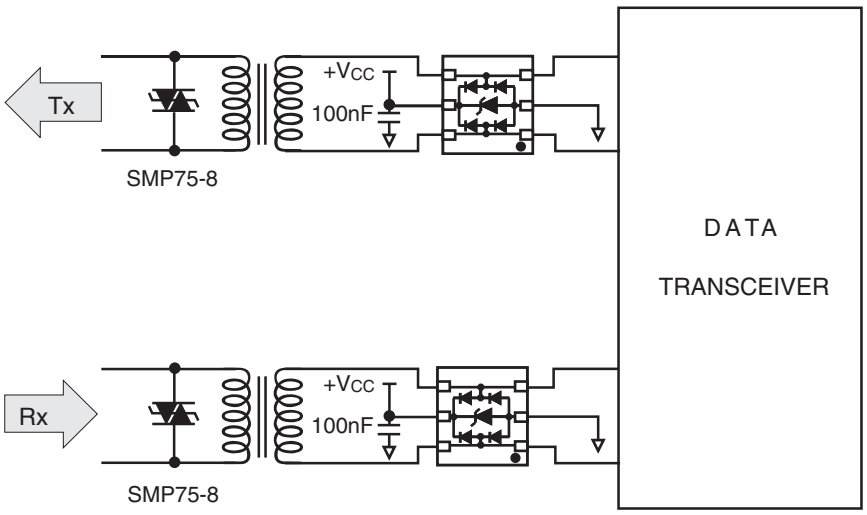


Figure 13. T1/E1/Ethernet protection



2.1 PCB layout considerations

Figure 14. PCB layout example

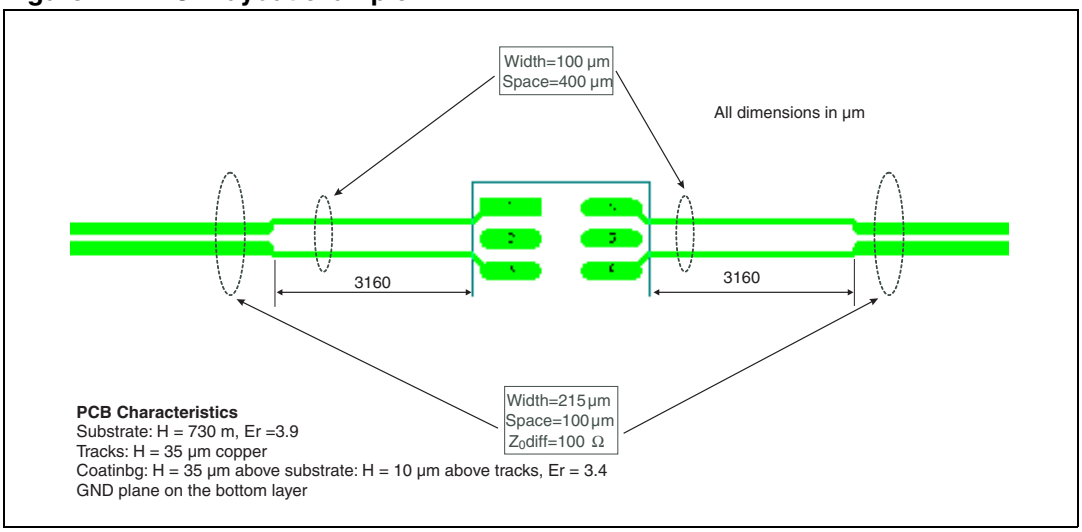
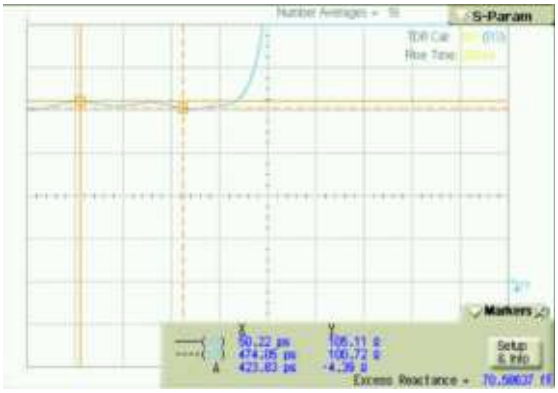


Figure 15. TDR results for HDMIULC6-2M6 with PCB layout example



3 Technical information

3.1 Surge protection

The HDMIULC6-2x6 is particularly optimized to perform ESD surge protection based on the rail to rail topology.

The clamping voltage V_{CL} can be calculated as follows:

$V_{CL}+ = V_{TRANSIL} + V_F$ for positive surges

$V_{CL}- = - V_F$ for negative surges

with: $V_F = V_T + R_d.I_p$

(V_F forward drop voltage) / (V_T forward drop threshold voltage)

and $V_{TRANSIL} = V_{BR} + R_{d_TRANSIL} . I_P$

Calculation example

We assume that the value of the dynamic resistance of the clamping diode is typically: $R_d = 0.5\ \Omega$ and $V_T = 1.1$ V.

We assume that the value of the dynamic resistance of the transil diode is typically $R_{d_TRANSIL} = 0.5\ \Omega$ and $V_{BR} = 6.1$ V

For an IEC 61000-4-2 surge Level 4 (Contact Discharge: V_g= 8 kV, R_g= 330 Ω), V_{BUS} = +5 V, and, in first approximation, we assume that: $I_p = V_g / R_g$ = 24 A.

We find:

$V_{CL}+ = +31.2$ V

$V_{CL}- = -13.1$ V

Note: The calculations do not take into account phenomena due to parasitic inductances.

3.2 Surge protection application example

If we consider that the connections from the pin V_{BUS} to V_{CC}, from I/O to data line, and from GND to PCB GND plane are two tracks 10 mm long and 0.5 mm wide, we can assume that the parasitic inductances, L_{VBUS}, $L_{I/O}$, and L_{GND}, of these tracks are about 6 nH. So when an IEC 61000-4-2 surge occurs on the data line, due to the rise time of this spike (tr = 1 ns), the voltage V_{CL} has an extra value equal to $L_{I/O}.dI/dt + L_{GND}.dI/dt$.

The dI/dt is calculated as: dI/dt = Ip/tr = 24 A/ns for an IEC 61000-4-2 surge level 4 (contact discharge V_g = 8 kV, R_g = 330 Ω)

The over voltage due to the parasitic inductances is:
$L_{I/O}.dI/dt = L_{GND}.dI/dt = 6 \times 24 = 144$ V

By taking into account the effect of these parasitic inductances due to unsuitable layout, the clamping voltage will be:

$V_{CL}+ = +31.2 + 144 + 144 = 319.2$ V

$V_{CL}- = -13.1 - 144 - 144 = -301.1$ V

We can reduce as much as possible these phenomena with simple layout optimization.

Figure 16. ESD behavior: parasitic phenomena due to unsuitable layout

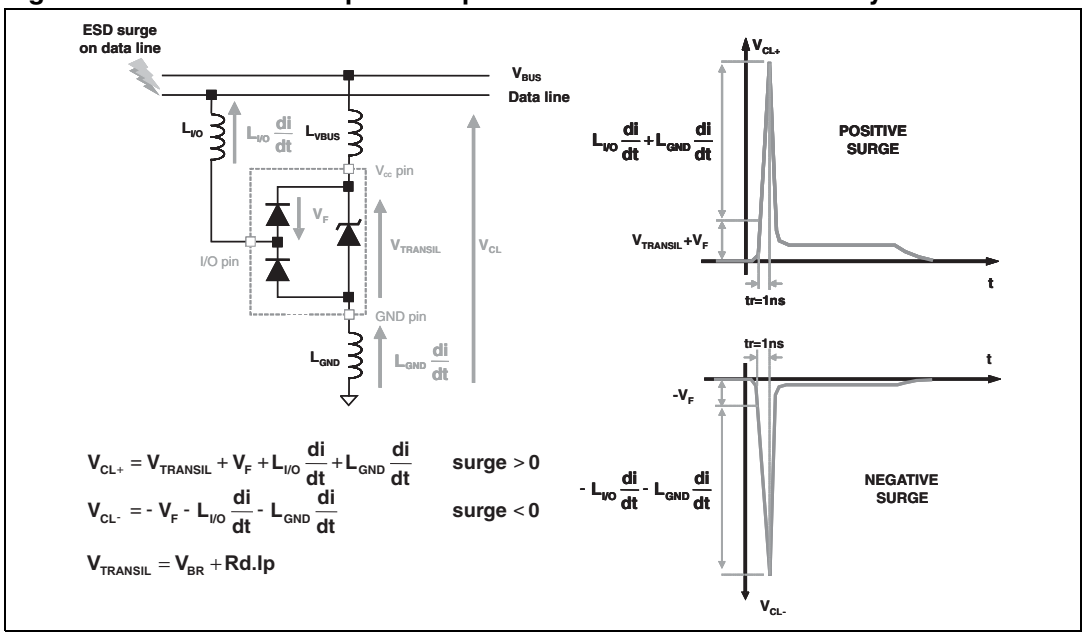


Figure 17. ESD behavior - measurement conditions

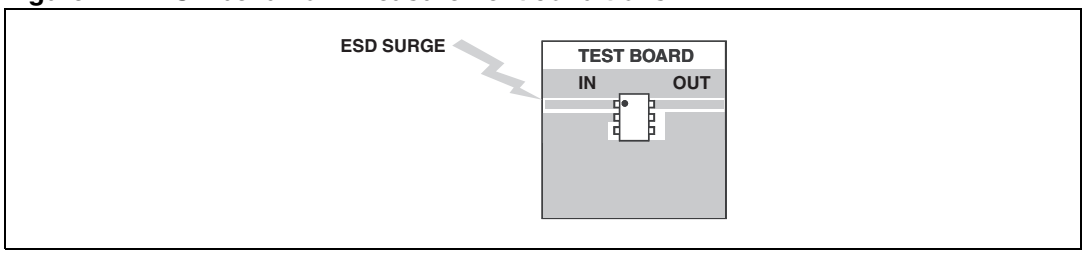


Figure 18. Remaining voltage after the HDMIULC6-2M6 during positive ESD surge

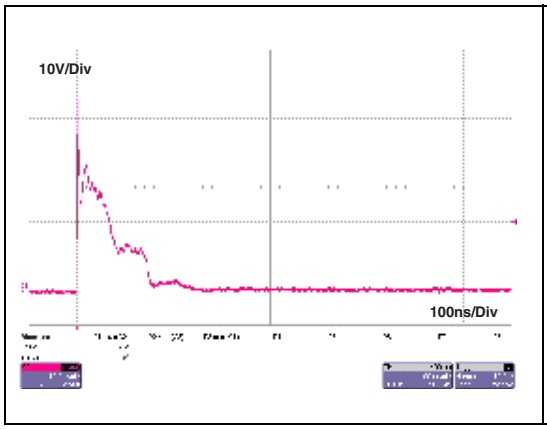


Figure 19. Remaining voltage after the HDMIULC6-2M6 during negative ESD surge

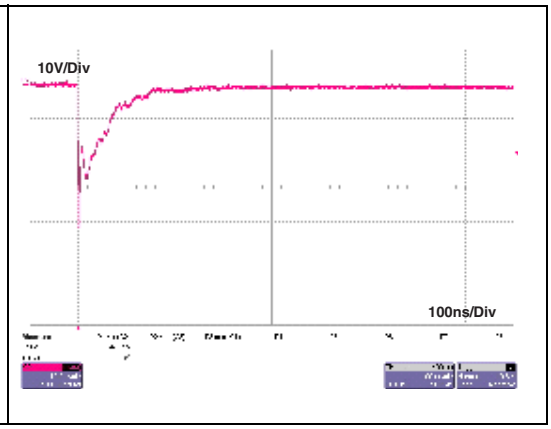


Figure 20. Remaining voltage after the HDMIULC6-2P6 during positive ESD surge

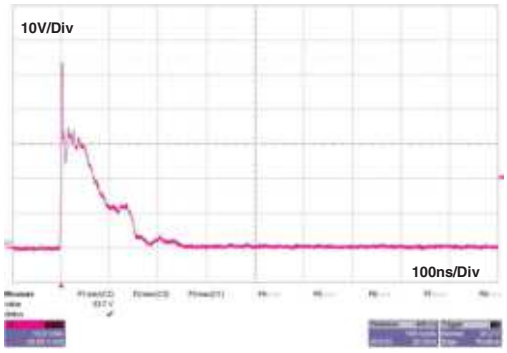
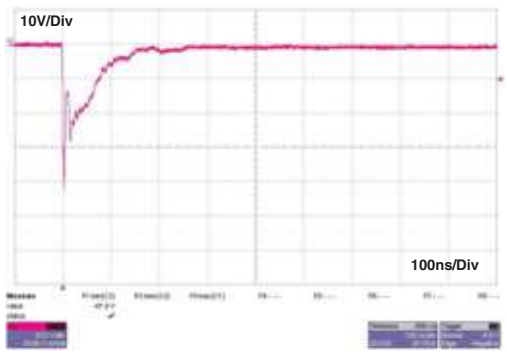


Figure 21. Remaining voltage after the HDMIULC6-2P6 during negative ESD surge

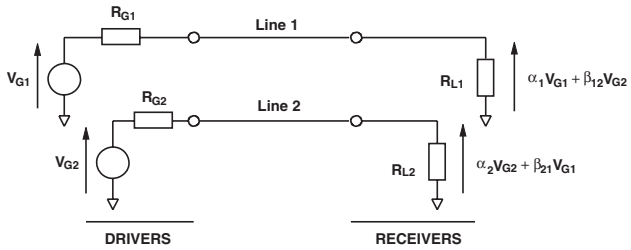


Important

An important precaution to take is to put the protection device as close as possible to the disturbance source (generally the connector).

3.3 Crosstalk behavior

Figure 22. Crosstalk phenomena



The crosstalk phenomena is due to the coupling between 2 lines. The coupling factor (β_{12} or β_{21}) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Figure 23. Analog crosstalk measurements

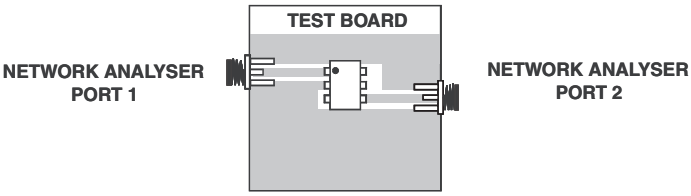


Figure 23 gives the measurement circuit for the analog application. In usual frequency range of analog signals (up to 240 MHz) the effect on disturbed line is less than -40 dB (see *Figure 24* and *Figure 25*).

Figure 24. Analog crosstalk results (typical values) for HDMIULC6-2M6

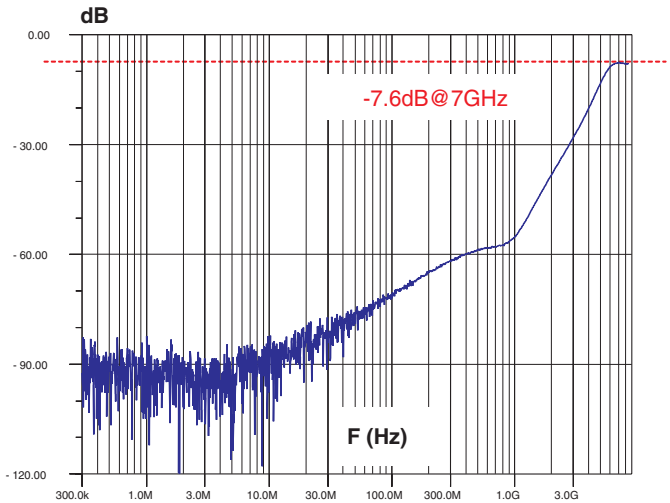
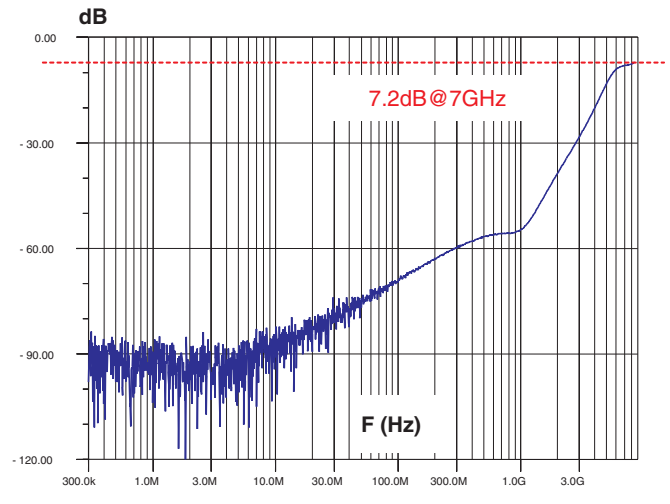


Figure 25. Analog crosstalk results (typical values) for HDMIULC6-2P6

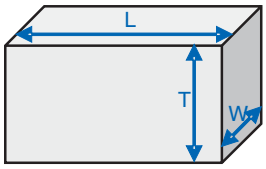


4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness)

Figure 26. Stencil opening dimensions.



   b) General Design Rule

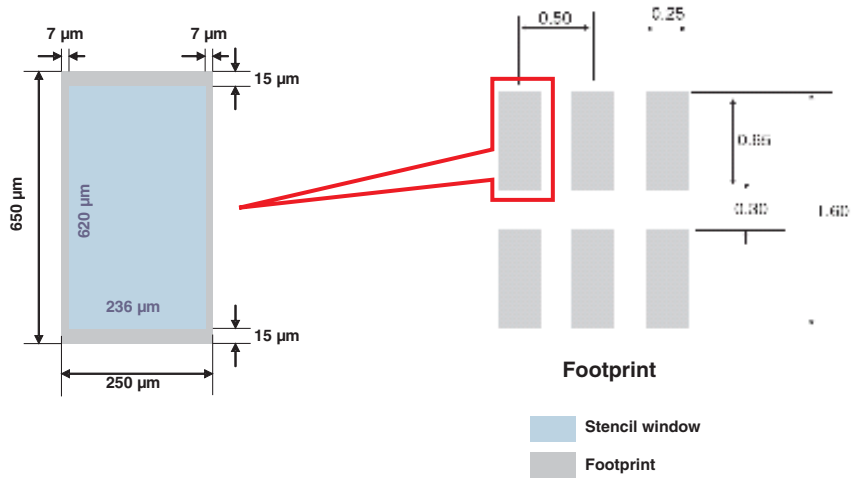
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 27. Recommended stencil window position (µQFN only)



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

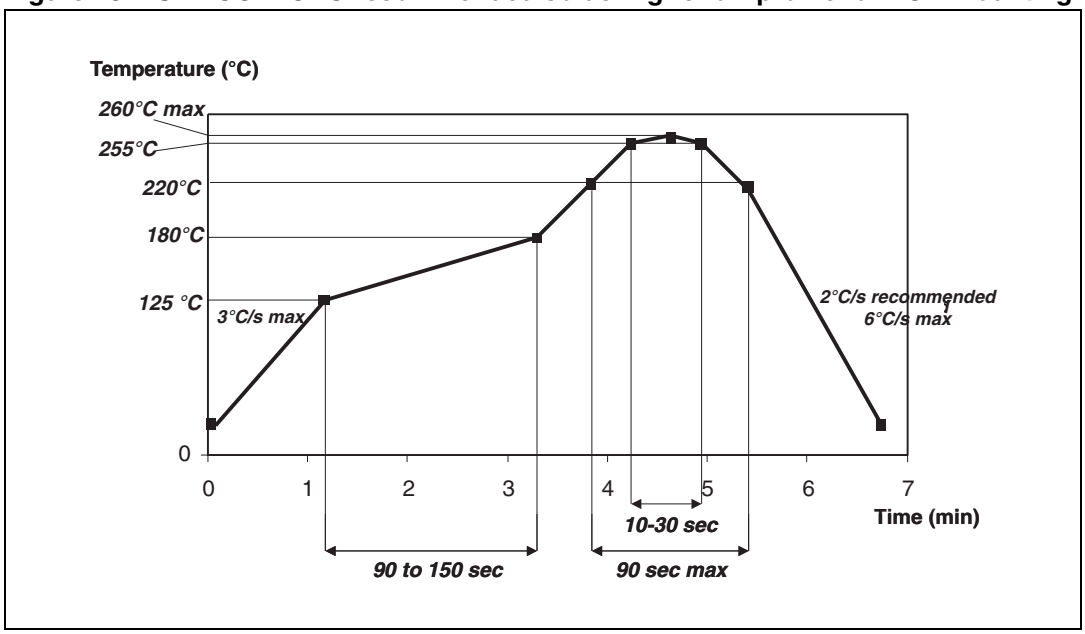
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 28. ST ECOPACK® recommended soldering reflow profile for PCB mounting



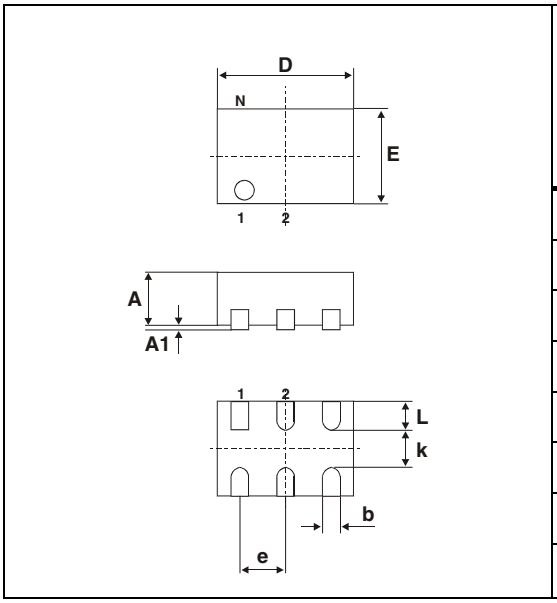
Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Package information

- Epoxy meets UL94, V0

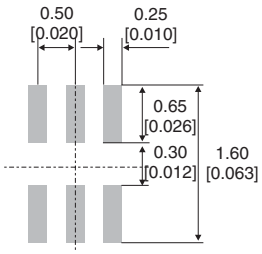
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Table 3. Micro QFN 1.45x1.00 6L dimensions



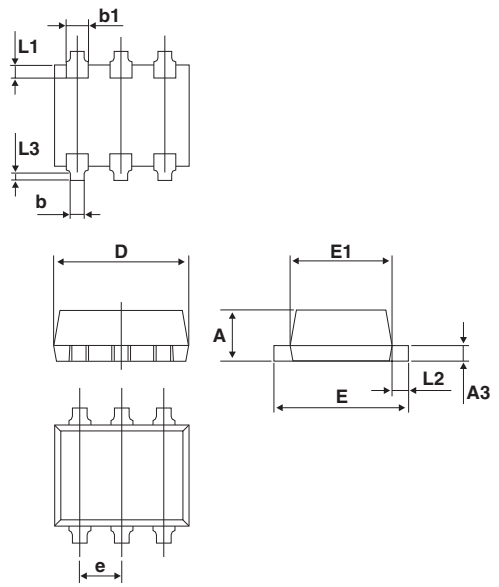
Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
D		1.45			0.057	
E		1.00			0.039	
e		0.50			0.020	
K	0.20			0.008		
L	0.30	0.35	0.40	0.012	0.014	0.016

Figure 29. µQFN 6 leads footprint dimensions in mm [inches]



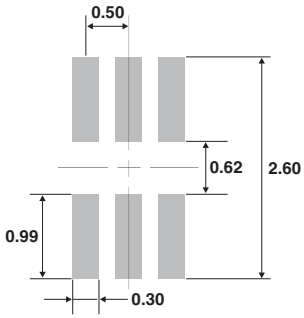
Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Table 4. SOT-666 dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45		0.60	0.018		0.024
A3	0.08		0.18	0.003		0.007
b	0.17		0.34	0.007		0.013
b1	0.19	0.27	0.34	0.007	0.011	0.013
D	1.50		1.70	0.059		0.067
E	1.50		1.70	0.059		0.067
E1	1.10		1.30	0.043		0.051
e		0.50			0.020	
L1		0.19			0.007	
L2	0.10		0.30	0.004		0.012
L3		0.10			0.004	

Figure 30. Footprint (dimensions in mm)



6 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
HDMIULC6-2M6	T(1)	µQFN 6 leads	2.2 mg	3000	Tape and reel
HDMIULC6-2P6	R	SOT-666	2.9 mg	3000	Tape and reel

1. The marking can be rotated by 90° to diferentiate assembly location

7 Revision history

Table 6. Document revision history

Date	Revision	Description of changes
06-May-2008	1	First issue.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2008 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com