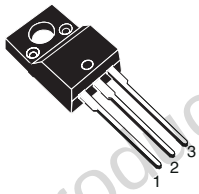
STP5NK65ZFP

N-channel 650 V, 1.5 Ω, 4.5 A TO-220FP Zener-protected SuperMESH™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	Pw
STP5NK65ZFP	650 V	< 1.8 Ω	4.5 A	25 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability
- Improved ESD capability



TO-220FP

Applications

- Switching application

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products

Figure 1. Internal schematic diagram

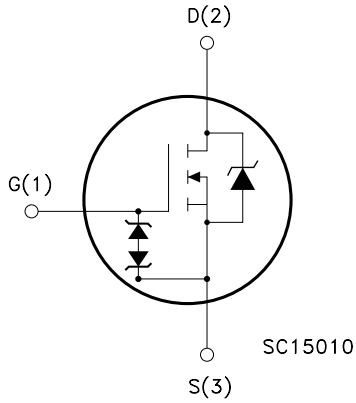


Table 1. Device summary

Order codes	Marking	Package	Packaging
STP5NK65ZFP	P5NK65ZFP	TO-220FP	Tube

Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	650	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	4.5 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	3.1 (1)	A
I_{DM} (2)	Drain current (pulsed)	18 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	25	W
	Derating factor	0.6	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100 pF, R=1.5 kΩ)	2000	V
dv/dt (3)	Peak diode recovery voltage slope	4.5	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)	2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	V

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq$ 5.7 A, di/dt $\leq$ 200 A/µs, VDD =80% $V_{(BR)DSS}$.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case Max	5	V
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient Max	62.5	V
T_l	Maximum lead temperature for soldering purpose	300	A

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4.2	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	170	mJ

Obsolete Product(s) - Obsolete Product(s)

2 Electrical characteristics

(Tcase =25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D =1 mA, V_{GS} = 0	650	-	-	V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS}=max rating V_{DS}=max rating @125 °C	-	-	1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V	-	-	±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.1 A	-	1.5	1.8	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =10 V, I_D = 2.1 A	-	5	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1MHz, V_{GS} = 0	-	680 80 17	-	pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	98	-	pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 4.5 A, V_{GS} = 10 V *Figure 16*	-	25 4.4 13.7	35	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 325 V, I_D = 2.1 A, R_G = 4.7 Ω, V_{GS} = 10 V *Figure 15*	-	20 15 140 40	-	ns ns ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	V_{DD} = 325 V, I_D = 2.1 A, R_G = 4.7 Ω, V_{GS} = 10 V *Figure 15*	-	12 7 15	-	ns ns ns

Obsolete Product(s) - Obsolete Product(s)

Table 8. Source Drain Diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-	-	4.5 18	A A
V_{SD} (2)	Forward On voltage	I_{SD} = 4.5 A, V_{GS} = 0	-	-	1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4.5 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C *Figure 20*	-	375 1.76 10	-	ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1mA (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

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2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

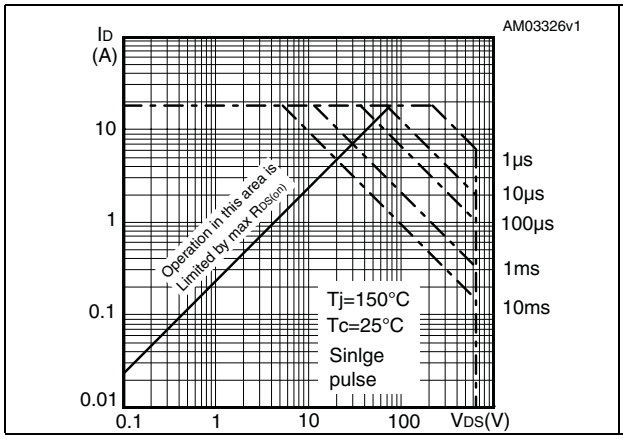


Figure 3. Thermal impedance

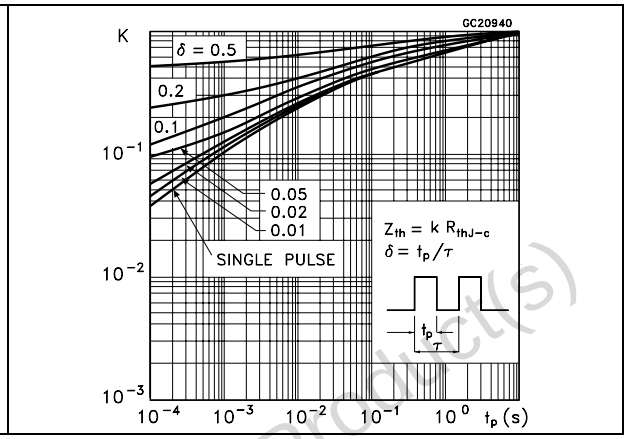


Figure 4. Output characteristics

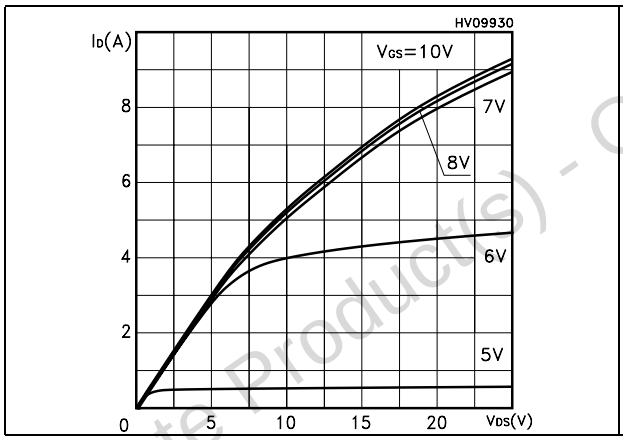


Figure 5. Transfer characteristics

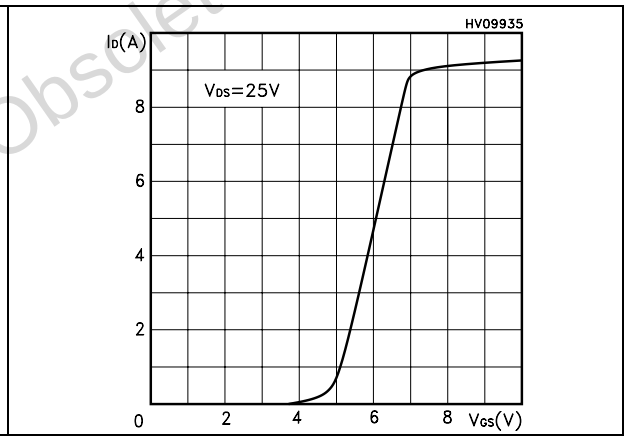


Figure 6. Transconductance

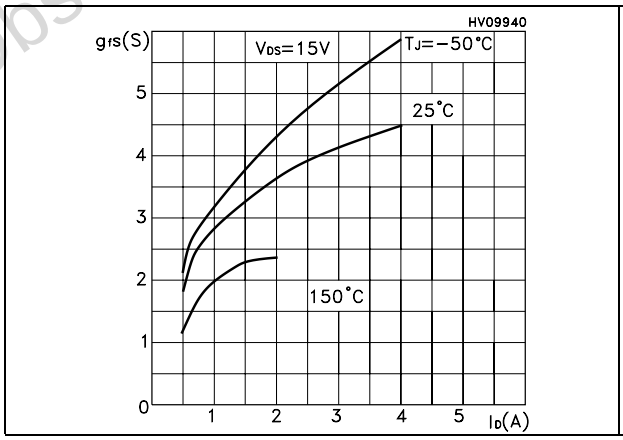
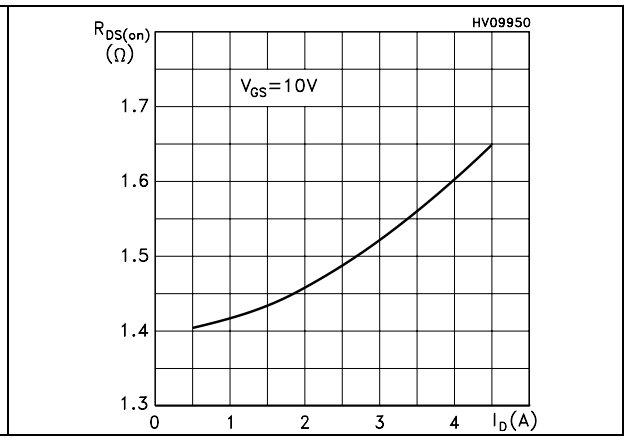


Figure 7. Static drain source on resistance



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Figure 8. Gate charge vs gate-source voltage

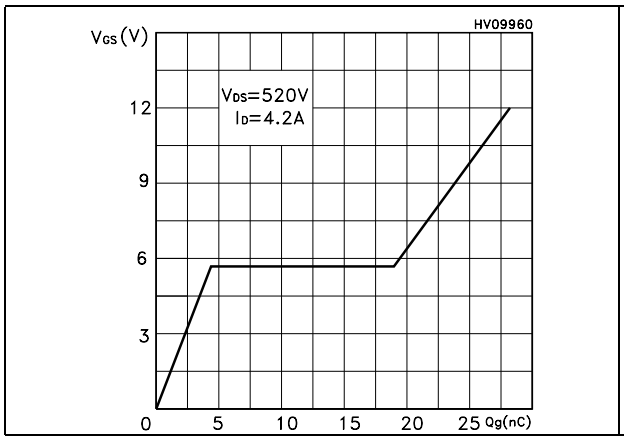


Figure 9. Capacitance variations

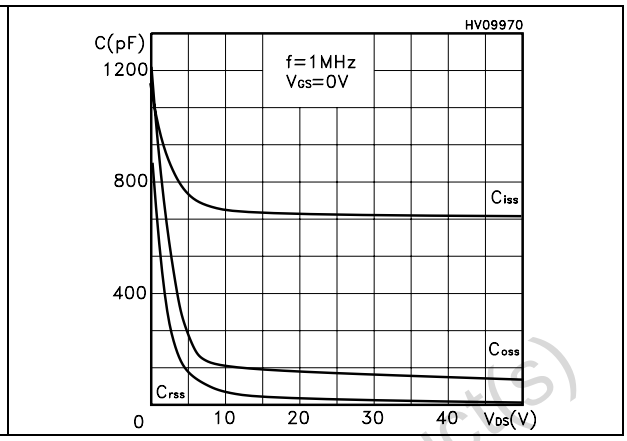


Figure 10. Normalized gate threshold voltage vs temperature

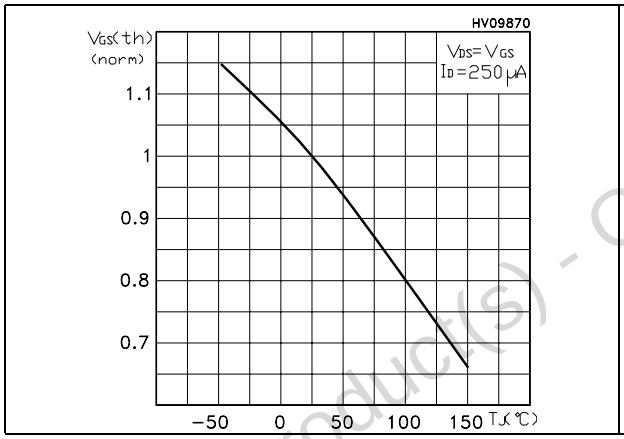


Figure 11. Normalized on resistance vs temperature

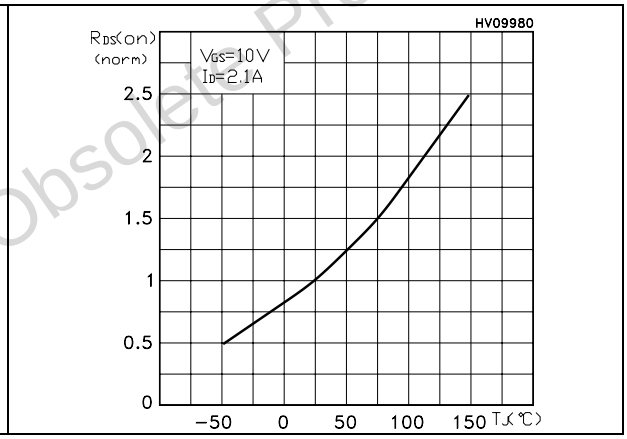


Figure 12. Source-drain diode forward characteristics

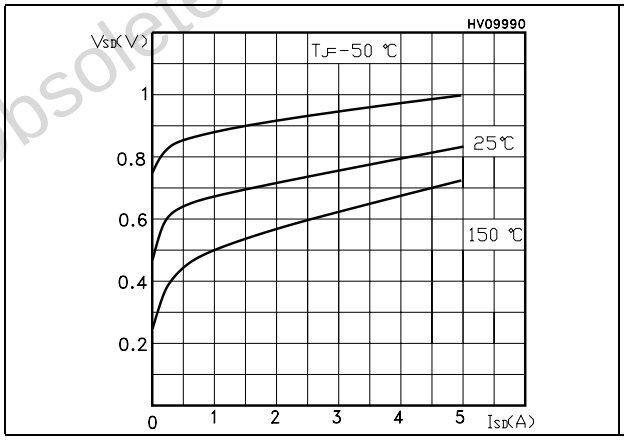
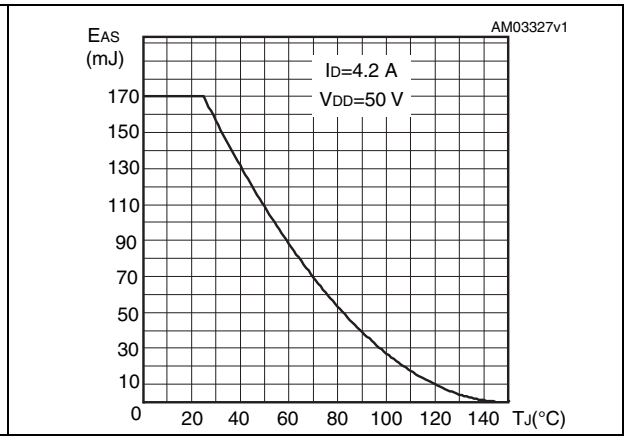
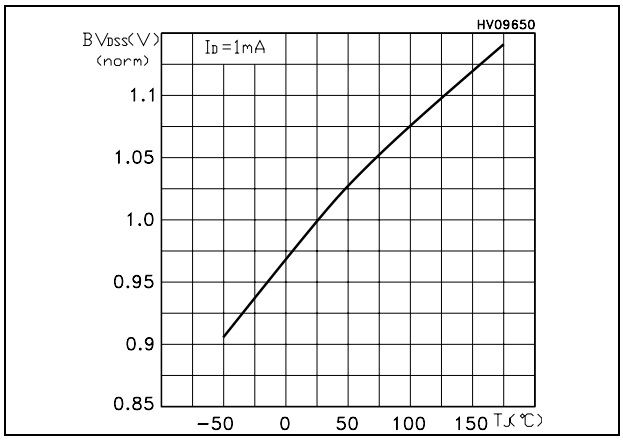


Figure 13. Avalanche energy vs starting Tj



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Figure 14. Normalized BV_{DSS} vs temperature



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3 Test circuits

Figure 15. Switching times test circuit for resistive load

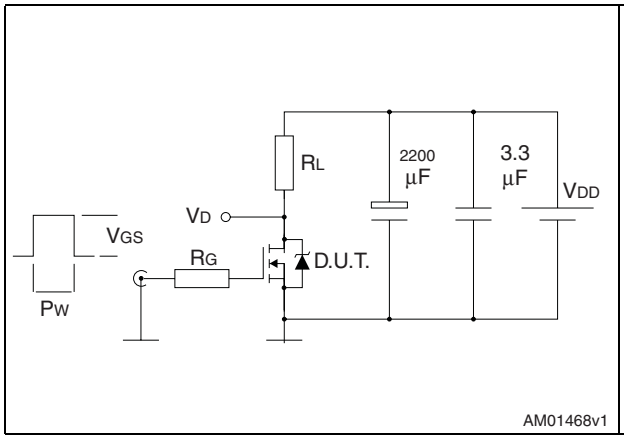


Figure 16. Gate charge test circuit

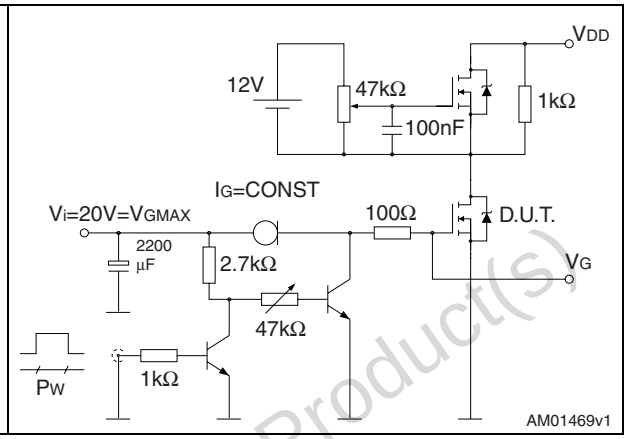


Figure 17. Test circuit for inductive load switching and diode recovery times

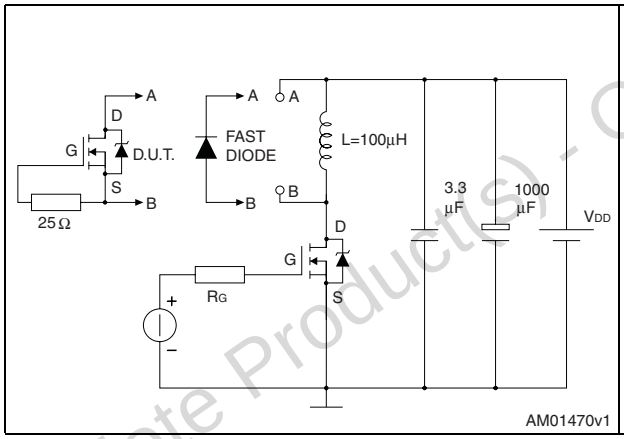


Figure 18. Unclamped inductive load test circuit

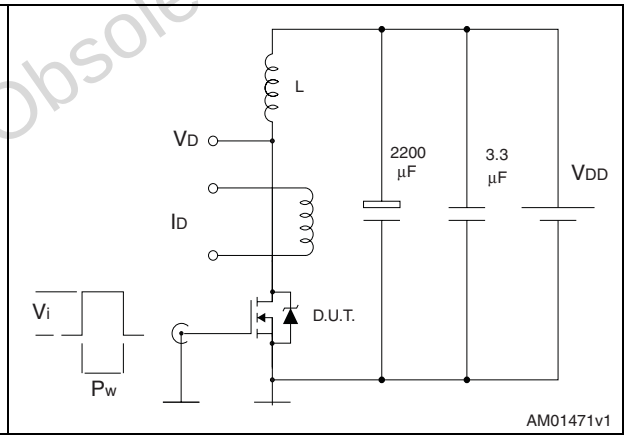


Figure 19. Unclamped inductive waveform

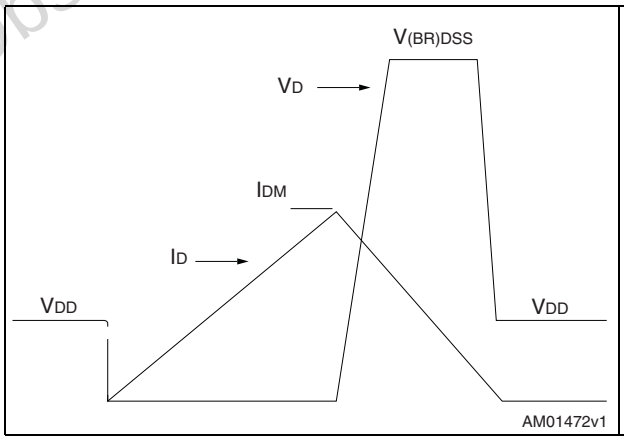
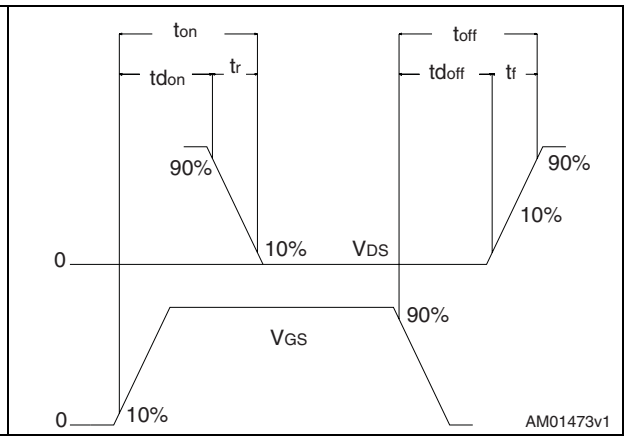


Figure 20. Switching time waveform



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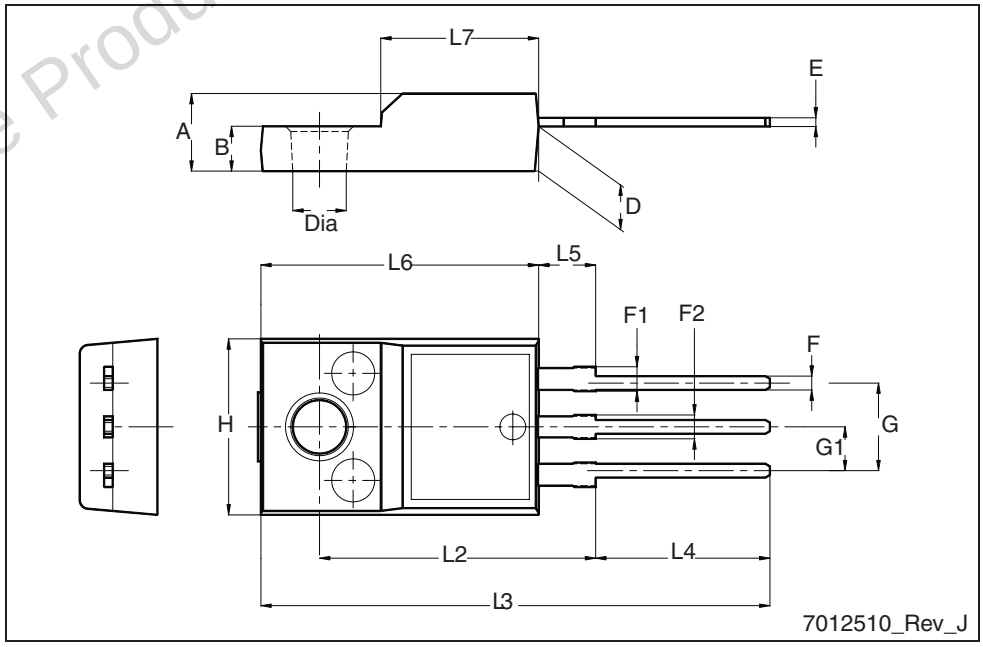
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

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TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.5
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



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5 Revision history

Table 10. Document revision history

Date	Revision	Changes
16-Apr-2009	1	First issue

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