VIPER25

Datasheet

Off-line high voltage converters



SO16 Narrow

Product status link

VIPER25

Product label

SUSTAINABLE TECHNOLOGY

Features

- 800 V avalanche rugged power section
- Quasi-resonant (QR) control for valley switching operation
- Standby power < 50 mW at 265 Vac
- Limiting current with adjustable set point
- Adjustable and accurate overvoltage protection
- On-board soft-start
- Safe auto-restart after a fault condition
- Hysteretic thermal shutdown

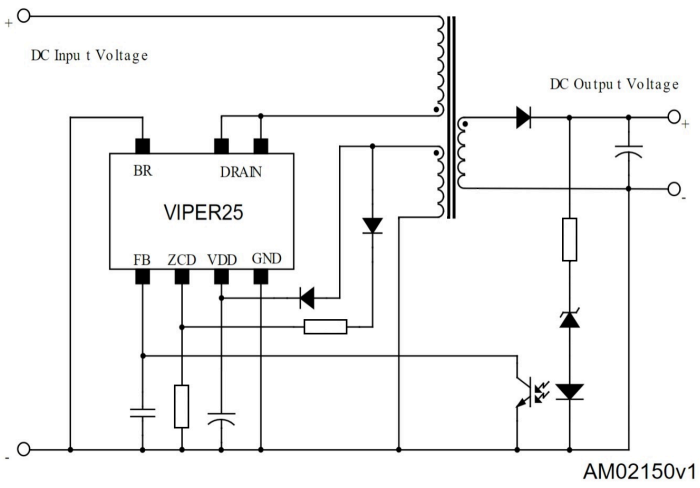
Application

- Adapters for PDA, camcorders, shavers, cellular phones, cordless phones, videogames
- Auxiliary power supply for LCD/PDP TV, monitors, audio systems, computer, industrial systems, LED driver, No el-cap LED driver, utility power meter
- SMPS for set-top boxes, DVD players andrecorders, white goods

Description

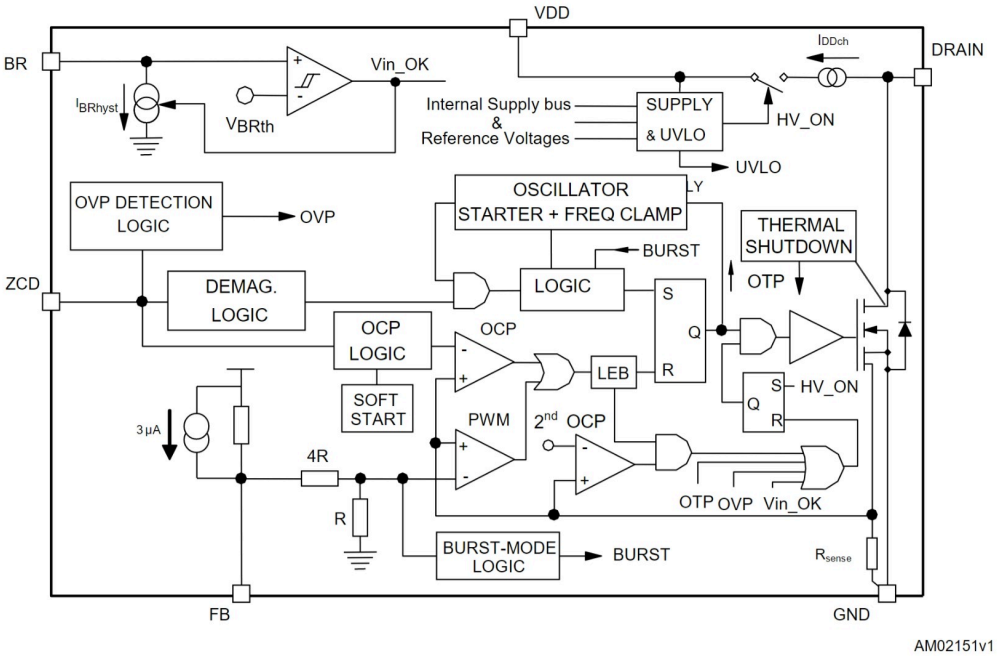
VIPER25 is an off-line converter with an 800 V rugged power section, a PWM control, double levels of overcurrent protection, overvoltage and overload protections, hysteretic thermal protection, soft-start and safe auto-restart after any fault condition removal. Burst mode operation and device very low consumption helps to meet the standby energy saving regulations. The quasiresonant feature reduces EMI filter cost. Brownout and brown-in function protects the switch mode power supply when the rectified input voltage level is below the normal minimum level specified for the system. The high voltage start-up circuit is embedded in the device.

Figure 1. Typical topology



1 Block diagram

Figure 2. **Block diagram**



2 Typical power

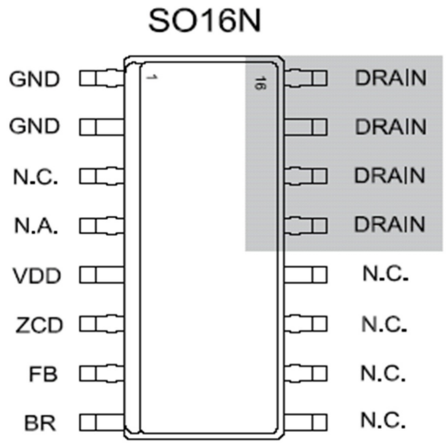
Table 1. Typical power

Part number	230 V_{AC}		85-265 V_{AC}	
	Adapter(1)	Open frame(2)	Adapter (1)	Open frame(2)
VIPER25	18W	20 W	10 W	12 W

1. *Typical continuous power in non ventilated enclosed adapter measured at 50 °C ambient.*
2. *Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heat sinking.*

3 Pin settings

Figure 3. Connection diagram (top view)



Note: The copper area for heat dissipation has to be designed under the DRAIN pins.

Table 2. Pin description

Pin n. SO16	Name	Function
1...2	GND	This pin represents the device ground and the source of the power section.
3	N.C.	Not available for user. It can be connected to GND (pins 1-2) or left not connected.
4	N.A.	Not available for user. It can be connected to GND (pins 1-2) or left not connected.
5	VDD	Supply voltage of the control section. This pin also provides the charging current of the external capacitor during power-up.
6	ZCD	This is a multifunction pin. 1. Input for the zero current detection circuit for transformer demagnetization sensing.(i.e. R_{LIM}, R_{FF}, R_{OVP} and D_{OVP}, Figure 34) 2. User defined drain current limit set-point and voltage feed forward. The resistor, R_{LIM}, connected between ZCD pin and GND causes the current I_{ZCD} and then it limits the static maximum drain current. 3. The resistor R_{FF}, between ZCD pin and the auxiliary winding, performs the feed-forward operation and then the drain current limitation changes according to the converter input voltage. 4. Output overvoltage protection. Avoltage exceeding V_{OVP} threshold, (see Table 7. Controller section), shuts the IC down reducing the device consumption. This function is strobed and digitally filtered for high noise immunity.
7	FB	Control input for duty cycle control. Internal current generator provides bias current for loop regulation. A voltage below the threshold V_{FBbm} activates the burst-mode operation. A level close to the threshold V_{FBlin} means that we are approaching the cycle-by-cycle over-current set point.
8	BR	Brownout protection input with hysteresis. A voltage below the threshold V_{BRth} shuts down (not latch) the device and lowers the power consumption. Device operation restarts as the voltage exceeds the threshold V_{BRth} + V_{BRhyst}. It can be connected to ground when not used.
13...16	DRAIN	High voltage drain pin. The built-in high voltage switched start-up bias current is drawn from this pin too. Pins connected to the metal frame to facilitate heat dissipation.

4 Electrical data

4.1 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{DRAIN}	Drain-to-source (ground) voltage		800	V
E_{AV}	Repetitive avalanche energy (limited by T_J = 150 °C)		5	mJ
I_{AR}	Repetitive avalanche current (limited by T_J=150 °C)		1.5	A
I_{DRAIN}	Pulse drain current (limited by T_J = 150 °C)		3	A
V_{ZCD}	Control input pin voltage (with I_{ZCD} = 1 mA)	-0.3	Self limited	V
V_{FB}	Feedback voltage	-0.3	5.5	V
V_{BR}	Brown-out input pin voltage (with I_{BR} = 0.5 mA)	-0.3	Self limited	V
V_{DD}	Supply voltage (I_{DD} = 25 mA)	-0.3	Self limited	V
I_{DD}	Input current		25	mA
P_{TOT}	Power dissipation at T_A <60 °C (SO16N)		1.5	W
T_J	Operating junction temperature range	-40	150	°C
T_{STG}	Storage temperature	-55	150	°C

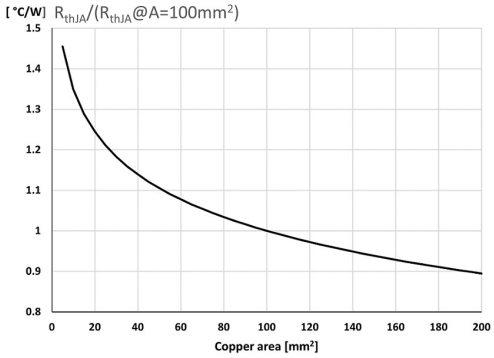
4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value	Unit
R_{TH-JC}	Thermal resistance junction to case (1) (Dissipated power = 1 W)	10	°C/W
R_{TH-JA}	Thermal resistance junction ambient (1) (Dissipated power = 1 W)	120	°C/W
R_{TH-JC}	Thermal resistance junction to case (2) (Dissipated power = 1 W)	5	°C/W
R_{TH-JA}	Thermal resistance junction ambient (2) (Dissipated power = 1 W)	85	°C/W

1. *When mounted on a standard, single side FR4 board with minimum copper area.*
2. *When mounted on a standard, single side FR4 board with 100 mm^2 of Cu (35 µm thick).*

Figure 4. **R_{th_JA} versus copper area**



4.3 Electrical characteristics

(T_J = -25 to 125 °C, V_{DD} = 14 V [(a)]; unless otherwise specified)

Table 5. **Power section**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BVDSS}	Break-down voltage	I_{DRAIN} =1 mA, V_{FB} =GND T_J =25 °C	800			V
I_{OFF}	OFF state drain current	V_{DRAIN}=max rating, V_{FB} =GND			60	µA
$R_{DS(on)}$	Drain-source on state resistance	I_{DRAIN} =0.2 A, V_{FB} =3 V, V_{BR} = GND, T_J= 25 °C			7	Λ
		I_{DRAIN} =0.2 A, V_{FB} =3 V, V_{BR} = GND, T_J= 125 °C			14	Λ

Table 6. **Supply section**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Voltage						
V_{DRAIN_START}	Drain-source start voltage		60	80	100	V
I_{DDch}	Start-up charging current	V_{DRAIN} =120 V, V_{BR} =GND, V_{FB}=GND, V_{DD} = 4V	-2	-3	-4	mA
		V_{DRAIN} =120 V, V_{BR} =GND, V_{FB}=GND, V_{DD} = 4 V after fault.	-0.4	-0.6	-0.8	mA
V_{DD}	Operating voltage range	After turn-on	8.5		23.5	V
$V_{DDclamp}$	V_{DD} clamp voltage	I_{DD}=20 mA	23.5			V
V_{DDon}	V_{DD} start-upthreshold	V_{DRAIN}=120 V, V_{BR} =GND, V_{FB}=GND	13	14	15	V
V_{DDoff}	V_{DD} under voltage shutdown threshold		7.5	8	8.5	V
$V_{DD(RESTART)}$	V_{DD} restartvoltage threshold	V_{DRAIN}=120 V, V_{BR} =GND, V_{FB}=GND	4	4.5	5	V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Current						
I_{DD0}	Operating supply current, not switching	V_{FB} =GND, F_{SW} =0 kHz, V_{BR} =GND, V_{DD}= 10 V			0.9	mA
I_{DD1}	Operating supply current, switching	V_{DRAIN}=120 V,			3.5	mA
I_{DD_FAULT}	Operating supply current, with protection tripping				400	µA
I_{DD_OFF}	Operating supply current with V_{DD} <V_{DDoff}	V_{DD} = 7 V			270	µA

Note: Adjust V_{DD} above V_{DDon} start-up threshold before settings to 14 V.

Table 7. Controller section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Feedback pin						
V_{FBolp}	Over load shutdown threshold		4.5	4.8	5.2	V
V_{FBlin}	Linear dynamics upper limit		3.2	3.3	3.4	V
V_{FBbm}	Burst mode threshold	Voltage falling		0.6		V
$V_{FBbmhys}$	Burst mode hysteresis	Voltage rising		100		mV
I_{FB}	Feedback sourced current	V_{FB} =0.3 V	-150	-200	-280	uA
		3.3 V< V_{FB}< 4.8 V		-3		uA
$R_{FB(DYN)}$	Dynamic resistance	V_{FB} < 3.3 V	14		19	k
H_{FB}	ΔV_{FB} /ΔI_D		2		6	V/A
ZCD pin						
V_{ZCDCLh}	Upper clamp voltage	I_{ZCD} =1 mA	5	5.5	6	V
V_{ZCDAth}	Armingvoltage threshold	Positive-going edge		0.8		V
V_{ZCDTth}	Triggering voltage threshold	Negative-going edge		0.6		V
I_{ZCD}	Internal pull-up			-10		µA
T_{BLANK}	Turn-on inhibit time after MOSFET's turn-off	V_{ZCD} <1 V		6.3		µs
		V_{ZCD} >1 V		2.5		µs
Current limitation						
I_{Dlim}	Max drain current limitation	V_{FB} = 4 V, I_{ZCD} = -10 µA T_J= 25 °C	0.66	0.7	0.74	A
t_{SS}	Softstart time	VIPER25L			3.5	ms
		VIPER25H			4.2	ms
t_{SU}	Start up time	VIPER25L	7.5		15	ms
		VIPER25H	9.5		18	ms

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{ON_MIN}	Minimum turn ON time		220	400	480	ns
t_d	Propagation delay			100		ns
t_{LEB}	Leading edge blanking			300		ns
I_{D_BM}	Peak drain current duringburst mode	V_{FB} =0.6 V		160		mA
Overcurrent protection (2nd OCP)						
I_{DMAX}	Second overcurrent threshold			1.2		A
Overvoltage protection						
V_{OVP}	Overvoltage protection threshold		3.8	4.2	4.6	V
T_{STROBE}	Overvoltage protection strobe time			2.2		µs
Oscillator section						
F_{OSClim}	Internal frequency limit	VIPER25L	122	136	150	kHz
	Internal frequency limit	VIPER25H	200	225	250	kHz
$F_{STARTER}$	Starter frequency	V_{FB}=1 V, V_{ZCD}<$V_{ZCDT\ th}$ t<t_{SU}		1/4 FOSClim		kHz
		V_{FB}=1 V, V_{ZCD}<$V_{ZCDT\ th}$ t>t_{SU}		1/8 FOSClim		kHz
F_{OSCmin}		V_{FB} =1 V, V_{ZCD} >V_{ZCDA_th}		1/64 FOSClim		kHz
Brown-out protection						
V_{BRth}	Brown-out threshold	Voltage falling	0.41	0.45	0.49	V
V_{BRhyst}	Voltage hysteresis above VBRth	Violate rising		50		mV
I_{BRhyst}	Current hysteresis		7		12	µA
$V_{BRclamp}$	Clamp voltage	I_{BR} = 250 µA		3		V
V_{DIS}	Brown-out disable voltage		50		150	mV
Thermal shutdown						
T_{SD}	Thermal shutdown temperature		150	160		°C
T_{HYST}	Thermalshutdownhysteresis			30		°C

Figure 5. **Minimum turn-on time test circuit**

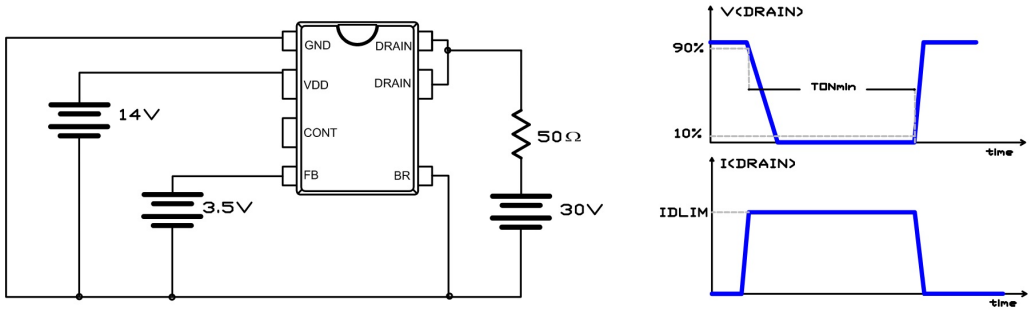


Figure 6. **Brown-out threshold test circuits**

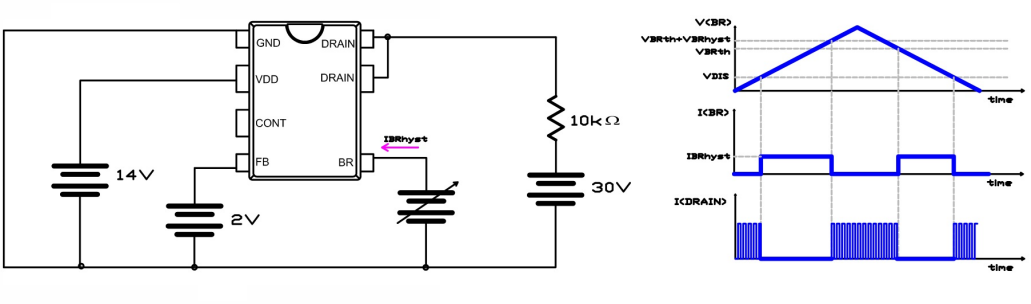
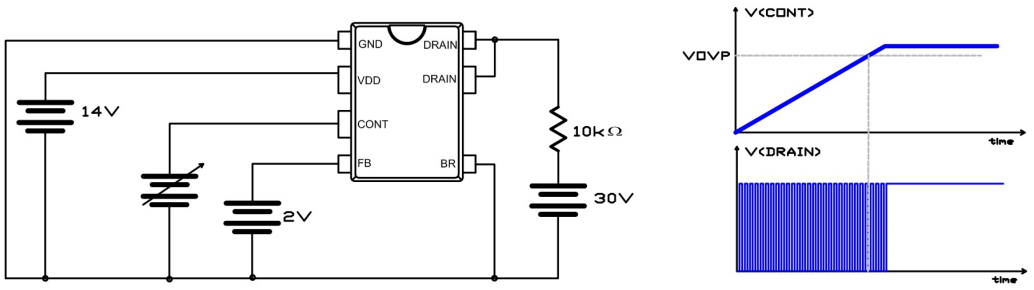


Figure 7. **OVP threshold test circuits**



Note: Adjust V_{DD} above V_{DDon} start-upthreshold before settings to 14 V

5 Typical electrical characteristics

Figure 8. Current limit vs T_J

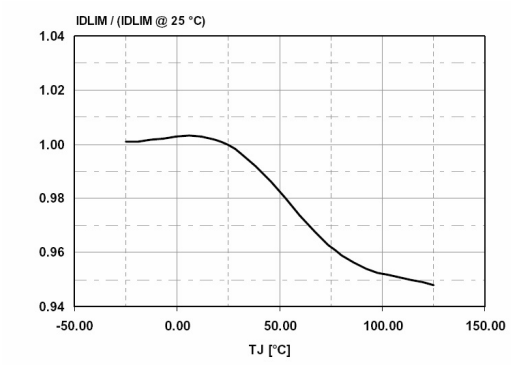


Figure 9. Drain start voltage vs T_J

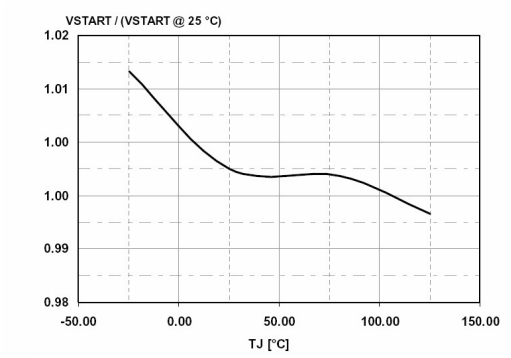


Figure 10. HFB vs T_J

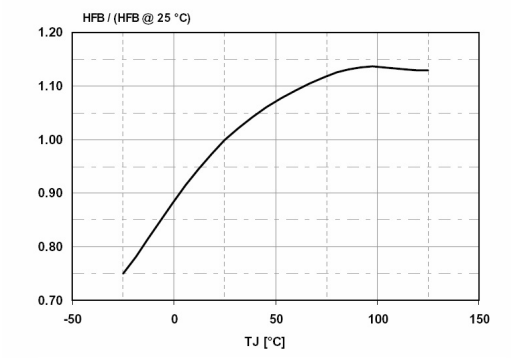


Figure 11. Brown-out threshold vs T_J

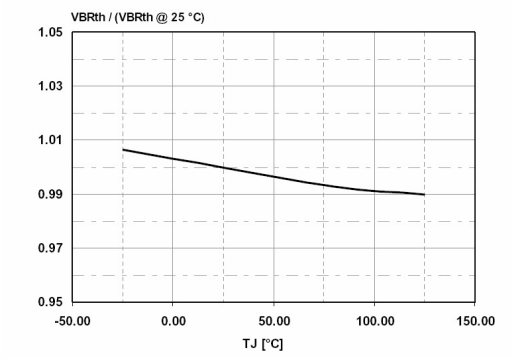


Figure 12. Brown-out hysteresis vs TJ

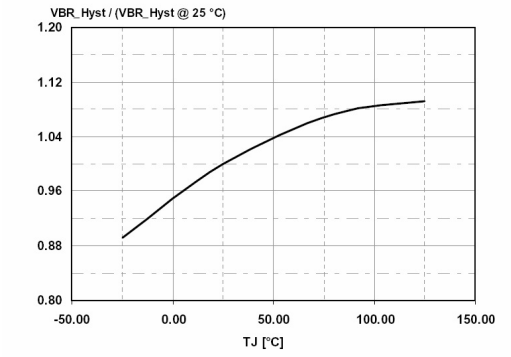


Figure 13. . Brown-out hysteresis current vs T_J

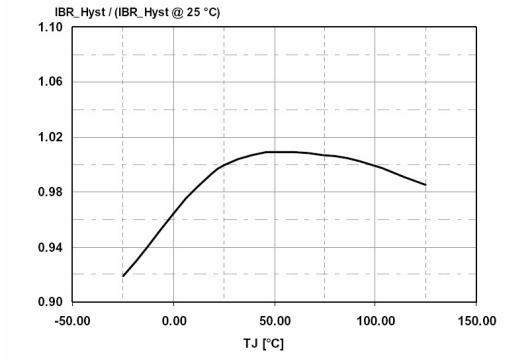


Figure 14. Operating supply current (no switching) vs T_J

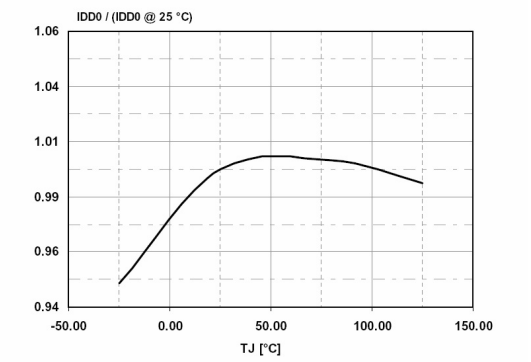


Figure 15. Operating supply current (switching) vs TJ

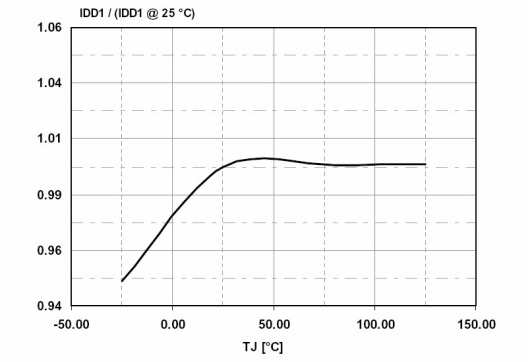


Figure 16. V_{ZCD} vs I_{ZCD}

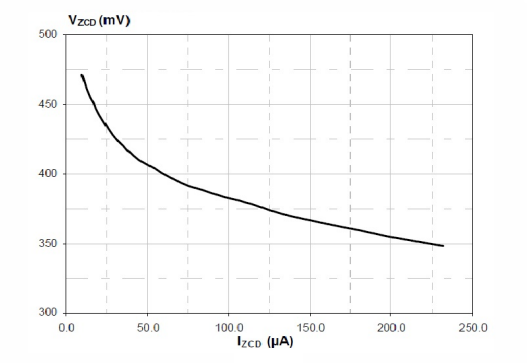


Figure 17. Current limit vs I_{ZCD}

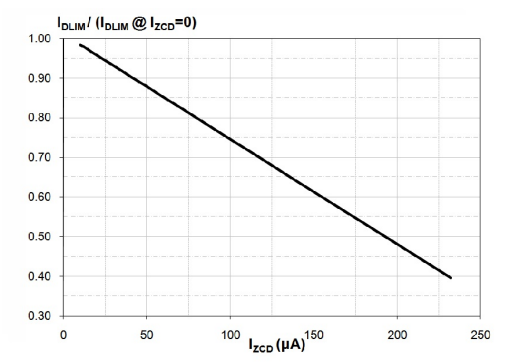


Figure 18. Power MOSFET on-resistance vs T_J

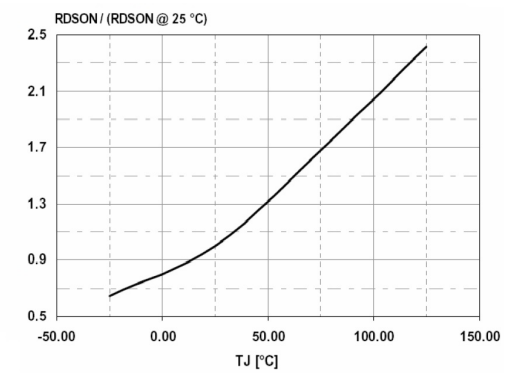


Figure 19. Power MOSFET break down voltage vs T_J

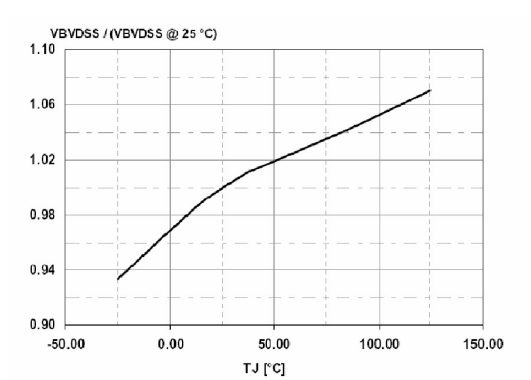


Figure 20. COSS characteristic

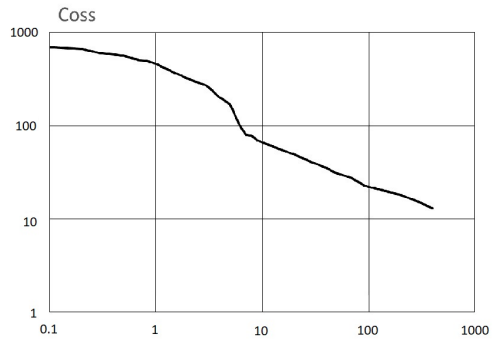
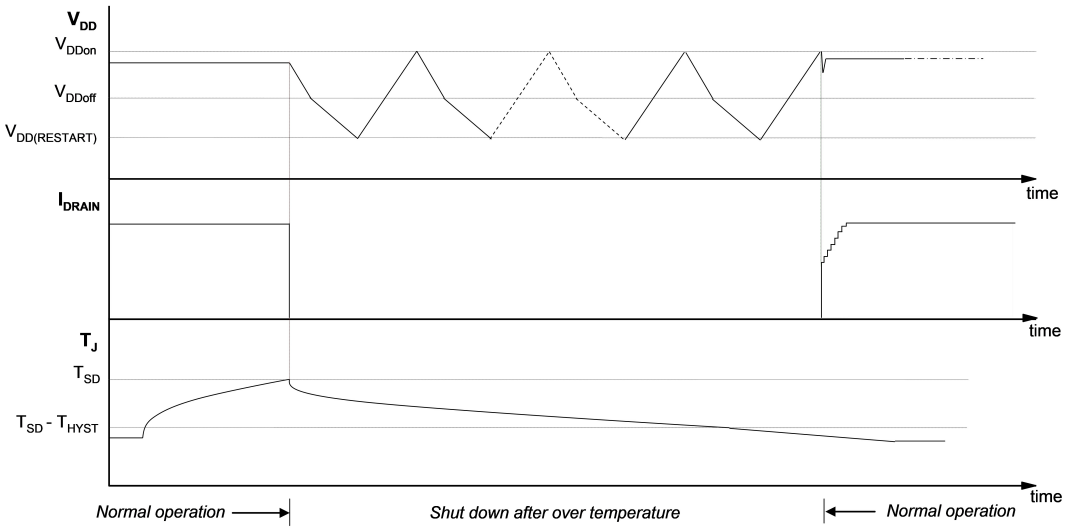


Figure 21. Thermal shutdown



6 Typical circuits

Figure 22. **Min-features QR flyback application**

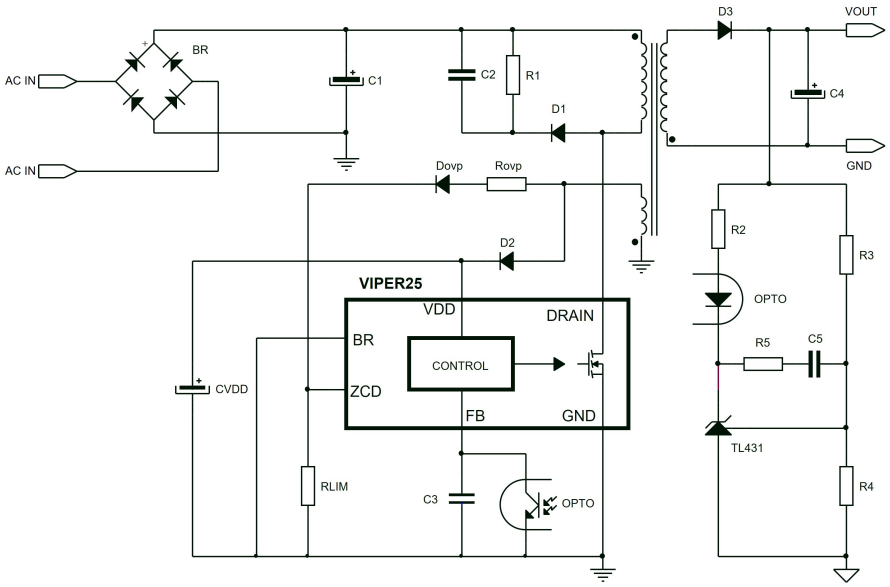
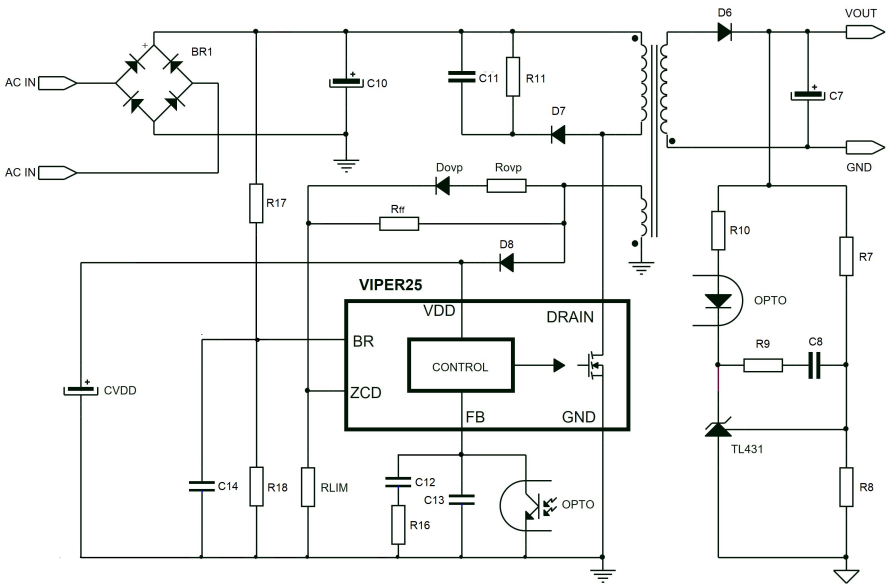


Figure 23. **Full-features QR flyback application**



7 Operation description

VIPER25 is a high-performance low-voltage PWM controller IC with an 800 V, avalanche rugged power section.

The controller includes the current-mode PWM logic and the ZCD (zero current detect) circuit for QR operation, the start-up circuitry with soft-start feature, an oscillator for frequency foldback function, the current limit circuit with adjustable set point, the second overcurrent circuit, the burst mode management circuit, the brown-out circuit, the UVLO circuit, the auto-restart circuit and the thermal shutdown circuit.

The current limit set-point is set by the ZCD pin. The burst mode operation guaranties high performance in the stand-by mode and helps in the energy saving norm accomplishment.

All the fault protections are built in auto-restart mode with very low repetition rate to prevent IC's over heating.

7.1 Power section and gate driver

The power section is implemented with an avalanche ruggedness N-channel MOSFET, which guarantees safe operation within the specified energy rating as well as high dv/dt capability. The power section has a B_{VDSS} of 800 V min. and a typical $R_{DS(on)}$ of 7 Ω at 25 °C.

The integrated SenseFET structure allows a virtually loss-less current sensing.

The gate driver is designed to supply a controlled gate current during both turn-on and turn- off in order to minimize common mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the power section cannot be turned on accidentally.

7.2 High voltage startup generator

The HV current generator is supplied through the DRAIN pin and it is enabled only if the input bulk capacitor voltage is higher than V_{DRAIN_START} threshold, reported on Table 6. When the HV current generator is ON, the I_{DDch} current (see Table 6) is delivered to the capacitor on the V_{DD} pin. In case of Auto-restart mode after a fault event, the I_{DDch} current is reduced to 0.6 mA, in order to have a slow duty cycle during the restart phase.

7.3 Power-up description

Ifthe input voltage rises up till the device start level, V_{DRAIN_START}, the V_{DD} voltage begins to grow due to the I_{DDch} current (see Table 6) coming from the internalhigh voltage start-up circuit. If the V_{DD} voltage reaches the V_{DDon} threshold (See Table 6) the power MOSFET starts switching and the HV current generator is turned OFF, see Figure 25.

The IC is powered by the energy stored in the capacitor on the V_{DD} pin, C_{VDD}, until when the self-supply circuit (typically an auxiliary winding of the transformer and a steering diode) develops a voltage high enough to sustain the operation.

C_{VDD} capacitor must be sized enough to avoid fast discharge and keep the needed voltage value higher than V_{DDoff} threshold. In fact, a too low capacitance value could terminate the switching operation before the controller receives any energy from the auxiliary winding.

The following formula can be used for the V_{DD} capacitor calculation:

Equation 1

$$C_{VDD} = \frac{I_{DDch} \cdot t_{SSaux}}{V_{DDon} - V_{DDoff}} \quad (1)$$

The t_{SSaux} is the time needed for the steady state of the auxiliary voltage. This time is estimated by applicator according to the output stage configurations (transformer, outputcapacitances, etc.).

During normal operation, the power MOSFET is switched ON immediately after transformerdemagnetization, detected by the VIPER25, through the voltage V_{ZCD} sensed on the ZCD pin. At power up the initial output voltage is zero and then the voltage V_{ZCD} is not high enough to correctly arm the internal ZCD circuit. In this case, the power MOSFET is turned ON with a fixed frequency determined by the internal oscillator. This fixed switching frequency is $F_{STARTER}$ (see Table 7). As soon as the voltage on ZCD pin is able to arm the ZCD circuit (i.e. its positive value exceeds V_{ZCDAth}), the turn-on of the power MOSFET is driven by this circuit and is no more related to the internal oscillator (except for the frequency fold-back function).

The start-up phase is managed by a dedicated internal logic and is activated every time the device exits from UVLO because the V_{DD} voltage exceeds the threshold V_{DDon}. An internal timing (t_{SU}, see Table 7) defines the end of the start-up phase.

During the first part of the start-up phase soft start takes place: the drain peak current is increased cycle-by-cycle from zero as far as the maximum value, I_{Dlim}, (see Figure 26 or Figure 27). The duration of soft-start is t_{SS}, (t_{SS} < t_{SU}, see Table 7).

During soft-start and until the output voltage reaches its regulated value, the feedback loop is open. To prevent an improper activation of the OLP function (see Section 7.13) during soft-start and until the start-up phase is over (t = t_{SU}), the feedback voltage is clamped at V_{FBlin} (see Figure 26).

In this way, the feedback voltage can exceed V_{FBlin} and ramp up as far as the overload threshold, V_{FBolp} (see Figure 27), which would activate the OLP function, only at the end of the start-up phase (t > t_{SU}) if the output voltage is still below the regulated value.

As soon as the output voltage reaches the regulatedvalue, the regulation loop takes over and the drain current is regulated below its limit, I_{Dlim}, by the feedback voltage, which settles at a value lower than the threshold V_{FBlin}.

Figure 24. I_{DD} current during start-up and burst mode

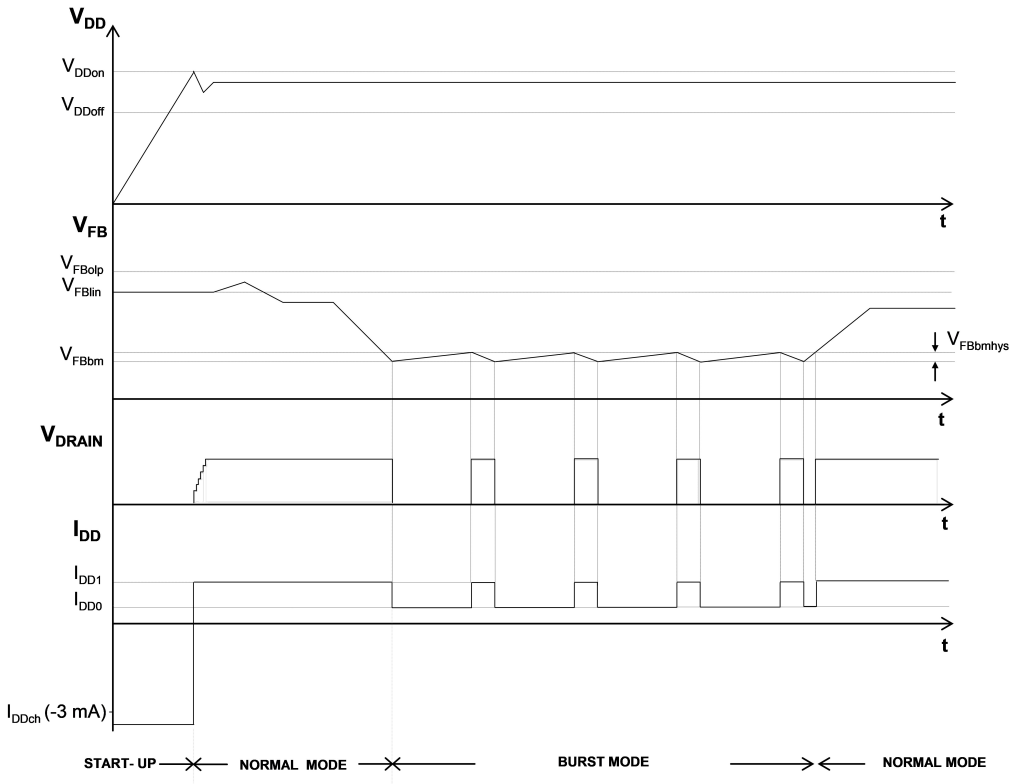


Figure 25. **Timing diagram: normal power-up and power-down sequences**

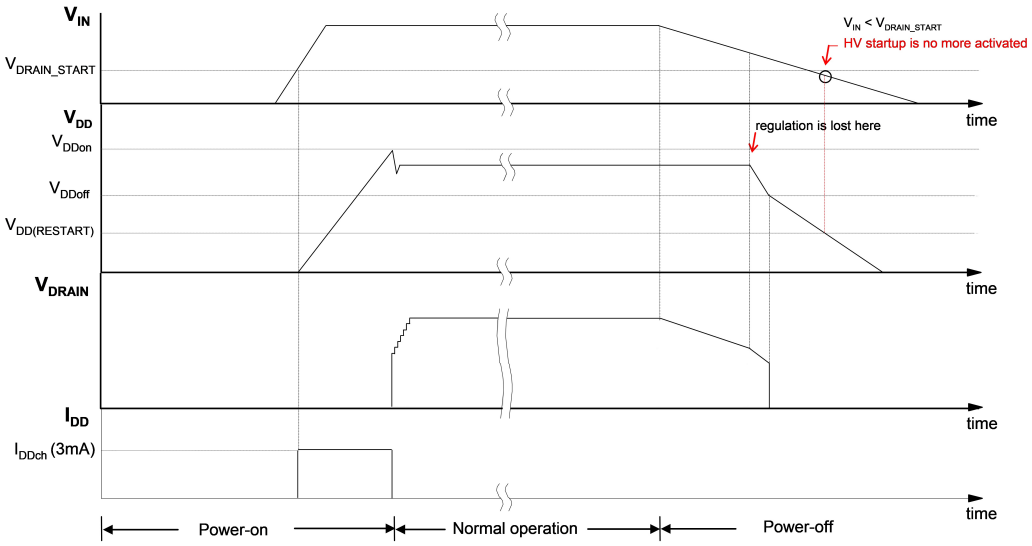


Figure 26. **Timing diagram: Start-up phase and soft start (case 1)**

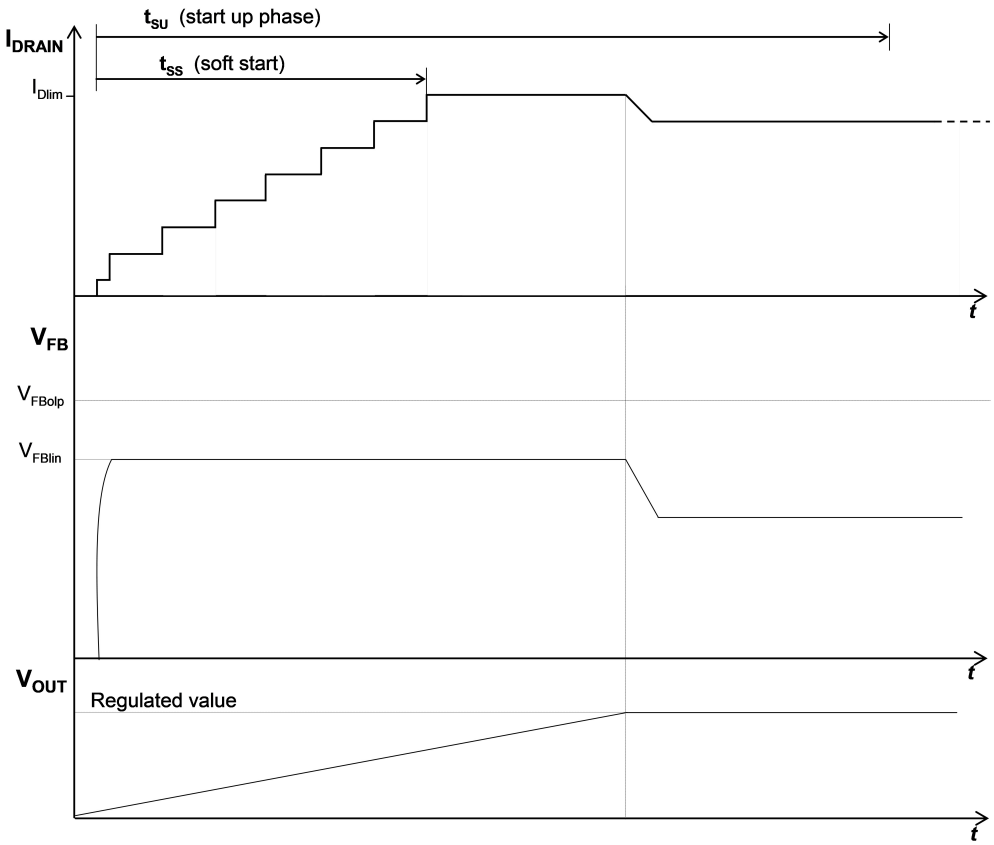
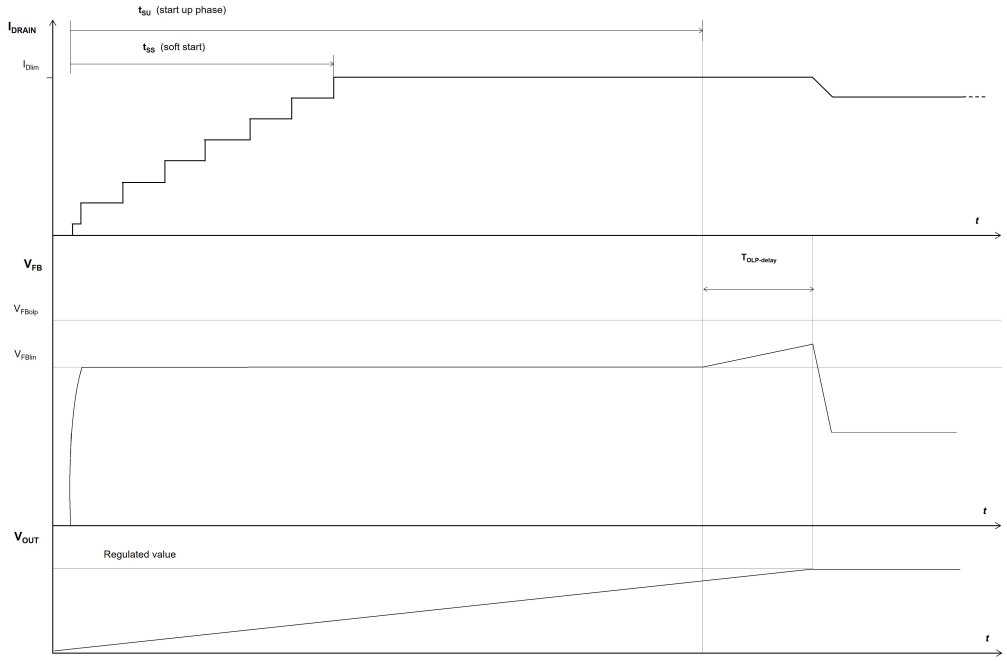


Figure 27. **Timing diagram: Start-up phase and soft start (case 2)**



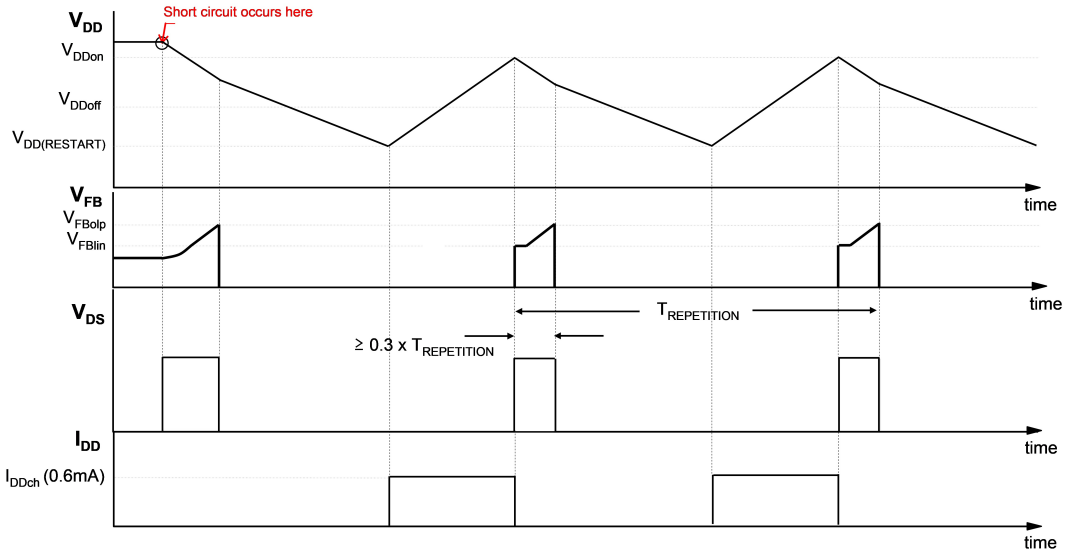
7.4 Power-down description

At converter power-down, the system loses regulation as soon as the input voltage is so low that thepeak currentlimitation is reached. The V_{DD} voltage drops and when it falls below the V_{DDoff} threshold the power MOSFET is switched OFF, the energy transfers to the IC is interrupted and consequently the V_{DD} voltages decreases, see Figure 25. Later, if the V_{IN} is lower than the threshold V_{DRAIN_START}, the start-up sequence is inhibited and the power-down completed. This feature is useful to prevent converter's restart attempts and ensures monotonic outputvoltage decay during the system power-down.

7.5 Auto-restart description

If after a converter power-down, the V_{IN} is higher thanV_{DRAIN_START}, the power-up sequence is not inhibited and will be activatedonly whentheV$_{DD}$ voltage drops down the $V_{DD(RESTART)}$ threshold (reported on Table 6). This means that the HV start-up current generator restarts the V_{DD} capacitor charging only when the V_{DD} voltage drops below $V_{DD(RESTART)}$. The scenario above described is for instance a power-down because of a fault condition. After a fault condition, the charging current, I_{DDch}, is reduced to 0.6 mA instead of 3 mA of the normal power-up converter phase. This feature together with the low $V_{DD(RESTART)}$ threshold (reported on Table 6) ensures that, after a fault, the restart attempts of the IC has a very long repetition rate and the converter works safely with extremely low power throughput. The Figure 28 shows the IC behavioral after a short circuit event.

Figure 28. **Timing diagram: behavior after short circuit**



7.6 Quasi-resonant operation

The control core of theVIPER25 is a current-mode PWM controller with a the zero current detection circuit designed for Quasi-Resonant (QR) operation, a technique that provides the benefits of minimum turn-on losses, low EMI emission and safe behavior in case of short circuit. At heavy load the converter operates in quasi-resonant mode: operation lies in synchronizing MOSFET's turn-on to the transformer's demagnetization by detecting the resulting negative-going edge of the voltage across any winding of the transformer. The system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer and the switching frequency will be different for different line/load conditions. See the hyperbolic-like portion reported in Figure 29.

At medium/ light load, depending also from the converter input voltage, the device enters in Valley-skipping mode. The internal oscillator, synchronized to MOSFET's turn-on, defines the maximum operating frequency of the converter, F_{OSClim}.

The VIPER25 is available as type 'L' or type 'H', depending from the value of F_{OSClim}, see Table 7. During the normal operation the converter works with a frequency below F_{OSClim}, so the 'L' type is suitable for application where the priority is on the EMI filter minimization. The 'H' type is suitable when an extended QR operation range is a plus or the priority is the transformer size reduction.

As the load is reduced, and the switching frequency tends to exceeds the limit F_{OSClim}, MOSFET's turn-on will not any more occur on the first valley but on the second one, the third one and so on, see Figure 31. In this way a "frequency clamp" effect is achieved, piecewise linear portion in Figure 29.

When the load is extremely light or disconnected, the converter enters in burst mode operation, see the relevant Section 7.14 . Decreasing the load will then result in frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations or recommendations. Being the peak current low enough, no issue of audible noise.

The above mentioned way of operation is based on the ZCD pin. This pin is the input of the integrated ZCD circuit which allows the power section turn-on at the end of the transformer demagnetization. The input signal for the ZCD is obtained as a partition of the auxiliary voltage used to supply the device, see Figure 30.

When the integrated triggering circuit senses the negative going edge of the voltage V_{ZCD}, going below the threshold V_{ZCDTth}, the power MOSFET is turned on with a delay that helps to achieve the minimum drain-source voltage during the switch on. The mentioned triggering circuit has to be previously armed by a positive going edge of the voltage V_{ZCD}, exceeding the threshold V_{ZCDAth}. See Table 7.

After the MOSFET turn-off there is a typical noise generated by the transformer's leakage inductance resonance ringing and coupled with the ZCD pin. The blanking time, T_{BLANK}, helps to filter this noise avoiding false triggers of the ZCD circuit.

Figure 29. **Switching frequency vs output load**

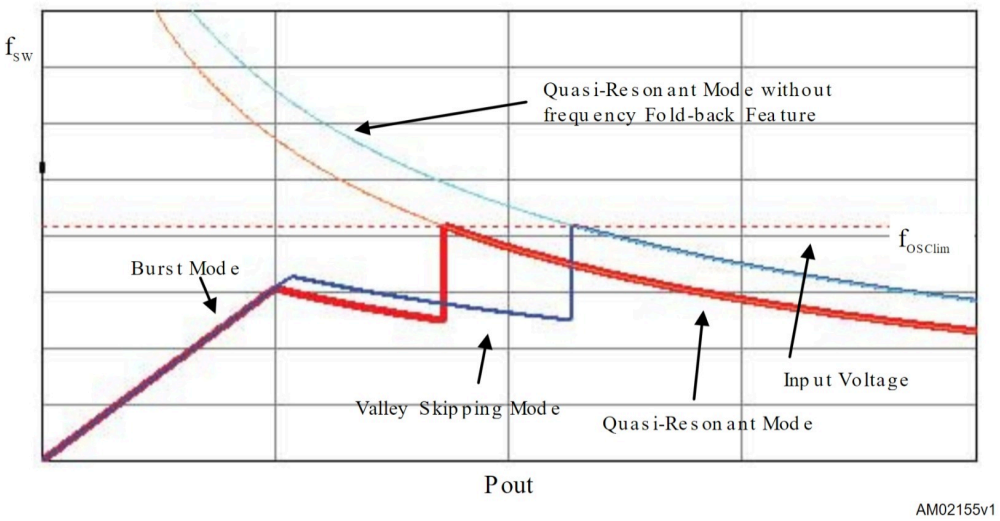
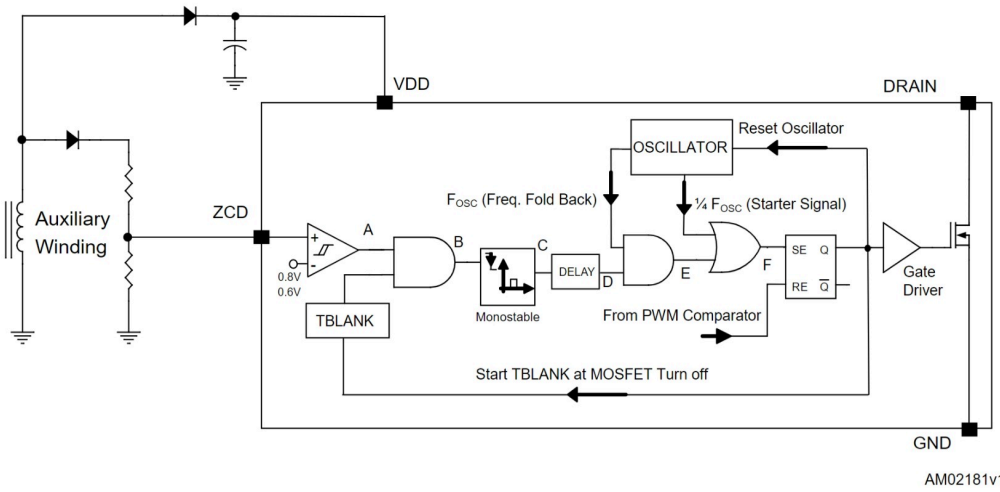


Figure 30. **Zero current detection circuit and oscillator circuit**



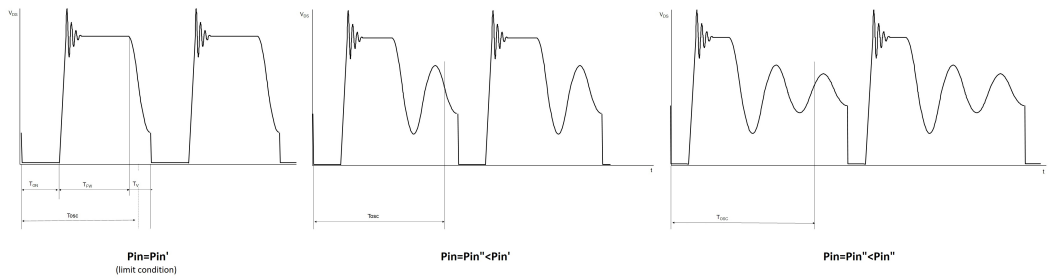
7.7 Frequency foldback function and valley skipping mode

The switching frequency, in Quasi Resonant mode, is not fixed and it depends on both the load and the converter'sinput voltage. The switching frequency increases when the load decreases, orwhen the input voltage mains increases, and vice versa. In principle it could reach an infinite value. To avoid that, the VIPER25 taps the maximum switching frequency of the application by its control logic.

The frequency limit is realized with an internal oscillator switching at 136 kHz for VIPER25L or at 225 kHz for the VIPER25H, sees the parameter F_{OSClim} on Table 7. This oscillator is synchronized with power MOSFET turn-on. When the power MOSFET is off, if the first negative-going edge voltage of the ZCD pin, resulting from transformer's demagnetization, appears after at least one oscillator cycle has been completed, the MOSFET is turned ON and the oscillator re-synchronized.

Otherwise, if the first negative-going edge voltage appears before completing one oscillator cycle, the signal is ignored. Due to the ringing of the drain voltage, the ZCD pin will experience another positive-going edge voltage that arms the circuit and a subsequent negative-going edge voltage. Again, if this appears before the oscillator cycle is complete, it is ignored, otherwise the MOSFET is turned ON and the oscillator re-synchronized. In this way, one or more drain ringing cycles will be skipped (Figure 31 shows the so called "valley-skipping mode") and the switching frequency will be prevented from exceeding the limit F_{OSClim}.

Figure 31. Drain ringing cycle skipping as the load is progressively reduced



When the system operates in valley skipping-mode, uneven switching cycles may be observed under some line/load conditions,due to the fact that the OFF-time of the power MOSFET is allowed to change with discrete steps of one ringing cycle, while the OFF-time needed for cycle-by-cycle energy balance could fall in between. Thus one or more longer switching cycles will be compensated by oneor more shorter cycles and vice versa.This mechanism is natural and there is no appreciable effect on the converter's performances and on its output voltage.

The operation described so far does not consider the blanking time T_{BLANK} after power MOSFET's turn OFF. Actually T_{BLANK} does not come into play as long as the following condition is met:

Equation 2

$$D \leq 1 - \frac{T_{BLANK}}{T_{OSClim}} = 1 - T_{BLANK} \cdot F_{OSClim} \quad (2)$$

where D is the MOSFET duty cycle. Ift his condition is not met, the time during which MOSFET's turn-ON is inhibited is extended beyond T_{OSClim} by a fraction of T_{BLANK}. As a consequence, the maximum switching frequency willbe a little lower than the internal limit set by the oscillator and valley-skipping mode will take place slightly earlier than expected.

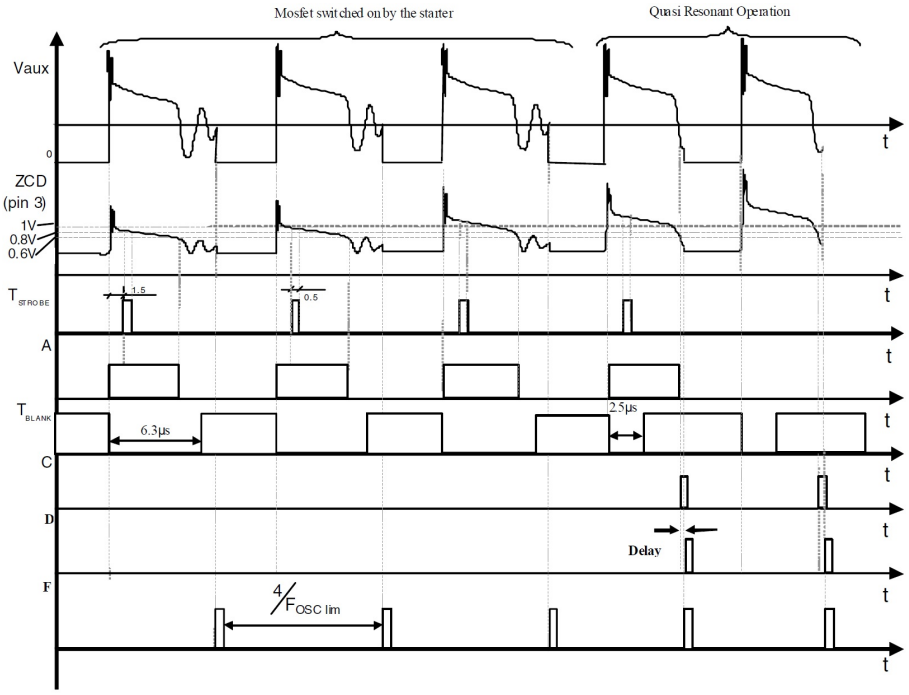
7.8 Double blanking time

The blanking time, T_{BLANK}, can have two different values: the lower one is 2,5 ms (typical value) and the higher one is 6,3 ms (typical value). The value is linked to the voltage V_{ZCD}, sampled during the time T_{STROBE} defined as for the over voltage protection (see the relevant Section 7.11). The time T_{BLANK} has the lower value if is detected V_{ZCD} < 1 V or it has the higher value if is detected V_{ZCD} > 1 V, refer to Table 7 and Figure 32

The higher value of the blanking time is normally activated during the start-up phase or in case of output short circuit; when the output voltage of the converter is quite lower than the regulated value. In this condition can happens that during the demagnetization of the transformer, the V_{ZCD} is very close to the arming and triggering thresholds (V_{ZCDAth} and V_{ZCDTth}) and the ZCD circuit can be erroneously trigged, leading the system to work at higher frequency and in continuous mode. This false trigger is inhibited by the selection of the higher value of T_{BLANK} when V_{ZCD} is lower than 1 V.

During the normal operation, insteady state condition, the voltageV_{ZCD} during the demagnetization is higher than 1 V and the selected T_{BLANK} value is the lower one. Figure 32 shows thetypical waveforms during the power up and the linked T_{BLANK} selection.

Figure 32. **Double T_{BLANK} timing diagram**



7.9 Starter

If the amplitudeof the voltage on ZCD pin at the end of one oscillator cycle is smaller than the V_{ZCDAth} arming threshold, in which case MOSFET's turn-ON could not be triggered, the system would stop.

This is what normally happens during converter's power-up or under overload/short circuit conditions.

During the converter's startup phase, the voltage on ZCD pin is not high enough to arm the triggering circuit. Thus, the converter operates at a fixed frequency, $F_{STARTER}$ (see Table 7). As the voltage developed across the auxiliary winding becomes high enough to arm the ZCD circuit, MOSFET's turn-ON is locked to transformer demagnetization, hence setting up quasi-resonant operation.

As protection, in case the ZCD voltage is permanently above the threshold V_{ZCDAth}, the switching frequency is reduced to the minimum value, F_{OSCmin}, reported on Table 7.

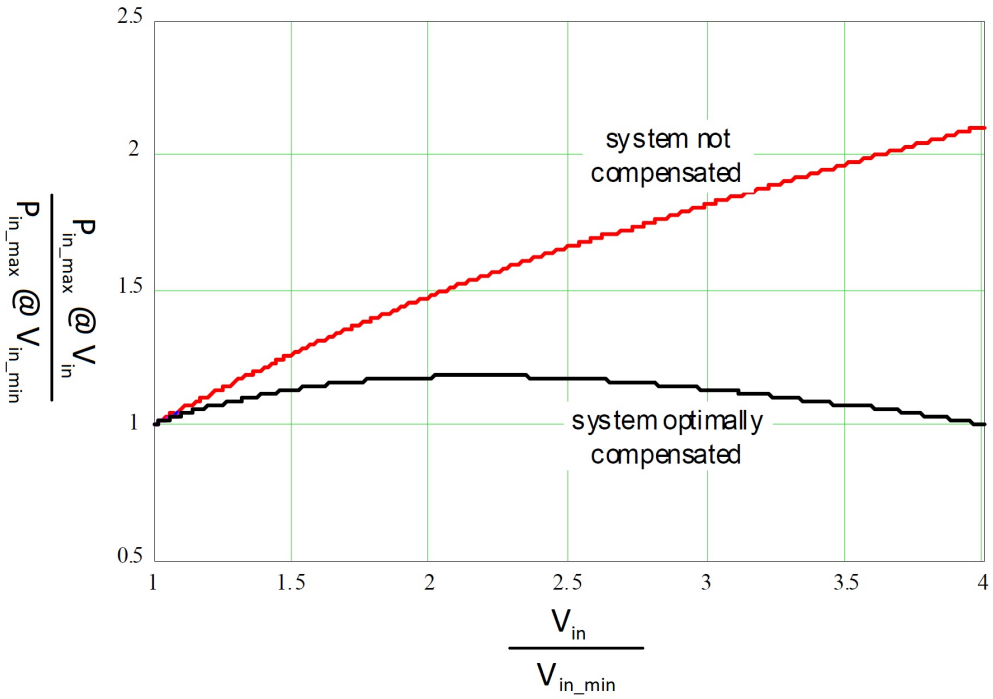
7.10 Current limit set point and feed-forward option

The VIPER25 is a current mode converter and the drain current is limited cycle by cycle according to the FB pin voltage value that is related with the feedback loop response and the load. When the drain current, sensed by the integrated Sense-FET, reaches the current limitation, after the internal propagation delay, the MOSFET is switched OFF. The current limitation cannot exceed a certain value, I_{Dlim}, that can be adjusted actingon the current sunk from the ZCD pin during MOSFET's ON-time.

Usually a resistor, R_{LIM}, connected from ZCD pin to ground is used to fix this sunk current and then the peak drain current set-point: the lower the resistor is, the lower I_{Dlim} will be.

For a QR fly-back converter the power capability strongly depends on the input voltage. In wide-range applications at maximum line the power capability can be more than twice the value at minimum line, as shown by the upper curve in the diagram of Figure 33. To reduce this dependence, the current limit I_{Dlim} has to be reduced according to the increment of the input voltage, implementing the so called line feed-forward. It's realized with a resistor, R_{FF}, connected between the ZCD pin and the auxiliary winding, see Figure 34. Since the voltage across the auxiliary winding during MOSFET's on-time is proportional to the input voltage through the auxiliary-to-primary turns ratio N_{AUX}/N_P, a current proportional to the input voltage is sunk from the ZCD pin, thus lowering the over current set point.

Figure 33. **Typical power capability vs input voltage in quasi-resonant converter's**



Inorder to proper select the value of the resistance R_{FF} (see Figure 34), once are known the proper I_{Dlim} set points at minimum and at the maximum converter input voltage. The following approximatedf ormula calculates the valueof the resistor R_{FF}

Equation 3

$$R_{FF} = \frac{V_{in_max} - V_{in_min}}{n_{aux} \cdot (I_{ZCD1} - I_{ZCD2})} \quad (3)$$

Where:

- V_{in_Max} and V_{in_min} are the maximum and minimum converter rectified input voltage
- η_{aux} is the primary to auxiliary winding turn ratio
- I_{ZCD1}, and I_{ZCD2} are the currents needed to sink from the ZCD pin, in order to obtain the selected I_{Dlim} set points, respectively at V_{in_max} and V_{in_min}, the graph I_{Dlim} vs I_{ZCD} current is reported on Figure 17).

The R_{LIM} value can be calculated from the following formula knowing the R_{FF} value:

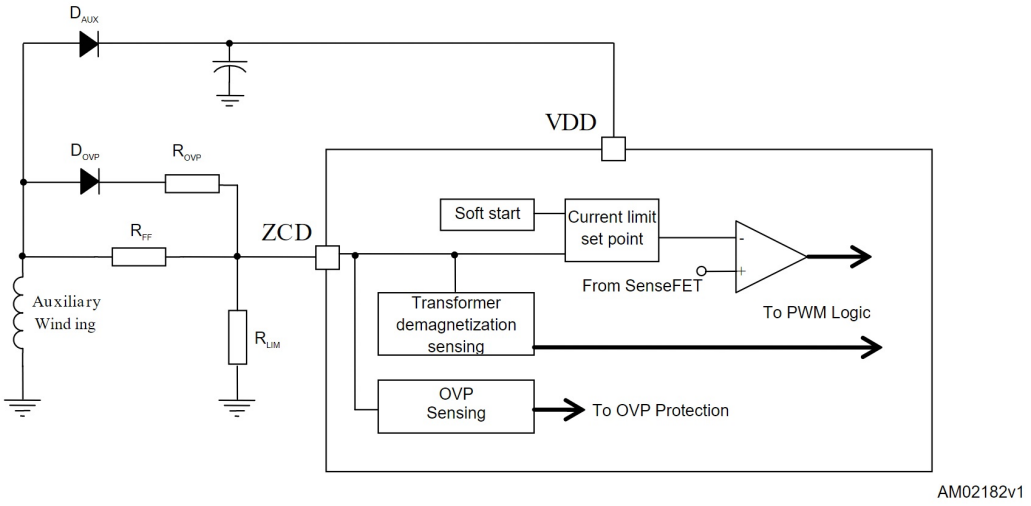
Equation 4

$$R_{LIM} = Max\left(\frac{V_{ZCD1}}{I_{ZCD1} - \frac{\frac{V_{in_min}}{n_{aux}} + V_{ZCD1}}{R_{FF}}}, \frac{V_{ZCD2}}{I_{ZCD2} - \frac{\frac{V_{in_max}}{n_{aux}} + V_{ZCD2}}{R_{FF}}}\right) \quad (4)$$

where:

V_{ZCD1} and V_{ZCD2} are the ZCD pin voltages when the sunk current is I_{ZCD1} and I_{ZCD2}respectively (see Figure 16)

Figure 34. **ZCD pin typical external configuration**



7.11 Overvoltage protection (OVP)

The VIPER25 has integrated the logic for the monitor of the output voltageusing as input signal the voltage V_{ZCD} during the OFF time of the power MOSFET. This is the time when the voltage from the auxiliary winding tracks the output voltage, through the turn ratio N_{AUX} /N_{SEC}.

The ZCD pin has to be connected to the auxiliary winding through the diode D_{OVP} and the resistors R_{OVP} and R_{LIM} as shows Figure 34. When, during the OFF time, the voltage V_{ZCD} exceeds, four consecutive times, the reference voltage V_{OVP} (reported on Table 7) the over voltage protection will stop the power MOSFET and the converter enters the auto-restart mode.

In order to bypass the noise after the turn off of the power MOSFET, the voltage V_{ZCD} is sampled inside a short window after the time T_{STROBE}, see Table 7and Figure 35. The sampled signal, if higher than V_{OVP}, trigger the internal OVP digital signal and increments the internal counter. The same counter is reset every time the signal OVP is not triggered in one oscillator cycle.

Referring to Figure 34, the resistors divider ratio k_{OVP} will be given by:

Equation 5

$$k_{OVP} = \frac{V_{OVP}}{\frac{N_{aux}}{N_{sec}} \cdot \left(V_{OUTOVP} + V_{DSEC}\right) - V_{DAUX}} \quad (5)$$

Equation 6

$$k_{OVP} = \frac{R_{LIM}}{R_{LIM} + R_{OVP}} \quad (6)$$

where:

- V_{OVP} is the OVP threshold (see Table 7)
- $V_{OUT\ OVP}$ is the converter output voltage value to activate the OVP (set by designer) designer
- N_{AUX} is the auxiliary winding turns
- N_{SEC} is the secondary winding turns
- V_{DSEC} is the secondary diode forward voltage
- V_{DAUX} is the auxiliary diode forward voltage
- R_{OVP} together R_{LIM} make the output voltage divider

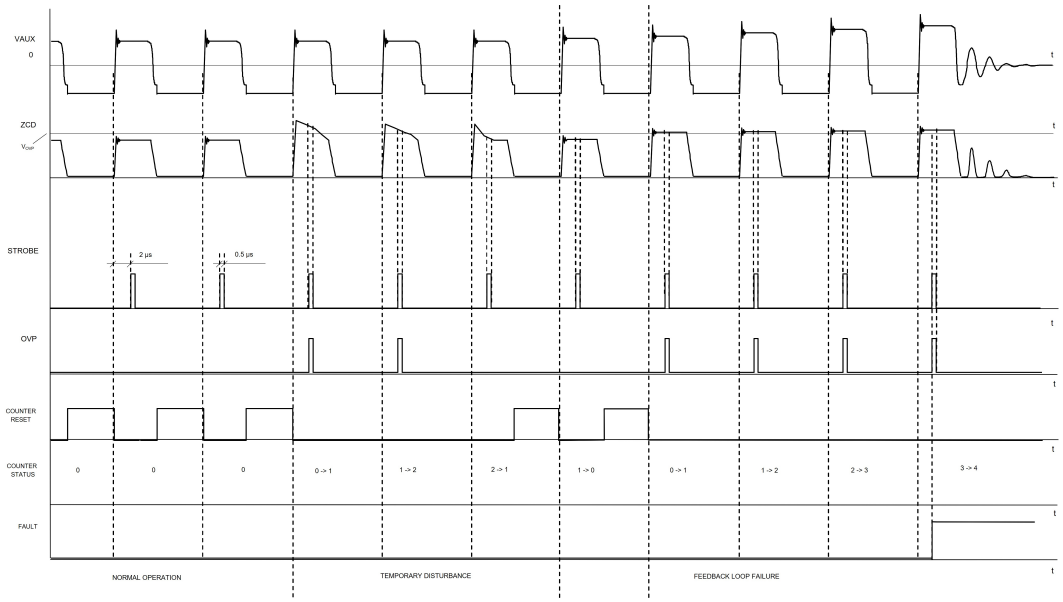
Than, fixed R_{LIM}, according to the desired I_{Dlim}, the R_{OVP} can be calculating by:

Equation 7

$$R_{OVP} = R_{LIM} \cdot \frac{1 - k_{OVP}}{k_{OVP}} \quad (7)$$

The resistor values willbe such that the current sourced and sunk by the ZCD pin be within the rated capability of the internal clamp.

Figure 35. OVP timing diagram



7.12 Summary on ZCD pin

Referring to Figure 34, the circuitry connected to the ZCD pin enables to implement the following functions:

1. Current limit, I_{Dlim}, set point
2. Line feed-forward compensation
3. Output overvoltage protection (OVP)
4. Zero current detection for QR operation

Chosen R_{LIM}, R_{FF} and R_{OVP} as described in previous paragraphs this function are automatically defined.

Table 8 refers to Figure 34 and list the external resistance combinations needed to activate one or more functions associated to the ZCD pin.

Table 8. ZCDpin configurations

Function / component	R_{LIM}	R_{OVP}	R_{FF}	D_{OVP}
I_{Dlim} set point	See Equation 4	Required for ZCD	Not required	Yes
OVP	22 KΩ	See Equation 7	Not required	Yes
Line feed-forward	22 KΩ	Required for ZCD	See Equation 3	Yes
I_{Dlim} set point and OVP	See Equation 4 with RFF= ∞	See Equation 7	Not required	Yes
OVP and line feed-forward	22 KΩ	See Equation 7	See Equation 3	Yes
I_{Dlim} set point and line feed-forward	See Equation 4	Required for ZCD	See Equation 3	Yes
I_{Dlim} reduction+ OVP +Line feed-forward	See Equation 4	See Equation 7	See Equation 3	Yes

7.13 Feedback and overload protection (OLP)

The feedback pin (FB) controls the PWM operation, enters the burst mode and manages the delayed overload protection.

The thresholds V_{FBbm} and V_{FBlin} (reported on Table 7) are respectively the low and the high limit of the PWM operations, where the drain current is sensed trough the integrated resistor R_{SENSE} and applied to the comparator PWM. The PWM logic turns OFF the power MOSFET as soon as the sensed voltage is equal to the voltage applied to the FB pin and trough the integrated resistors network, see Figure 2 and Figure 22

As shows the IC block diagram reported in Figure 2, in parallel with the PWM comparator there is the OCP comparator that limits the drain current as maximum to the value I_{Dlim}, reported on Table 7.

In case of higher load the voltage V_{FB} increases, when it reaches the threshold V_{FBlin} the drain current is limited to I_{Dlim} and the internal current starts the charge of the capacitor C_{FB}.

As soon as the voltage V_{FB} reaches the threshold V_{FBolp}, see Figure 38, the protection turns off the IC. After, the auto-restart mode is activated using the low value of the current I_{DDch}, see Table 6.

The time, from the high load detection, V_{FB}= V_{FBlin}, to the over load turn-off, V_{FB}= V_{FBolp}, depends from the value of the capacitor C_{FB} and from the internal charge current, I_{FB}. The OLP delay time can becalculating by the formula:

Equation 8

$$T_{OLP_delay} = C_{FB} \cdot \frac{V_{FBolp} - V_{FBlin}}{3\mu A} \quad (8)$$

The current, I_{FB}, is 3 µA as minimum value.The components connected to the FB pin are also a part of the compensation loop, so they have to be selected taking into account the proper delay and loop stability consideration. The Figure 36 and Figure 37 show two different feedback networks.

In Figure 35, the capacitor, C_{FB}, connected to FB pin is used as part of the circuit to compensate the feedback loop but also as element to delay the OLP shut down owing to the time needed to charge the capacitor (see Equation 8).

After the start-up time, t_{SU}, during which the feedback voltage is fixed at V_{FBlin}, the output capacitor could not be at its nominal value and the controller interpreter this situation as an over load condition. In this case, the OLP delay helps to avoid an incorrect device shut down during the start-up. See the relevant Section 7.3 .

Owing to the above considerations, the OLP delay time must be long enough to by-pass the initial output voltage transient and check the over load condition only when the output voltage is in steady state. The output transient time depends from the value of the output capacitor and from the load.

When the value of the C_{FB} capacitor calculated for the loop stability is too low and cannot ensure enough OLP delay, an alternative compensation network can be used and it is showed in Figure 37.

Using this alternative compensation network, two poles (f_{PFB}, f_{PFB1}) and one zero (f_{ZFB}) are introduced by the capacitors C_{FB} and C_{FB1} and the resistor R_{FB1}.

The capacitor C_{FB} introduces a pole (f_{PFB}) at higher frequency than f_{ZB} and f_{PFB1}. This pole is usually used to compensate the high frequency zero due to the ESR (Equivalent Series Resistor) of the output capacitance of the fly-back converter.

The mathematical expressions of these poles and zero frequency, considering the scheme in Figure 37, are reported by the equations below:

Equation 9

$$f_{ZFB} = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot R_{FB1}} \quad (9)$$

Equation 10

$$f_{PFB} = \frac{R_{FB(DYN)} - R_{FB1}}{2 \cdot \pi \cdot C_{FB} \cdot \left(R_{FB(DYN)} \cdot R_{FB1}\right)} \quad (10)$$

Equation 11

$$f_{PFB} = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot \left(R_{FB1} + R_{FB(DYN)}\right)} \quad (11)$$

The $R_{FB(DYN)}$ is the dynamic resistance seen by the FB pin and reported on Table 7.

The C_{FB1} capacitor fixes the OLP delay and usually C_{FB1} results much higher than C_{FB}. The Equation 8 can be still used to calculate the OLP delay time but C_{FB1} has to be considered instead of C_{FB}. Using the alternative compensation network, the designer can satisfy, in all case, the loop stability and the enough OLP delay time alike.

Figure 36. **FB pin configuration 1**

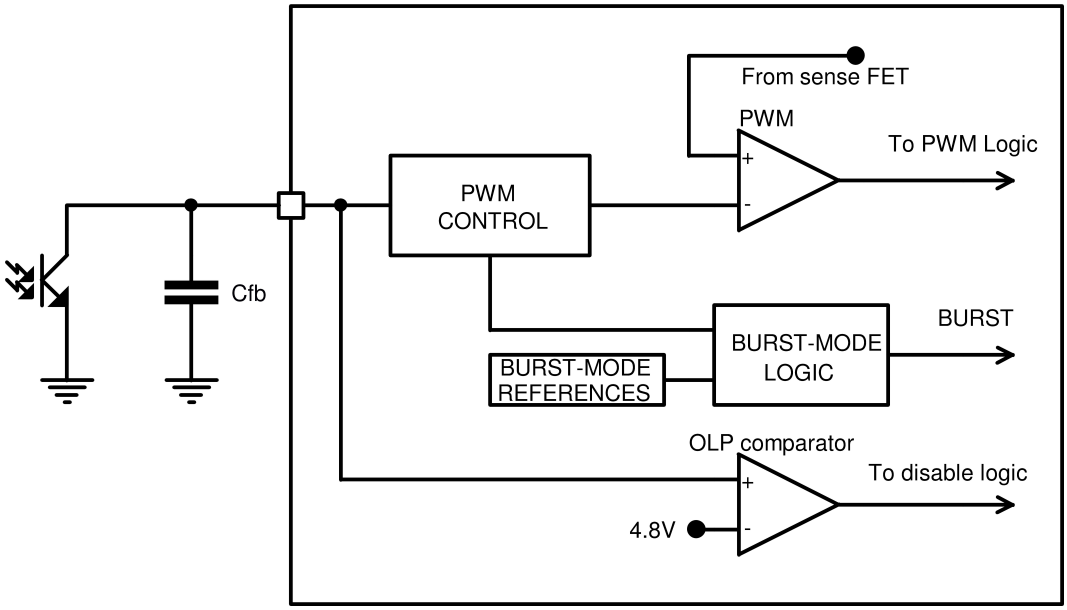


Figure 37. **FB pin configuration 2**

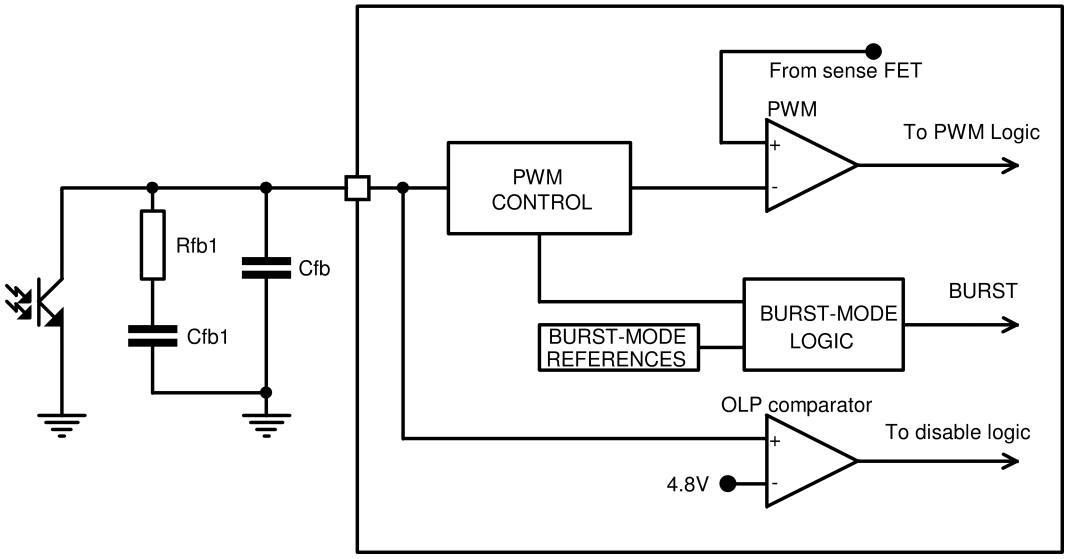
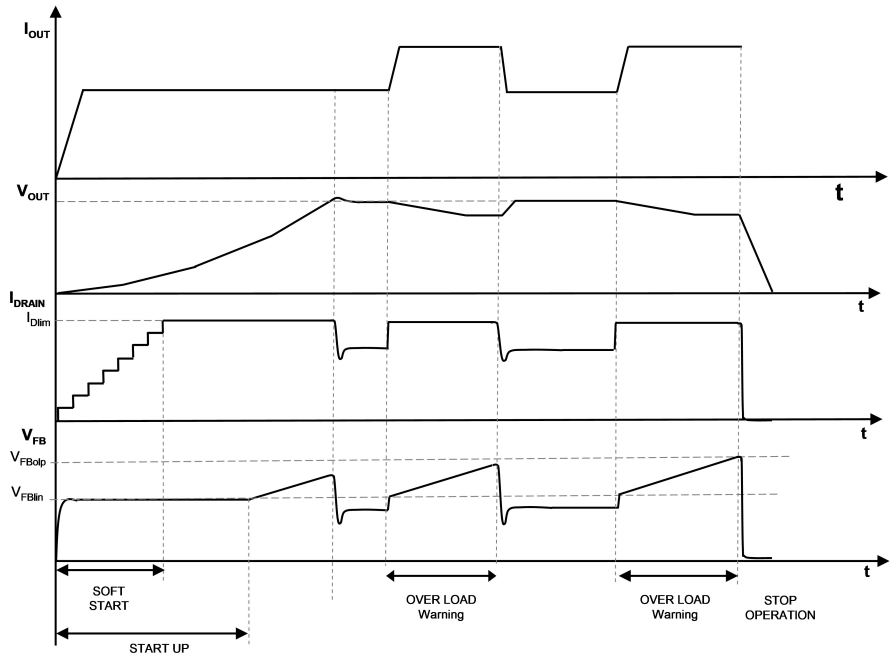


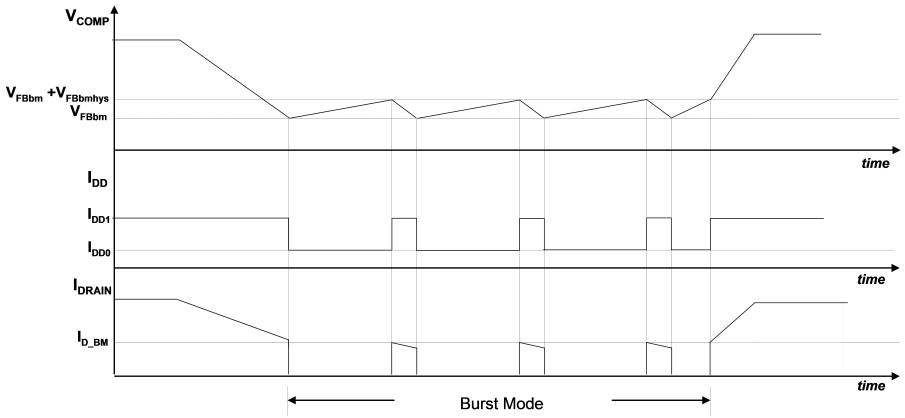
Figure 38. **Timing diagram: Overload protection**



7.14 Burst-mode operation at no load or very light load

When the load decrease the feedback loop reacts lowering the feedback pin voltage. If it falls down the burst mode threshold, V_{FBbm}, the power MOSFET is not more allowed to be switched on. After the MOSFET stops, as a result of the feedback reaction to the energy delivery stop, the feedback pin voltage increases and exceeding the level, $V_{FBbm} + V_{FBbmhys}$, the power MOSFET starts switching again. The burst mode thresholdsare reported on Table 7 and Figure 39 shows this behavior. Systems alternates period of time where power MOSFET is switching to period of time where power MOSFET is not switching; this device working mode is the burst mode. The power delivered to output during switching periods exceeds the load power demands; the excess of power is balanced from not switching period where no power is processed.The advantage of burst mode operation is an average switching frequency much lower then the normal operation working frequency, up to some hundred of hertz, minimizing all frequency related losses. During the burst-mode the draincurrent peak is clamped to the level, I_{D_BM}, reported on Table 7.

Figure 39. **Burst mode timing diagram, light load management**



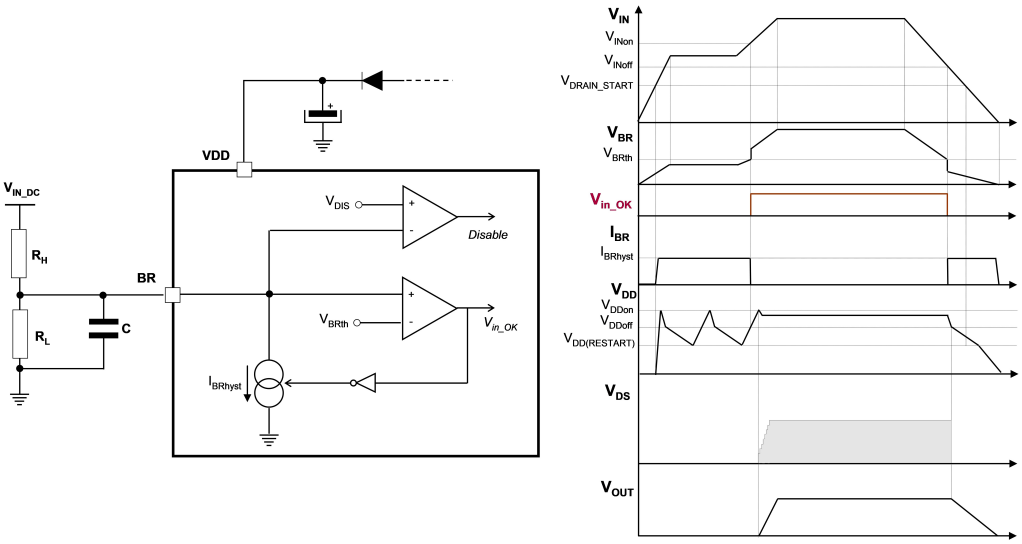
7.15 Brown-out protection

Brown-out protection is a not-latched shutdown function activated when a condition of mains under voltage is detected. The Brown-out comparator is internally referenced to V_{BRth} threshold, see Table 7, and disables the PWM if the voltage applied at the BR pin is below this internal reference. Under this condition the power MOSFET is turned off. Until the Brownout condition ispresent, the VDD voltage continuously oscillates between the V_{DDon} and the UVLO thresholds, as shown in the timing diagram of Figure 40. A voltage hysteresis is present to improve the noise immunity.

The switching operation is restarted as the voltage on the pin is above the reference plus the before said voltage hysteresis. See Figure 6.

The Brown-out comparator is provided also with a current hysteresis, I_{BRhyst}. The designer has to set the rectified input voltage above which the power MOSFET starts switching after brown out event, V_{INon}, and the rectified input voltage below which the power MOSFET is switched off, V_{INoff}. Thanks to the I_{BRhyst}, see Table 7, these two thresholds can be set separately.

Figure 40. Brown-out protection: BR external setting and timing diagram



Fixed the V_{INon} and the V_{INoff} levels, with reference to Figure 40, the following relationships can bee stablished for the calculation of the resistors R_H and R_L:

Equation 12

$$R_L = -\frac{V_{BRhyst}}{I_{BRhyst}} + \frac{V_{INon} - V_{INoff} - V_{BRhyst}}{V_{INon} - V_{BRth}} \cdot \frac{V_{BRth}}{I_{BRhyst}} \quad (12)$$

Equation 13

$$R_H = \frac{V_{INon} - V_{INoff} - V_{BRhyst}}{I_{BRhyst}} \cdot \frac{R_L}{R_L + \frac{V_{BRhyst}}{I_{BRhyst}}} \quad (13)$$

For a proper operation of this function, $V_{IN\ on}$ must be less than the peak voltage at minimum mains and $V_{IN\ off}$ less than the minimum voltage onthe input bulk capacitor at minimum mains and maximum load.

The BR pin is a high impedance input connected to high value resistors, thus it is prone to pick up noise, which might alter the OFF threshold when the converter operates or gives origin to undesired switch-off of the device during ESD tests.

It is possible to bypass the pin to ground with a small film capacitor (e.g. 1-10 nF) to prevent any malfunctioning of this kind.

If the brown-out function is not used the BR pin has to be connected to GND, ensuring that the voltage is lower than the minimum of V_{DIS} threshold (50 mV, see Table 7). In order to enable the brown-out function the BR pin voltage has to be higher than the maximum of V_{DIS} threshold (150 mV, see Table 7).

7.16 2nd level over current protection and hiccup mode

The VIPER25 is protected against short circuit of the secondary rectifier, short circuiton the secondary winding or a hard-saturation of fly-back transformer. Such as anomalous condition is invoked when the drain current exceed the threshold I_{DMAX}, see Table 7.

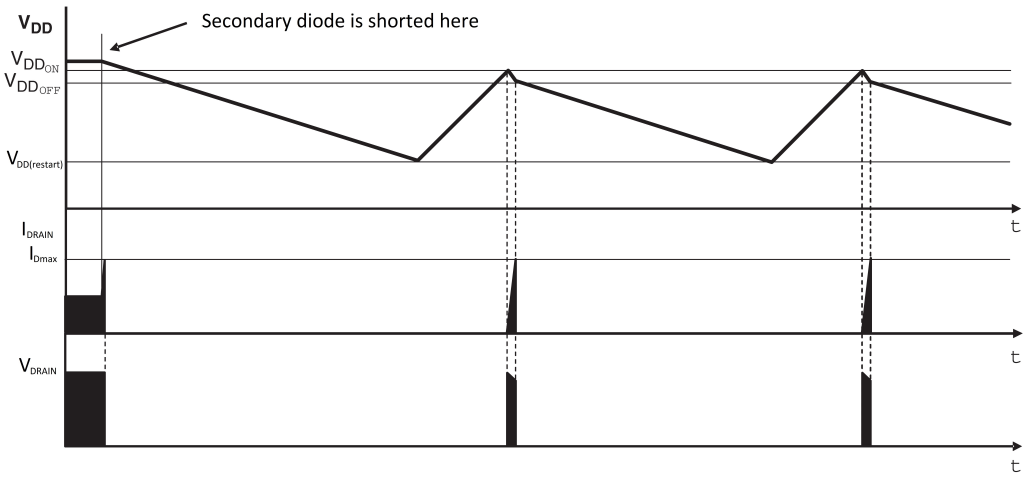
To distinguish a real malfunction from a disturbance (e.g. induced during ESD tests) a “warning state” is entered after the first signal trip. If in the subsequent switching cycle the signal is not tripped, a temporary disturbance is assumed and the protection logic will be reset in its idle state; otherwise if the I_{DMAX} threshold is exceeded for two consecutive switching cycles a real malfunction is assumed and the power MOSFET is turned OFF.

The shutdown condition is latched as long as the device is supplied. While it is disabled, no energy is transferred from the auxiliary winding; hence the voltage on the V_{DD} capacitor decays till the V_{DD} under voltage threshold (V_{DDoff}), which clears the latch.

The start up HV current generator is still off, until V_{DD} voltage goes below its restart voltage, $V_{DD(RESTART)}$. After this condition the V_{DD} capacitor is charged again by 600 µA current, and the converter switching restarts if the V_{DDon} occurs. If the fault condition is not removed the device enters in auto-restart mode. This behavioral results in a low-frequency intermittent operation (Hiccup-mode operation), with very low stress on the power circuit.

See the timing diagram of Figure 41.

Figure 41. Hiccup-mode OCP: timing diagram



8 Package information

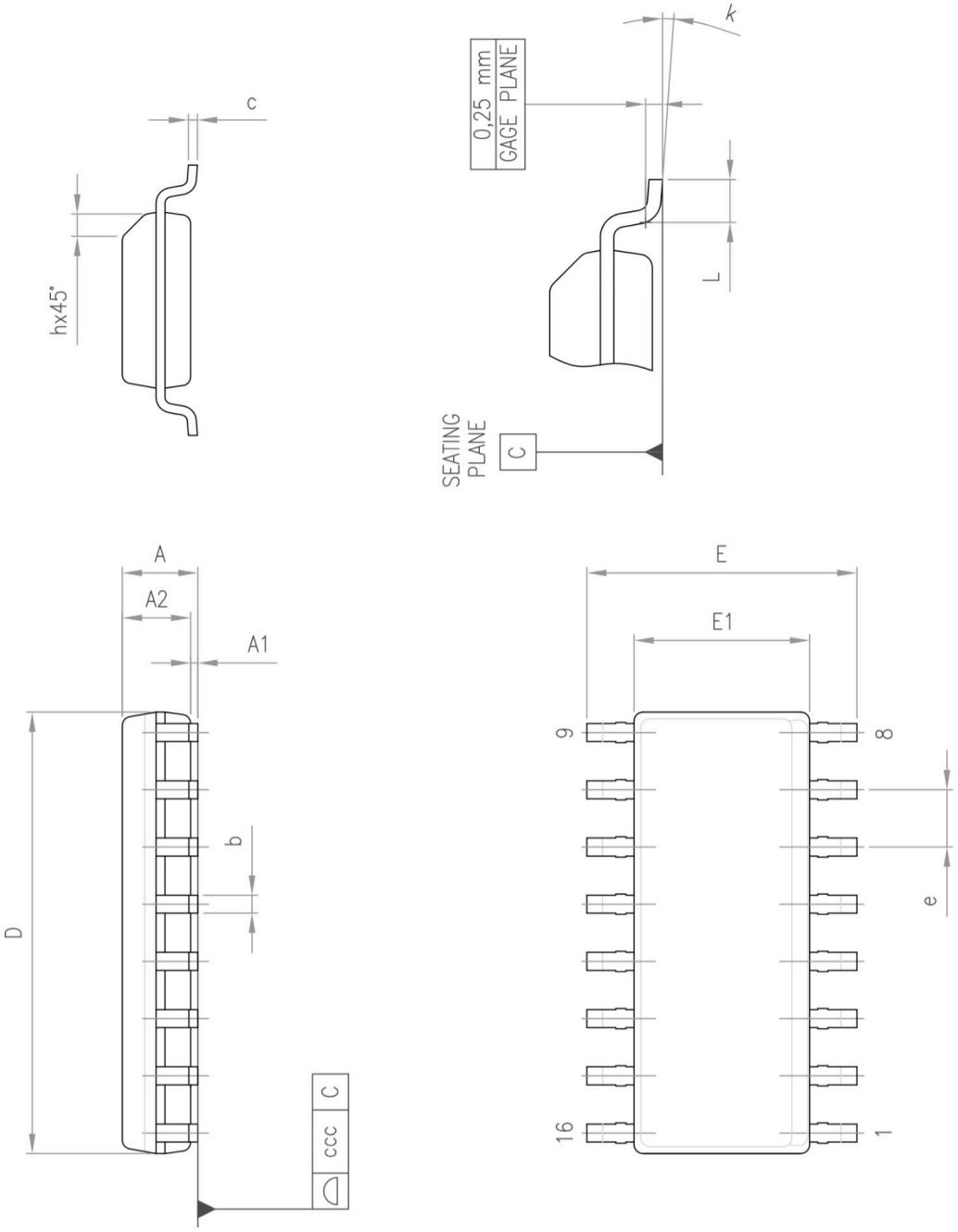
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 Package mechanical data

Table 9. SO16 narrow mechanical data

Dim.	Databook (mm.)		
	Min.	Typ.	Max.
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

Figure 42. **SO16 package dimensions**



9 Ordering information

Table 10. **Device summary**

Order codes	Package	Packaging
VIPER25HD / VIPER25LD	SO16 narrow	Tube
VIPER25HDTR /VIPER25LDTR		Tape and reel

Revision history

Table 11. **Document revision history**

Date	Version	Changes
17-Apr-2009	1	Initial release
09-Jun-2009	2	Updated application paragraph in coverpage and Table 8
26-Aug-2009	3	Content reworked to improve readability, no technical changes
21-Jul-2010	4	Updated Table 8 and Fig 38
11-Feb-2022	5	Removal of DIP7 package due to PTN on DIP

Contents

1 **Block diagram** 2
2 **Typical power** 3
3 **Pin settings** 4
4 **Electrical data** 5
4.1 Maximum ratings 5
4.2 Thermal data 5
4.3 Electrical characteristics 6
5 **Typical electrical characteristics** 10
6 **Typical circuits** 13
7 **Operation description** 14
7.1 Power section and gate driver 14
7.2 High voltage startup generator 14
7.3 Power-up description 14
7.4 Power-down description 17
7.5 Auto-restart description 17
7.6 Quasi-resonant operation 18
7.7 Frequency foldback function and valley skipping mode 19
7.8 Double blanking time 20
7.9 Starter 21
7.10 Current limit set point and feed-forward option 21
7.11 Overvoltage protection (OVP) 23
7.12 Summary on ZCD pin 24
7.13 Feedback and overload protection (OLP) 24
7.14 Burst-mode operation at no load or very light load 27
7.15 Brown-out protection 28
7.16 2nd level over current protection and hiccup mode 29
8 **Package information** 30
8.1 Package mechanical data 30
9 **Ordering information** 32
Revision history 33
List of tables 35
List of figures 36

List of tables

Table 1. Typical power . . . 3
Table 2. Pin description . . . 4
Table 3. Absolute maximum ratings . . . 5
Table 4. Thermal data . . . 5
Table 5. Power section . . . 6
Table 6. Supply section . . . 6
Table 7. Controller section . . . 7
Table 8. ZCDpin configurations . . . 24
Table 9. SO16 narrow mechanical data . . . 30
Table 10. Device summary . . . 32
Table 11. Document revision history . . . 33

List of figures

Figure 1. Typical topology . . . 1
Figure 2. Block diagram . . . 2
Figure 3. Connection diagram (top view) . . . 4
Figure 4. R_{th_JA} versus copper area . . . 6
Figure 5. Minimum turn-on time test circuit . . . 9
Figure 6. Brown-out threshold test circuits . . . 9
Figure 7. OVP threshold test circuits . . . 9
Figure 8. Current limit vs T_J . . . 10
Figure 9. Drain start voltage vs T_J . . . 10
Figure 10. HFB vs T_J . . . 10
Figure 11. Brown-out threshold vs T_J . . . 10
Figure 12. Brown-out hysteresis vs TJ . . . 10
Figure 13. . Brown-out hysteresis current vs T_J . . . 10
Figure 14. Operating supply current (no switching) vs T_J . . . 11
Figure 15. Operating supply current (switching) vs TJ . . . 11
Figure 16. V_{ZCD} vs I_{ZCD} . . . 11
Figure 17. Current limit vs I_{ZCD} . . . 11
Figure 18. Power MOSFET on-resistance vs T_J . . . 11
Figure 19. Power MOSFET break down voltage vs T_J . . . 11
Figure 20. COSS characteristic . . . 12
Figure 21. Thermal shutdown . . . 12
Figure 22. Min-features QR flyback application . . . 13
Figure 23. Full-features QR flyback application . . . 13
Figure 24. I_{DD} current during start-up and burst mode . . . 15
Figure 25. Timing diagram: normal power-up and power-down sequences . . . 16
Figure 26. Timing diagram: Start-up phase and soft start (case 1) . . . 16
Figure 27. Timing diagram: Start-up phase and soft start (case 2) . . . 17
Figure 28. Timing diagram: behavior after short circuit . . . 18
Figure 29. Switching frequency vs output load . . . 19
Figure 30. Zero current detection circuit and oscillator circuit . . . 19
Figure 31. Drain ringing cycle skipping as the load is progressively reduced . . . 20
Figure 32. Double T_{BLANK} timing diagram . . . 21
Figure 33. Typical power capability vs input voltage in quasi-resonant converter's . . . 22
Figure 34. ZCD pin typical external configuration . . . 23
Figure 35. OVP timing diagram . . . 24
Figure 36. FB pin configuration 1 . . . 26
Figure 37. FB pin configuration 2 . . . 26
Figure 38. Timing diagram: Overload protection . . . 27
Figure 39. Burst mode timing diagram, light load management . . . 27
Figure 40. Brown-out protection: BR external setting and timing diagram . . . 28
Figure 41. Hiccup-mode OCP: timing diagram . . . 29
Figure 42. SO16 package dimensions . . . 31

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved