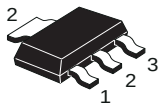
VNN7NV04P-E, VNS7NV04P-E

OMNIFET II
fully autoprotected Power MOSFET

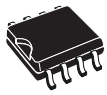
Features

Type	$R_{DS(on)}$	I_{lim}	V_{clamp}
VNN7NV04P-E VNS7NV04P-E	60 mΩ	6 A	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET in compliance with the 2002/95/EC European Directive



SOT-223


SO-8

Description

The VNN7NV04P-E, VNS7NV04P-E, are monolithic devices designed in STMicroelectronics VIPower™ M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 kHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SOT-223	-	VNN7NV04PTR-E
SO-8	VNS7NV04P-E	VNS7NV04PTR-E

Contents

1 Block diagram and pin description 5

2 Electrical specifications 6

2.1 Absolute maximum ratings 6

2.2 Thermal data 7

2.3 Electrical characteristics 7

3 Protection features 9

3.1 Electrical characteristics curves 12

3.2 SO-8 maximum demagnetization energy 16

3.3 SOT-223 maximum demagnetization energy 17

4 Package and PCB thermal data 18

4.1 SO-8 thermal data 18

4.2 SOT-223 thermal data 20

5 Package and packing information 23

5.1 SOT-223 mechanical data 23

5.2 SO-8 mechanical data 24

5.3 SOT-223 packing information 26

5.4 SO-8 packing information 27

6 Revision history 28

List of tables

Table 1. Device summary . . . 1
Table 2. Absolute maximum ratings . . . 6
Table 3. Thermal data . . . 7
Table 4. Electrical characteristics . . . 7
Table 5. SO-8 thermal parameter . . . 19
Table 6. SOT-223 thermal parameter . . . 22
Table 7. SOT-223 mechanical data . . . 23
Table 8. SO-8 mechanical data . . . 24
Table 9. Document revision history . . . 28

List of figures

Figure 1. Block diagram . . . 5
Figure 2. Configuration diagram (top view) . . . 5
Figure 3. Current and voltage conventions . . . 6
Figure 4. Switching time test circuit for resistive load . . . 10
Figure 5. Test circuit for diode recovery times . . . 10
Figure 6. Unclamped inductive load test circuits . . . 11
Figure 7. Input charge test circuit . . . 11
Figure 8. Unclamped inductive waveforms . . . 11
Figure 9. Derating curve . . . 12
Figure 10. Transconductance . . . 12
Figure 11. Static drain-source on resistance vs input voltage (part 1/2) . . . 12
Figure 12. Static drain-source on resistance vs input voltage (part 2/2) . . . 12
Figure 13. Source-drain diode forward characteristics . . . 12
Figure 14. Static drain source on resistance . . . 12
Figure 15. Turn-on current slope (part 1/2) . . . 13
Figure 16. Turn-on current slope (part 2/2) . . . 13
Figure 17. Transfer characteristics . . . 13
Figure 18. Static drain-source on resistance vs Id . . . 13
Figure 19. Input voltage vs input charge . . . 13
Figure 20. Turn-off drain source voltage slope (part 1/2) . . . 13
Figure 21. Turn-off drain source voltage slope (part 2/2) . . . 14
Figure 22. Capacitance variations . . . 14
Figure 23. Output characteristics . . . 14
Figure 24. Normalized on resistance vs temperature . . . 14
Figure 25. Switching time resistive load (part 1/2) . . . 14
Figure 26. Switching time resistive load (part 2/2) . . . 14
Figure 27. Normalized input threshold voltage vs temperature . . . 15
Figure 28. Normalized current limit vs junction temperature . . . 15
Figure 29. Step response current limit . . . 15
Figure 30. SO-8 maximum turn-off current versus load inductance . . . 16
Figure 31. SO-8 demagnetization . . . 16
Figure 32. SOT-223 maximum turn-off current versus load inductance . . . 17
Figure 33. SOT-223 demagnetization . . . 17
Figure 34. SO-8 PC board . . . 18
Figure 35. Rthj-amb vs PCB copper area in open box free air condition . . . 18
Figure 36. SO-8 thermal impedance junction ambient single pulse . . . 19
Figure 37. Thermal fitting model of an OMNIFET II in SO-8 . . . 19
Figure 38. SOT-223 PC board . . . 20
Figure 39. Rthj-amb vs PCB copper area in open box free air condition . . . 20
Figure 40. SOT-223 thermal impedance junction ambient single pulse . . . 21
Figure 41. Thermal fitting model of an OMNIFET II in SOT-223 . . . 21
Figure 42. SOT-223 package dimensions . . . 23
Figure 43. SO-8 package dimensions . . . 25
Figure 44. SOT-223 tape and reel shipment (suffix “TR”) . . . 26
Figure 45. SO-8 tube shipment (no suffix) . . . 27
Figure 46. SO-8 tape and reel shipment (suffix “TR”) . . . 27

1 Block diagram and pin description

Figure 1. Block diagram

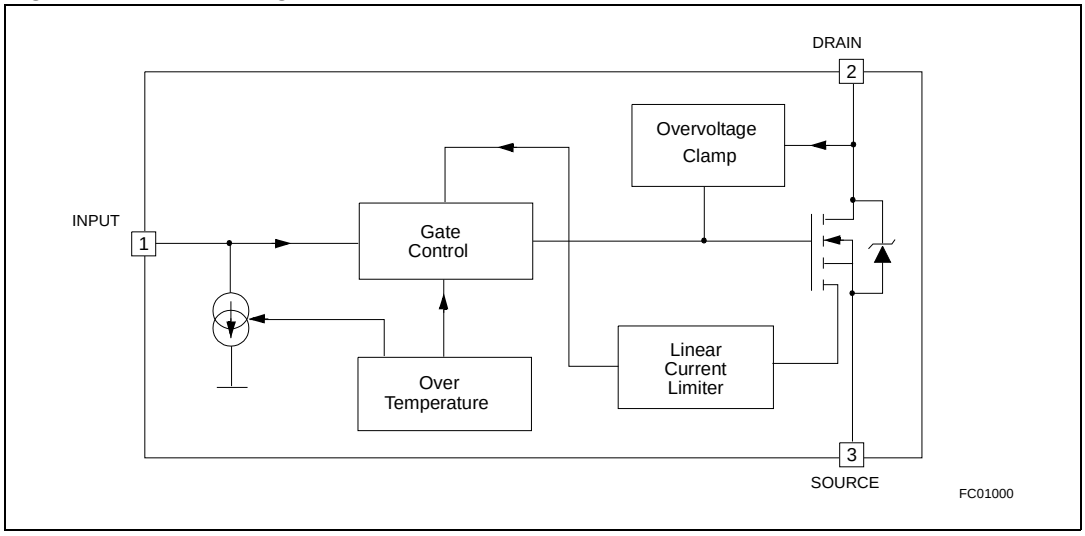
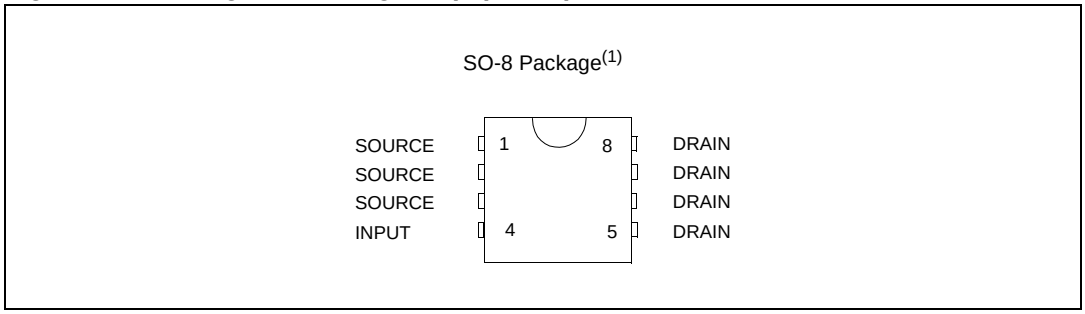


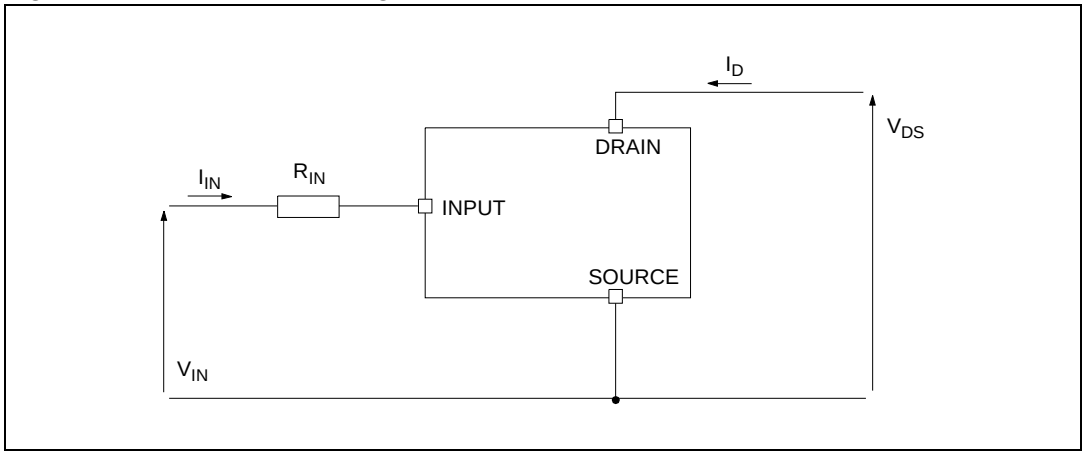
Figure 2. Configuration diagram (top view)



1. For the pins configuration related to SOT-223 see outlines at page 1.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SOT-223	SO-8	
V_{DS}	Drain-source voltage (V_{IN} = 0 V)	Internally clamped		V
V_{IN}	Input voltage	Internally clamped		V
I_{IN}	Input current	+/-20		mA
$R_{IN\ MIN}$	Minimum input series impedance	150		Ω
I_D	Drain current	Internally limited		A
I_R	Reverse DC output current	-10.5		A
V_{ESD1}	Electrostatic discharge (R = 1.5 KΩ, C = 100 pF)	4000		V
V_{ESD2}	Electrostatic discharge on output pin only (R = 330 Ω, C = 150 pF)	16500		V
P_{tot}	Total dissipation at T_c = 25 °C	7	4.6	W
E_{MAX}	Maximum switching energy (L = 0.7 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; I_L = 9 A)	40		mJ
E_{MAX}	Maximum switching energy (L = 0.6 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; I_L = 9 A)		37	mJ
T_j	Operating junction temperature	Internally limited		°C
T_c	Case operating temperature	Internally limited		°C
T_{stg}	Storage temperature	-55 to 150		°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		SOT-223	SO-8	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	18		°C/W
$R_{thj\text{-}lead}$	Thermal resistance junction-lead max		27	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	96(1)	90(1)	°C/W

1. When mounted on a standard single-sided FR4 board with 0.5 mm^2 of Cu (at least 35 µm thick) connected to all DRAIN pins.

2.3 Electrical characteristics

-40 °C < T_j < 150 °C, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Off						
V_{CLAMP}	Drain-source clamp voltage	V_{IN} = 0 V; I_D = 3.5 A	40	45	55	V
V_{CLTH}	Drain-source clamp threshold voltage	V_{IN} = 0 V; I_D = 2 mA	36			V
V_{INTH}	Input threshold voltage	V_{DS} = V_{IN}; I_D = 1 mA	0.5		2.5	V
I_{ISS}	Supply current from input pin	V_{DS} = 0 V; V_{IN} = 5 V		100	150	µA
V_{INCL}	Input-source clamp voltage	I_{IN} = 1 mA	6	6.8	8	V
		I_{IN} = -1 mA	-1.0		-0.3	V
I_{DSS}	Zero input voltage drain current (V_{IN} = 0 V)	V_{DS} = 13 V; V_{IN} = 0 V; T_j = 25 °C			30	µA
		V_{DS} = 25 V; V_{IN} = 0 V			75	µA
On						
$R_{DS(on)}$	Static drain-source on resistance	V_{IN} = 5 V; I_D = 3.5 A; T_j = 25 °C			65	mΩ
		V_{IN} = 5 V; I_D = 3.5 A			130	mΩ
Dynamic (T_j = 25 °C, unless otherwise specified)						
g_{fs}(1)	Forward transconductance	V_{DD} = 13 V; I_D = 3.5 A		9		S
C_{OSS}	Output capacitance	V_{DS} = 13 V; f = 1 MHz; V_{IN} = 0 V		220		pF

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Switching (T_j = 25 °C, unless otherwise specified)						
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V; I_D = 3.5 A; V_{gen} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 150 Ω; (see figure *Figure 4*)		100	300	ns
t_r	Rise time			470	1500	ns
$t_{d(off)}$	Turn-off delay time			500	1500	ns
t_f	Fall time			350	1000	ns
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V; I_D = 3.5 A; V_{gen} = 5 V; R_{gen} = 2.2 KΩ; (see figure *Figure 4*)		0.75	2.3	µs
t_r	Rise time			4.6	14.0	µs
$t_{d(off)}$	Turn-off delay time			5.4	16.0	µs
t_f	Fall time			3.6	11.0	µs
$(dI/dt)_{on}$	Turn-on current slope	V_{DD} = 15 V; I_D = 3.5 A; V_{gen} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 150 Ω		6.5		A/µs
Q_i	Total input charge	V_{DD} = 12 V; I_D = 3.5 A; V_{IN} = 5 V; I_{gen} = 2.13 mA (see figure *Figure 7*)		18		nC
Source drain diode (T_j = 25 °C, unless otherwise specified)						
V_{SD}(1)	Forward on voltage	I_{SD} = 3.5 A; V_{IN} = 0 V		0.8		V
t_{rr}	Reverse recovery time	I_{SD} = 3.5 A; dI/dt = 20 A/µs; V_{DD} = 30 V; L = 200 µH; (see test circuit, figure *Figure 5*)		220		ns
Q_{rr}	Reverse recovery charge			0.28		µC
I_{RRM}	Reverse recovery current			2.5		A
Protections (-40 °C < T_j < 150 °C, unless otherwise specified)						
I_{lim}	Drain current limit	V_{IN} = 5 V; V_{DS} = 13 V	6	9	12	A
t_{dlim}	Step response current limit	V_{IN} = 5 V; V_{DS} = 13 V		4.0		µs
T_{jsh}	Overtemperature shutdown		150	175	200	°C
T_{jrs}	Overtemperature reset		135			°C
I_{gf}	Fault sink current	V_{IN} = 5 V; V_{DS} = 13 V; T_j = T_{jsh}		15		mA
E_{as}	Single pulse avalanche energy	starting T_j = 25 °C; V_{DD} = 24 V; V_{IN} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 150 Ω; L = 24 mH; (see *Figure 6* and *Figure 8*)	200			mJ

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

3 Protection features

During normal operation, the input pin is electrically connected to the gate of the internal Power MOSFET through a low impedance path.

The device then behaves like a standard Power MOSFET and can be used as a switch from DC up to 50 kHz. The only difference from the user's standpoint is that a small DC current I_{ISS} (typ. 100µA) flows into the input pin in order to supply the internal circuitry.

The device integrates:

- Overvoltage clamp protection: internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- Linear current limiter circuit: limits the drain current I_D to I_{lim} whatever the input pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh}.
- Overtemperature and short circuit protection: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15 °C below shutdown temperature.
- Status feedback: in the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the input pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the input pin driver is not able to supply the current I_{gf}, the input pin falls to 0 V. This however not affects the device operation: no requirement is put on the current capability of the input pin driver except to be able to supply the normal operation drive current I_{ISS}.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL logic circuit.

Figure 4. Switching time test circuit for resistive load

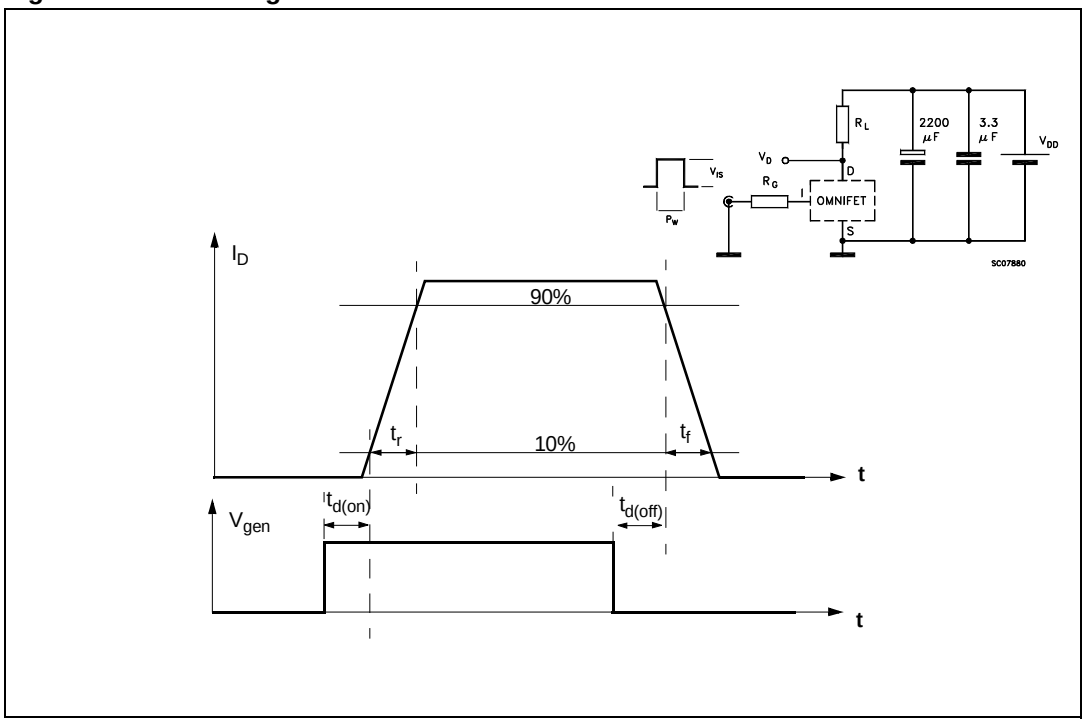


Figure 5. Test circuit for diode recovery times

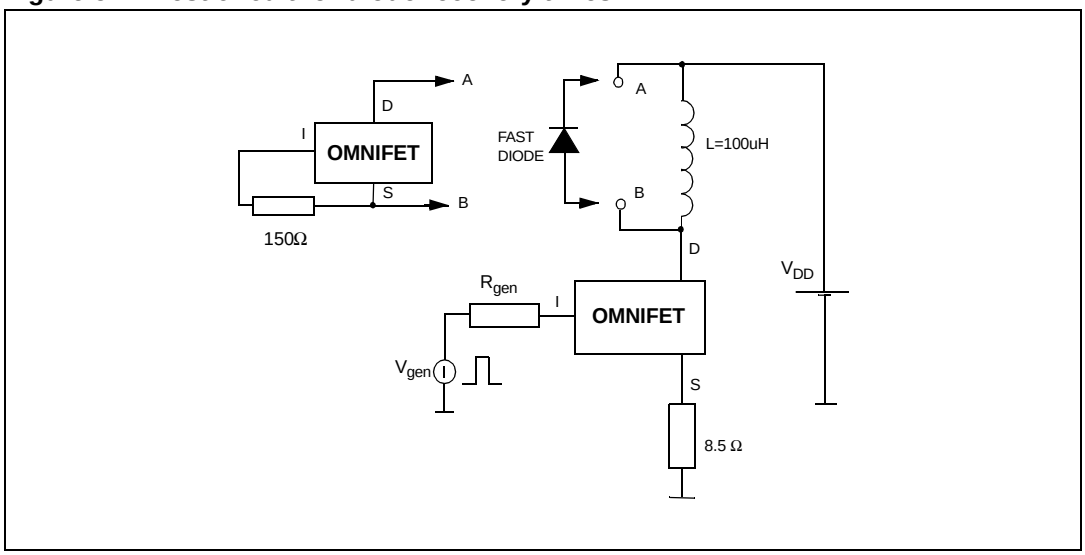


Figure 6. Unclamped inductive load test circuits

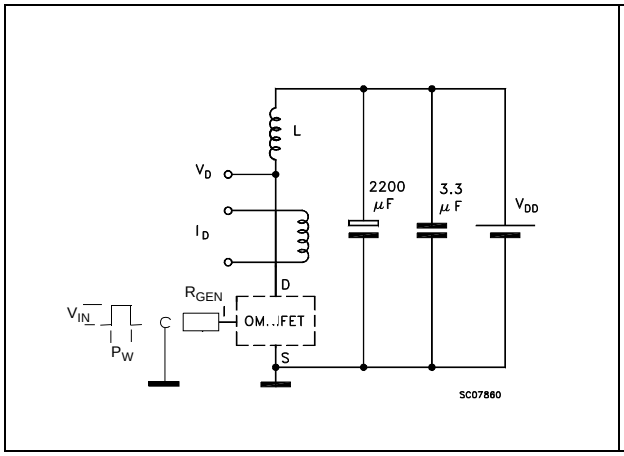


Figure 7. Input charge test circuit

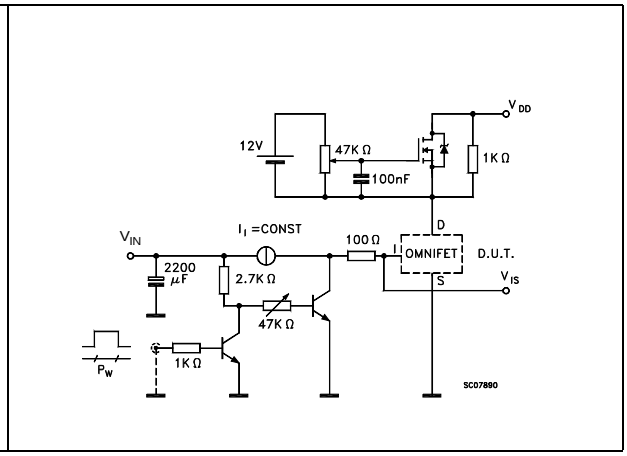
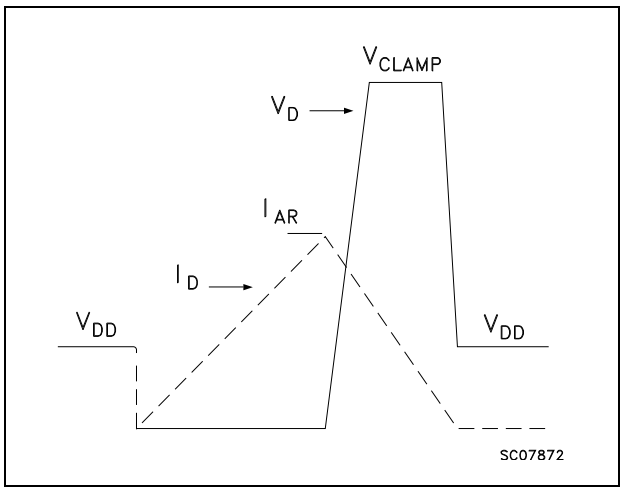


Figure 8. Unclamped inductive waveforms



3.1 Electrical characteristics curves

Figure 9. Derating curve

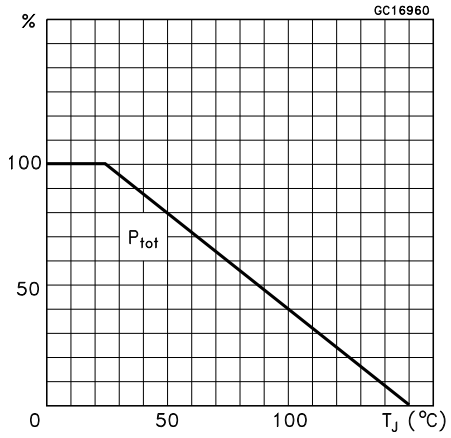


Figure 10. Transconductance

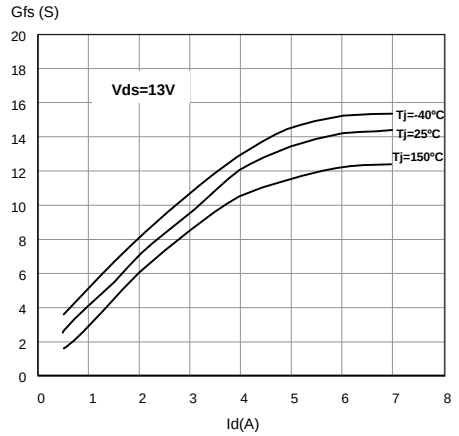


Figure 11. Static drain-source on resistance vs input voltage (part 1/2)

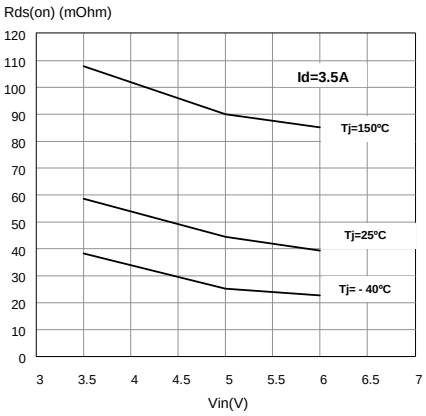


Figure 12. Static drain-source on resistance vs input voltage (part 2/2)

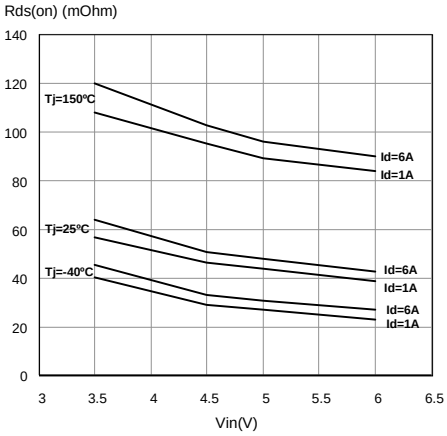


Figure 13. Source-drain diode forward characteristics

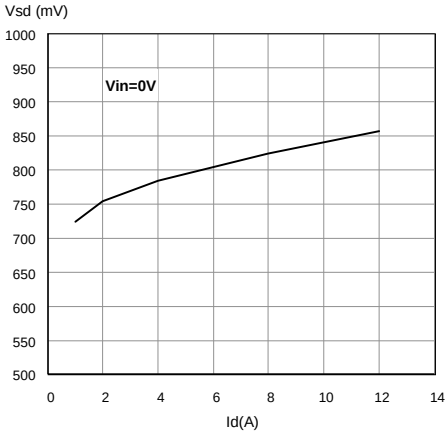


Figure 14. Static drain source on resistance

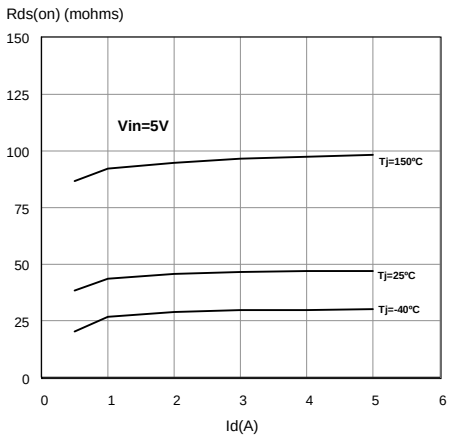


Figure 15. Turn-on current slope (part 1/2)

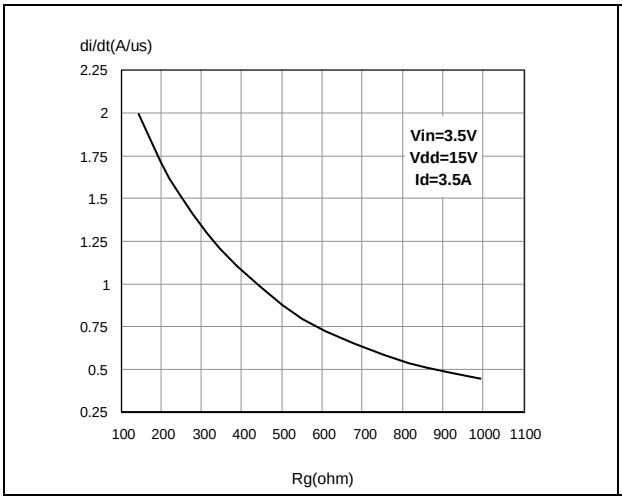


Figure 16. Turn-on current slope (part 2/2)

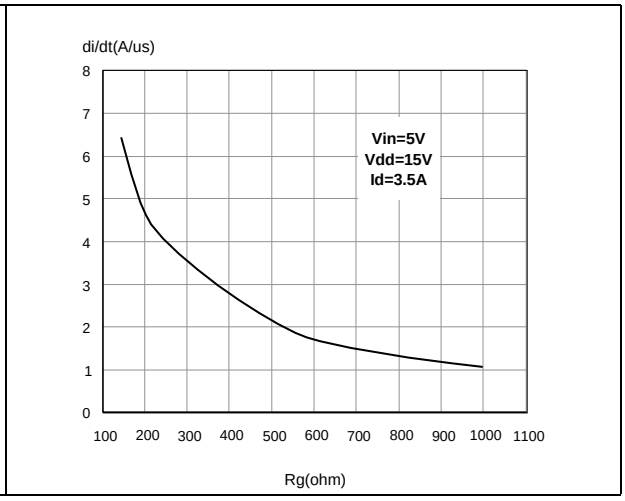


Figure 17. Transfer characteristics

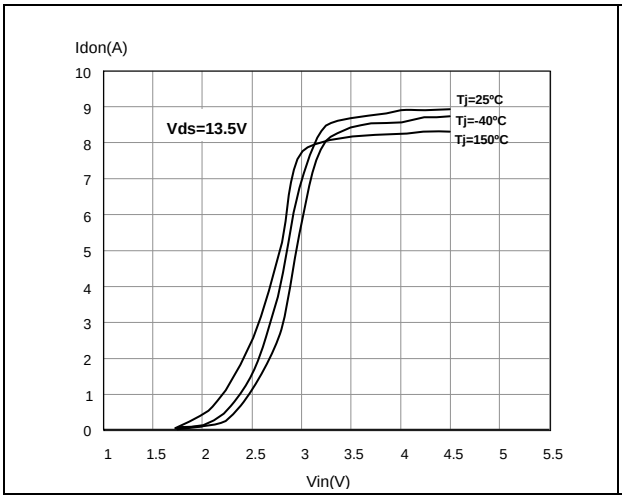


Figure 18. Static drain-source on resistance vs Id

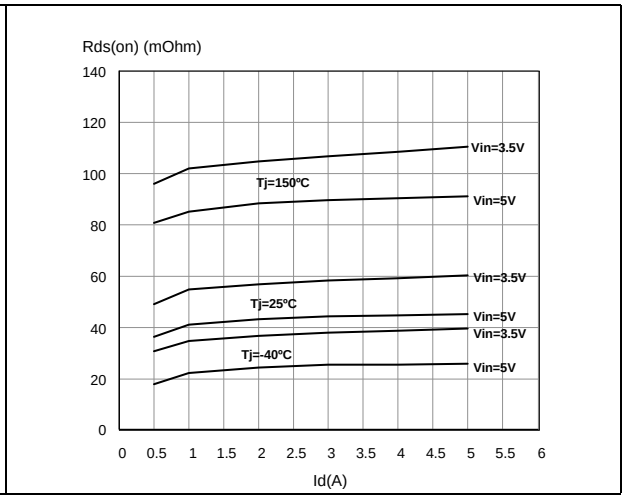


Figure 19. Input voltage vs input charge

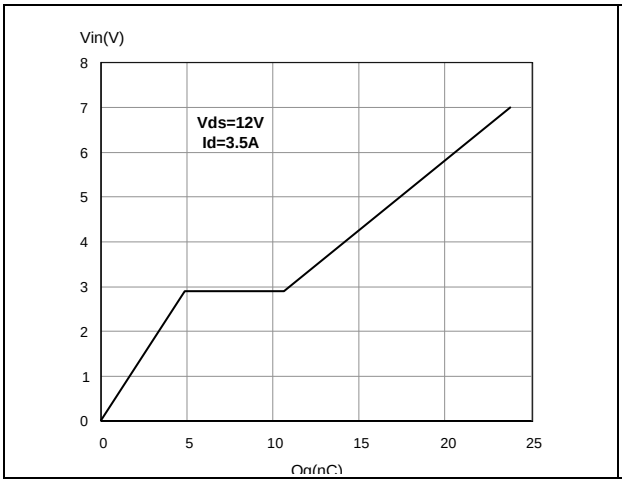


Figure 20. Turn-off drain source voltage slope (part 1/2)

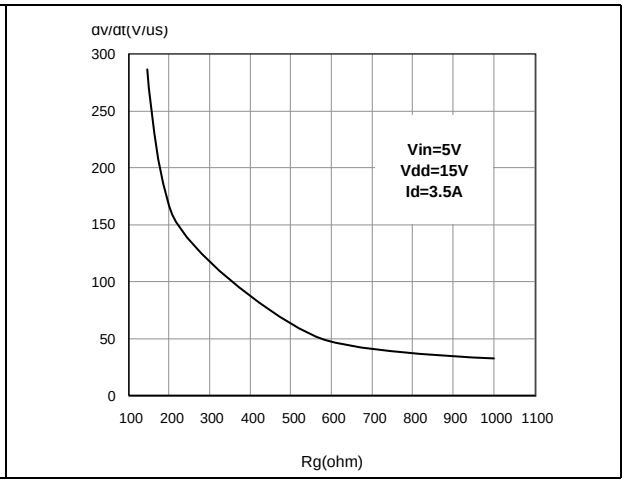


Figure 21. Turn-off drain source voltage slope (part 2/2)

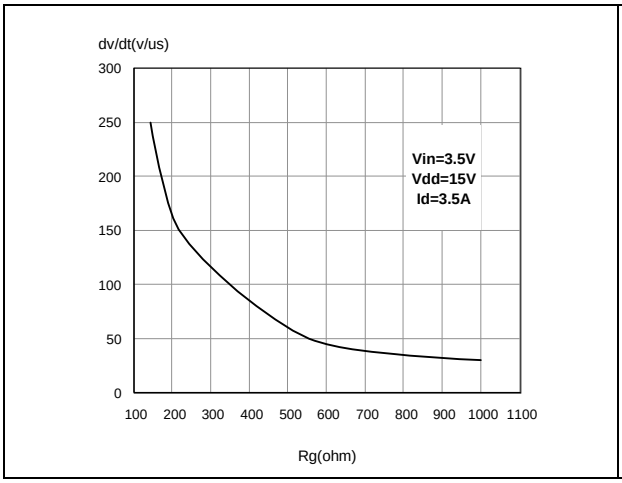


Figure 22. Capacitance variations

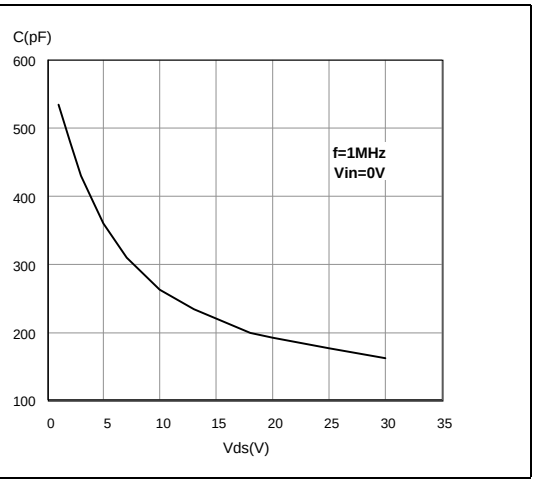


Figure 23. Output characteristics

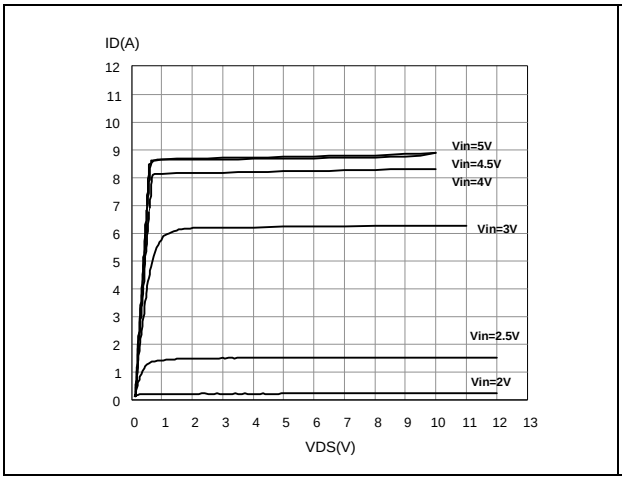


Figure 24. Normalized on resistance vs temperature

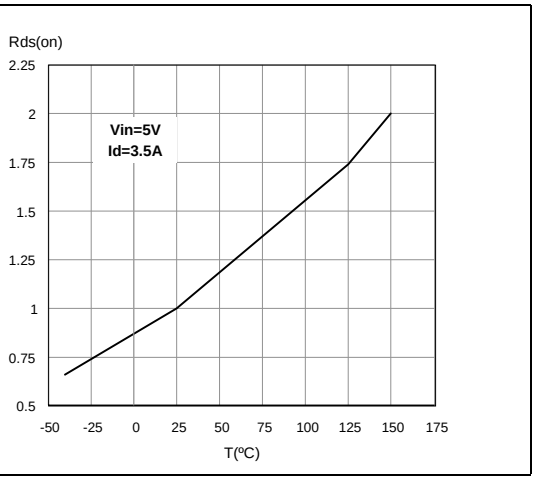


Figure 25. Switching time resistive load (part 1/2)

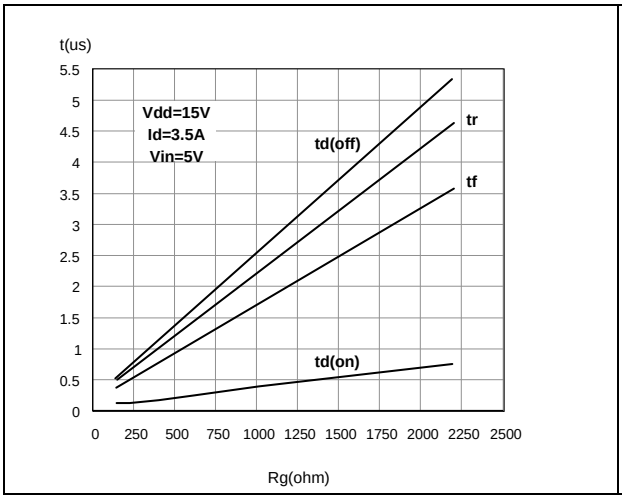


Figure 26. Switching time resistive load (part 2/2)

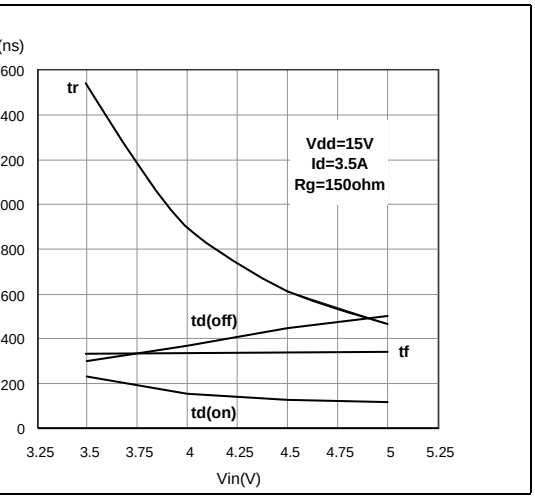


Figure 27. Normalized input threshold voltage vs temperature

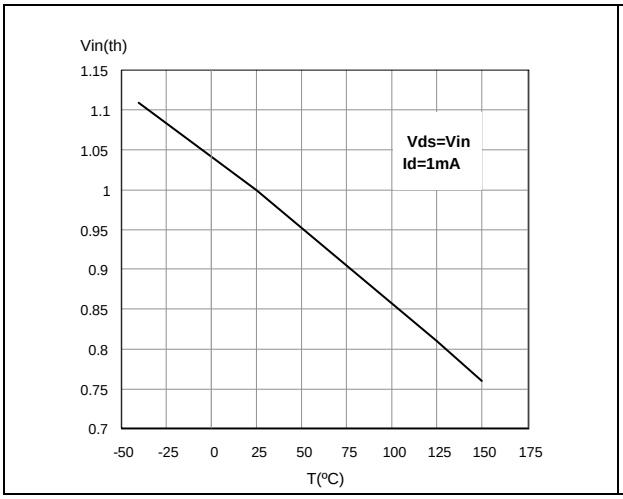


Figure 28. Normalized current limit vs junction temperature

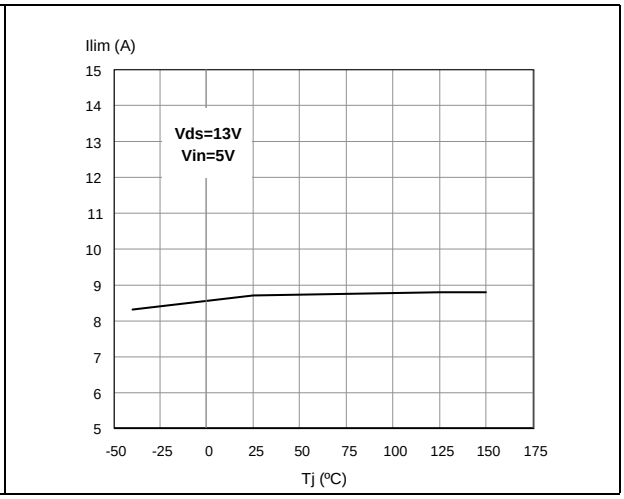
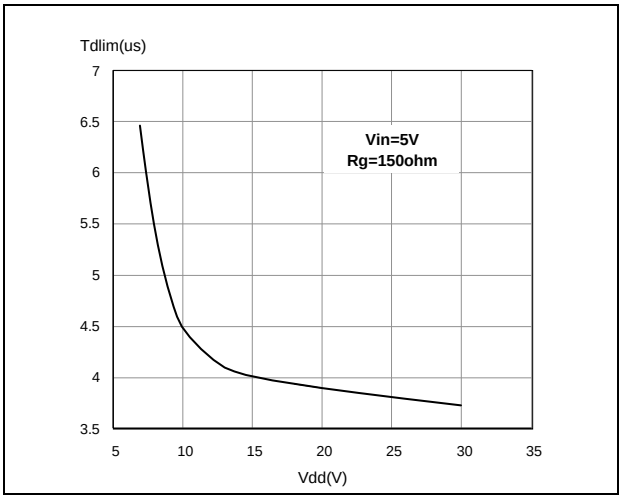
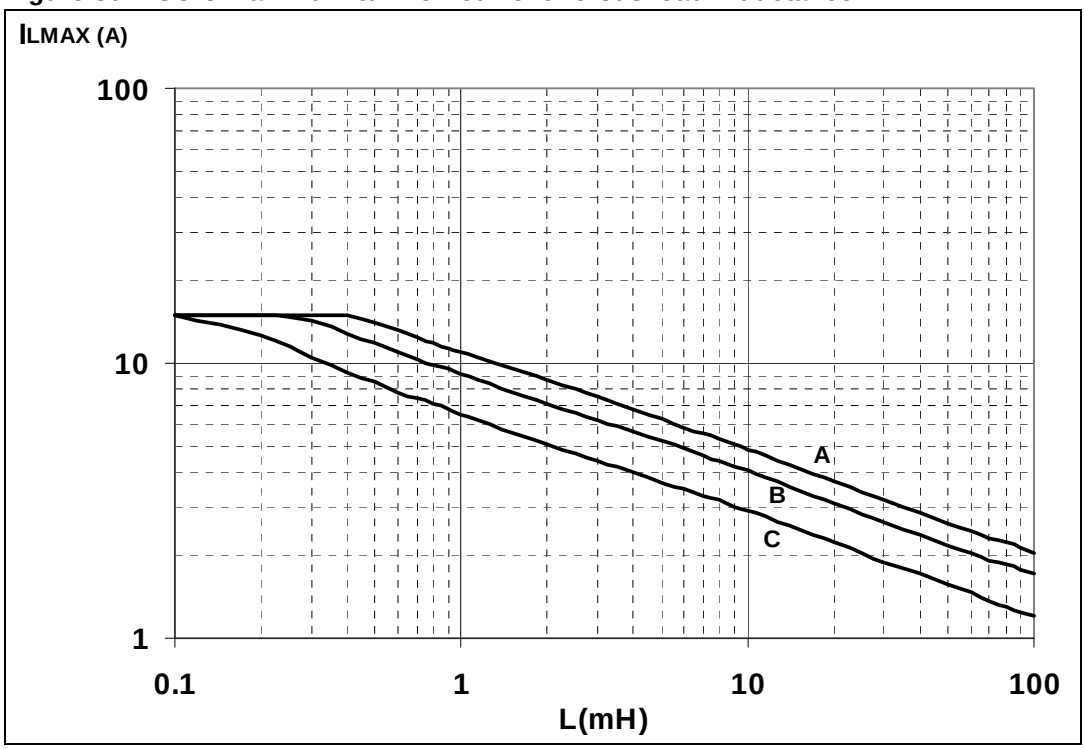


Figure 29. Step response current limit



3.2 SO-8 maximum demagnetization energy

Figure 30. SO-8 maximum turn-off current versus load inductance



Legend

A = Single Pulse at T_{Jstart} = 150 °C

B = Repetitive pulse at T_{Jstart} = 100 °C

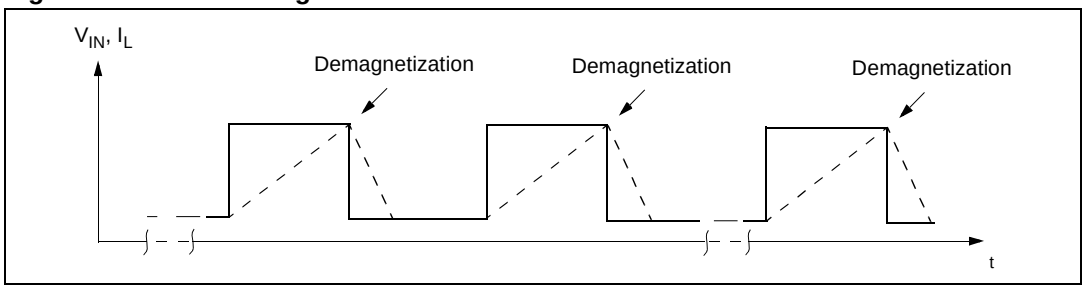
C = Repetitive Pulse at T_{Jstart} = 125 °C

Conditions:

V_{CC} = 13.5 V

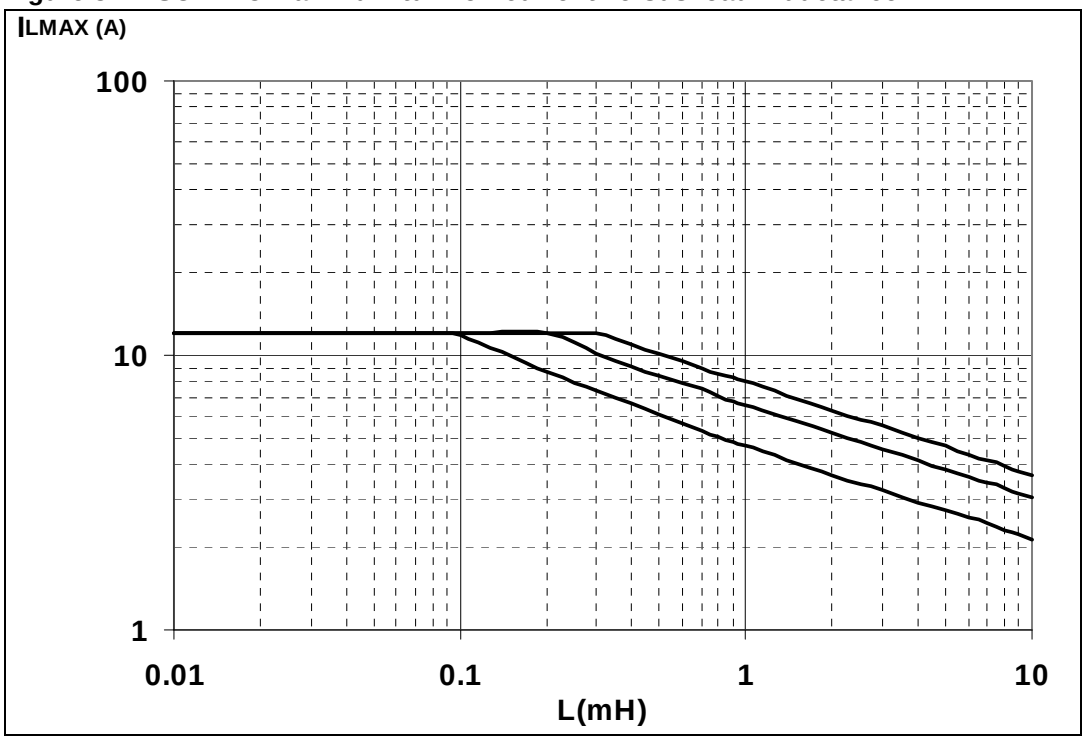
Values are generated with R_L = 0 Ω. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Figure 31. SO-8 demagnetization



3.3 SOT-223 maximum demagnetization energy

Figure 32. SOT-223 maximum turn-off current versus load inductance



Legend

A = Single Pulse at T_{Jstart} = 150 °C

B = Repetitive pulse at T_{Jstart} = 100 °C

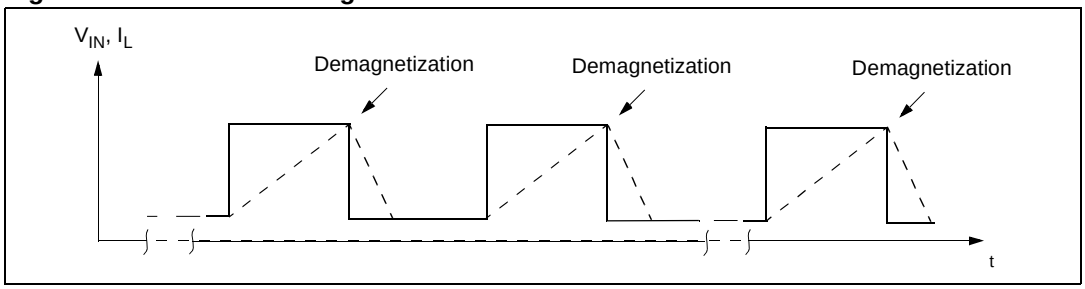
C = Repetitive Pulse at T_{Jstart} = 125 °C

Conditions:

V_{CC} = 13.5 V

Values are generated with R_L = 0 Ω. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

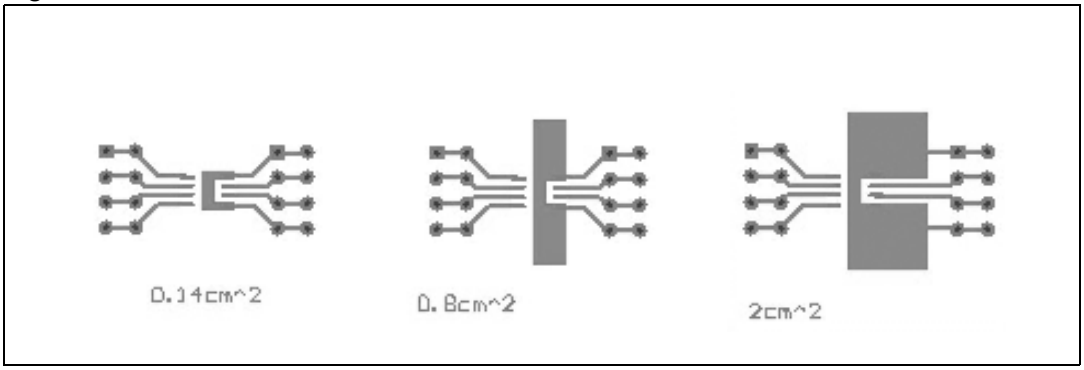
Figure 33. SOT-223 demagnetization



4 Package and PCB thermal data

4.1 SO-8 thermal data

Figure 34. SO-8 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 µm, Copper areas: 0.14 cm^2, 0.8 cm^2, 2 cm^2).

Figure 35. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

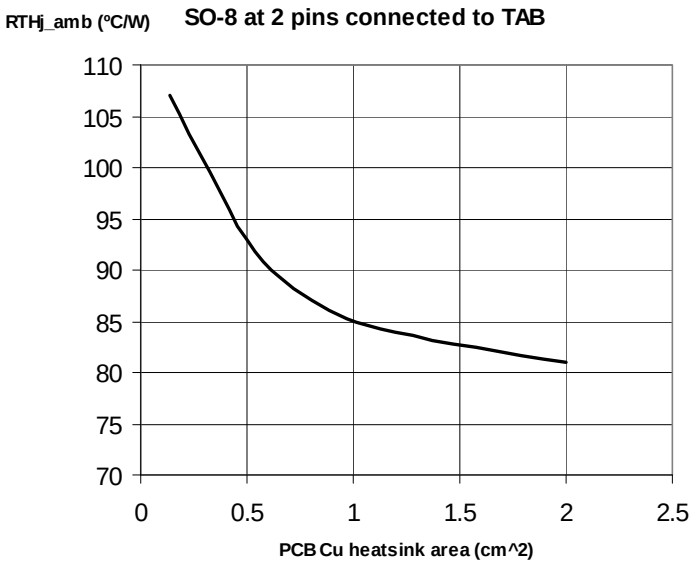


Figure 36. SO-8 thermal impedance junction ambient single pulse

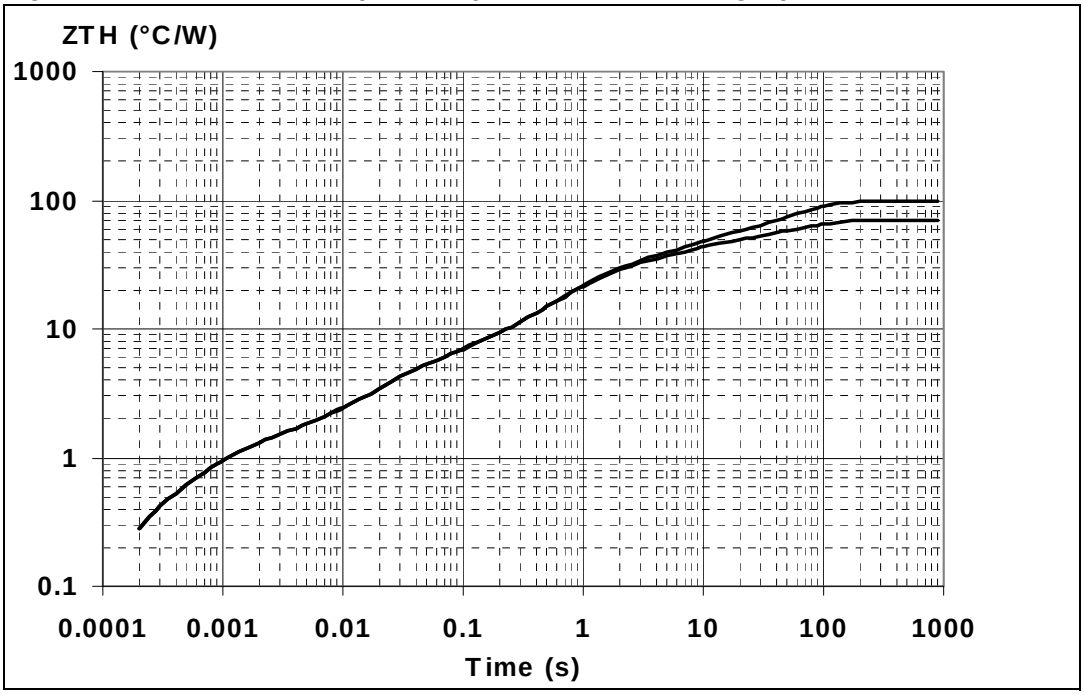
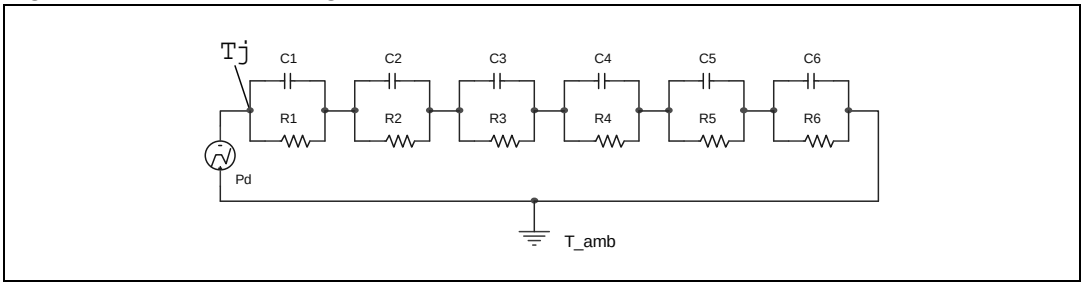


Figure 37. Thermal fitting model of an OMNIFET II in SO-8



Equation 1 Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 5. SO-8 thermal parameter

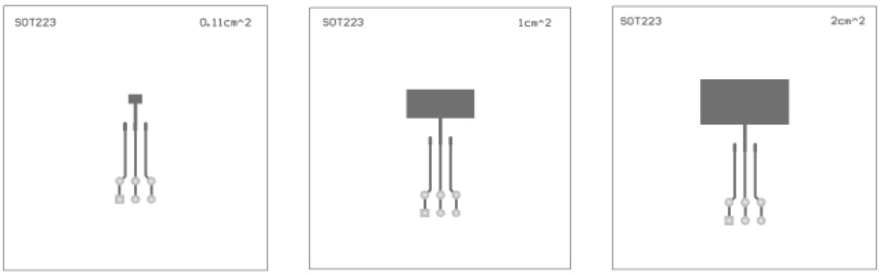
Area/island (cm^2)	Footprint	2
R1 (°C/W)	0.2	
R2 (°C/W)	0.9	
R3 (°C/W)	3.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	3.00E-04	

Table 5. SO-8 thermal parameter (continued)

Area/island (cm^2)	Footprint	2
C2 (W.s/°C)	9.00E-04	
C3 (W.s/°C)	7.50E-03	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

4.2 SOT-223 thermal data

Figure 38. SOT-223 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 µm, Copper areas: 0.11 cm^2, 1 cm^2, 2 cm^2).

Figure 39. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

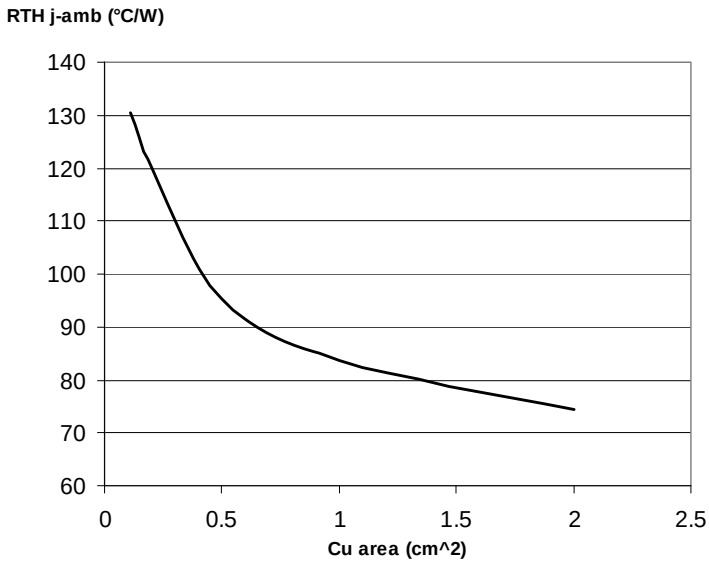


Figure 40. SOT-223 thermal impedance junction ambient single pulse

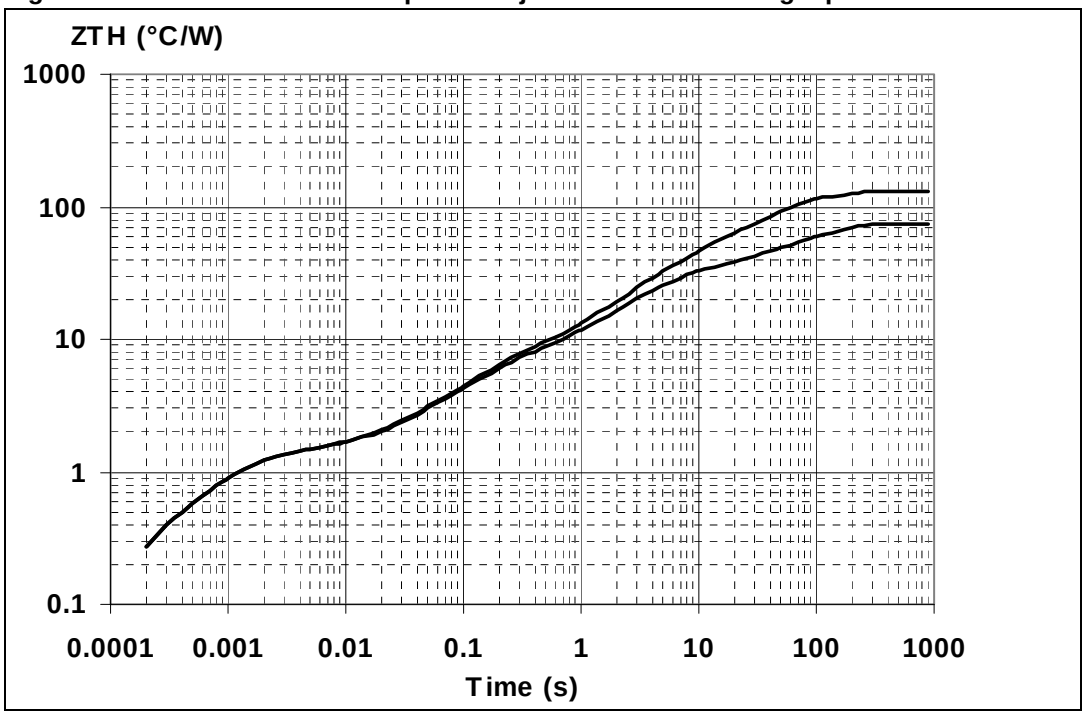
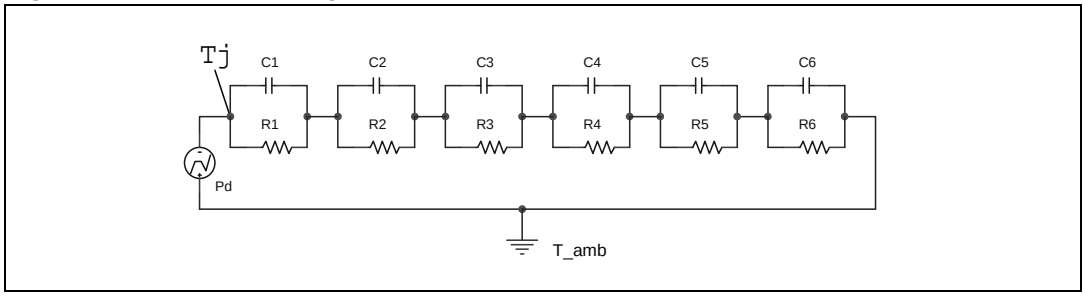


Figure 41. Thermal fitting model of an OMNIFET II in SOT-223



Equation 2 Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 6. SOT-223 thermal parameter

Area/island (cm^2)	Footprint	2
R1 (°C/W)	0.2	
R2 (°C/W)	1.1	
R3 (°C/W)	4.5	
R4 (°C/W)	24	
R5 (°C/W)	0.1	
R6 (°C/W)	100	45
C1 (W.s/°C)	3.00E-04	
C2 (W.s/°C)	9.00E-04	
C3 (W.s/°C)	3.00E-02	
C4 (W.s/°C)	0.16	
C5 (W.s/°C)	1000	
C6 (W.s/°C)	0.5	2

5 Package and packing information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

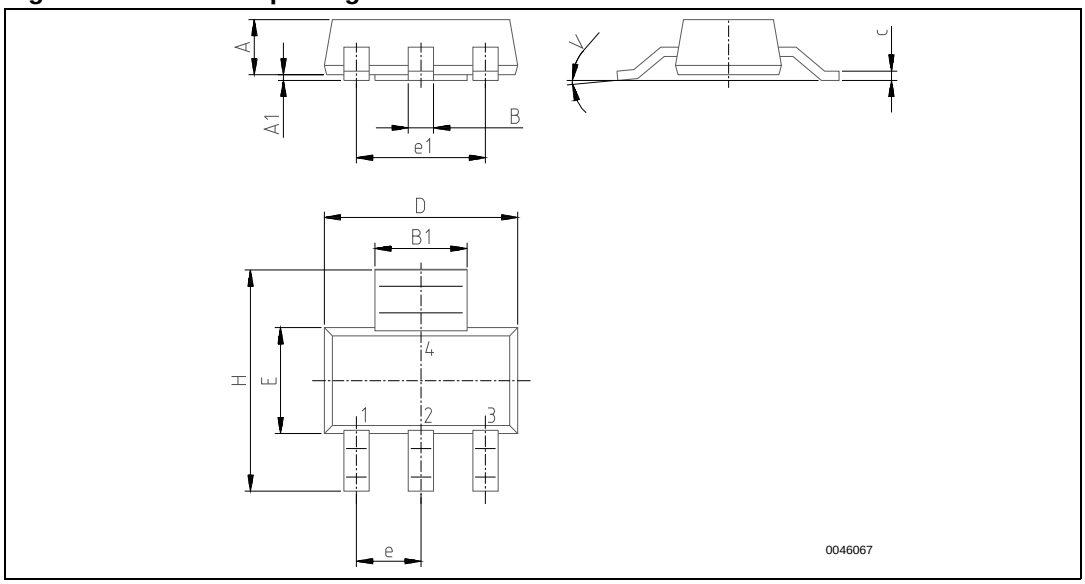
ECOPACK® is an ST trademark.

5.1 SOT-223 mechanical data

Table 7. SOT-223 mechanical data

Symbol	millimeters		
	Min.	Typ.	Max.
A			1.8
B	0.6	0.7	0.85
B1	2.9	3	3.15
c	0.24	0.26	0.35
D	6.3	6.5	6.7
e		2.3	
e1		4.6	
E	3.3	3.5	3.7
H	6.7	7	7.3
V	10 (max)		
A1	0.02		0.1

Figure 42. SOT-223 package dimensions

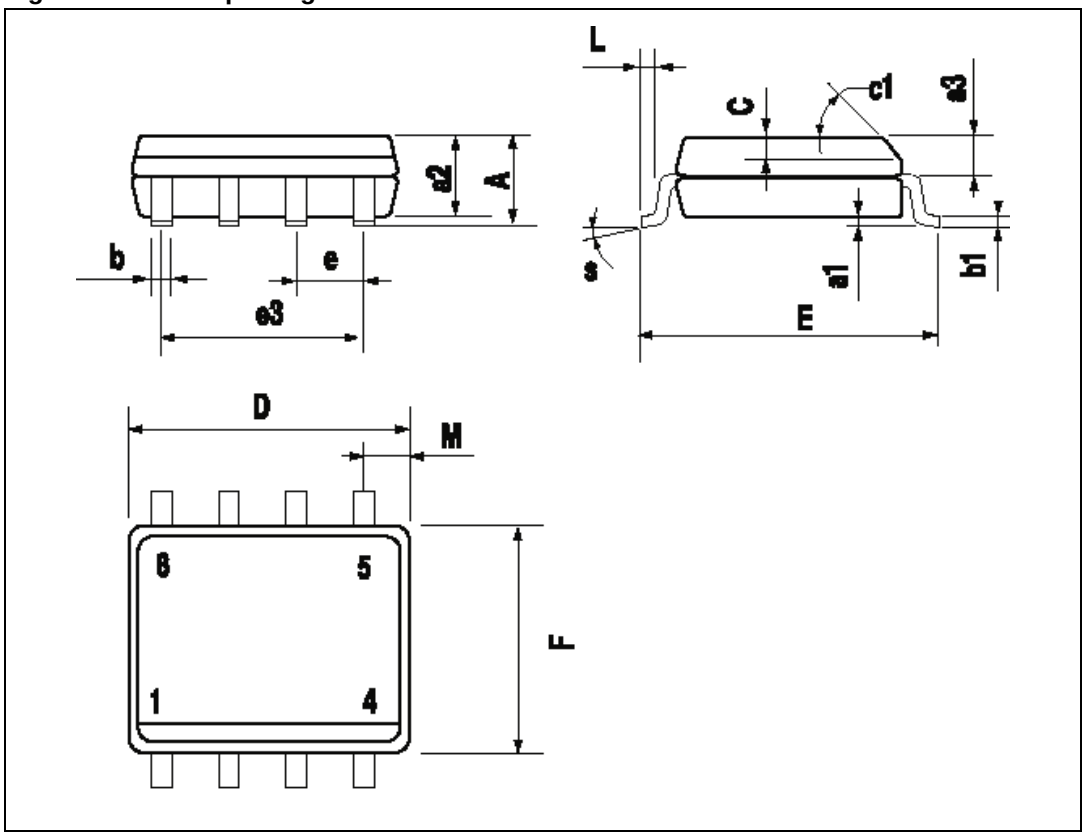


5.2 SO-8 mechanical data

Table 8. SO-8 mechanical data

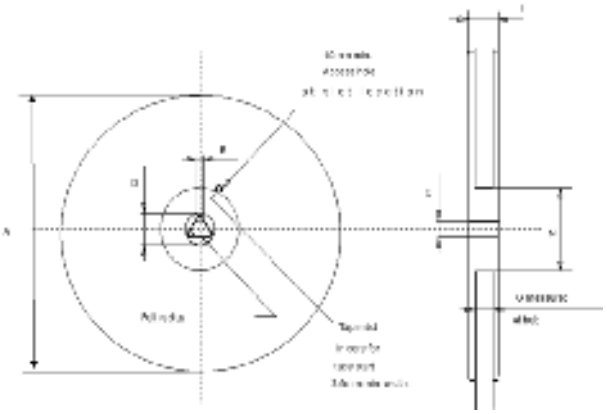
Dim.	mm		
	Min.	Typ.	Max.
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
b1	0.19		0.25
C	0.25		0.5
c1	45 (typ.)		
D	4.8		5
E	5.8		6.2
e		1.27	
e3		3.81	
F	3.8		4
L	0.4		1.27
M			0.6
S	8 (max.)		
L1	0.8		1.2

Figure 43. SO-8 package dimensions



5.3 SOT-223 packing information

Figure 44. SOT-223 tape and reel shipment (suffix “TR”)



REEL DIMENSIONS

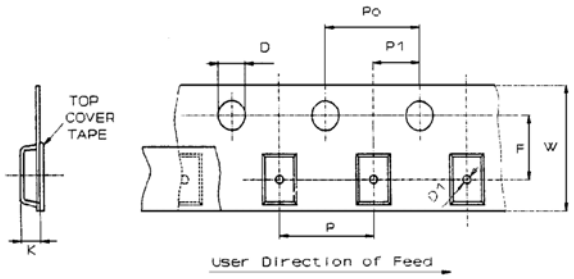
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

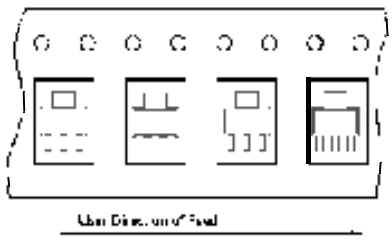
TAPE DIMENSIONS

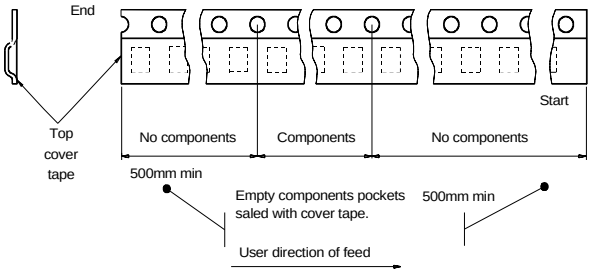
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.

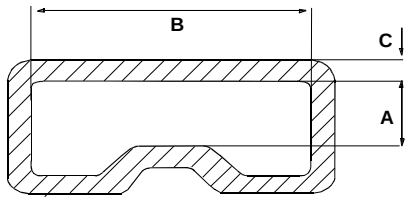






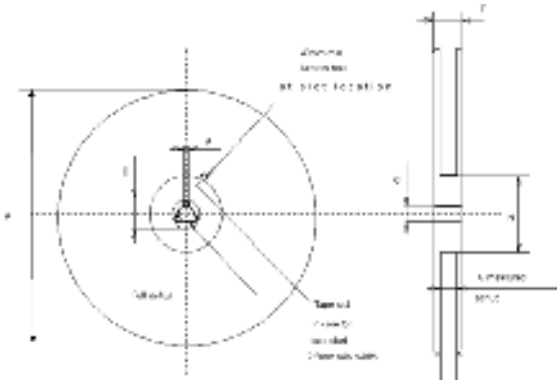
5.4 SO-8 packing information

Figure 45. SO-8 tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

Figure 46. SO-8 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

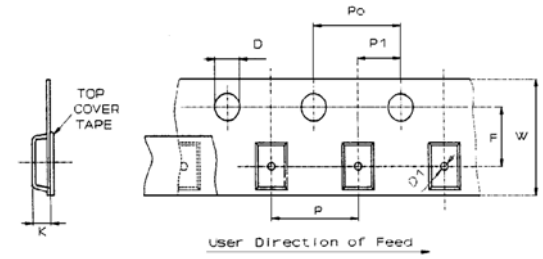
All dimensions are in mm.

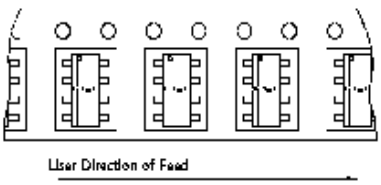
TAPE DIMENSIONS

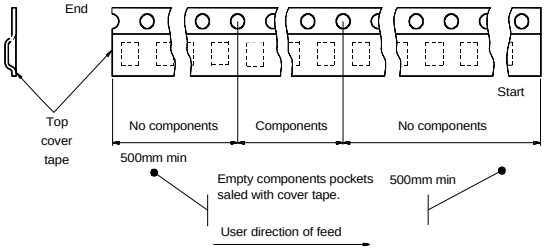
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	12
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	8
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	5.5
Compartment Depth	**K (max)**	4.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







6 Revision history

Table 9. Document revision history

Date	Revision	Changes
15-Oct-2009	1	Initial release.
26-Oct-2009	2	Updated *Figure 43: SO-8 package dimensions*. Updated *Table 8: SO-8 mechanical data*.
05-Jul-2011	3	*Table 4: Electrical characteristics*: – $R_{DS(on)}$: updated maximum values – $t_{d(on)}$, t_r, $t_{d(off)}$, t_f: updated min, typ and max values
18-Sep-2013	4	Updated Disclaimer.

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