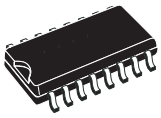
L6563H

High voltage start-up transition-mode PFC

Datasheet - production data



SO16

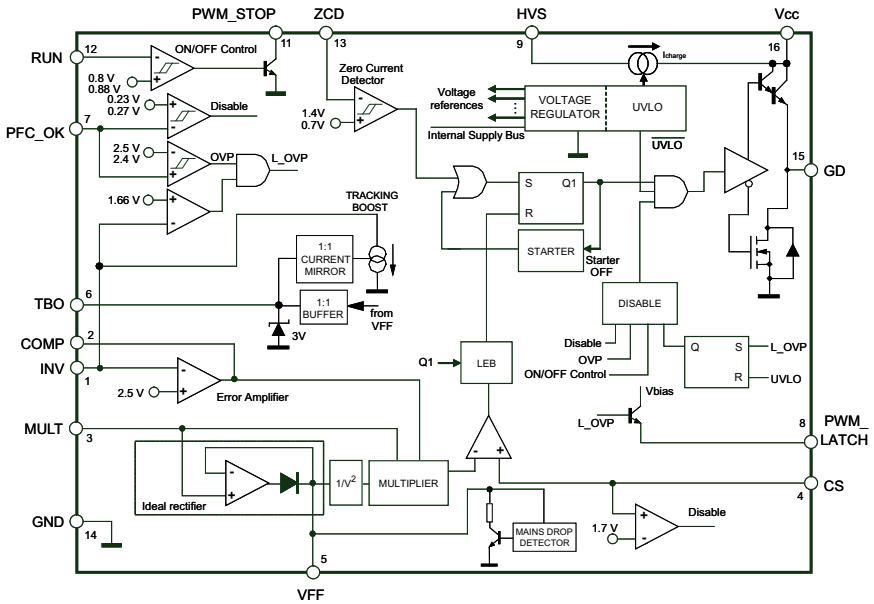
Features

- On-board 700 V start-up source
- Tracking boost function
- Fast “bidirectional” input voltage feedforward (1/V^2 correction)
- Interface for cascaded converter's PWM controller
- Remote ON/OFF control
- Accurate adjustable output overvoltage protection
- Protection against feedback loop disconnection (latched shutdown)
- Inductor saturation protection
- Low (≤ 100 µA) start-up current
- 6 mA max. operating bias current
- 1% (at T_J = 25 °C) internal reference voltage
- -600/+800 mA totem pole gate driver with active pull-down during UVLO

Applications

- PFC pre-regulators for:
  - Hi-end AC-DC adapter/charger
  - IEC61000-3-2 or JEITA-MITI compliant SMPS, in excess of 400 W
- SMPS for LED luminaires

Figure 1. Block diagram



This is information on a product in full production. www.st.com

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1 Description

The L6563H is a current-mode PFC controller operating in transition mode (TM) which embeds the same features existing in the L6563S with the addition of a high voltage start-up source. These functions make the IC especially suitable for applications that have to be compliant with energy saving regulations and where the PFC pre-regulator works as the master stage.

The highly linear multiplier, along with a special correction circuit that reduces crossover distortion of the mains current, allows wide-range-mains operation with an extremely low THD even over a large load range.

The output voltage is controlled by means of a voltage-mode error amplifier and an accurate (1% at Tj = 25 °C) internal voltage reference. Loop's stability is optimized by the voltage feedforward function ($1/V^2$ correction), which in this IC uses a proprietary technique that considerably improves line transient response as well in case of mains both drops and surges (“bidirectional”).

Additionally, the IC provides the option for tracking boost operation, i.e. the output voltage is changed tracking the mains voltage.

The device includes disable functions suitable for remote ON/OFF control too.

In addition to an over voltage protection able to keep the output voltage under control during transient conditions, the IC is provided also with a protection against feedback loop failures or erroneous settings. Other on-board protection functions allow that brownout conditions and boost inductor saturation can be safely handled.

An interface with the PWM controller of the DC-DC converter supplied by the PFC pre-regulator is provided: the purpose is to stop the operation of the converter in case of anomalous conditions for the PFC stage (feedback loop failure, boost inductor's core saturation, etc.) and to handle the PFC stage in case of light load for the DC-DC converter, to make it easier to comply with energy saving regulations (Blue Angel, EnergyStar, Energy2000, etc.).

The totem-pole output stage, capable of 600 mA source and 800 mA sink current, is suitable for big MOSFET or IGBT drive. This, combined with the other features and the possibility to operate with ST's proprietary fixed-off-time control, makes the device an excellent solution for SMPS up to 400 W that need to be compliant with EN61000-3-2 and JEITA-MITI standards.

2 Maximum ratings

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{HVS}	9	Voltage range (referred to ground)	-0.3 to 700	V
I_{HVS}	9	Output current	Self-limited	I_{HVS}
Vcc	16	IC supply voltage (Icc = 20 mA)	Self-limited	V
-	1, 3, 7	Max. pin voltage (I_{pin} =1 mA)	Self-limited	V
-	2, 4 to 6, 8, 11, 12	Analog inputs and outputs	-0.3 to 8	V
I_{PWM_STOP}	11	Max. sink current	3	mA
I_{ZCD}	13	Zero current detector max. current	-10 (source) 10 (sink)	mA

2.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Max. thermal resistance, junction to ambient	120	°C/W
Ptot	Power dissipation at T_A = 50 °C	0.75	W
T_J	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

3 Pin connection

Figure 2. Pin connection

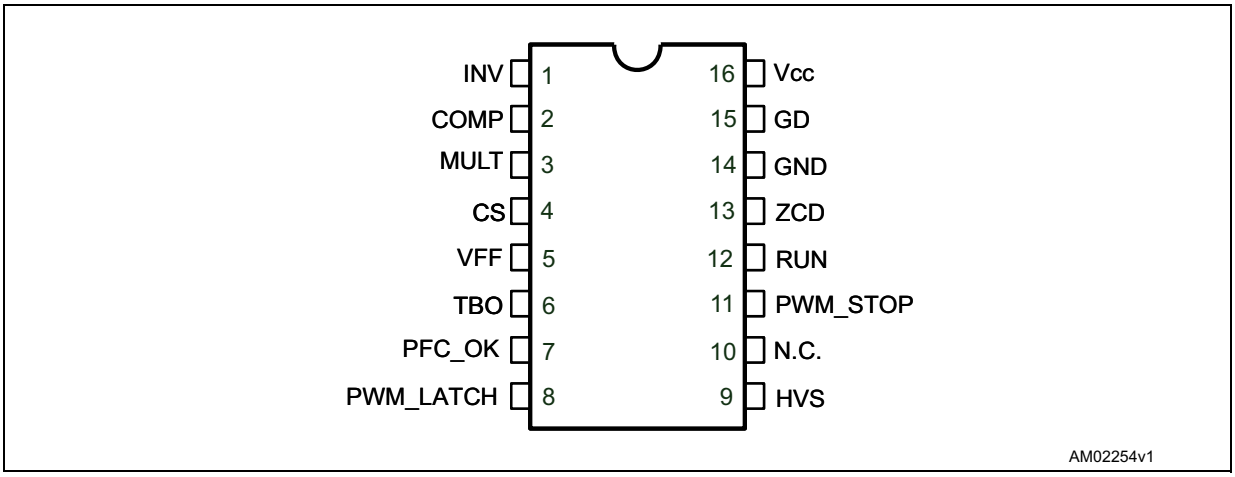


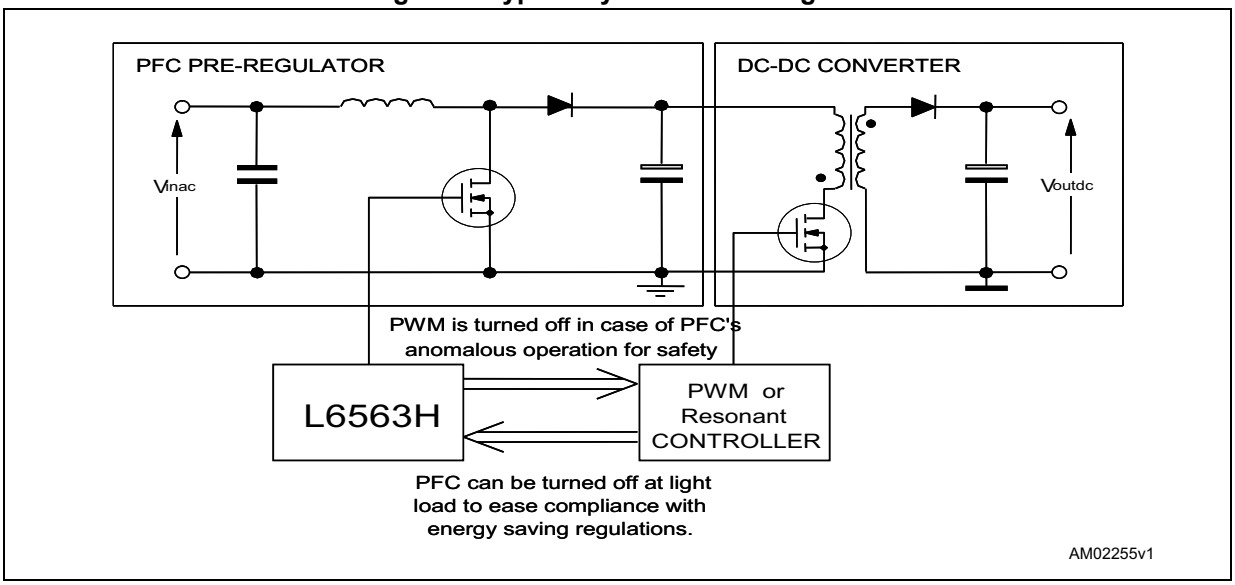
Table 3. Pin description

No.	Name	Function
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider. The pin normally features high impedance but, if the tracking boost function is used, an internal current generator programmed by TBO (pin 6) is activated. It sinks current from the pin to change the output voltage so that it tracks the mains voltage.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV (pin 1) to achieve stability of the voltage control loop and ensure high power factor and low THD. To avoid uncontrolled rise of the output voltage at zero load, when the voltage on the pin falls below 2.4 V the gate driver output is inhibited (burst-mode operation).
3	MULT	Mains input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop. The voltage on this pin is used also to derive the information on the RMS mains voltage.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal reference to determine MOSFET's turn-off. A second comparison level at 1.7 V detects abnormal currents (e.g. due to boost inductor saturation) and, on this occurrence, activates a safety procedure that temporarily stops the converter and limits the stress of the power components.
5	VFF	Second input to the multiplier for $1/V^2$ function. A capacitor and a parallel resistor must be connected from the pin to GND. They complete the internal peak-holding circuit that derives the information on the RMS mains voltage. The voltage at this pin, a dc level equal to the peak voltage on pin MULT (3), compensates the control loop gain dependence on the mains voltage. Never connect the pin directly to GND but with a resistor ranging from 100 kΩ (minimum) to 2 M Ω (maximum).
6	TBO	Tracking boost function. This pin provides a buffered VFF voltage. A resistor connected between this pin and GND defines a current that is sunk from pin INV (1). In this way, the output voltage is changed proportionally to the mains voltage (tracking boost). If this function is not used leave this pin open.

Table 3. Pin description (continued)

No.	Name	Function
7	PFC_OK	PFC pre-regulator output voltage monitoring/disable function. This pin senses the output voltage of the PFC pre-regulator through a resistor divider and is used for protection purposes. If the voltage on the pin exceeds 2.5 V the IC stops switching and restarts as the voltage on the pin falls below 2.4 V. However, if at the same time the voltage of the INV pin falls below 1.66V, a feedback failure is assumed. In this case the device is latched off and the PWM_LATCH (8) pin is asserted high. Normal operation can be resumed only by cycling Vcc bringing its value lower than 6V before to move up to Turn on threshold. If the voltage on this pin is brought below 0.23 V the IC is shut down. To restart the IC the voltage on the pin must go above 0.27 V. This can be used as a remote on/off control input.
8	PWM_LATCH	Output pin for fault signaling. During normal operation this pin features high impedance. If a feedback failure is detected (PFC_OK > 2.5 V and INV < 1.66 V) the pin is asserted high. Normally, this pin is used to stop the operation of the dc-dc converter supplied by the PFC pre-regulator by invoking a latched disable of its PWM controller. If not used, the pin is left floating.
9	HVS	High voltage start-up. The pin, able to withstand 700 V, is to be tied directly to the rectified mains voltage. A 1 mA internal current source charges the capacitor connected between pin Vcc (16) and pin GND (14) until the voltage on the pin Vcc reaches the start-up threshold, then it is shut down. Normally, the generator is re-enabled when the Vcc voltage falls below 6 V to ensure a low power throughput during short-circuit. Otherwise, when a latched protection is tripped the generator is re-enabled as Vcc reaches the UVLO threshold to keep the latch supplied.
10	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
11	PWM_STOP	Output pin for fault signaling. During normal operation this pin features high impedance. If the IC is disabled by a voltage below 0.8 V on pin RUN (12) the voltage on the pin is pulled to ground. Normally, this pin is used to temporarily stop the operation of the dc-dc converter supplied by the PFC pre-regulator by disabling its PWM controller. A typical usage of this function is brownout protection in systems where the PFC pre-regulator is the master stage. If not used, the pin is left floating.
12	RUN	Remote ON/OFF control. A voltage below 0.8 V shuts down (not latched) the IC and brings its consumption to a considerably lower level. PWM_STOP is asserted low. The IC restarts as the voltage at the pin goes above 0.88V. Connect this pin to pin VFF (5) either directly or through a resistor divider to use this function as brownout (AC mains undervoltage) protection.
13	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
14	GND	Ground. Current return for both the signal part of the IC and the gate driver.
15	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12 V to avoid excessive gate voltages.
16	Vcc	Supply voltage of both the signal part of the IC and the gate driver. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC.

Figure 3. Typical system block diagram



4 Electrical characteristics

T_J = -25 to 125 °C, V_{CC} = 12 V, C_O = 1 nF between pin GD and GND, C_{FF} = 1 µF and R_{FF} = 1 MΩ between pin VFF and GND; unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
Vcc	Operating range	After turn-on	10.3	-	22.5	V
Vcc_{On}	Turn-on threshold	(1)	11	12	13	V
Vcc_{Off}	Turn-off threshold	(1)	8.7	9.5	10.3	V
$Vcc_{restart}$	Vcc for resuming from latch	OVP latched	5	6	7	V
Hys	Hysteresis	-	2.3	-	2.7	V
V_Z	Zener voltage	Icc = 20 mA	22.5	25	28	V
Supply current						
$I_{start-up}$	Start-up current	Before turn-on, Vcc = 10 V	-	90	150	µA
I_q	Quiescent current	After turn-on, V_{MULT} = 1 V	-	4	5	mA
I_{CC}	Operating supply current	At 70 kHz	-	5	6.0	mA
I_{qdis}	Idle state quiescent current	$V_{PFC_OK} > V_{PFC_OK_S}$ AND $V_{INV} < V_{PFC_OK} - V_{FFD}$	-	180	280	µA
		$V_{PFC_OK} < V_{PFC_OK_D}$ OR $V_{RUN} < V_{DIS}$	-	1.5	2.2	mA
I_q	Quiescent current	$V_{PFC_OK} > V_{PFC_OK_S}$ OR V_{COMP} < 2.3 V	-	2.2	3	mA
High voltage start-up generator						
V_{HV}	Breakdown voltage	I_{HV} < 100 µA	700	-	-	V
$V_{HVstart}$	Start voltage	I_{Vcc} < 100 µA	65	80	100	V
I_{charge}	Vcc charge current	$V_{HV} > V_{Hvstart}$, Vcc > 3 V	0.55	0.85	1	mA
$I_{HV, ON}$	ON-state current	$V_{HV} > V_{Hvstart}$, Vcc > 3 V	-	-	1.6	mA
		$V_{HV} > V_{Hvstart}$, Vcc = 0	-	-	0.8	
$I_{HV, OFF}$	OFF-state leakage current	V_{HV} = 400 V	-	-	40	µA
$V_{CCrestart}$	Vcc restart voltage	Vcc falling	5	6	7	V
		IC latched off (1)	8.7	9.5	10.3	
Multiplier input						
I_{MULT}	Input bias current	V_{MULT} = 0 to 3 V	-	-0.2	-1	µA
V_{MULT}	Linear operation range	-	0 to 3	-	-	V
V_{CLAMP}	Internal clamp level	I_{MULT} = 1 mA	9	9.5	-	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
ΔVcs ΔV_{MULT}	Output max. slope	V_{MULT} =0 to 0.4 V, V_{VFF} = 0.8 V V_{COMP} = Upper clamp	2.2	2.34	-	V/V
K_M	Gain(2)	V_{MULT} = 1 V, V_{COMP} = 4 V	0.375	0.45	0.525	1/V
Error amplifier						
V_{INV}	Voltage feedback input threshold	T_J = 25 °C	2.475	2.5	2.525	V
		10.3 V < Vcc < 22.5 V (3)	2.455	-	2.545	
	Line regulation	Vcc = 10.3 V to 22.5 V	-	2	5	mV
I_{INV}	Input bias current	TBO open, V_{INV} = 0 to 4 V	-	-0.2	-1	µA
$V_{INVCLAMP}$	Internal clamp level	I_{INV} = 1 mA	8	9	-	V
Gv	Voltage gain	Open loop	60	80	-	dB
GB	Gain-bandwidth product	-	-	1	-	MHz
I_{COMP}	Source current	V_{COMP} = 4 V, V_{INV} = 2.4 V	2	4	-	mA
	Sink current	V_{COMP} = 4 V, V_{INV} = 2.6 V	2.5	4.5	-	mA
V_{COMP}	Upper clamp voltage	I_{SOURCE} = 0.5 mA	5.7	6.2	6.7	V
	Burst-mode voltage	(3)	2.3	2.4	2.5	
	Lower clamp voltage	I_{SINK} = 0.5 mA (3)	2.1	2.25	2.4	
Current sense comparator						
I_{CS}	Input bias current	V_{CS} = 0	-	-	1	µA
t_{LEB}	Leading edge blanking	-	100	150	250	ns
$td_{(H-L)}$	Delay to output	-	100	200	300	ns
$V_{CSclamp}$	Current sense reference clamp	V_{COMP} = upper clamp, V_{MULT} =1 V V_{VFF} = 1 V	1.0	1.08	1.16	V
Vcs_{ofst}	Current sense offset	V_{MULT} = 0, V_{VFF} = 3 V	-	40	70	mV
		V_{MULT} = 3 V, V_{VFF} = 3 V	-	20	-	
Boost inductor saturation detector						
V_{CS_th}	Threshold on current sense	(3)	1.6	1.7	1.8	V
I_{INV}	E/A input pull-up current	After V_{CS} > V_{CS_th}, before restarting	7	10	13	µA
PFC_OK functions						
I_{PFC_OK}	Input bias current	V_{PFC_OK} = 0 to 2.6 V	-	-0.1	-1	µA
$V_{PFC_OK_C}$	Clamp voltage	I_{PFC_OK} = 1 mA	9	9.5	-	V
$V_{PFC_OK_S}$	OVP threshold	(1) voltage rising	2.435	2.5	2.565	V
$V_{PFC_OK_R}$	Restart threshold after OVP	(1) voltage falling	2.34	2.4	2.46	V
$V_{PFC_OK_D}$	Disable threshold	(1) voltage falling	0.12	-	0.35	V
$V_{PFC_OK_D}$	Disable threshold	(1) voltage falling T_J = 25 °C	0.17	0.23	0.29	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{PFC_OK_E}$	Enable threshold	(1) voltage rising	0.15	-	0.38	V
$V_{PFC_OK_E}$	Enable threshold	(1) voltage rising Tj = 25 °C	0.21	0.27	0.32	V
V_{FFD}	Feedback failure detection threshold (V_{INV} falling)	$V_{PFC_OK} = V_{PFC_OK_S}$	1.61	1.66	1.71	mV
Zero current detector						
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 2.5 mA	5.0	5.7	-	V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 2.5 mA	-0.3	0	0.3	V
V_{ZCDA}	Arming voltage (positive-going edge)	-	1.1	1.4	1.9	V
V_{ZCDT}	Triggering voltage (negative-going edge)	-	0.5	0.7	0.9	V
I_{ZCDb}	Input bias current	V_{ZCD} = 1 to 4.5 V	-	-	1	µA
I_{ZCDsrc}	Source current capability	-	-2.5	-4	-	mA
I_{ZCDsnk}	Sink current capability	-	2.5	5	-	mA
Tracking boost function						
ΔV	Dropout voltage VVFF-VTBO	I_{TBO} = 0.2 mA	-20	-	20	mV
I_{TBO}	Linear operation	-	0	-	0.2	mA
	I_{INV}-I_{TBO} current mismatch	I_{TBO} = 25 µA to 0.2 mA	-5.5	-	1.0	%
-	I_{INV}-I_{TBO} current mismatch	I_{TBO} = 25 µA to 0.2 mA T_J = 25 °C	-4.0	-	+0	%
$V_{TBOclamp}$	Clamp voltage	(3) V_{VFF} = 4 V	2.9	3	3.1	V
I_{TBO_Pull}	Pull-up current	V_{TBO} = 1 V $V_{FF} = V_{MULT}$ = 0 V	-	-	2	µA
PWM_STOP						
Ileak	High level leakage current	V_{PWM_STOP} = Vcc	-	-	1	µA
V_L	Low level	I_{PWM_STOP} = 0.5 mA	-	-	1	V
RUN function						
I_{RUN}	Input bias current	V_{RUN} = 0 to 3 V	-	-	-1	µA
V_{DIS}	Disable threshold	(3) voltage falling	0.745	0.8	0.855	V
V_{EN}	Enable threshold	(3) voltage rising	0.845	0.88	0.915	V
Start-up timer						
t_{START_DEL}	Start-up delay	First cycle after wake-up	25	50	75	µs
t_{START}	Timer period	-	75	150	300	µs
		Restart after $V_{CS} > V_{CS_th}$	150	300	600	

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Voltage feedforward						
V_{VFF}	Linear operation range	-	0.8	-	3	V
ΔV	Dropout V_{MULTpk}-V_{VFF}	Vcc < Vcc_{On}	-	-	800	mV
		Vcc > or = to Vcc_{On}	-	-	20	
ΔV_{VFF}	Line drop detection threshold	Below peak value	40	70	100	mV
ΔV_{VFF}	Line drop detection threshold	Below peak value T_J = 25 °C	50	70	90	mV
R_{DISCH}	Internal discharge resistor	T_J = 25 °C	7.5	10	12.5	kΩ
		-	5	-	20	
V_{VFF}	Linear operation range	-	0.8	-	3	V
PWM_LATCH						
Ileak	Low level leakage current	V_{PWM_LATCH} = 0	-	-	-1	µA
V_H	High level	I_{PWM_LATCH} = -0.5 mA	4.5	-	-	V
V_H	High level	I_{PWM_LATCH} = -0.25 mA Vcc = Vcc_{Off}	2.5	-	-	V
V_H	High level	I_{PWM_LATCH} = -0.25 mA Vcc = Vcc_{Off} T_J = 25 °C	2.8	-	-	V
Gate driver						
V_{OL}	Output low voltage	I_{sink} = 100 mA	-	0.6	1.2	V
V_{OH}	Output high voltage	I_{source} = 5 mA	9.8	10.3	-	V
I_{srcpk}	Peak source current	-	-0.6	-	-	A
I_{snkpk}	Peak sink current	-	0.8	-	-	A
t_f	Voltage fall time	-	-	30	60	ns
t_r	Voltage rise time	-	-	45	110	ns
V_{Oclamp}	Output clamp voltage	I_{source} = 5 mA; Vcc = 20 V	10	12	15	V
	UVLO saturation	Vcc= 0 to V_{CCon}, I_{sink} = 2 mA	-	-	1.1	V

1. Parameters tracking each other
2. The multiplier output is given by:

$$V_{cs} = V_{CS_Ofst} + K_M \cdot \frac{V_{MULT} \cdot (V_{COMP} - 2.5)}{V_{VFF}^2}$$

3. Parameters tracking each other

5 Typical electrical performance

Figure 4. IC consumption vs. V_{CC}

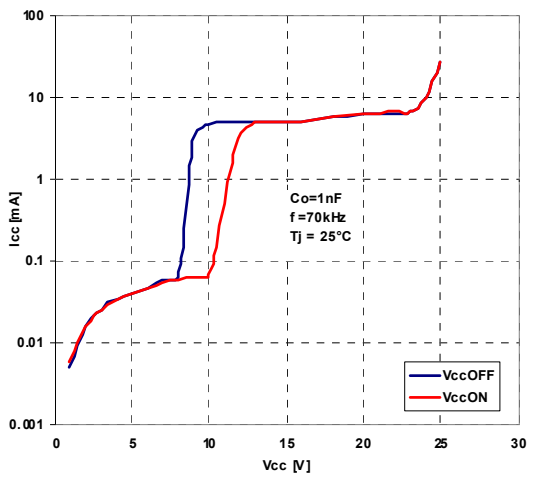


Figure 5. IC consumption vs. T_J

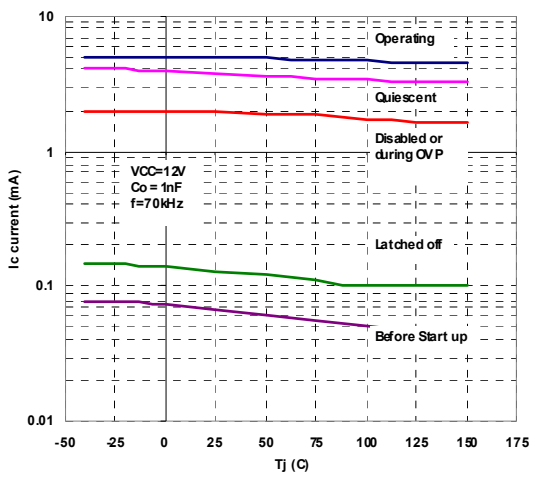


Figure 6. V_{CC} Zener voltage vs. T_J

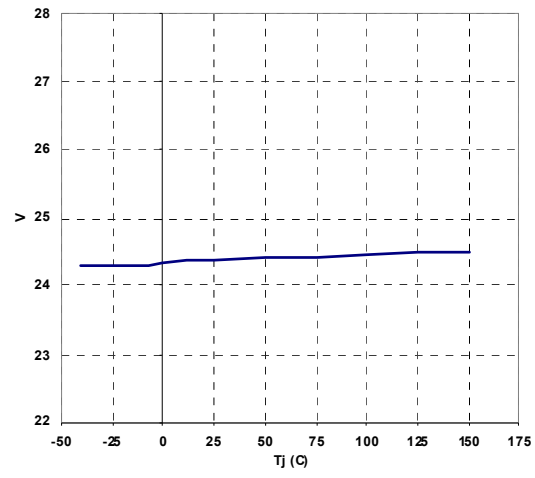


Figure 7. Start-up and UVLO vs. T_J

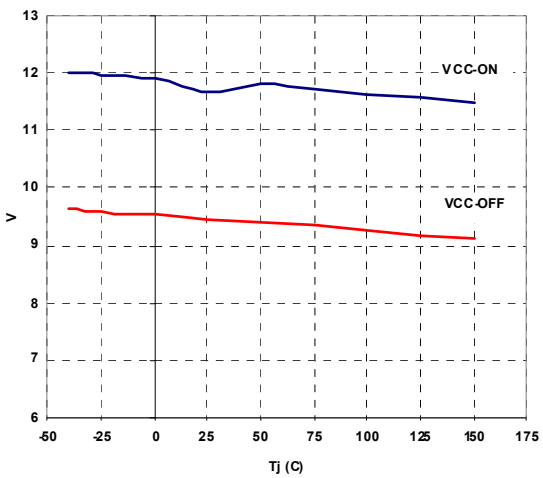


Figure 8. Feedback reference vs. T_J

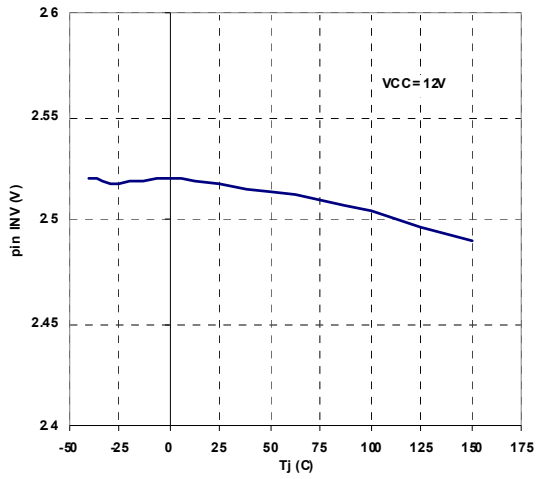


Figure 9. E/A output clamp levels vs. T_J

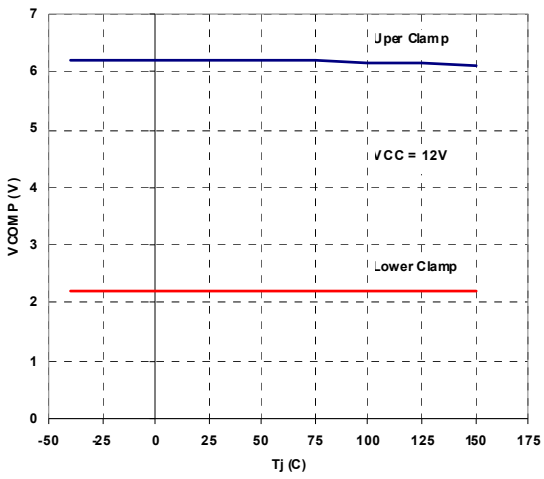


Figure 10. UVLO saturation vs. T_J

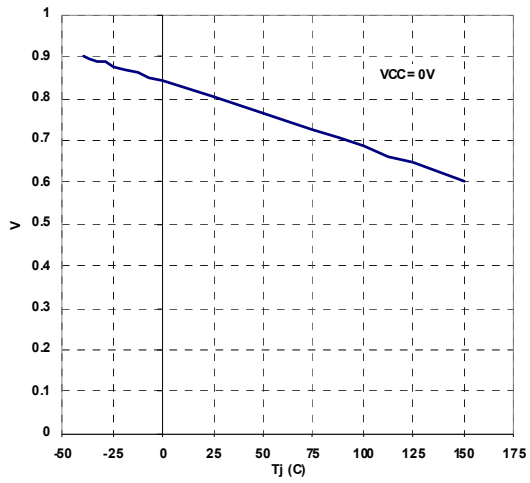


Figure 11. OVP levels vs. T_J

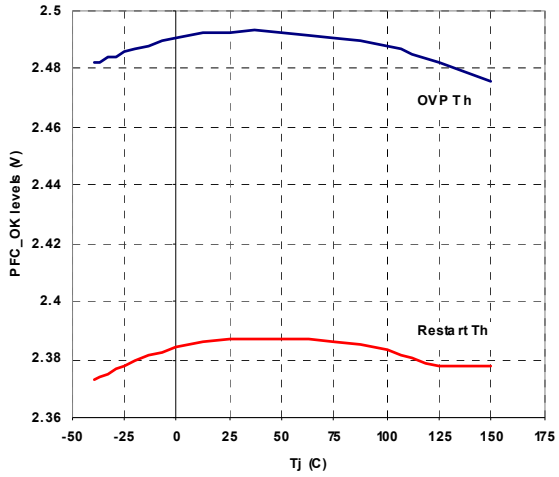


Figure 12. Inductor saturation threshold vs. T_J

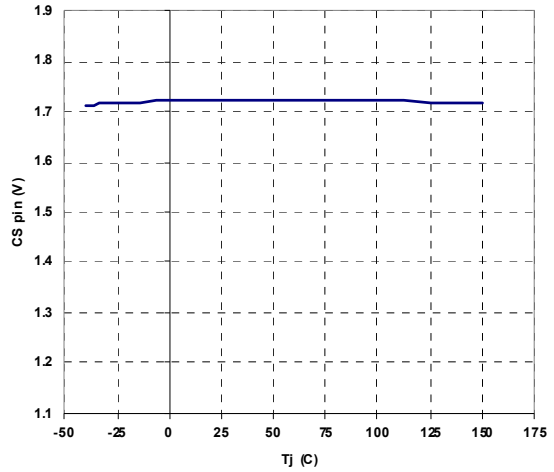


Figure 13. Vcs clamp vs. T_J

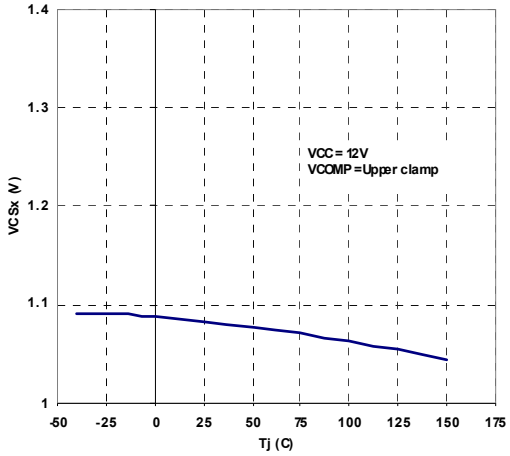


Figure 14. ZCD sink/source capability vs. T_J

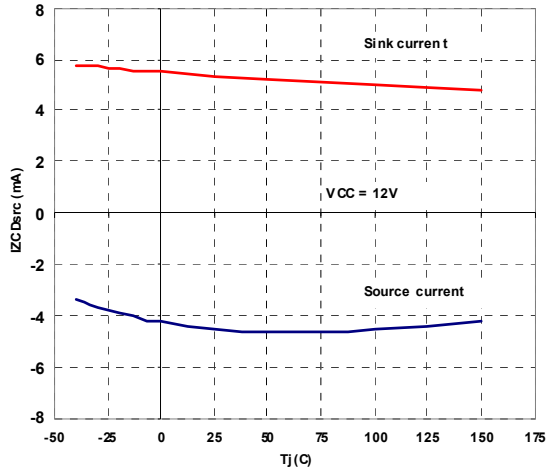


Figure 15. ZCD clamp level vs. T_J

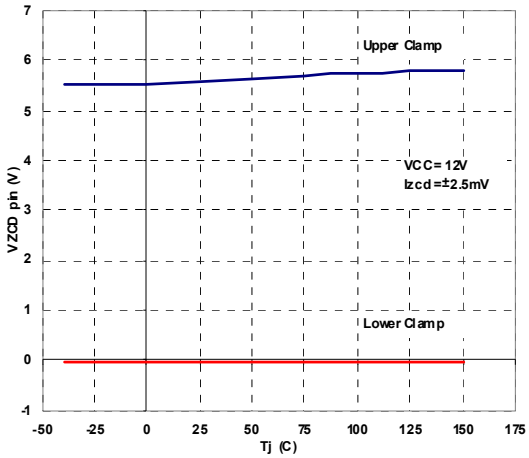


Figure 16. TBO clamp vs. T_J

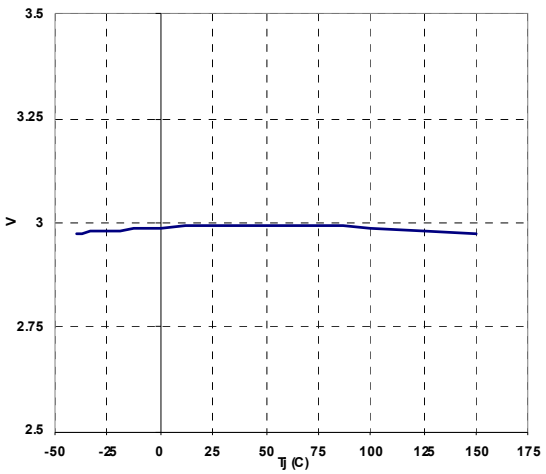


Figure 17. V_{VFF} - V_{TBO} dropout vs. T_J

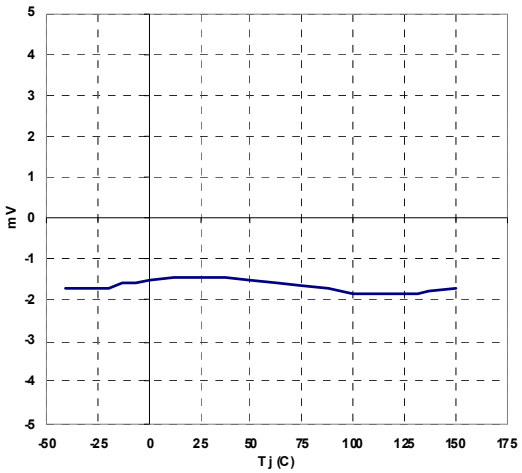


Figure 18. I_{INV} - I_{TBO} current mismatch vs. T_J

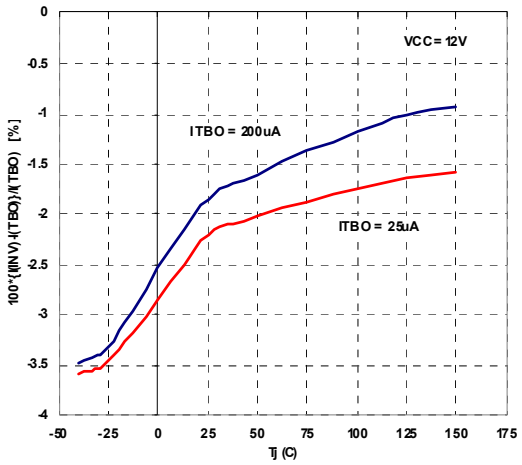


Figure 19. I_{INV} - I_{TBO} mismatch vs. I_{TBO} current

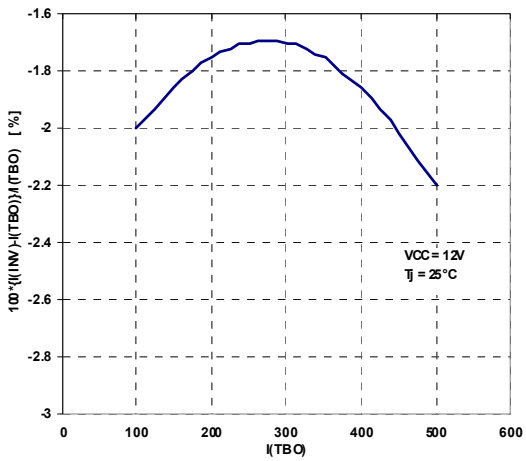


Figure 20. R discharge vs. T_J

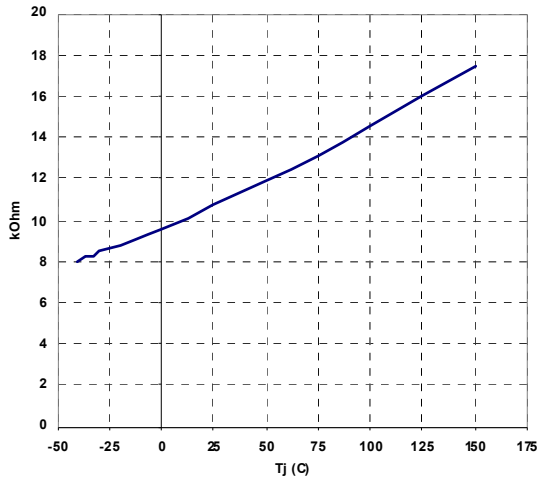


Figure 21. Line drop detection threshold vs. T_J

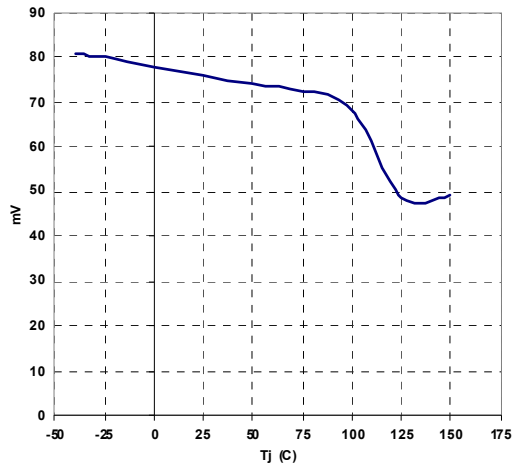


Figure 22. V_{MULTpk} - V_{VFF} dropout vs. T_J

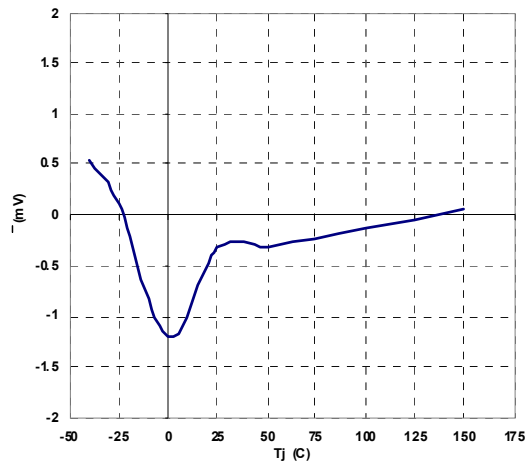


Figure 23. PFC_OK threshold vs. T_J

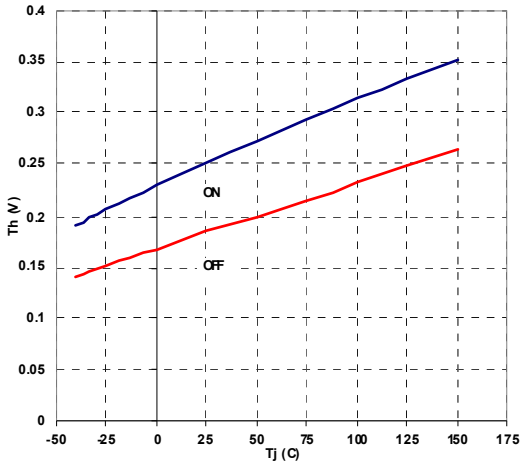


Figure 24. PFC_OK FFD threshold vs. T_J

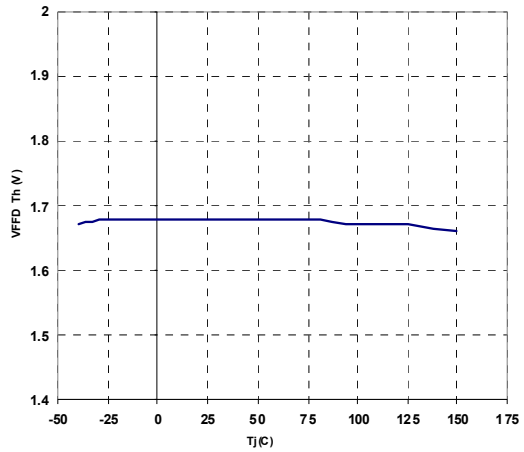


Figure 25. PWM_LATCH high saturation vs. T_J

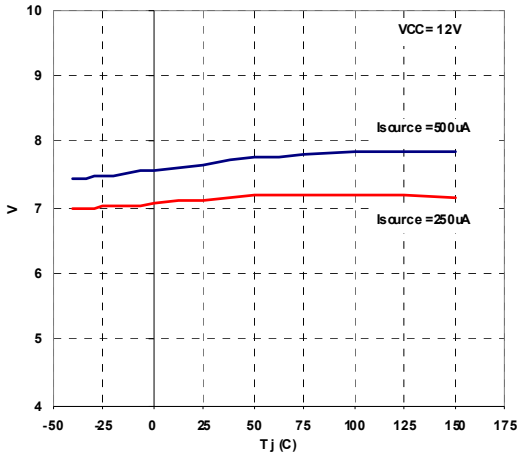


Figure 26. RUN threshold vs. T_J

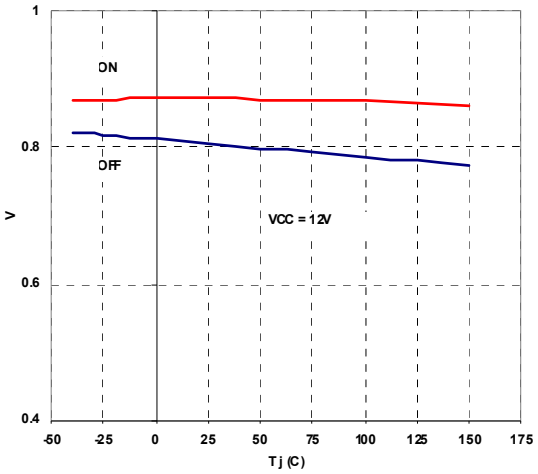


Figure 27. PWM_STOP low saturation vs. T_J

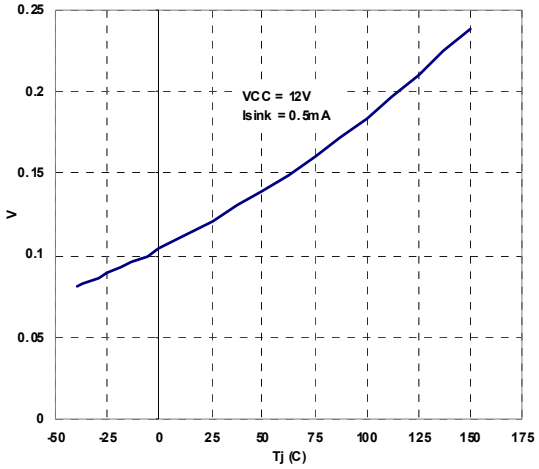


Figure 28. Multiplier characteristics at V_{FF} = 1 V

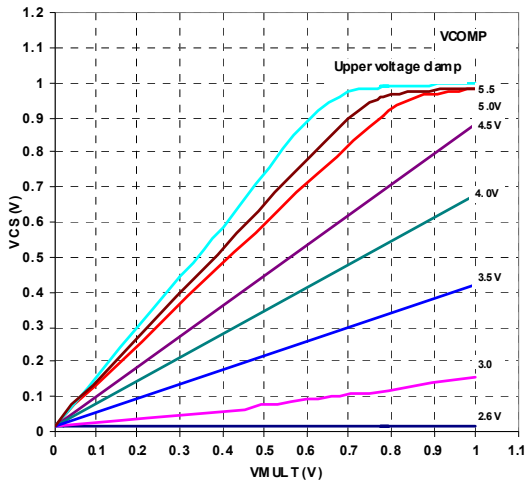


Figure 29. Multiplier characteristics at V_{FF} = 3 V

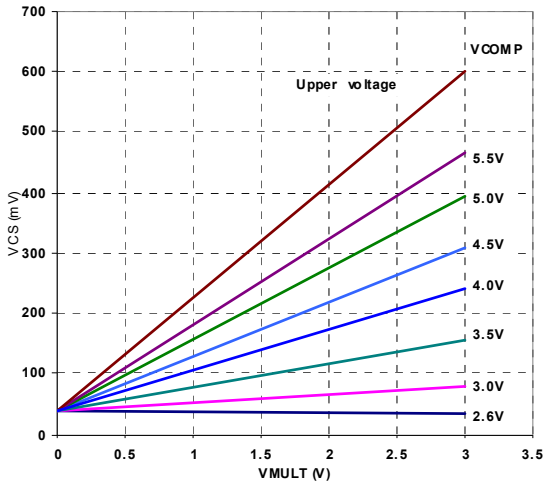


Figure 30. Multiplier gain vs. T_J

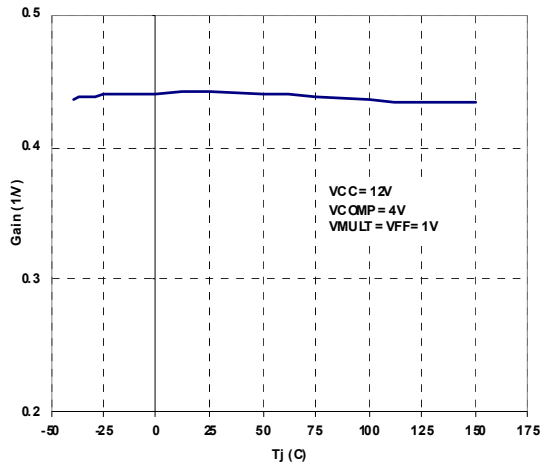


Figure 31. Gate drive clamp vs. T_J

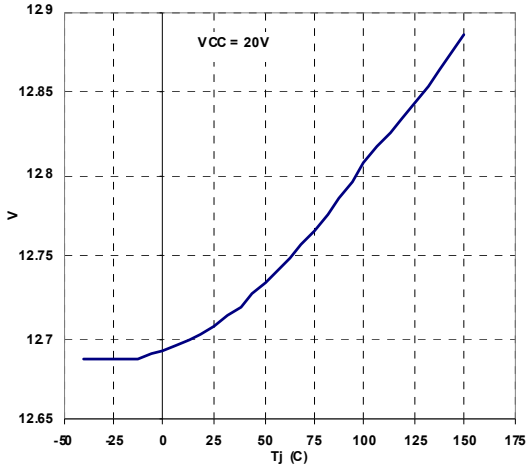


Figure 32. Gate drive output saturation vs. T_J

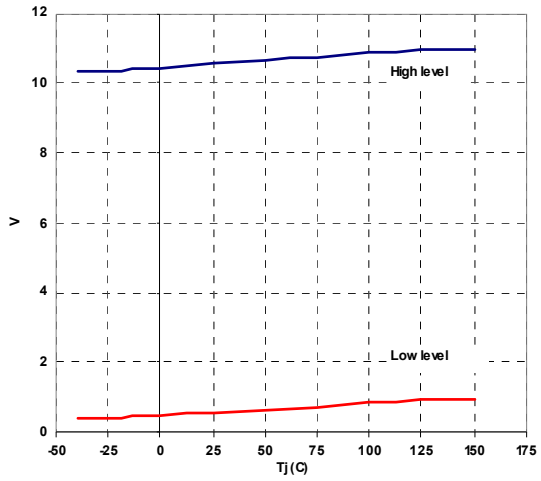


Figure 33. Delay to output vs. T_J

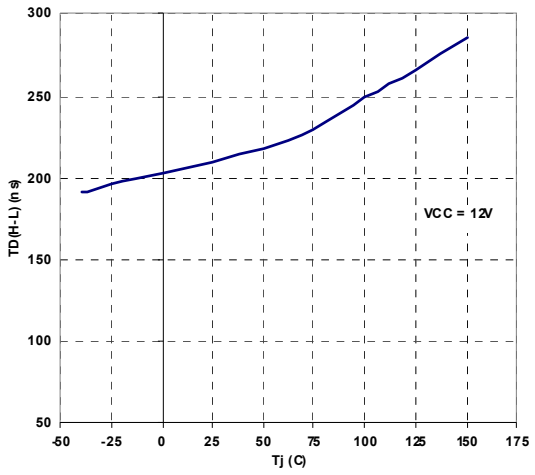


Figure 34. Start-up timer period vs. T_J

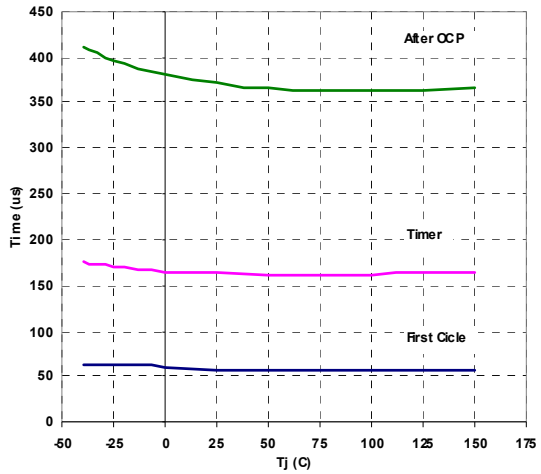


Figure 35. HV start voltage vs. T_J

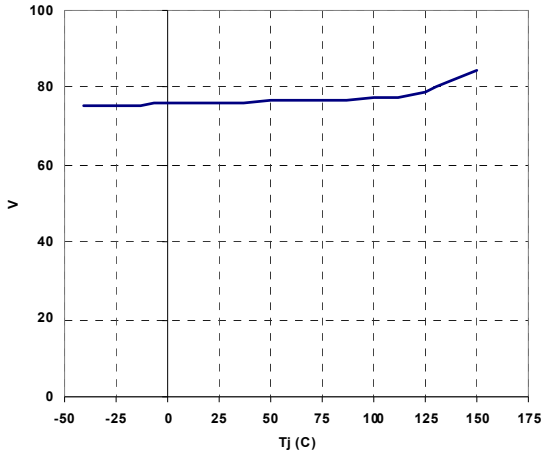


Figure 36. V_{CC} restart voltage vs. T_J

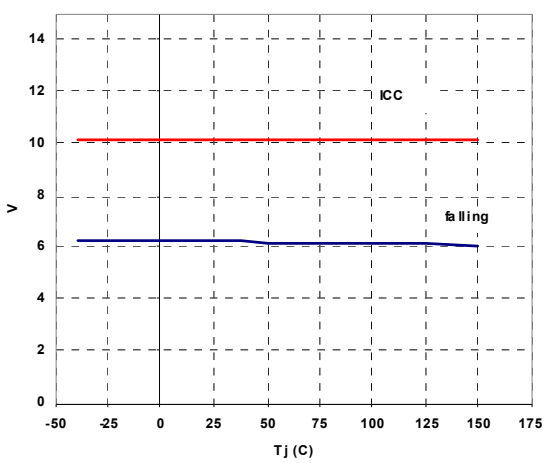
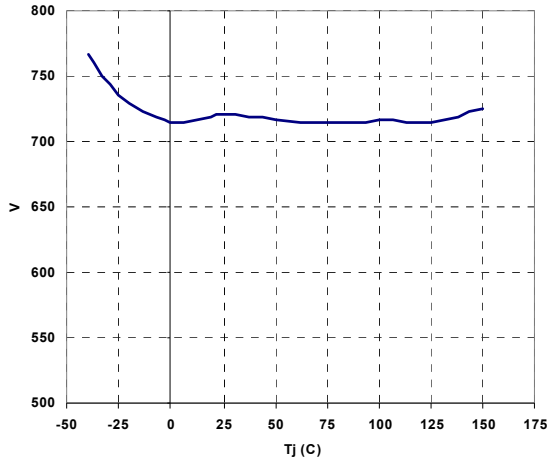


Figure 37. HV breakdown voltage vs. T_J



6 Application information

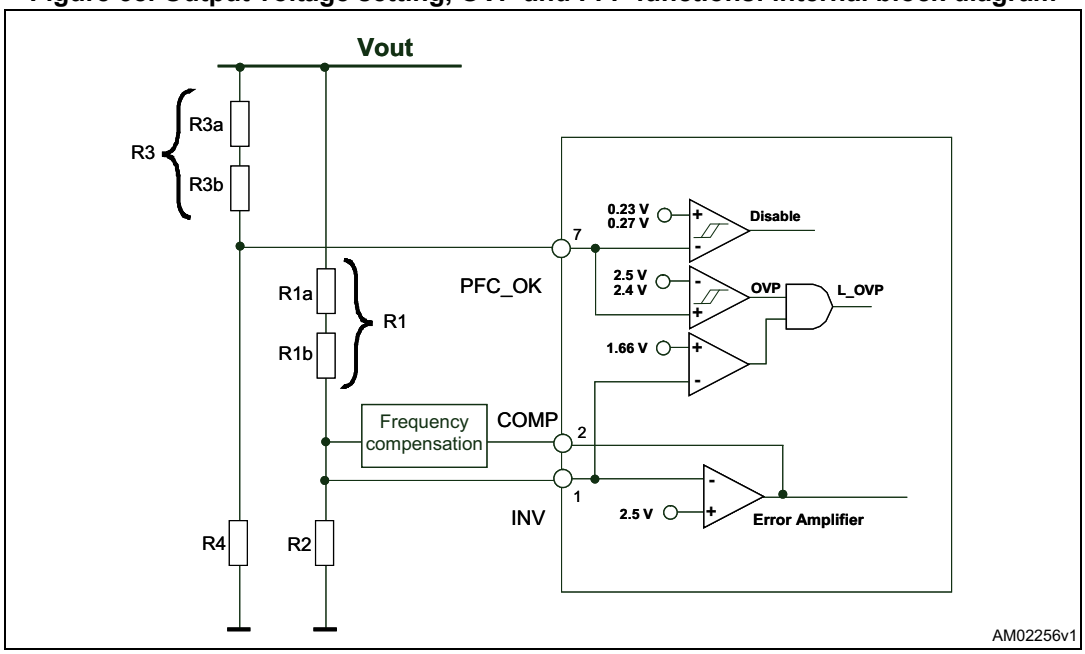
6.1 Overvoltage protection

Normally, the voltage control loop keeps the output voltage Vo of the PFC pre-regulator close to its nominal value, set by the ratio of the resistors R1 and R2 of the output divider. A pin of the device (PFC_OK) has been dedicated to monitor the output voltage with a separate resistor divider (R3 high, R4 low, see *Figure 38*). This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value, usually larger than the maximum Vo that can be expected.

Example: V_O = 400 V, V_{OX} = 434 V. Select: R3 = 8.8 MΩ; then: R4 = 8.8 MΩ ·2.5 / (434 - 2.5) = 51 kΩ.

When this function is triggered, the gate drive activity is immediately stopped until the voltage on the pin PFC_OK drops below 2.4 V. Notice that R1, R2, R3 and R4 can be selected without any constraints. The unique criterion is that both dividers have to sink a current from the output bus which needs to be significantly higher than the bias current of both INV and PFC_OK pins.

Figure 38. Output voltage setting, OVP and FFP functions: internal block diagram



6.2 Feedback failure protection (FFP)

The OVP function above described handles “normal” over voltage conditions, i.e. those resulting from an abrupt load/line change or occurring at start-up. In case the overvoltage is generated by a feedback disconnection, for instance when the upper resistor of the output divider (R1) fails open, comparator detects the voltage at pin INV. If the voltage is lower than 1.66 V and the OVP is active, the FFP is triggered, the gate drive activity is immediately stopped, the device is shut down, its quiescent consumption is reduced below 180 µA and the condition is latched as long as the supply voltage of the IC is above the UVLO threshold. At the same time the pin PWM_LATCH is asserted high. PWM_LATCH is an open source output able to deliver 2.8 V minimum with 0.25 mA load, intended for tripping a latched shutdown function of the PWM controller IC in the cascaded dc-dc converter, so that the entire unit is latched off. To restart the system it is necessary to recycle the input power, so that the Vcc voltage of both the L6563H goes below 6V and that one of the PWM controller goes below its UVLO threshold.

The pin PFC_OK doubles its function as a not-latched IC disable: a voltage below 0.23V shutdown the IC, reducing its consumption below 2 mA. In this case both PWM_STOP and PWM_LATCH keep their high impedance status. To restart the IC simply let the voltage at the pin go above 0.27 V.

Note that these functions offer a complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open or a PFC_OK pin floating results in shutting down the IC and stopping the pre-regulator.

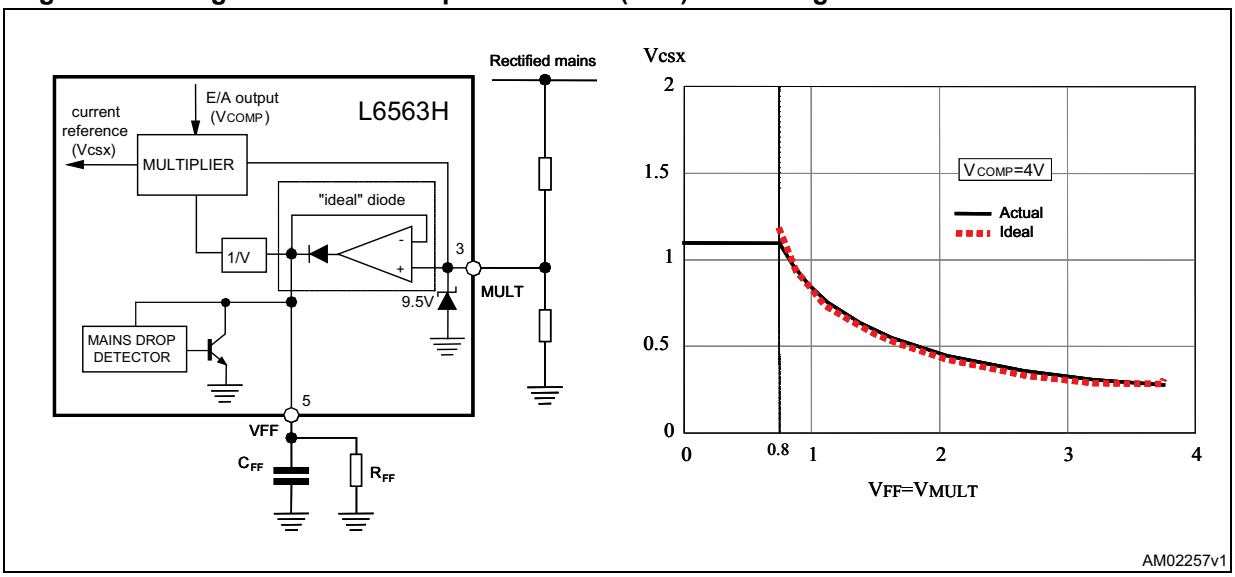
6.3 Voltage feedforward

The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage. So does the crossover frequency fc of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in the design.

For example, setting the gain of the error amplifier to get fc = 20 Hz at 264 Vac means having fc = 4 Hz at 88 Vac, resulting in a sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. But a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

Voltage Feedforward can compensate for the gain variation with the line voltage and allow minimizing all of the above-mentioned issues. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit (1/V2 corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop (see *Figure 39*).

Figure 39. Voltage feedforward: squarer-divider (1/V^2) block diagram and transfer characteristic



In this way a change of the line voltage causes an inversely proportional change of the half sine amplitude at the output of the multiplier (if the line voltage doubles the amplitude of the multiplier output is halved and vice versa) so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain is constant throughout the input voltage range, which improves significantly dynamic behavior at low line and simplifies loop design.

Actually, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small the voltage generated is affected by a considerable amount of ripple at twice the mains frequency that causes distortion of the current reference (resulting in high THD and poor PF); if it is too large there is a considerable delay in setting the right amount of feedforward, resulting in excessive overshoot and undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly a trade-off was required.

The L6563H realizes a NEW voltage feed forward that, with a technique that makes use of just two external parts, strongly minimizes this time constant trade-off issue whichever voltage change occurs on the mains, both surges and drops. A capacitor C_{FF} and a resistor RFF, both connected from the pin VFF (#5) to ground, complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on pin MULT (#3). In this way, in case of sudden line voltage rise, C_{FF} is rapidly charged through the low impedance of the internal diode; in case of line voltage drop, an internal “mains drop” detector enables a low impedance switch which suddenly discharges CFF avoiding long settling time before reaching the new voltage level. The discharge of CFF is stopped as its voltage equals the voltage on pin MULT or if the voltage on pin RUN (in case it is connected to VFF) falls below 0.88V, to prevent the “Brownout protection” function from being improperly activated (see “Power management/housekeeping functions” section).

As a result of the VFF pin functionality, an acceptably low steady-state ripple and low current distortion can be achieved with a limited undershoot or overshoot on the pre-regulator's output.

The twice-mains-frequency ($2 \cdot f_L$) ripple appearing across C_{FF} is triangular with a peak-to-peak amplitude that, with good approximation, is given by:

Equation 1

$$\Delta V_{FF} = \frac{2 V_{MULTpk}}{1 + 4 f_L R_{FF} C_{FF}}$$

where f_L is the line frequency. The amount of 3rd harmonic distortion introduced by this ripple, related to the amplitude of its $2 \cdot f_L$ component, is:

Equation 2

$$D_3\% = \frac{100}{2\pi f_L R_{FF} C_{FF}}$$

Figure 40 shows a diagram that helps choose the time constant $R_{FF} \cdot C_{FF}$ based on the amount of maximum desired 3rd harmonic distortion.

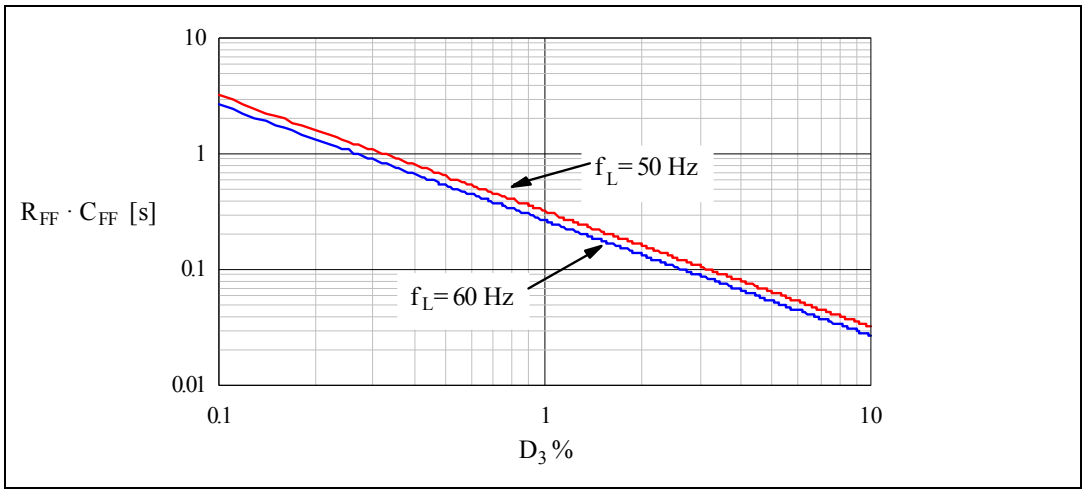
Note that there is a minimum value for the time constant $R_{FF} \cdot C_{FF}$ below which improper activation of the V_{FF} fast discharge may occur. In fact, the twice-mains-frequency ripple across C_{FF} under steady state conditions must be lower than the minimum line drop detection threshold (ΔV_{VFF_min} = 40 mV). Therefore:

Equation 3

$$R_{FF} \cdot C_{FF} > \frac{2 \frac{V_{MULTpk_max}}{\Delta V_{VFF_min}} - 1}{4 f_{L_min}}$$

Always connect R_{FF} and C_{FF} to the pin, the IC will not work properly if the pin is either left floating or connected directly to ground.

Figure 40. $R_{FF} \cdot C_{FF}$ as a function of 3rd harmonic distortion introduced in the input current



6.4 THD optimizer circuit

The L6563H is provided with a special circuit that reduces the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way the THD (total harmonic distortion) of the current is considerably reduced.

A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

To overcome this issue the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This results in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge.

Figure 41 shows the internal block diagram of the THD optimizer circuit.

Figure 41. THD optimizer circuit

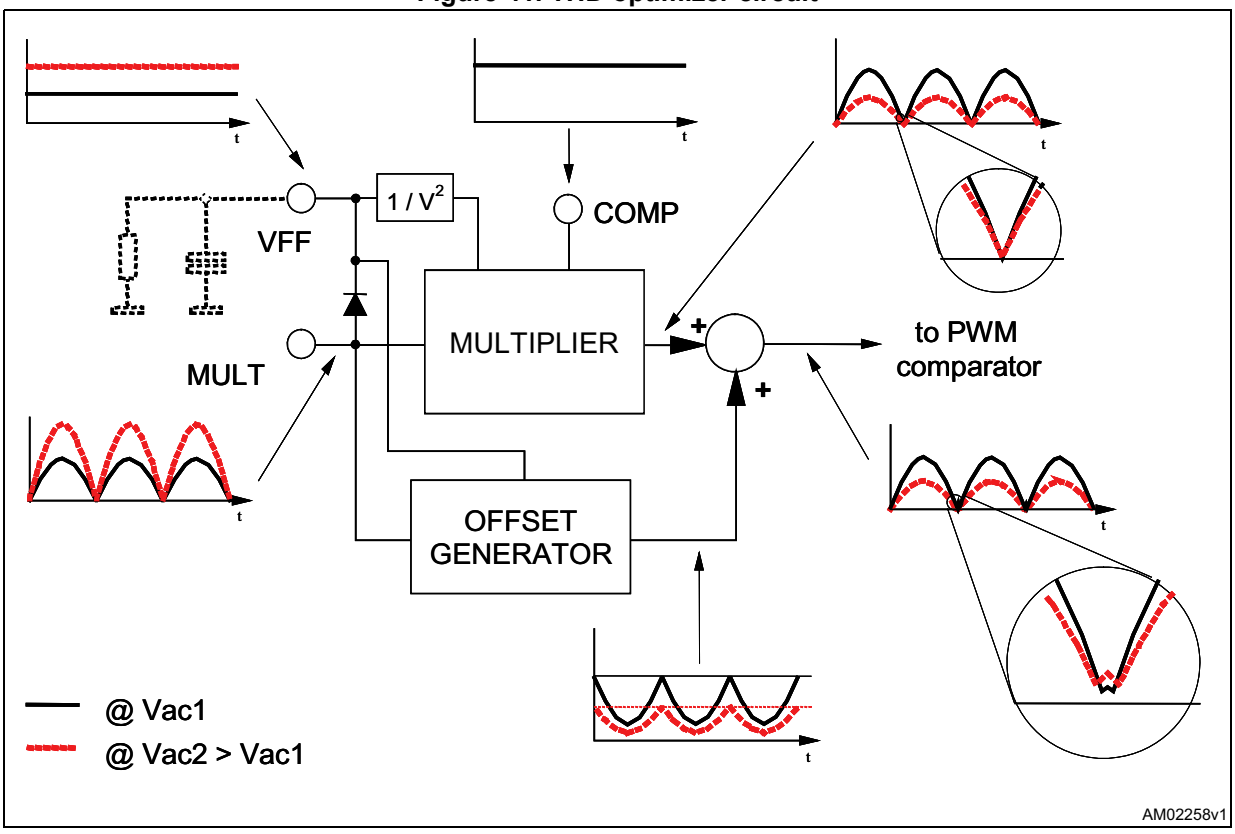
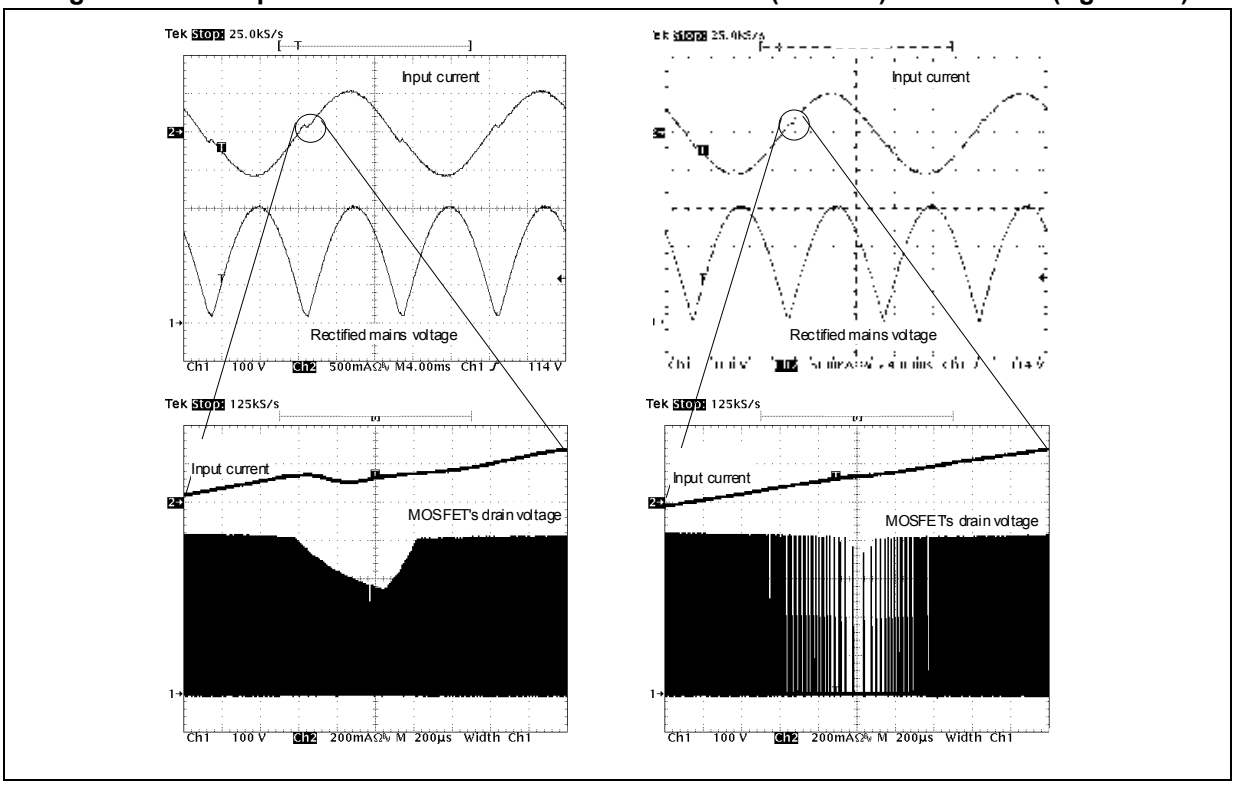


Figure 42. THD optimization: standard TM PFC controller (left side) and L6563H (right side)



Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid. Furthermore the offset is modulated by the voltage on the VFF pin (see “Voltage Feedforward” section) so as to have little offset at low line, where energy transfer at zero crossings is typically quite good, and a larger offset at high line where the energy transfer gets worse.

The effect of the circuit is shown in *Figure 42*, where the key waveforms of a standard TM PFC controller are compared to those of this chip.

To take maximum benefit from the THD optimizer circuit, the high-frequency filter capacitor after the bridge rectifier should be minimized, compatibly with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself - even with an ideal energy transfer by the PFC pre-regulator - thus reducing the effectiveness of the optimizer circuit.

6.5 Tracking boost function

In some applications it may be advantageous to regulate the output voltage of the PFC pre-regulator so that it tracks the RMS input voltage rather than at a fixed value like in conventional boost pre-regulators. This is commonly referred to as “tracking boost” or “follower boost” approach.

With the L6563H this can be realized by connecting a resistor (RT) between the TBO pin and ground. The TBO pin presents a DC level equal to the peak of the MULT pin voltage and is then representative of the mains RMS voltage. The resistor defines a current, equal

to V(TBO)/RT, that is internally 1:1 mirrored and sunk from pin INV (#1) input of the L6563H's error amplifier. In this way, when the mains voltage increases the voltage at TBO pin increases as well and so does the current flowing through the resistor connected between TBO and GND. Then a larger current is sunk by INV pin and the output voltage of the PFC pre-regulator is forced to get higher. Obviously, the output voltage moves in the opposite direction if the input voltage decreases.

To avoid undesired output voltage rise should the mains voltage exceed the maximum specified value, the voltage at the TBO pin is clamped at 3V. By properly selecting the multiplier bias it is possible to set the maximum input voltage above which input-to-output tracking ends and the output voltage becomes constant. If this function is not used, leave the pin open: the device regulates a fixed output voltage.

Starting from the following data:

- Vin_1 = minimum specified input RMS voltage;
- Vin_2 = maximum specified input RMS voltage;
- Vo_1 = regulated output voltage at Vin = Vin_1;
- Vo_2 = regulated output voltage at Vin = Vin_2;
- Vox = absolute maximum limit for the regulated output voltage;

to set the output voltage at the desired values use the following design procedure:

1. Determine the input RMS voltage Vinclamp that produces Vo = Vox:

Equation 4

$$Vin_{clamp} = \frac{Vox - Vo_1}{Vo_2 - Vo_1} \cdot Vin_2 - \frac{Vox - Vo_2}{Vo_2 - Vo_1} \cdot Vin_1$$

and choose a value Vin_x such that $Vin_2 \leq Vinx < Vinclamp$. This results in a limitation of the output voltage range below Vox (it is equal Vox if one chooses $Vin_x = Vin_{clamp}$)

2. Determine the divider ratio of the MULT pin (#3) bias:

Equation 5

$$k = \frac{3}{\sqrt{2} \cdot Vin_x}$$

and check that at minimum mains voltage Vin1 the peak voltage on pin 3 is greater than 0.65 V.

3. Determine R1, the upper resistor of the output divider, for instance 3 MΩ.

4. Calculate the lower resistor R2 of the output divider and the adjustment resistor RT:

Equation 6

$$\begin{cases} R2 = 2.5 \cdot R1 \cdot \dfrac{Vin_2 - Vin_1}{(Vo_1 - 2.5) \cdot Vin_2 - (Vo_2 - 2.5) \cdot Vin_1} \\ R_T = \sqrt{2} \cdot k \cdot R1 \cdot \dfrac{Vin_2 - Vin_1}{Vo_2 - Vo_1} \end{cases}$$

5. Check that the maximum current sourced by the TBO pin (#6) does not exceed the maximum specified (0.2 mA):

Equation 7

$$I_{TBOmax} = \frac{3}{R_T} \leq 0.2 \cdot 10^{-3}$$

Figure 43 shows the internal block diagram of the tracking boost function.

Figure 43. Tracking boost block

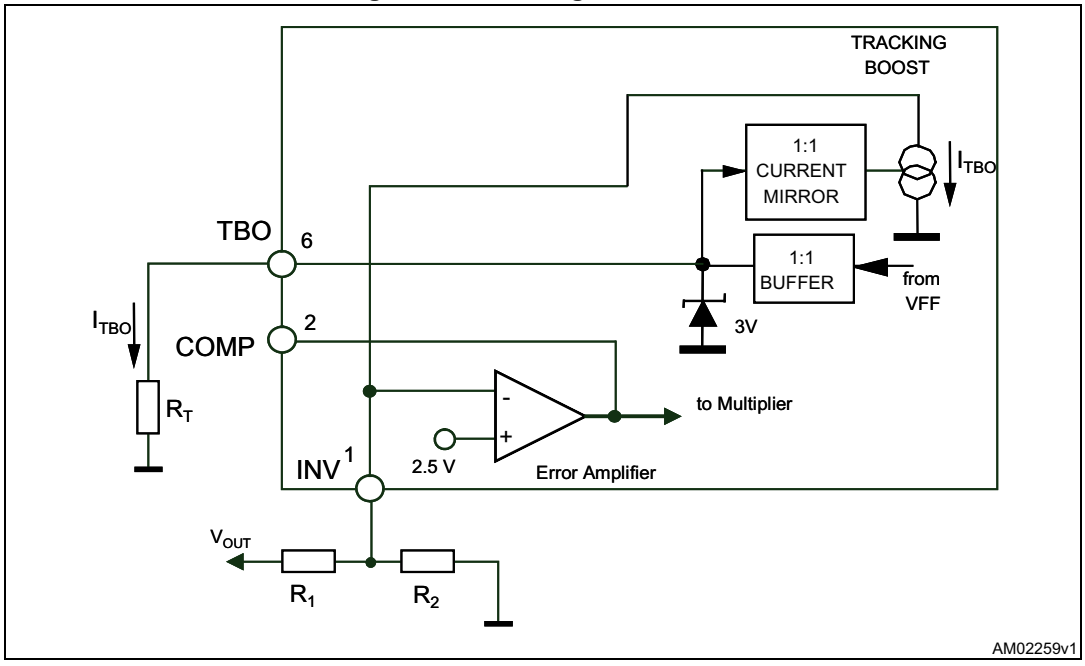
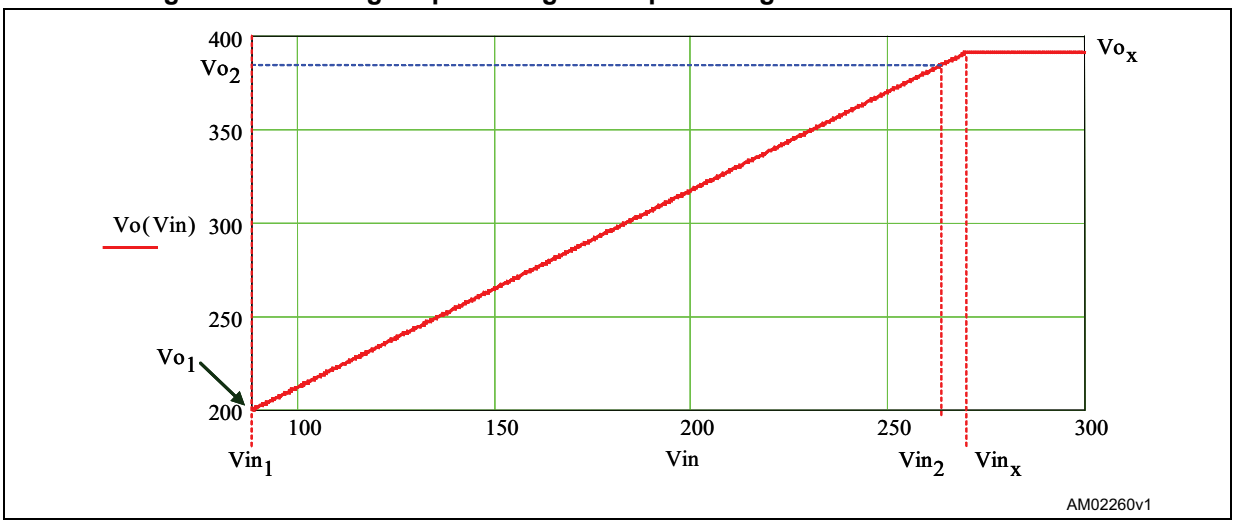


Figure 44. Tracking output voltage vs. input voltage characteristic with TBO



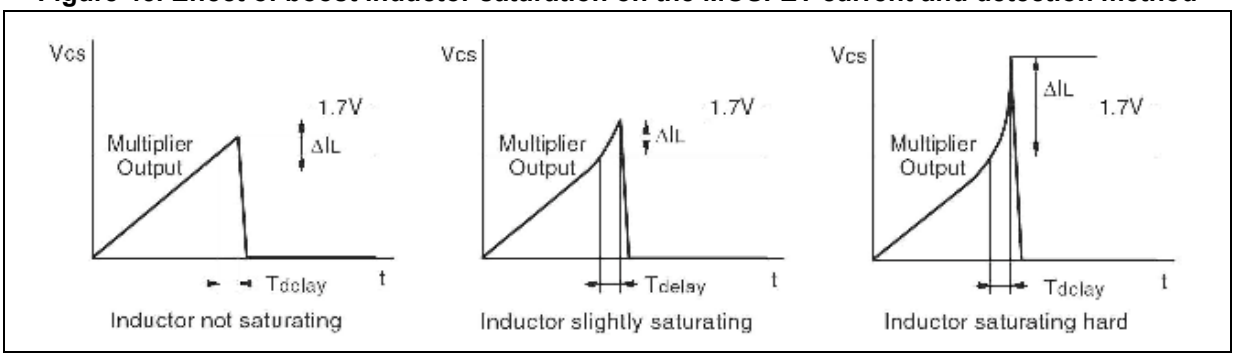
6.6 Inductor saturation detection

Boost inductor's hard saturation may be a fatal event for a PFC pre-regulator: the current up-slope becomes so large (50-100 times steeper, see *Figure 45*) that during the current sense propagation delay the current may reach abnormally high values. The voltage drop caused by this abnormal current on the sense resistor reduces the gate-to-source voltage, so that the MOSFET may work in the active region and dissipate a huge amount of power, which leads to a catastrophic failure after few switching cycles.

However, in some applications such as ac-dc adapters, where the PFC pre-regulator is turned off at light load for energy saving reasons, even a well-designed boost inductor may occasionally slightly saturate when the PFC stage is restarted because of a larger load demand. This happens when the restart occurs at an unfavorable line voltage phase, i.e. when the output voltage is significantly below the rectified peak voltage. As a result, in the boost inductor the inrush current coming from the bridge rectifier adds up to the switched current and, furthermore, there is little or no voltage available for demagnetization.

To cope with a saturated inductor, the L6563H is provided with a second comparator on the current sense pin (CS, pin 4) that stops the IC if the voltage, normally limited within 1.1 V, exceeds 1.7 V. After that, the IC attempts to restart by the internal starter circuitry; the starter repetition time is twice the nominal value to guarantee lower stress for the inductor and boost diode. Hence, the system safety is considerably increased.

Figure 45. Effect of boost inductor saturation on the MOSFET current and detection method



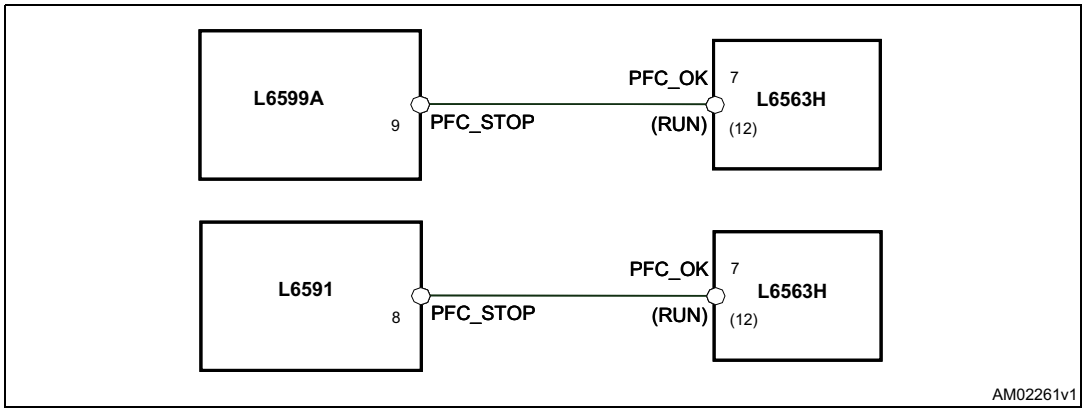
6.7 Power management/housekeeping functions

A special feature of this IC is that it facilitates the implementation of the “housekeeping” circuitry needed to co-ordinate the operation of the PFC stage to that of the cascaded DC-DC converter. The functions realized by the housekeeping circuitry ensure that transient conditions like power-up or power down sequencing or failures of either power stage be properly handled.

This device provides some pins to do that. One communication line between the IC and the PWM controller of the cascaded dc-dc converter is the pin PWM_LATCH (*Figure 47*b), which is normally open (high impedance) when the PFC works properly, and goes high if it loses control of the output voltage (because of a feedback loop disconnection) with the aim of latching off the PWM controller of the cascaded dc-dc converter as well (see “Feedback failure protection” section for more details).

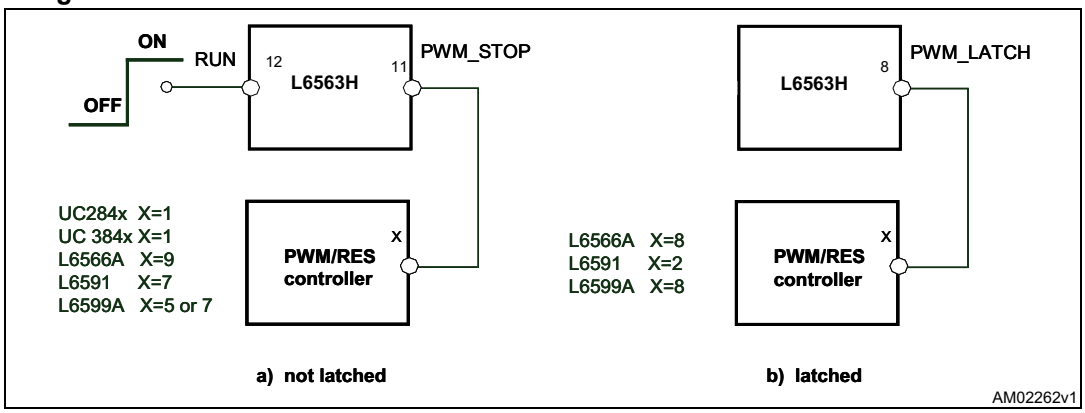
A second communication line can be established via the disable function included in the PFC_OK pin (see “Feedback failure protection” section for more details). Typically this line is used to allow the PWM controller of the cascaded dc-dc converter to drive in burst mode operation the L6563H in case of light load and to minimize the no-load input consumption. Interface circuits like those are shown in *Figure 46*.

Figure 46. Interface circuits that let dc-dc converter's controller IC drive L6563H in burst mode



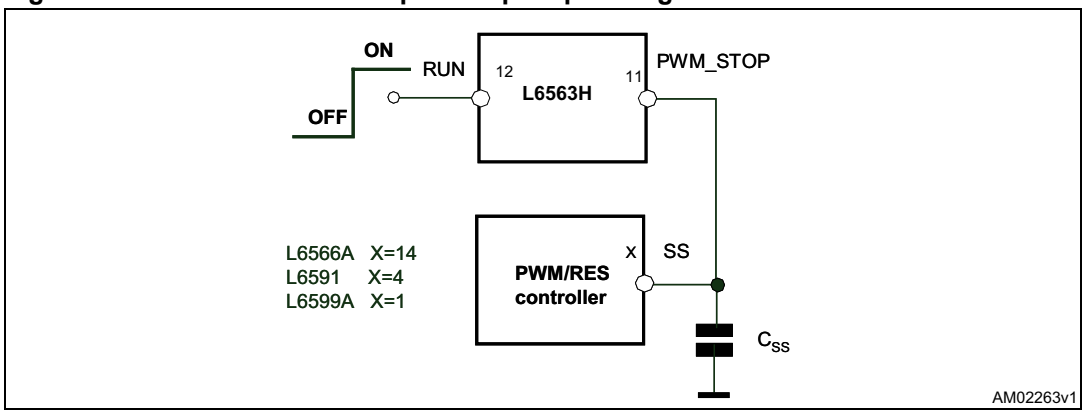
The third communication line is the pin PWM_STOP (#11), which works in conjunction with the pin RUN (#12). The purpose of the PWM_STOP pin is to inhibit the PWM activity of both the PFC stage and the cascaded dc-dc converter. The pin is an open collector, normally open, that goes low if the device is disabled by a voltage lower than 0.8 V on the RUN pin. The pin goes again open if the voltage on pin RUN exceeds 0.88 V. It is important to point out that this function works correctly in systems where the PFC stage is the master and the cascaded dc-dc converter is the slave or, in other words, where the PFC stage starts first, powers both controllers and enables/disables the operation of the dc-dc stage. The pin RUN can be used to start and stop the main converter. In the simplest case, to enable/disable the PWM controller the pin PWM_STOP can be connected to the output of the error amplifier (*Figure 47*a).

Figure 47. Interface circuits that let the L6563H switch on or off a PWM controller



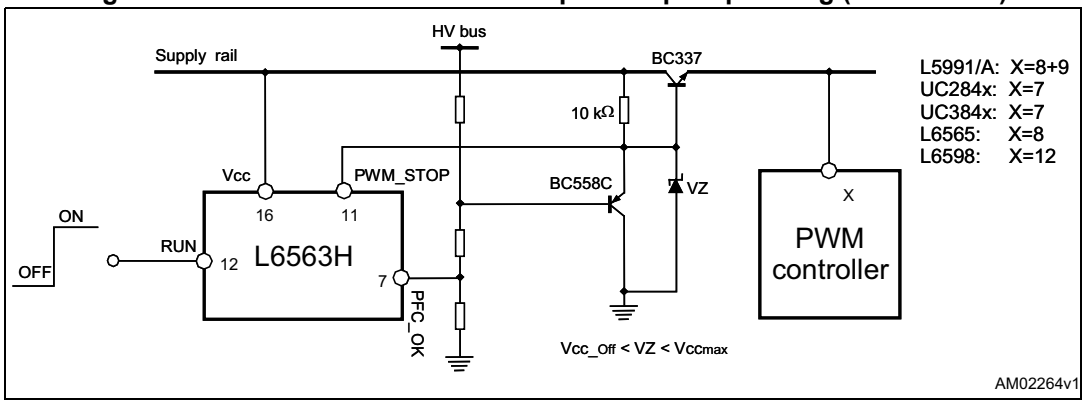
If the chip is provided with a soft-start pin, it is possible to delay the start-up of the dc-dc stage with respect to that of the PFC stage, which is often desired, as described in *Figure 48*. An underlying assumption in order for that to work properly is that the UVLO thresholds of the PWM controller are certainly higher than those of the L6563H.

Figure 48. Interface circuits for power up sequencing when dc-dc has the SS function



If this is not the case or it is not possible to achieve a start-up delay long enough (because this prevents the dc-dc stage from starting up correctly) or, simply, the PWM controller is devoid of soft start, the arrangement of *Figure 49* lets the dc-dc converter start-up when the voltage generated by the PFC stage reaches a preset value. The technique relies on the UVLO thresholds of the PWM controller.

Figure 49. Interface circuits for actual power-up sequencing (master PFC)



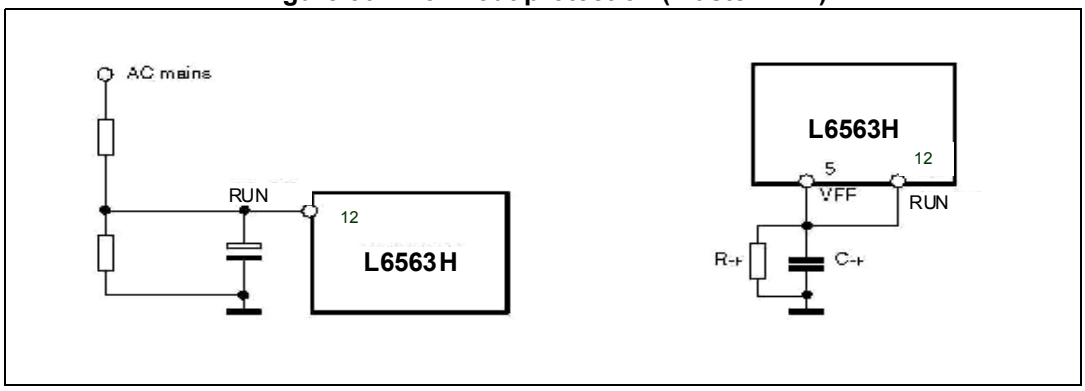
Another possible use of the RUN and PWM_STOP pins (again, in systems where the PFC stage is the master) is the brownout protection, thanks to the hysteresis provided.

The brownout protection is basically a not-latched device shutdown function that is activated when a condition of mains undervoltage is detected. This condition may cause overheating of the primary power section due to an excess of RMS current. Brownout can also cause the PFC pre-regulator to work open loop and this could be dangerous to the PFC stage itself and the downstream converter, should the input voltage return abruptly to its rated value. Another problem is the spurious restarts that may occur during converter power down and that cause the output voltage of the converter not to decay to zero monotonically. For these reasons it is usually preferable to shutdown the unit in case of brownout.

IC shutdown upon brownout can be easily realized as shown in *Figure 50*. The scheme on the left is of general use, that one on the right can be used if the bias levels of the multiplier and the R_{FF}·C_{FF} time constant are compatible with the specified brownout level and with the specified holdup time respectively. In this latest case, an additional resistor voltage divider and one capacitor are not needed.

In table 1 it is possible to find a summary of all of the above mentioned working conditions that cause the device to stop operating.

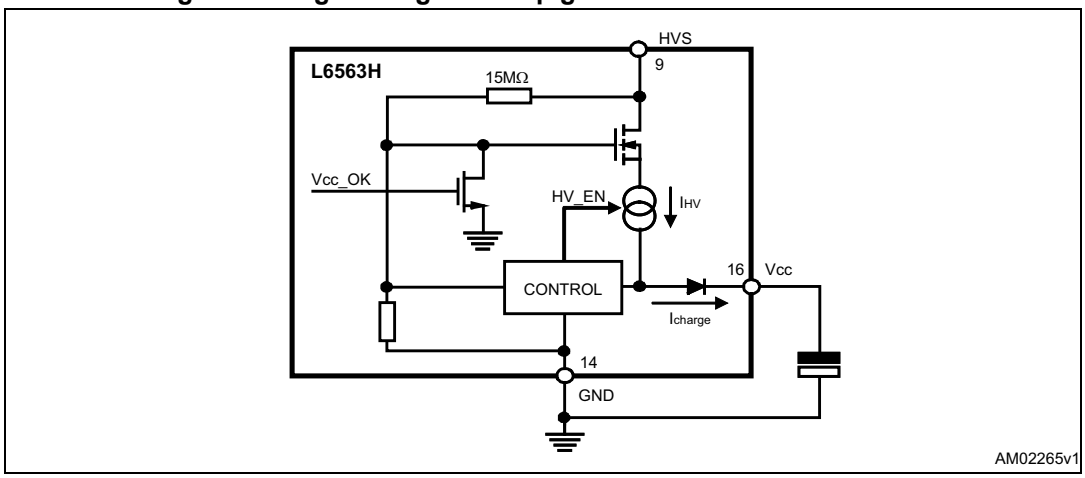
Figure 50. Brownout protection (master PFC)



6.8 High voltage start-up generator

Figure 51 shows the internal schematic of the high voltage start-up generator (HV generator). It is made up of a high voltage N-channel FET, whose gate is biased by a 15 MΩ resistor, with a temperature-compensated current generator connected to its source.

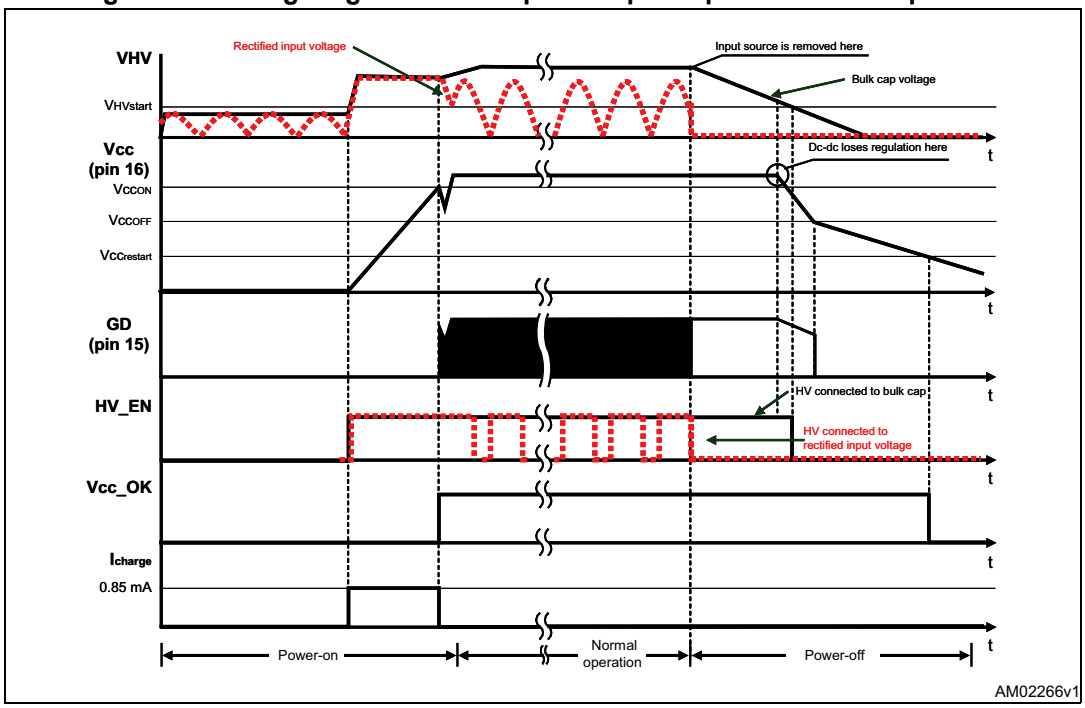
Figure 51. High voltage start-up generator: internal schematic



The HV generator is physically located on a separate chip, made with BCD off-line technology able to withstand 700 V, controlled by a low-voltage chip, where all of the control functions reside.

With reference to the timing diagram of *Figure 52*, when power is first applied to the converter the voltage on the bulk capacitor (Vin) builds up and, at about 80 V, the HV generator is enabled to operate (HV_EN is pulled high) so that it draws about 1 mA. This current, minus the device's consumption, charges the bypass capacitor connected from pin Vcc (16) to ground and makes its voltage rise almost linearly.

Figure 52. Timing diagram: normal power-up and power-down sequences



As the Vcc voltage reaches the start-up threshold (12 V typ.) the low-voltage chip starts operating and the HV generator is cut off by the Vcc_OK signal asserted high. The device is powered by the energy stored in the Vcc capacitor until the self-supply circuit (we assume

that it is made with an auxiliary winding in the transformer of the cascaded DC-DC converter and a steering diode) develops a voltage high enough to sustain the operation. The residual consumption of this circuit is just the one on the 15 MΩ resistor (10 mW at 400 Vdc), typically 50-70 times lower, under the same conditions, as compared to a standard start-up circuit made with external dropping resistors.

At converter power-down the dc-dc converter loses regulation as soon as the input voltage is so low that either peak current or maximum duty cycle limitation is tripped. Vcc then drops and stops IC activity as it falls below the UVLO threshold (9.5 V typ.). The Vcc_OK signal is de-asserted as the Vcc voltage goes below a threshold VCCrestart located at about 6 V. The HV generator can now restart. However, if Vin < VHVstart, HV_EN is de-asserted too and the HV generator is disabled. This prevents converter's restart attempts and ensures monotonic output voltage decay at power-down in systems where brownout protection (see the relevant section) is not used.

If the device detects a fault due to feedback failure the pin PWM_LATCH is asserted high (see “Feedback failure protection” section for more details) and, in order to maintain alive this signal to be provided to the DC-DC converter, the internal VCCrestart is brought up to over the VccOff (turn-off threshold). As a result, shown in *Figure 53*, the voltage at pin Vcc, oscillates between its turn-on and turn-off thresholds until the HV bus is recycled and drops below the start up threshold of the HV generator.

The high voltage start-up circuitry is capable to guarantee a safe behavior in case of short-circuit present on the dc-dc output when the Vcc of both controllers are generated by the same auxiliary winding. The *Figure 54* shows how the PFC manages the Vcc cycling and the associated power transfer. At short-circuit the auxiliary circuit is no longer able to sustain the Vcc which start dropping; reaching its VccOFF threshold the IC stops switching, reduces consumption and drops more until the Vccrestart threshold is tripped. Now, the high voltage start-up generator restarts and when the Vcc crosses again its turn on threshold the IC starts switching. In this manner the power is transferred from mains to PFC output only during a short time for each Trep cycle.

Figure 53. High voltage start-up behavior during latch-off protection

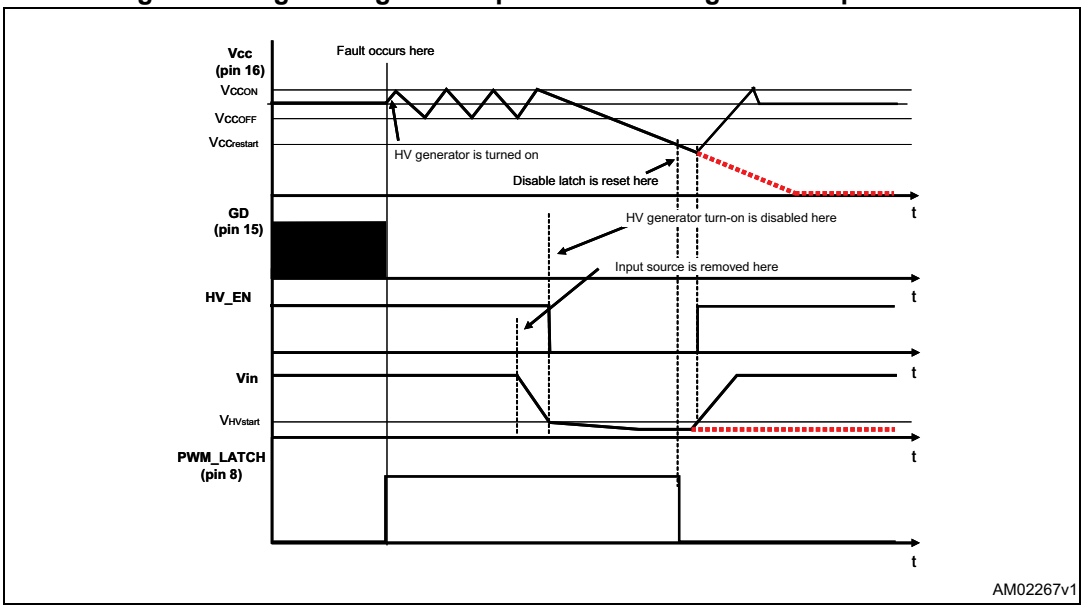


Figure 54. High voltage start-up managing the dc-dc output short-circuit

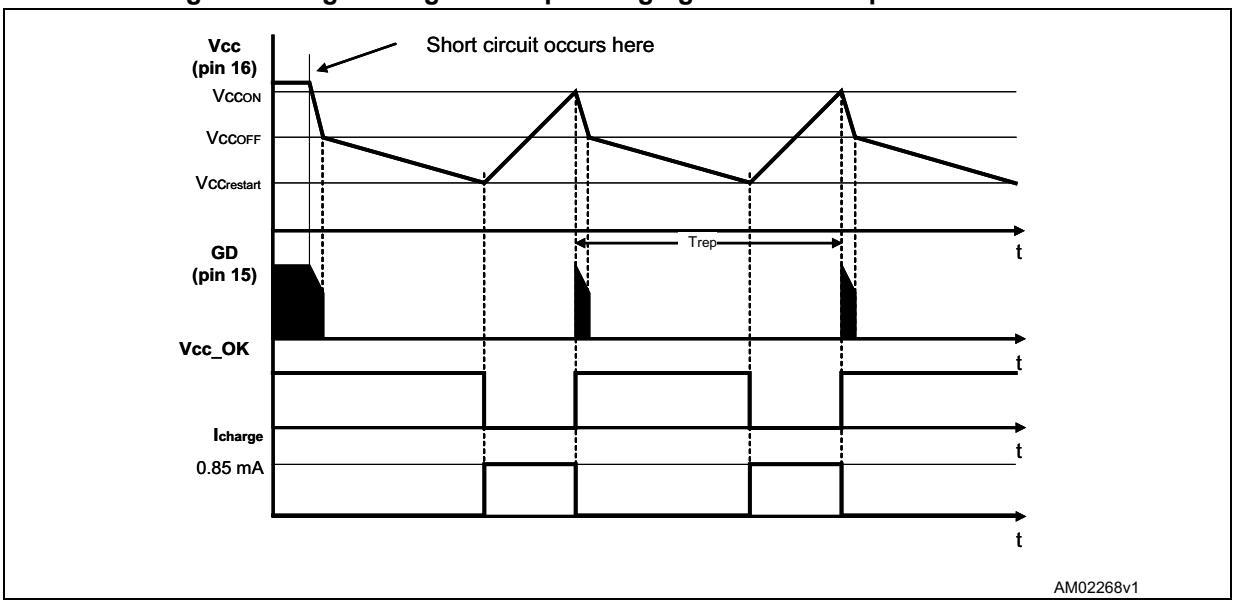


Table 5. Summary of L6563H idle states

Condition	Caused or revealed bey	IC behavior	Restart condition	Typical IC consumption	PWM_LATCH Status	PWM_STOP Status
UVLO	Vcc < Vcc_{Off}	Disabled	Vcc > Vcc_{On}	90 µA	Off	High
Feedback disconnected	PFC_OK > $V_{PFC_OK_S}$ AND INV < 1.66V	Latched	Vcc < $Vcc_{restart}$ then Vcc > Vcc_{On}	180 µA	High	High
Standby	PFC_OK < $V_{PFC_OK_D}$	Stop switching	PFC_OK > $V_{PFC_OK_E}$	1.5 mA	Off	High
AC brownout	RUN < V_{DIS}		RUN > V_{EN}	1.5 mA	Off	Low
OVP	PFC_OK > $V_{PFC_OK_S}$		PFC_OK < $V_{PFC_OK_R}$	2.2 mA	Off	High
Low consumption	COMP < 2.4V	Burst mode	COMP > 2.4V	2.2 mA	Off	High
Saturated boost inductor	Vcs > V_{CS_th}	Doubled Tstart	Auto restart	2.2 mA	Off	High

7 Application examples and ideas

Figure 55. Demonstration board EVL6563H-100W, wide-range mains: electrical schematic

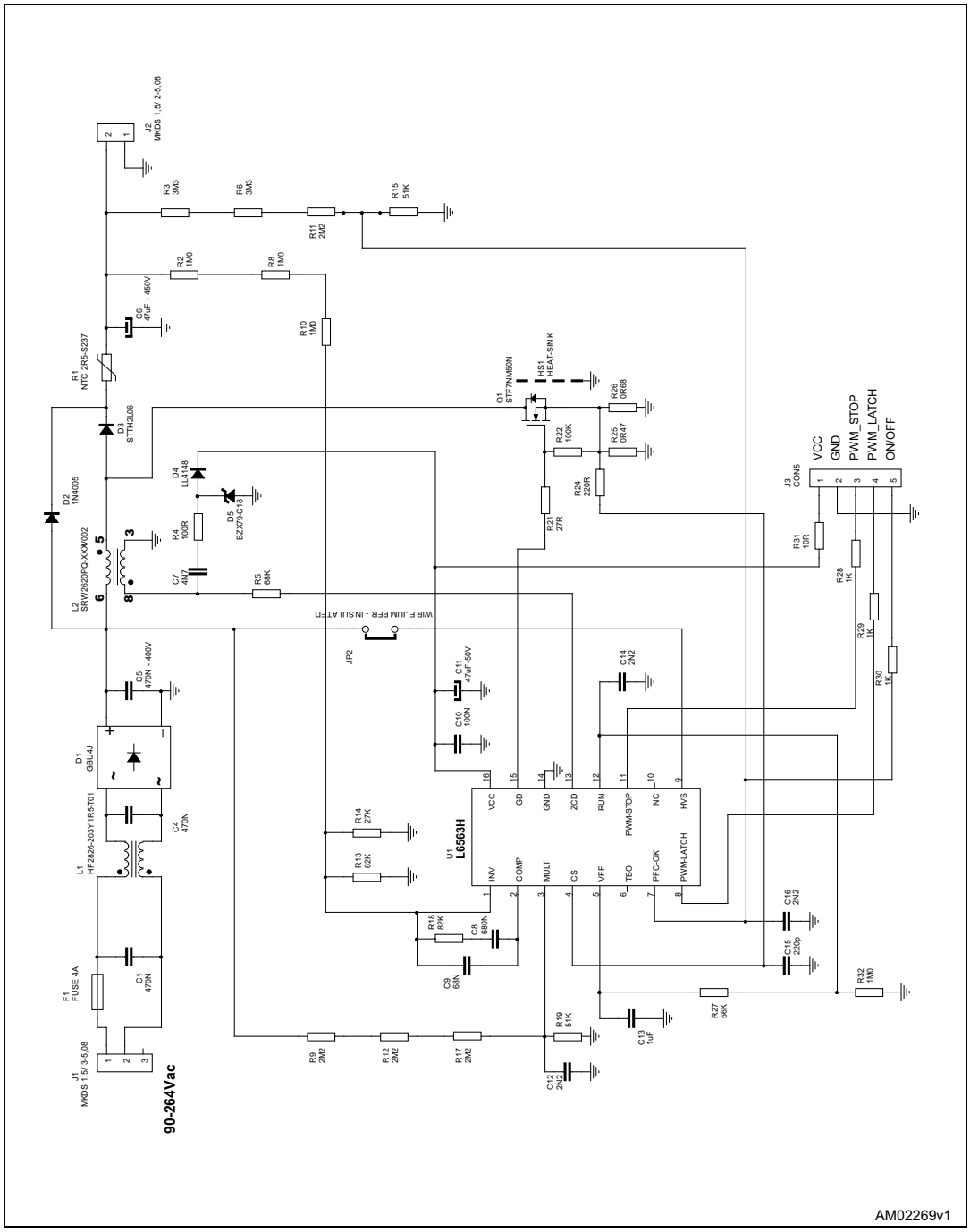
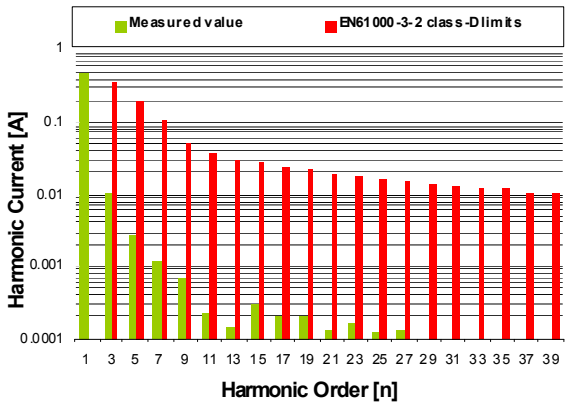


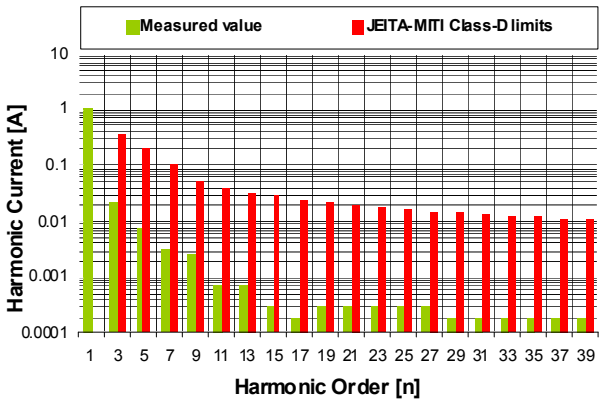
Figure 56. L6563H 100 W TM PFC evaluation board: compliance to EN61000-3-2 standard



Vin = 230 Vac - 50 Hz, Pout = 100 W

THD = 7.58%, PF = 0.979

Figure 57. L6563H 100 W TM PFC evaluation board: compliance to JEITA-MITI standard



Vin = 100 Vac - 50 Hz, Pout = 100 W

THD = 2.5%, PF = 0.997

Figure 58. L6563H 100 W TM PFC evaluation board: input current waveform at 230-50 Hz - 100 W load

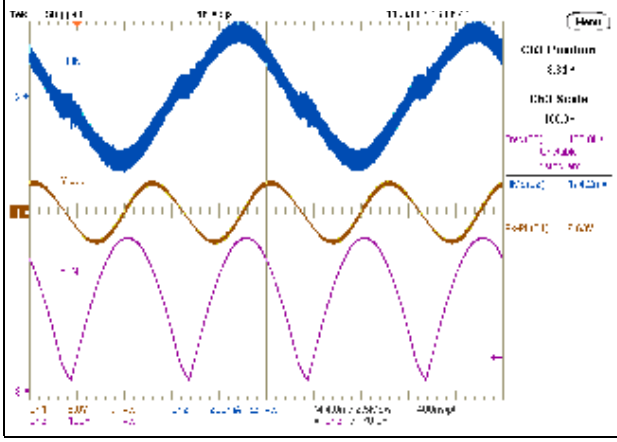


Figure 59. L6563H 100W TM PFC evaluation board: input current waveform at 100 V-50 Hz - 100 W load

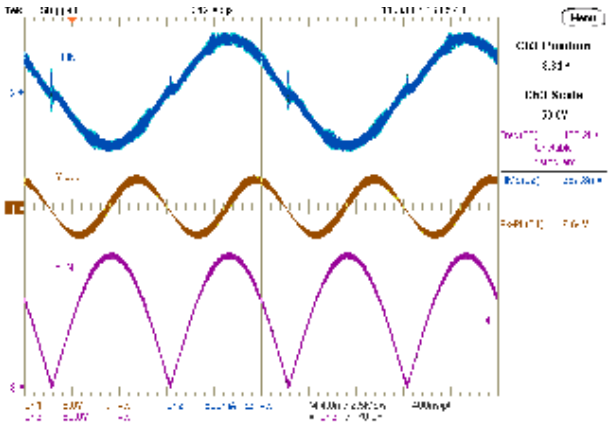


Figure 60. 90 W adapter with L6563H, L6599A, SRK2000A demonstration board: electrical schematic

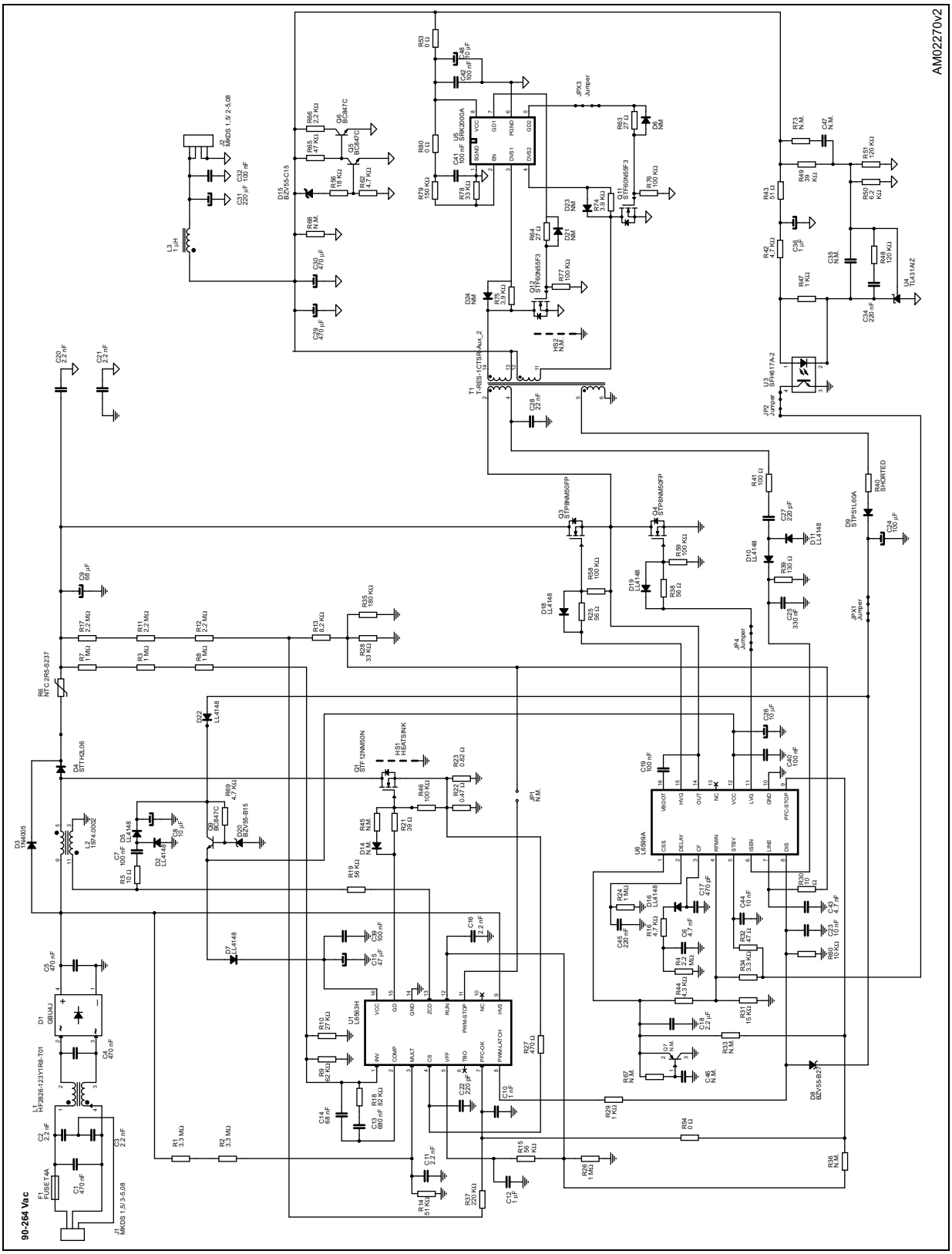


Figure 61. 150 W - 12 V adapter with L6563H, L6599A, SRK2000A: electrical schematic

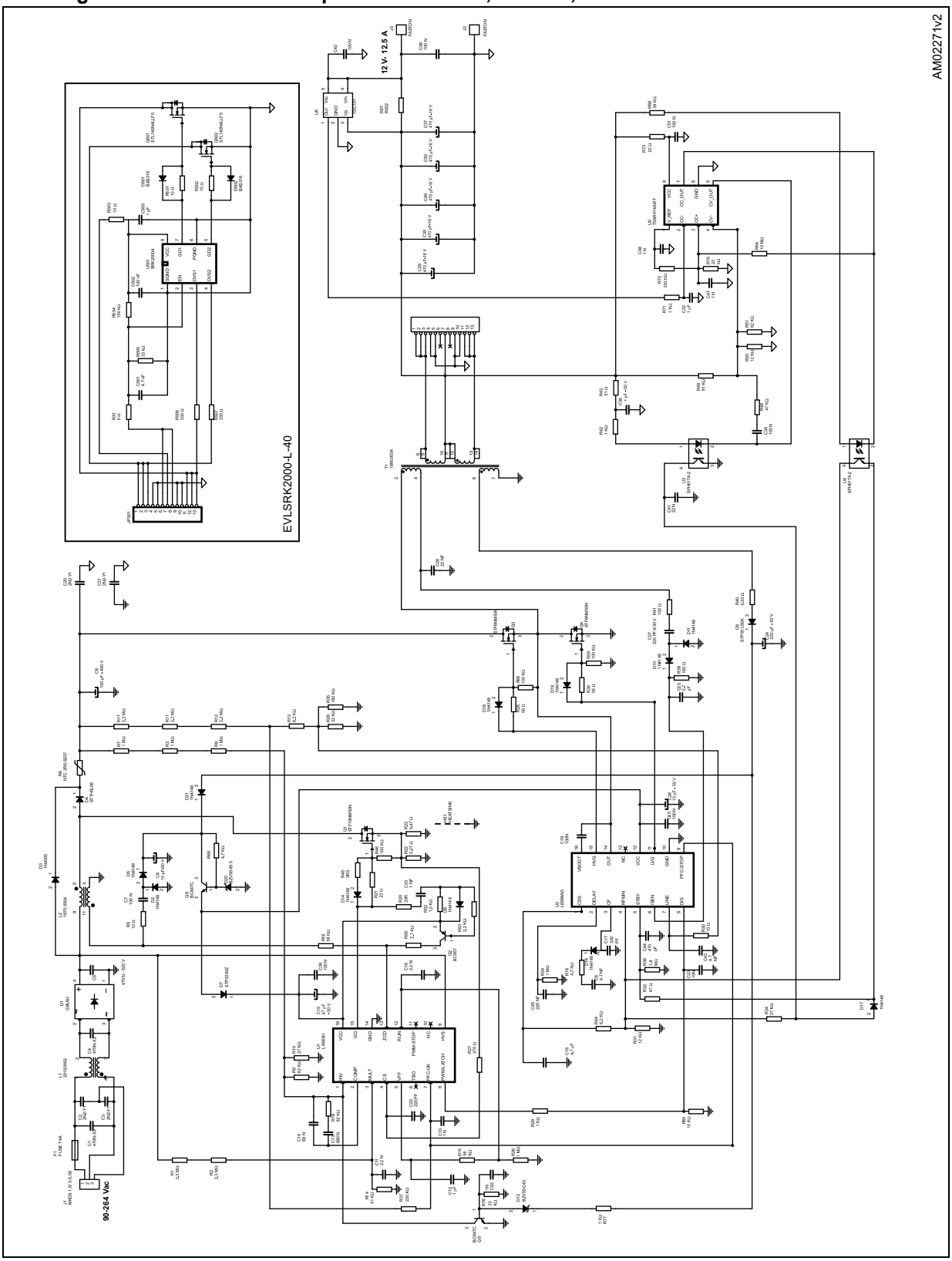


Figure 62. EVL6563H -250 W TM PFC demonstration board: electrical schematic

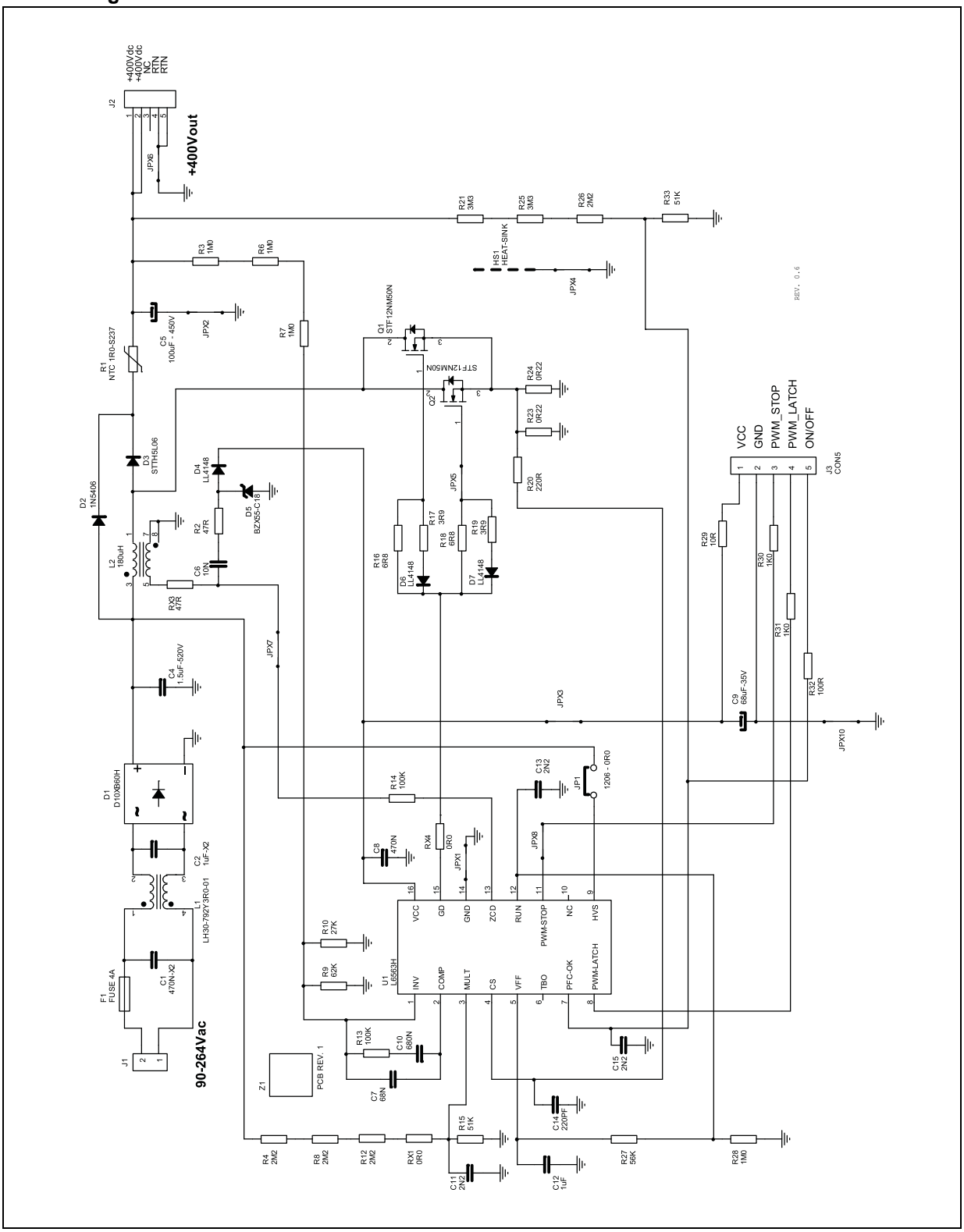
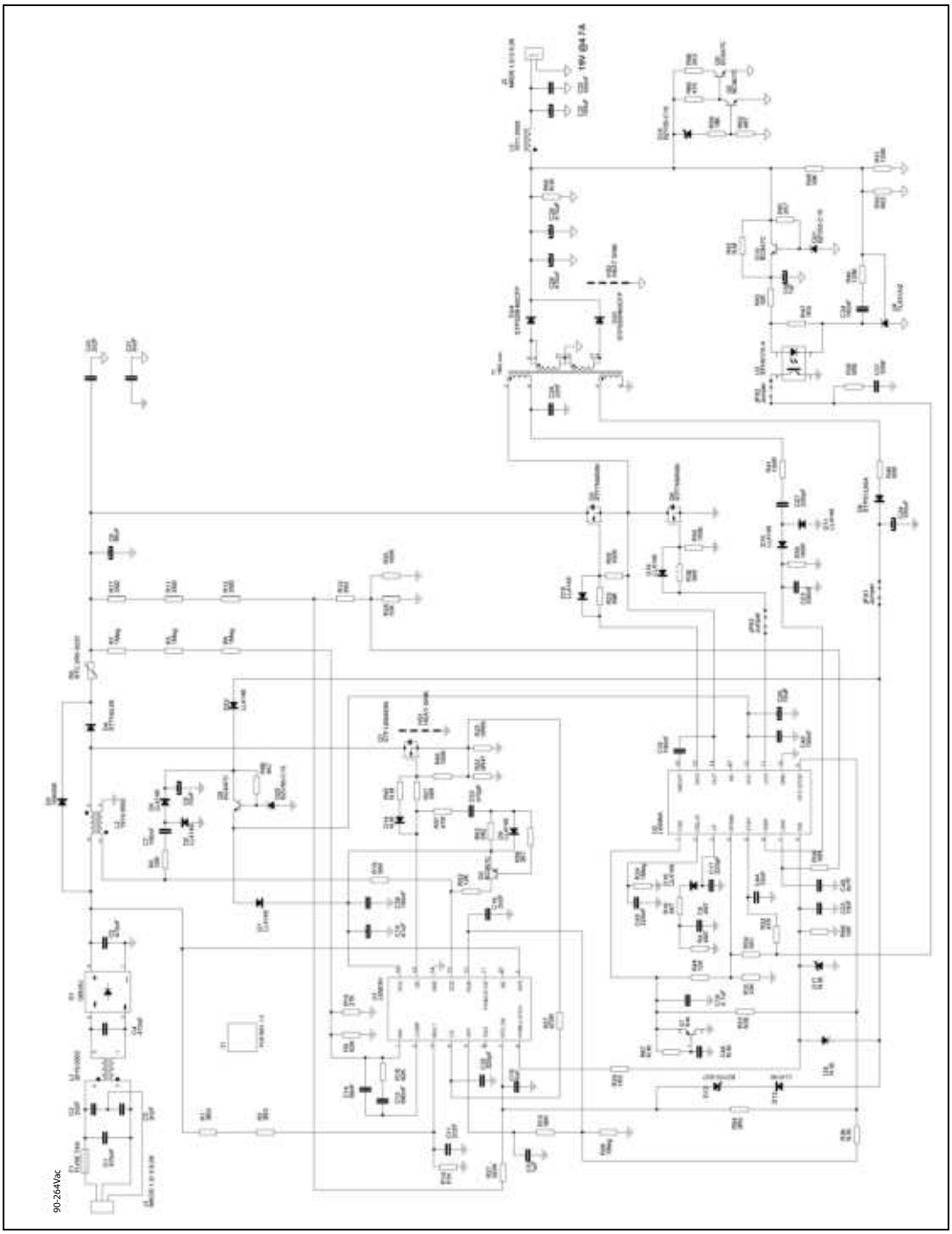


Figure 63. EVL6599A-90WADP 90 W adapter demonstration board: electrical schematic



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 SO16 package information

Figure 64. SO16 package outline

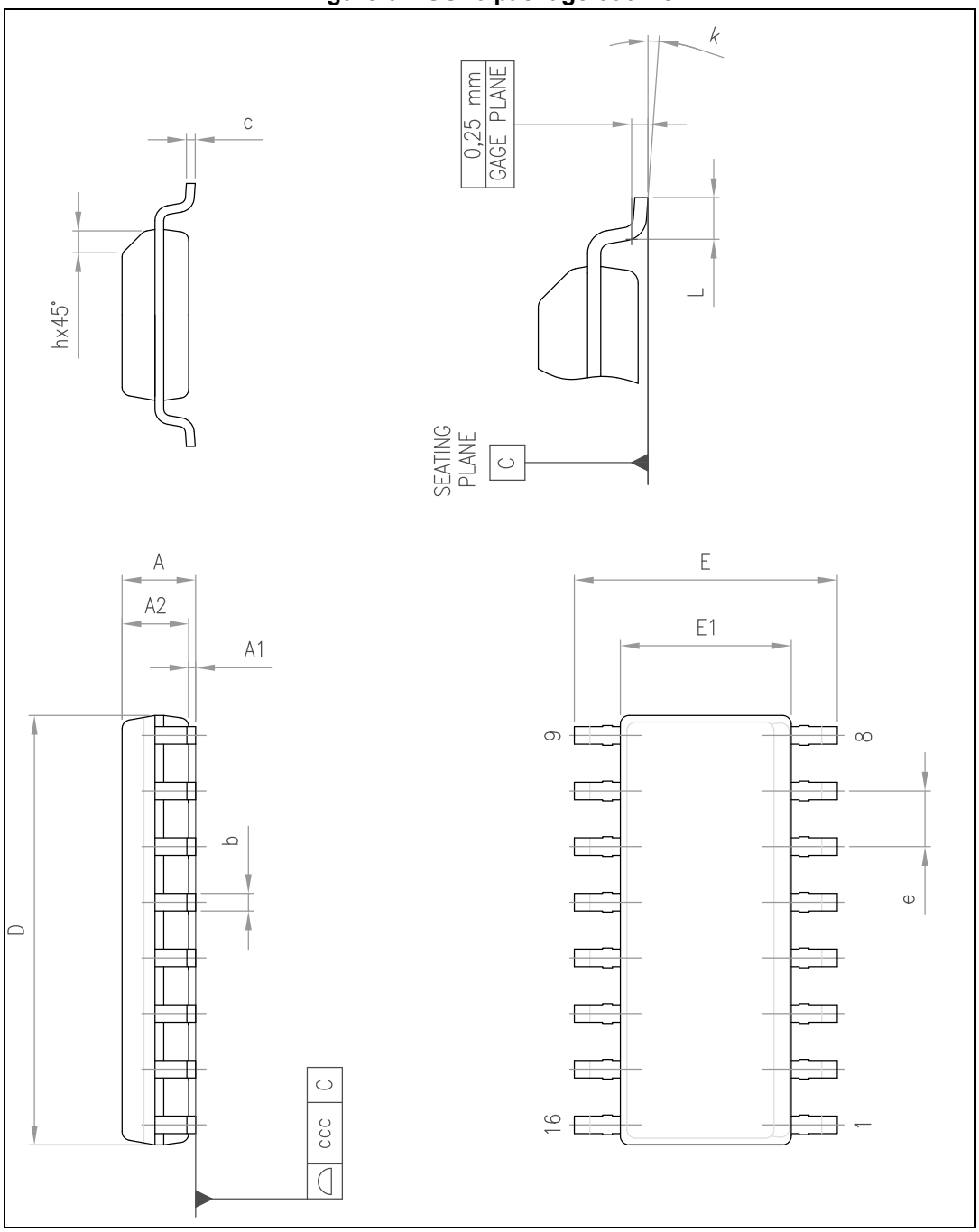


Table 6. SO16 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.1	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.17	-	0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e	-	1.27	-
h	0.25	-	0.5
L	0.4	-	1.27
k	0	-	8
ccc	-	-	0.1

9 Ordering codes

Table 7. Ordering information

Order codes	Package	Packing
L6563H	SO16	Tube
L6563HTR		Tape and reel

10 Revision history

Table 8. Document revision history

Date	Revision	Changes
22-Jul-2009	1	Initial release.
01-Feb-2010	2	Updated *Table 4 on page 11*
21-Dec-2010	3	Updated *Figure 1 on page 1*, *Figure 24 on page 20*, *Table 3 on page 8*, *Table 4 on page 11*, *Table 5 on page 34* and *Section 6.2 on page 25* and *Table 5 on page 38.*
07-Jun-2017	4	Updated *Figure 60 on page 41* and *Figure 61 on page 42* (updated titles and replaced figures by new ones). Minor modifications throughout document.

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