LCDP1521S

Dual line programmable transient voltage suppressor for SLIC protection

Datasheet - production data



SO-8

Features

- Dual line programmable transient voltage suppressor with separated gates
- Wide negative firing voltage range: V_{Gn} = -175 V max.
- Low dynamic switching voltages: V_{FP} and V_{DGL}
- Low gate triggering current: I_{GT} = 5 mA max
- Peak pulse current: I_{PP} = 40 A (5/310 µs)
- Holding current: I_H = 150 mA min.

Benefits

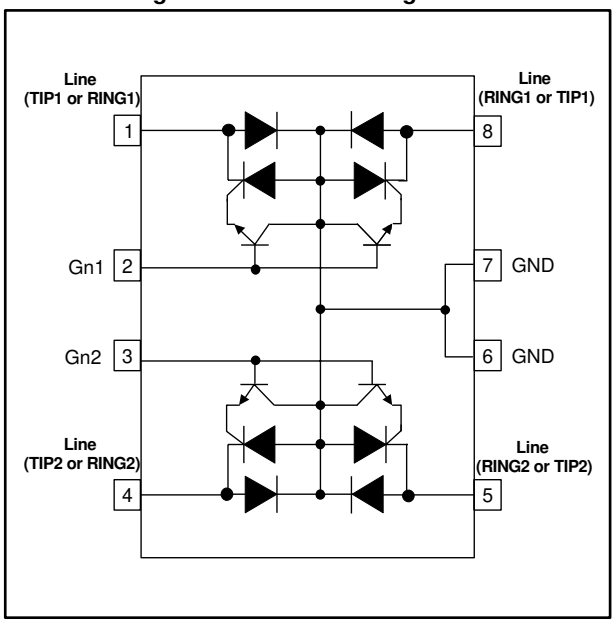
- A Trisil™ is not subject to ageing and provides a fail safe mode in short circuit for a better protection.
- Trisils are used to help equipment to meet various standards such as UL1950, IEC 60950 / CSA C22.2, UL1459 and TIA-968-A (formerly FCC part 68).
- Trisils have UL94 V0 resin approved (Trisils are UL497B approved - file: E136224).

Description

This device has been especially designed to protect 2 new high voltage, as well as classical SLICs, against transient overvoltages.

Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to -V_{BAT} through the gate. Separated gates allow the SLICs to be supplied by two different voltages.

Figure 1: Functional diagram



This is information on a product in full production.

1 Characteristics

Table 1: Standards compliance

Standard	Peak surge voltage (V)	Voltage waveform	Required peak current (A)	Current waveform	Minimum serial resistor to meet standard (Ω)
GR-1089 Core First level	2500 1000	2/10 µs 10/1000 µs	500 100	2/10 µs 10/1000 µs	20 30
GR-1089 Core Second level	5000	2/10 µs	500	2/10 µs	40
GR-1089 Core Intra-building	1500	2/10 µs	100	2/10 µs	0
ITU-T-K20/K21	6000 1500	10/700 µs	150 37.5	5/310 µs	110 0
ITU-T-K20 (IEC 61000-4-2)	8000 15000	1/60 ns	ESD contact discharge ESD air discharge		0 0
IEC 61000-4-5	4000 4000	10/700 µs 1.2/50 µs	100 100	5/310 µs 8/20 µs	60 5
TIA-968-A, lightning surge type A	1500 800	10/160 µs 10/560 µs	100 200	10/160 µs 10/560 µs	26 19
TIA-968-A, lightning surge type B	1000	9/720 µs	25	5/320 µs	0

Table 2: Thermal resistances

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to ambient	170	°C/W

Table 3: Absolute ratings ((0 °C < T_j < 70 °C, unless otherwise specified))

Symbol	Parameter			Value	Unit
I_{pp}	Peak pulse current(1)	Telcordia GR-1089-CORE Issue 6, May 2011, section 4	10/1000 µs	25	A
		TIA-968-A, lightning surge type A	10/560 µs	30	
		ITU-T K20/21/44/45, (10/700 µs open circuit voltage waveshape)	5/310 µs	40	
		TIA-968-A, lightning surge type A	10/160 µs	45	
		IEC 61000-4-5, (1.2/50 µs open circuit waveshape) with 10 Ω	2/40 µs	85	
		ITU-T K20/21/44/45, (1.2/50 µs open circuit voltage waveshape)	8/20 µs	90	
		Telcordia GR-1089-CORE Issue 6, (2/10 µs open circuit waveshape)	2/10 µs	100	
I_{TSM}	Non repetitive surge peak on-state current (50 Hz sinusoidal)(1)		t = 0.2 s t = 1 s t = 2 s t = 15 mn	5 3.5 3 1.3	A
V_{GN}	Negative battery voltage range		-40 °C < T_{amb} < +85 °C	-175	V
T_{stg}	Storage junction temperature range			-55 to + 150	°C
T_j	Maximum operating junction temperature				
T_L	Maximum temperature for soldering during 10 s			260	°C

Notes:

(1)The rated current values may be applied either to the Ring to GND or to the Tip to GND terminal pairs. Additionally, the four terminal pairs may have their rated current values applied simultaneously (in this case the GND terminal current will be four times the rated current value of an individual terminal pair)

Figure 2: Electrical characteristics (definitions)

Symbol	Parameter
I_{GT}	Gate triggering current
I_H	Holding current
I_{RG}	Reverse leakage current GATE / LINE
V_{GT}	Gate triggering voltage
V_F	Forward drop voltage LINE / GND
V_{FP}	Peak forward voltage LINE / GND
V_{DGL}	Dynamic switching voltage GATE / LINE
V_{GATE}	GATE / GND voltage
V_{RG}	Reverse voltage GATE / LINE
C	Capacitance LINE / GND

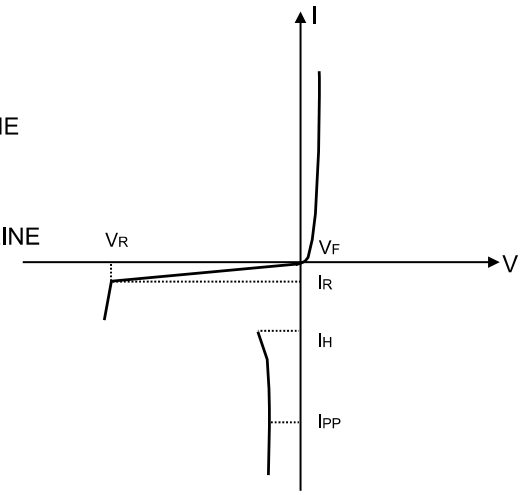


Figure 3: Pulse waveform

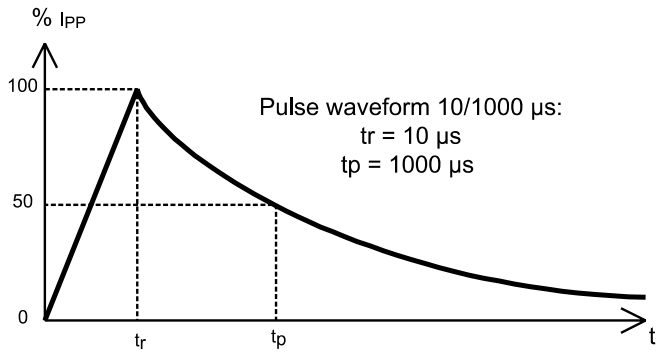


Table 4: Parameters (T_j = 25 °C unless otherwise specified)

Symbol	Test conditions		Min.	Typ.	Max.	Unit
I_{GT}	V_{LINE} = -48 V		0.05		5	mA
I_H	V_{Gn} = -48 V		150			mA
V_{GT}	at I_{GT}				2.5	V
I_{RG}	V_{RG} = -175 V V_{RG} = -175 V	T_j = 25 °C T_j = 85 °C			5 50	µA
V_{DGL} (1)	V_{Gn} = -48 V, 10/700 µs, 1.5 kV, R_S = 0 Ω, I_{PP} = 37.5 A				5	V
V_F	I_F = 1 A	t = 500 µs			2	V
V_{FP}	10/700 µs, 1.5 kV, R_S = 0 Ω, I_{PP} = 37.5 A				8	V
I_R	$V_{Gn\ /\ LINE}$ = -1 V, V_{LINE} = -175 V $V_{Gn\ /\ LINE}$ = -1 V, V_{LINE} = -175 V	T_j = 25 °C T_j = 85 °C			5 50	µA
C	V_{LINE} = -50 V, V_{RMS} = 1 V, f = 1 MHz V_{LINE} = -2 V, V_{RMS} = 1 V, f = 1 MHz			18 35		pF

Notes:

(1)The oscillations with a time duration lower than 50 ns are not taken into account.

Table 5: Recommended gate capacitance

Symbol	Component	Min.	Typ.	Max.	Unit
C_G	Gate decoupling capacitance	100	220	-	nF

2 Technical information

The LCDP1521S is particularly optimized for the new telecom applications such as the fiber in the loop, the WLL, the remote central office. In this case, the operating voltages are smaller than in the classical system. This makes the high voltage SLICs particularly suitable. The schematics of *Figure 4: "Protection of high voltage SLICs"* shows the topologies most frequently used for these applications.

Figure 4: Protection of high voltage SLICs

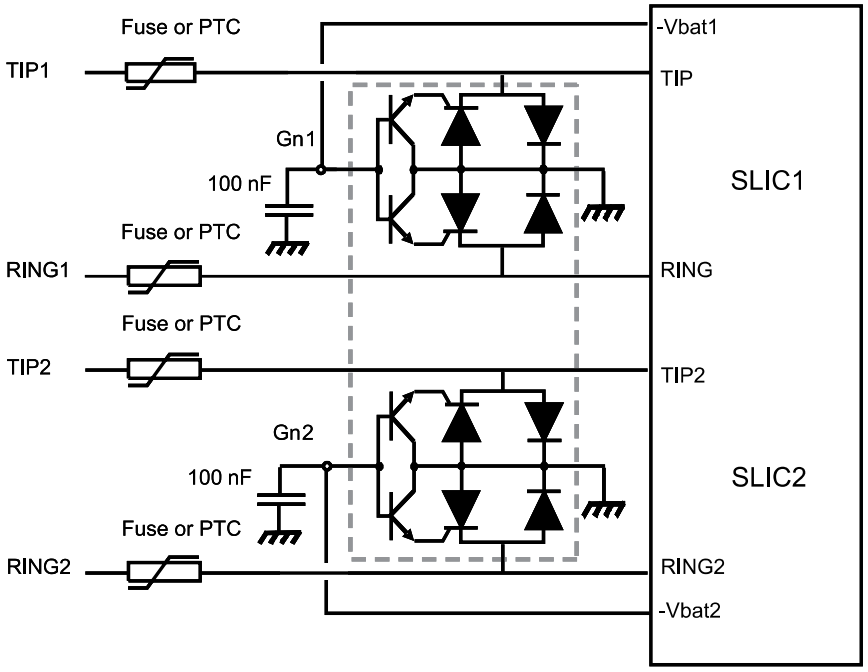


Figure 5: Surge peak current versus duration

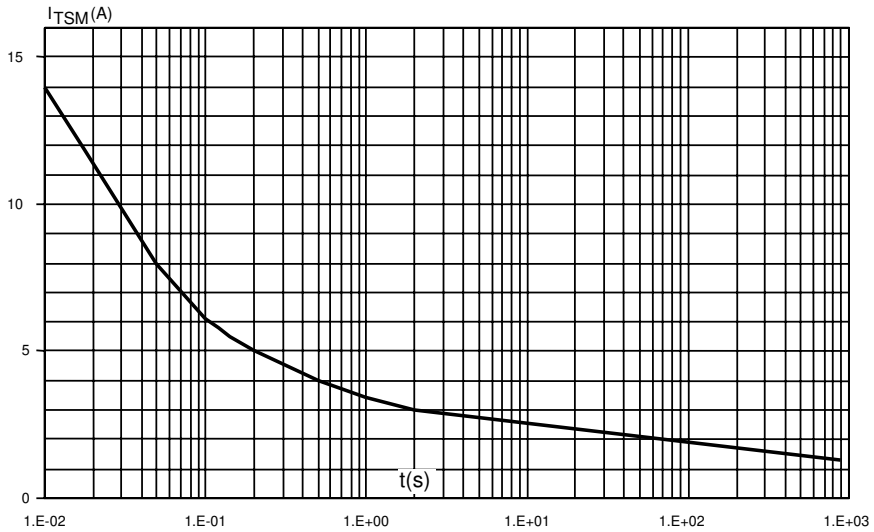
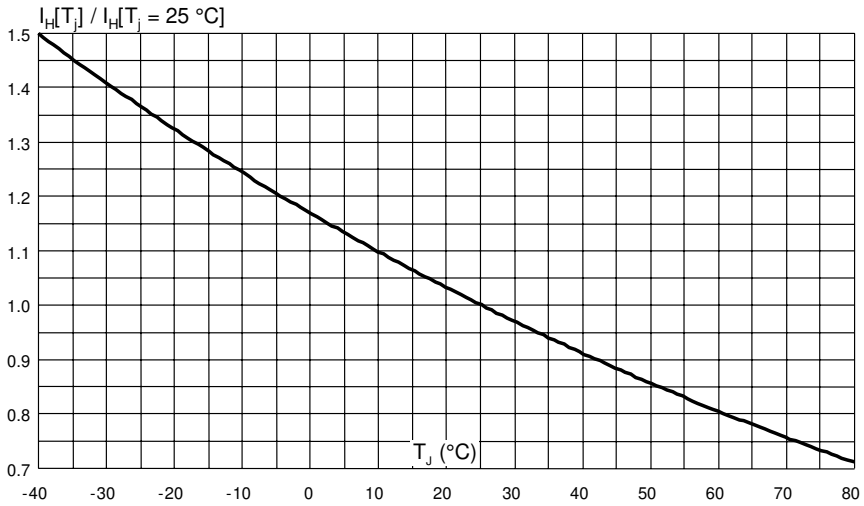


Figure 6: Relative variation of holding current versus junction temperature



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

3.1 SO-8 package information

Figure 7: SO-8 package outline

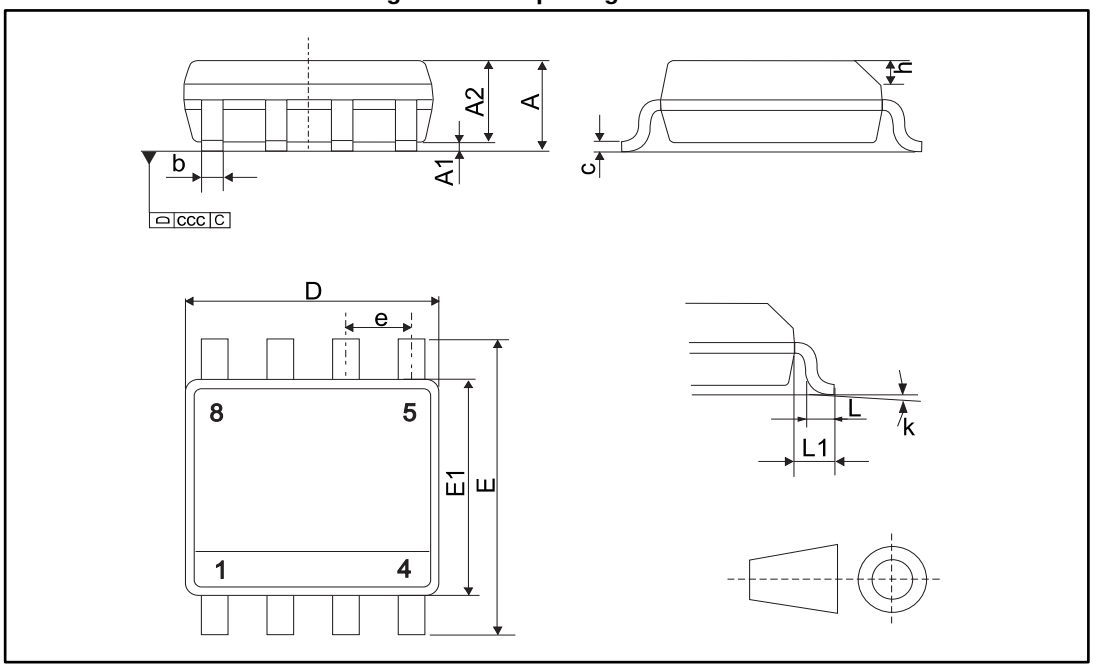


Table 6: SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.010
A2	1.25			0.049		
b	0.31		0.51	0.012		0.020
c	0.10		0.25	0.004		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.05
L1		1.04			0.041	
k°	0		8	0		8
ccc			0.10			0.004

Figure 8: Footprint recommendations, dimensions in mm (inches)

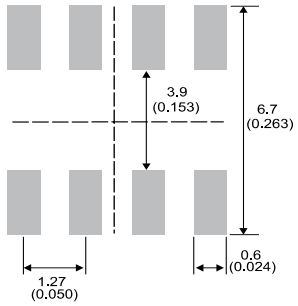


Figure 9: Marking layout (refer to ordering information table for marking)

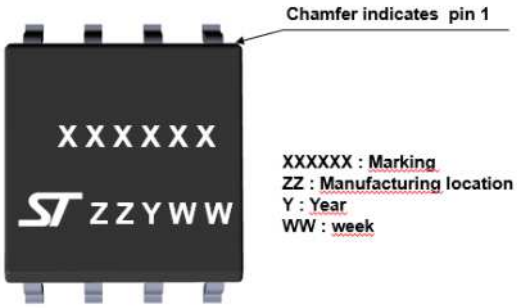
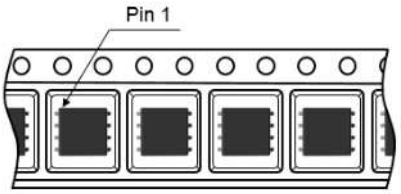


Figure 10: Package orientation in reel



Taped according to EIA-481
Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Figure 11: Tape and reel orientation

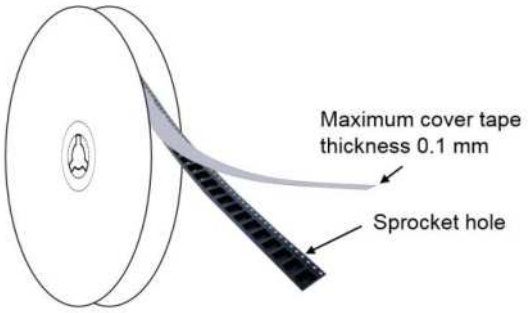


Figure 12: Reel dimensions (mm)

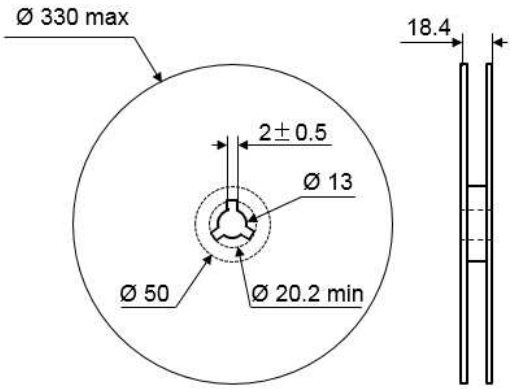


Figure 13: Inner box dimensions (mm)

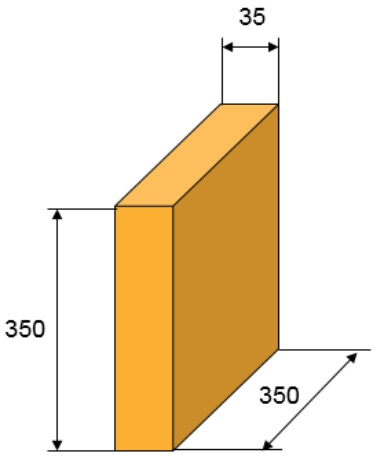


Figure 14: Tape and reel outline

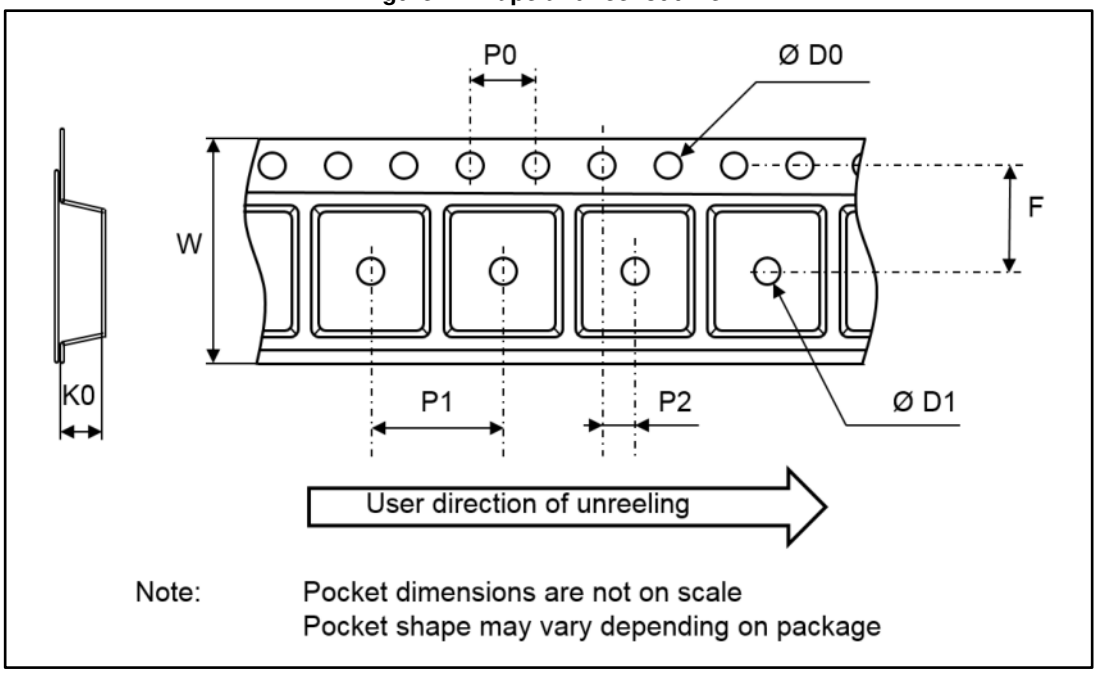
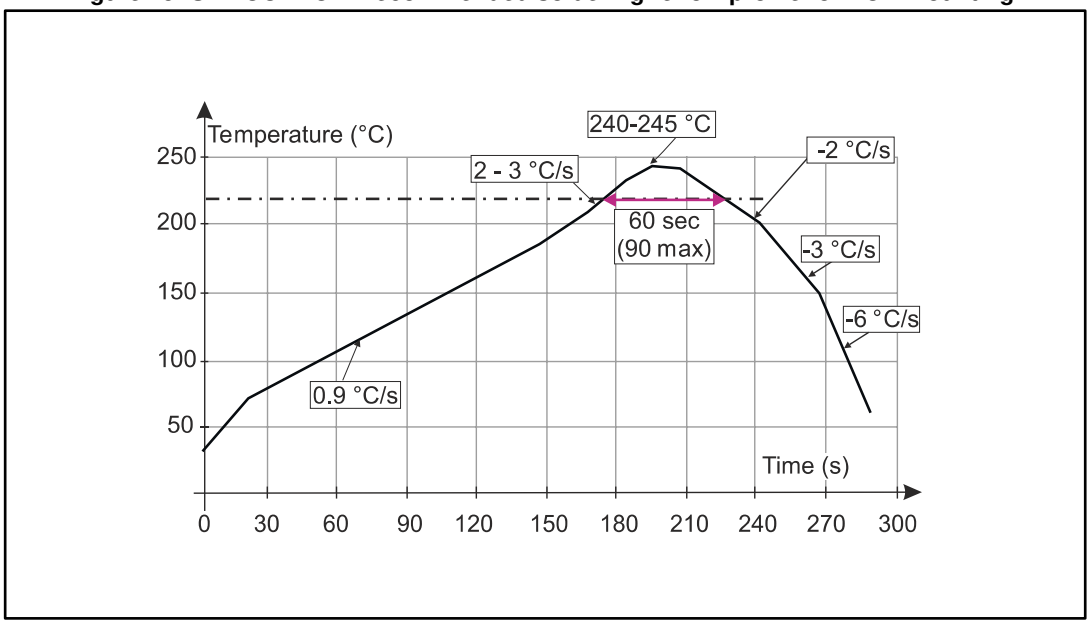


Table 7: Tape and reel mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
P0	3.9	4	4.1
P1	7.9	8	8.1
P2	1.95	2	2.05
ØD0	1.45	1.5	1.6
ØD1	1.6		
F	5.45	5.5	5.55
K0	2.5	2.6	2.7
W	11.7	12	12.3

Figure 15: ST ECOPACK® recommended soldering reflow profile for PCB mounting



Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 16: Ordering information scheme

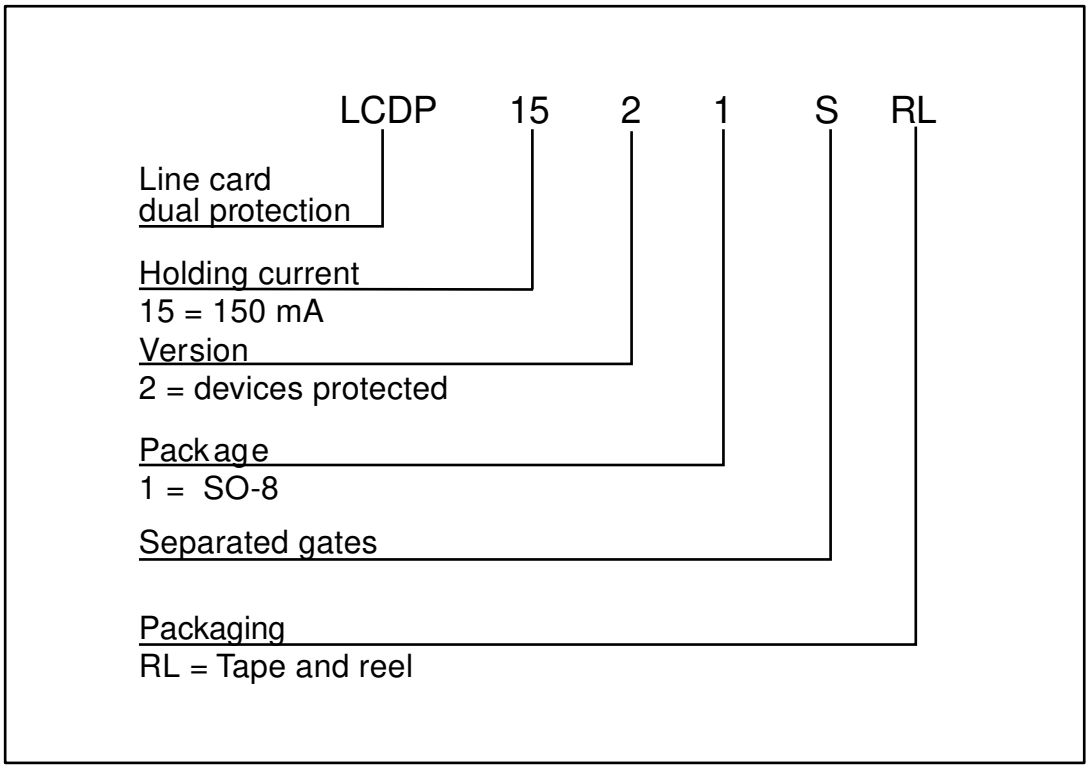


Table 8: Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
LCDP1521SRL	DP152S	SO-8	0.08 g	2500	Tape and reel

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
24-Sep-2009	1	First issue.
23-Feb-2012	2	Standardized nomenclature for Gn and Gp.
20-May-2015	3	Updated *Table 3* and package view.
02-Jul-2015	4	Updated package information.
08-Jul-2015	5	Updated *Figure 7*.
01-Oct-2016	6	Updated *Section 6: "Characteristics"* and *Section 8.1: "SO-8 package information"*. Minor format changes.
09-Feb-2017	7	Updated *Figure 7: "SO-8 package outline"*.

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