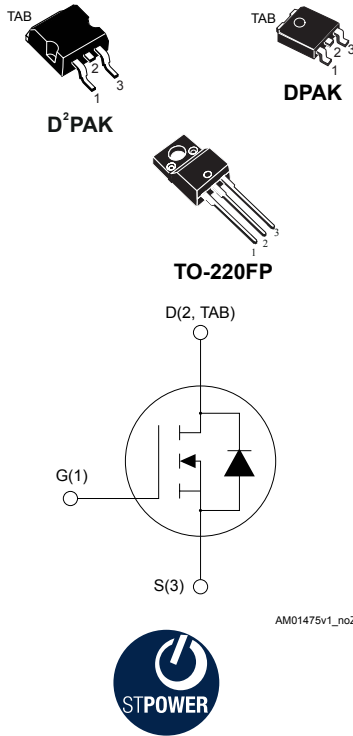




N-channel 650 V, 560 mΩ typ., 7 A MDmesh M5 Power MOSFETs in a D²PAK, DPAK and TO-220FP packages



Features

Order codes	$V_{DS} @ T_J \text{ max.}$	$R_{DS(on)} \text{ max.}$	I_D	P_{TOT}
STB8N65M5	710 V	600 mΩ	7 A	70 W
STD8N65M5				70 W
STF8N65M5				25 W

- 100% avalanche tested
- Excellent switching performance
- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Product status links

[STB8N65M5](#)

[STD8N65M5](#)

[STF8N65M5](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		D ² PAK	DPAK	TO-220FP	
V _{GS}	Gate-source voltage	±25			V
I _D	Drain current (continuous) at T _C = 25 °C	7		7 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	4.4		4.4 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	28		28 ⁽¹⁾	A
P _{TOT}	Total power dissipation at T _C = 25 °C	70		25	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15			V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2.5			kV
T _J	Operating junction temperature range	-55 to 150			°C
T _{stg}	Storage temperature range				

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 7\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		D ² PAK	DPAK	TO-220FP	
R _{thJC}	Thermal resistance, junction-to-case	1.79		5	°C/W
R _{thJA}	Thermal resistance, junction-to-ambient	30 ⁽¹⁾	50 ⁽¹⁾	62.5	°C/W

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J max.)	2	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	120	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			100	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 3.5\text{ A}$		560	600	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$		690		pF
C_{oss}	Output capacitance			18		
C_{rss}	Reverse transfer capacitance			2		
$C_{o(tr)}^{(1)}$	Equivalent output capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0\text{ V}$		17		pF
$C_{o(er)}^{(2)}$	Equivalent output capacitance energy related			52		pF
R_g	Gate input resistance	$f = 1\text{ MHz}$ open drain	2 ⁽³⁾	5	8 ⁽³⁾	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 3.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 18. Test circuit for gate charge behavior)		15		nC
Q_{gs}	Gate-source charge			3.6		
Q_{gd}	Gate-drain charge			6		

1. $C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.

2. $C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.

3. Specified by design, not tested in production.

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 400\text{ V}$, $I_D = 4\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 19. Test circuit for inductive load switching and diode recovery times and Figure 22. Switching time waveform)	-	50	-	ns
$t_{r(v)}$	Voltage rise time		-	14	-	
$t_{c(off)}$	Crossing time off		-	20	-	
$t_{f(i)}$	Current fall time		-	11	-	

Table 7. Source-drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		28	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	200		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100\text{ V}$ (see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	1.6		μC
I_{RRM}	Reverse recovery current		-	16		A
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	263		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	1.9		μC
I_{RRM}	Reverse recovery current		-	15		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

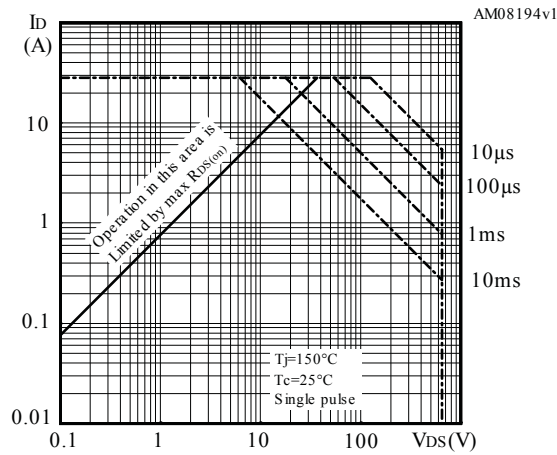
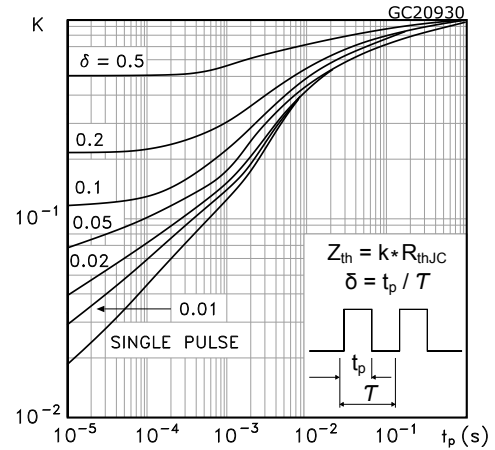
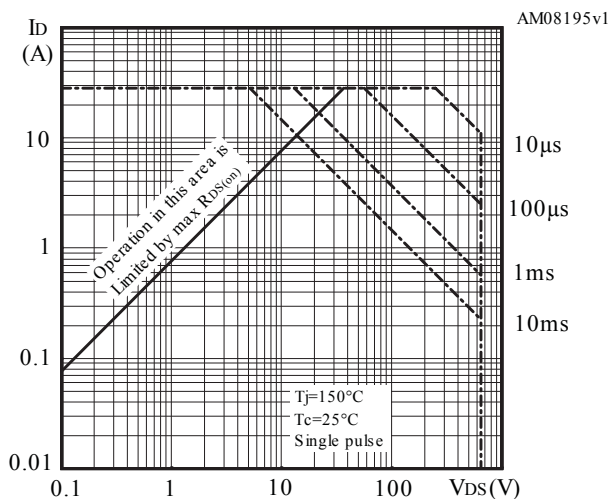
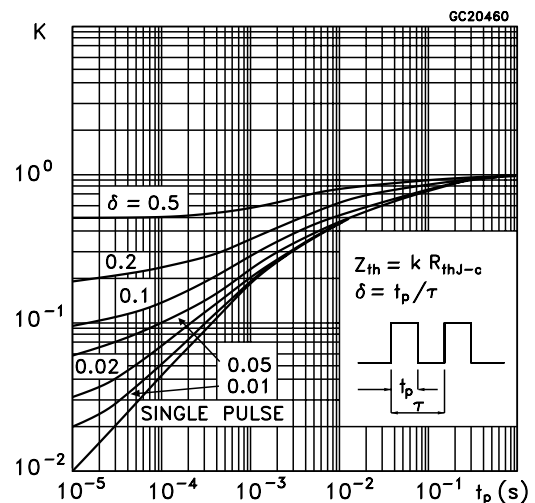
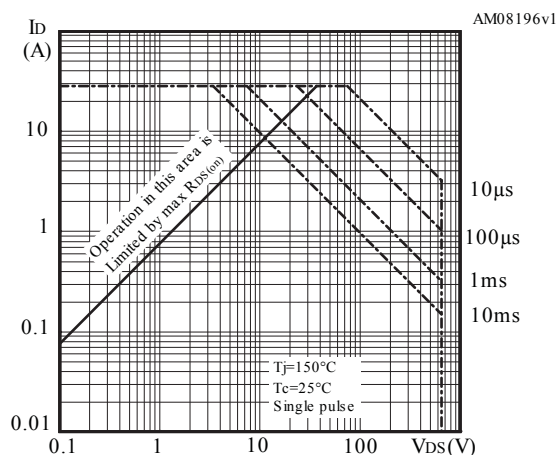
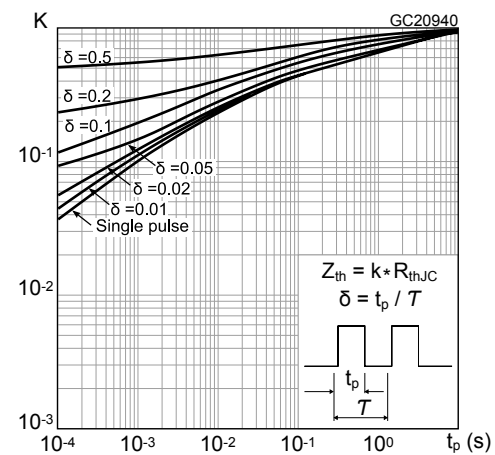
Figure 1. Safe operating area for D²PAK

Figure 2. Thermal impedance for D²PAK

Figure 3. Safe operating area for DPAK

Figure 4. Thermal impedance for DPAK

Figure 5. Safe operating area for TO-220FP

Figure 6. Thermal impedance for TO-220FP


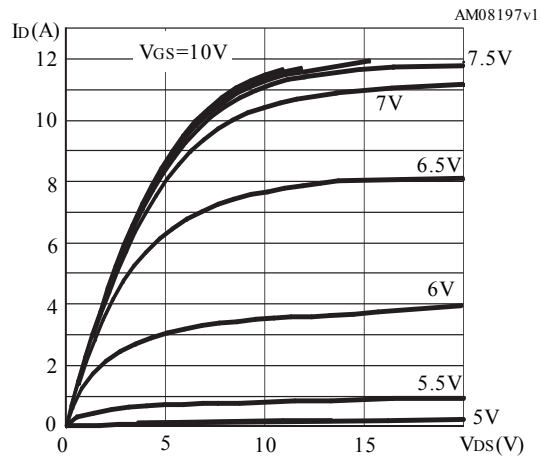
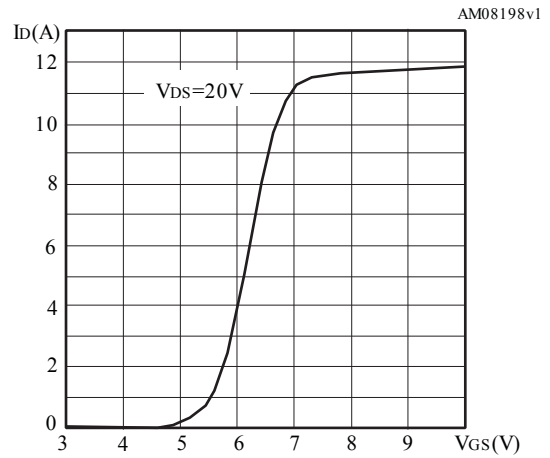
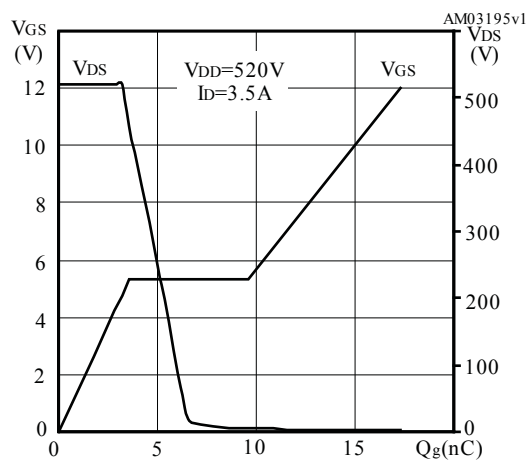
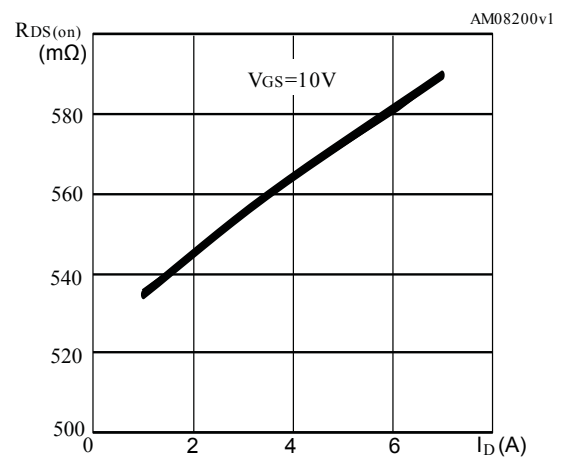
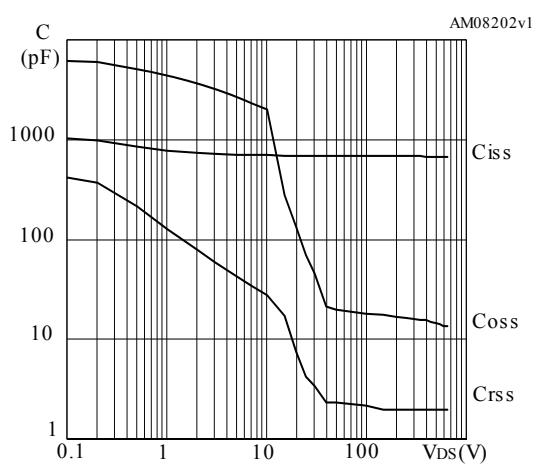
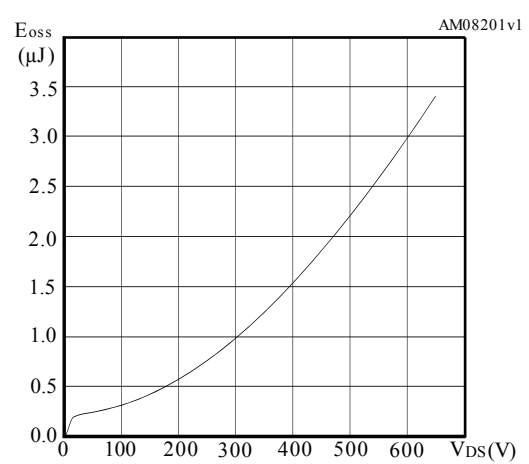
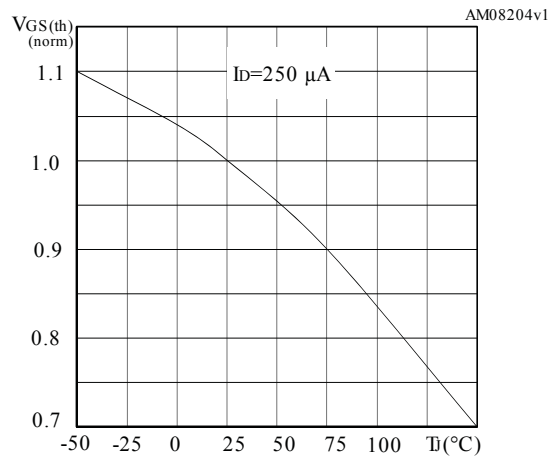
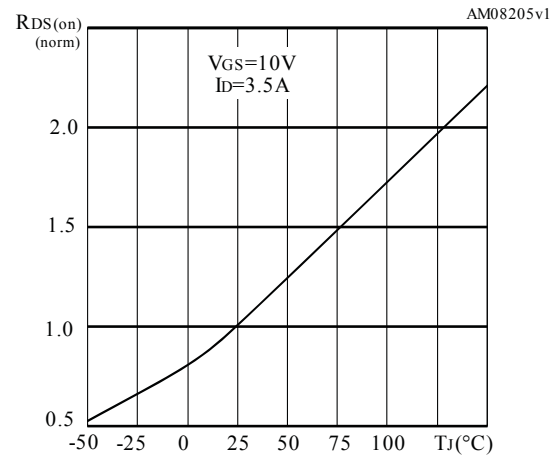
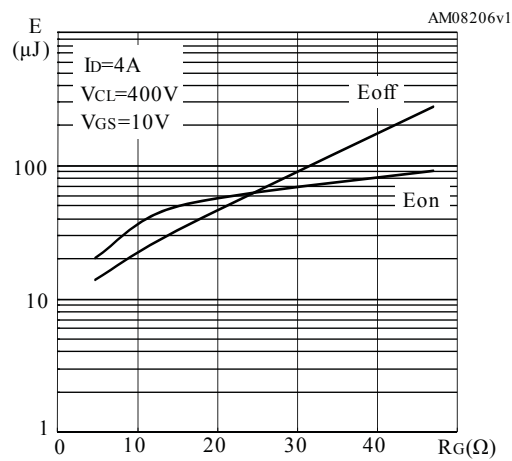
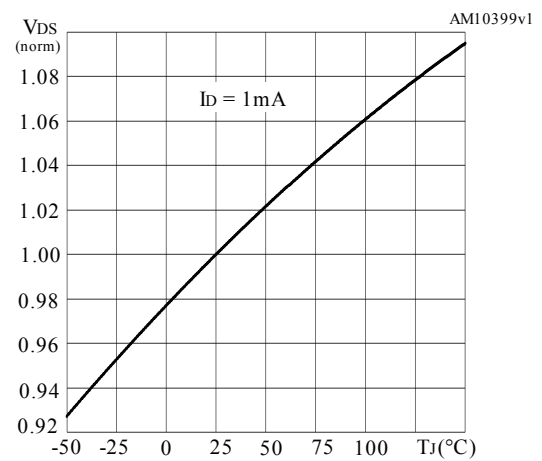
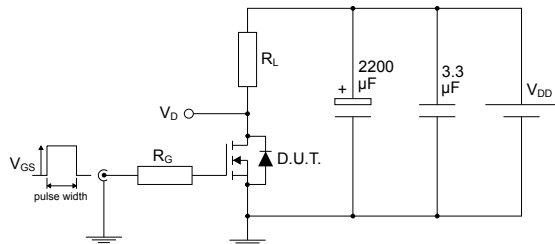
Figure 7. Output characteristics

Figure 8. Transfer characteristics

Figure 9. Gate charge vs gate-source voltage

Figure 10. Static drain-source on-resistance

Figure 11. Capacitance variations

Figure 12. Output capacitance stored energy


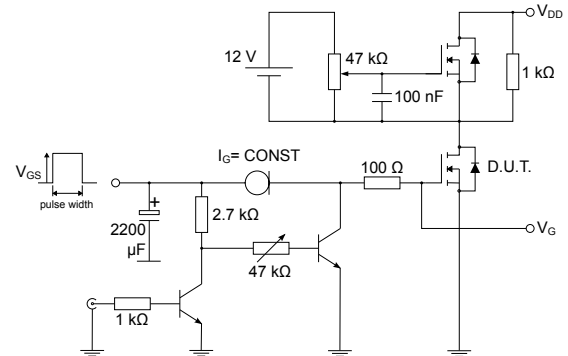
Figure 13. Normalized gate threshold voltage vs temperature

Figure 14. Normalized on-resistance vs temperature

Figure 15. Switching energy vs gate resistance

Figure 16. Normalized $V_{(BR)DSS}$ vs temperature


Note: E_{on} including reverse recovery of a SiC diode.

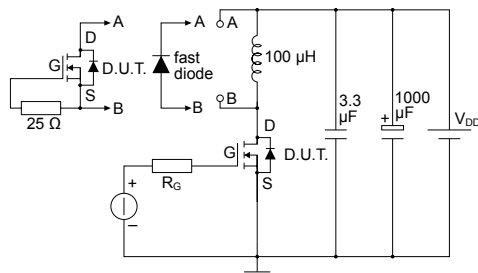
3 Test circuits

Figure 17. Test circuit for resistive load switching times


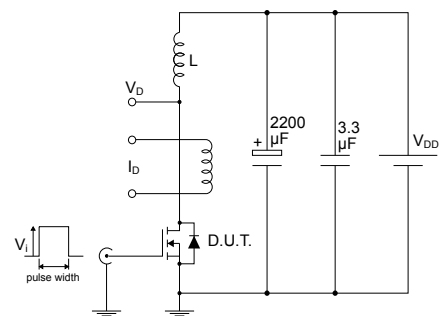
AM01468v1

Figure 18. Test circuit for gate charge behavior


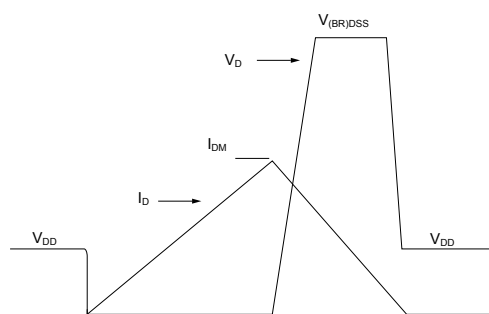
AM01469v1

Figure 19. Test circuit for inductive load switching and diode recovery times


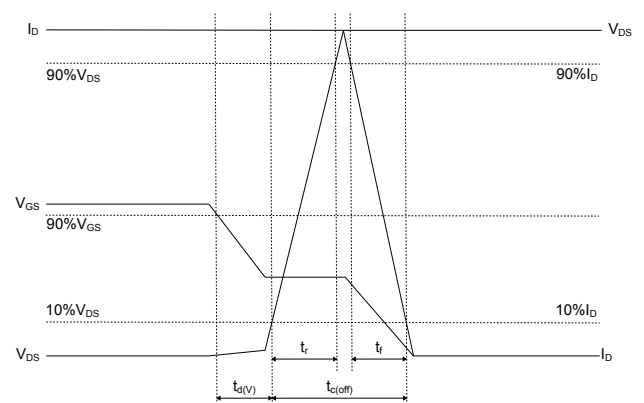
AM01470v1

Figure 20. Unclamped inductive load test circuit


AM01471v1

Figure 21. Unclamped inductive waveform


AM01472v1

Figure 22. Switching time waveform


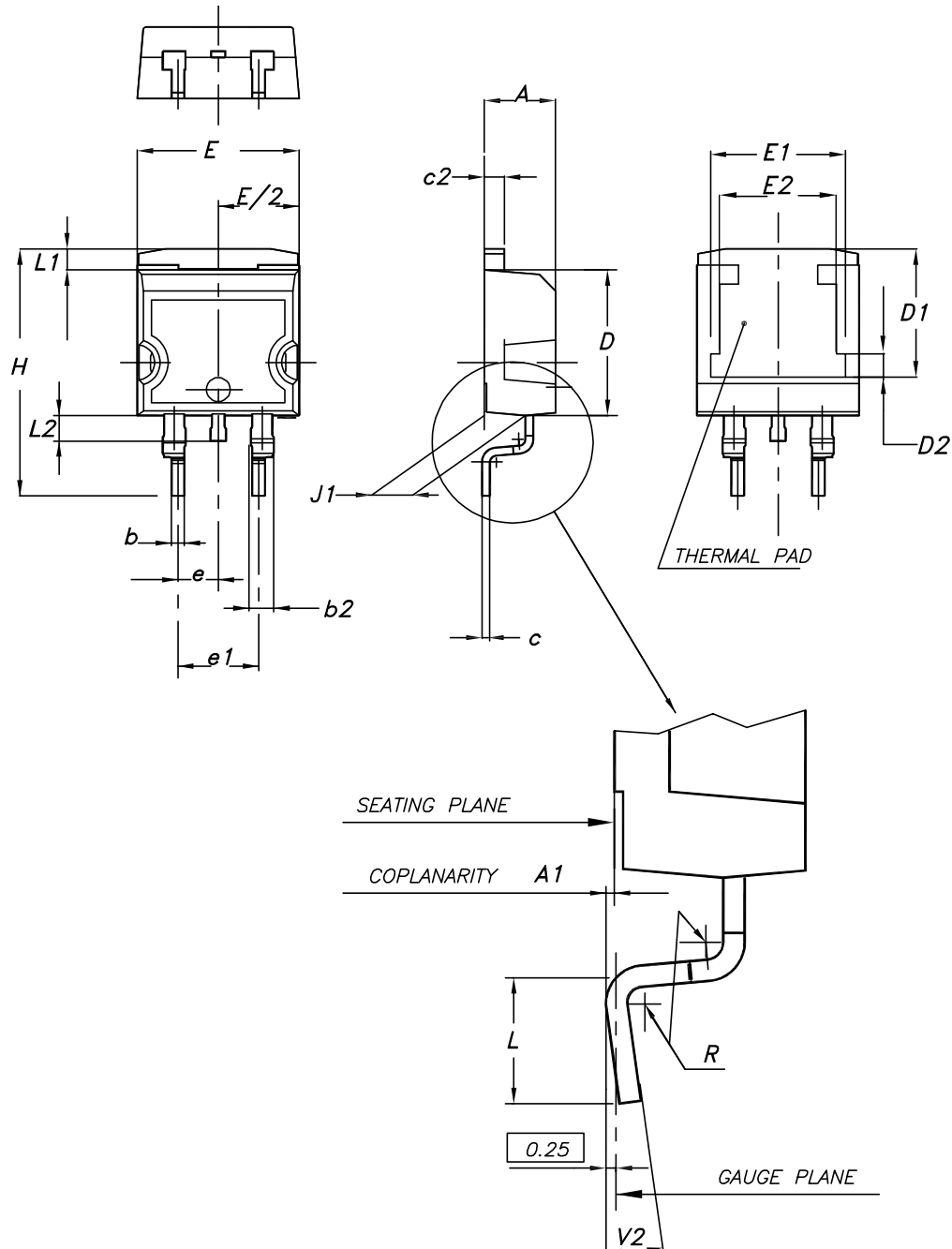
AM05540v2

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 23. D²PAK (TO-263) type A package outline

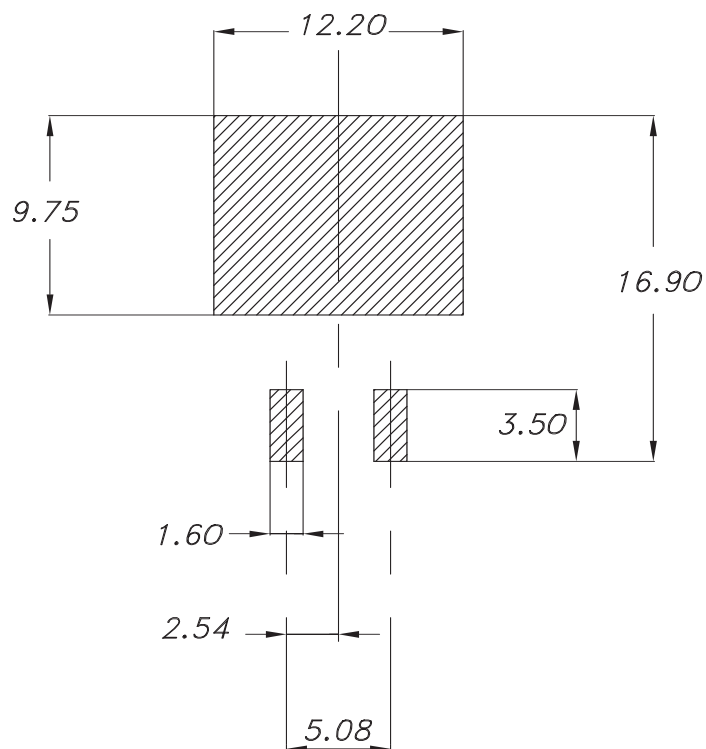


0079457_27

Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

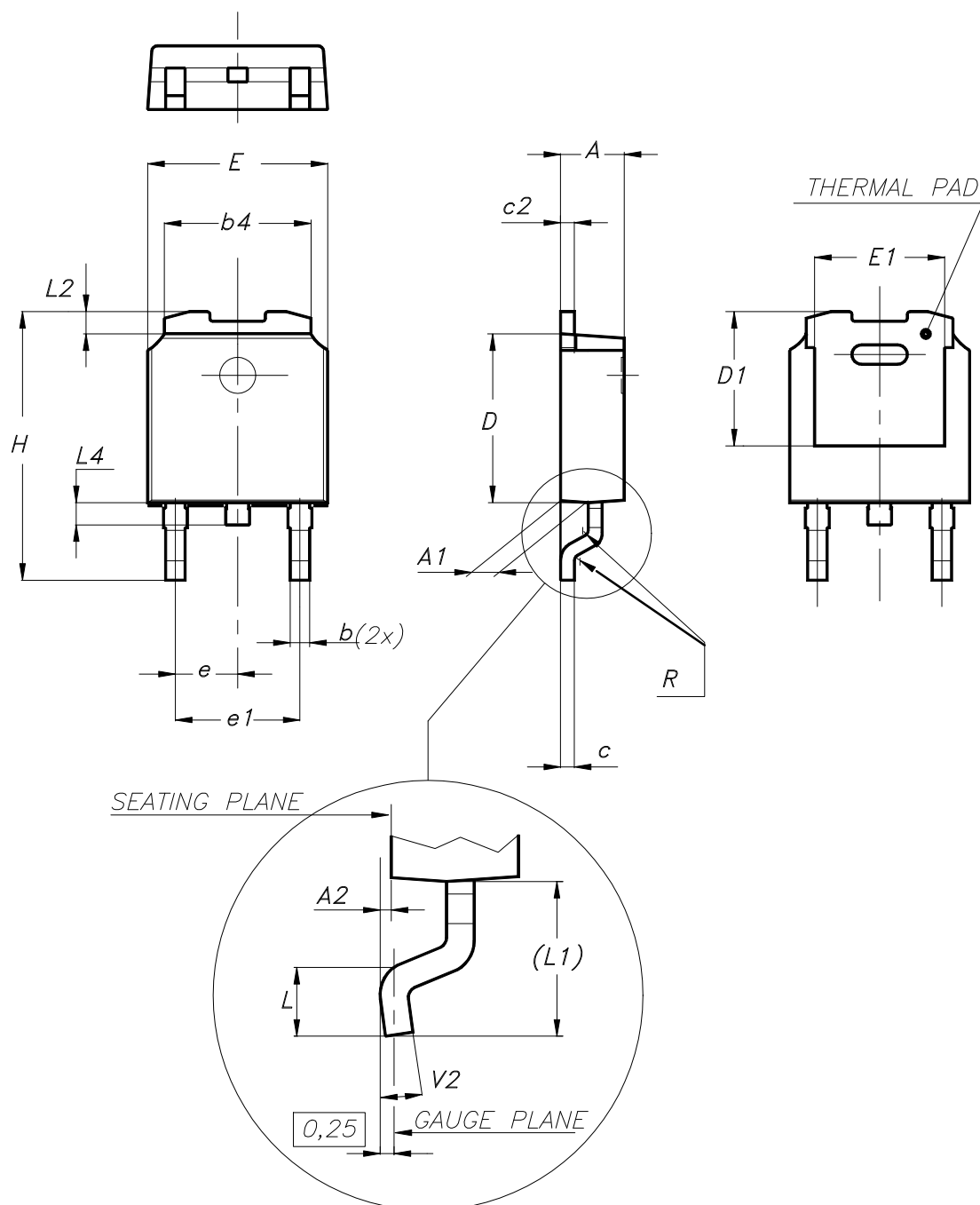
Figure 24. D²PAK (TO-263) recommended footprint (dimensions are in mm)



0079457_Rev27_footprint

4.2 DPAK (TO-252) type A package information

Figure 25. DPAK (TO-252) type A package outline



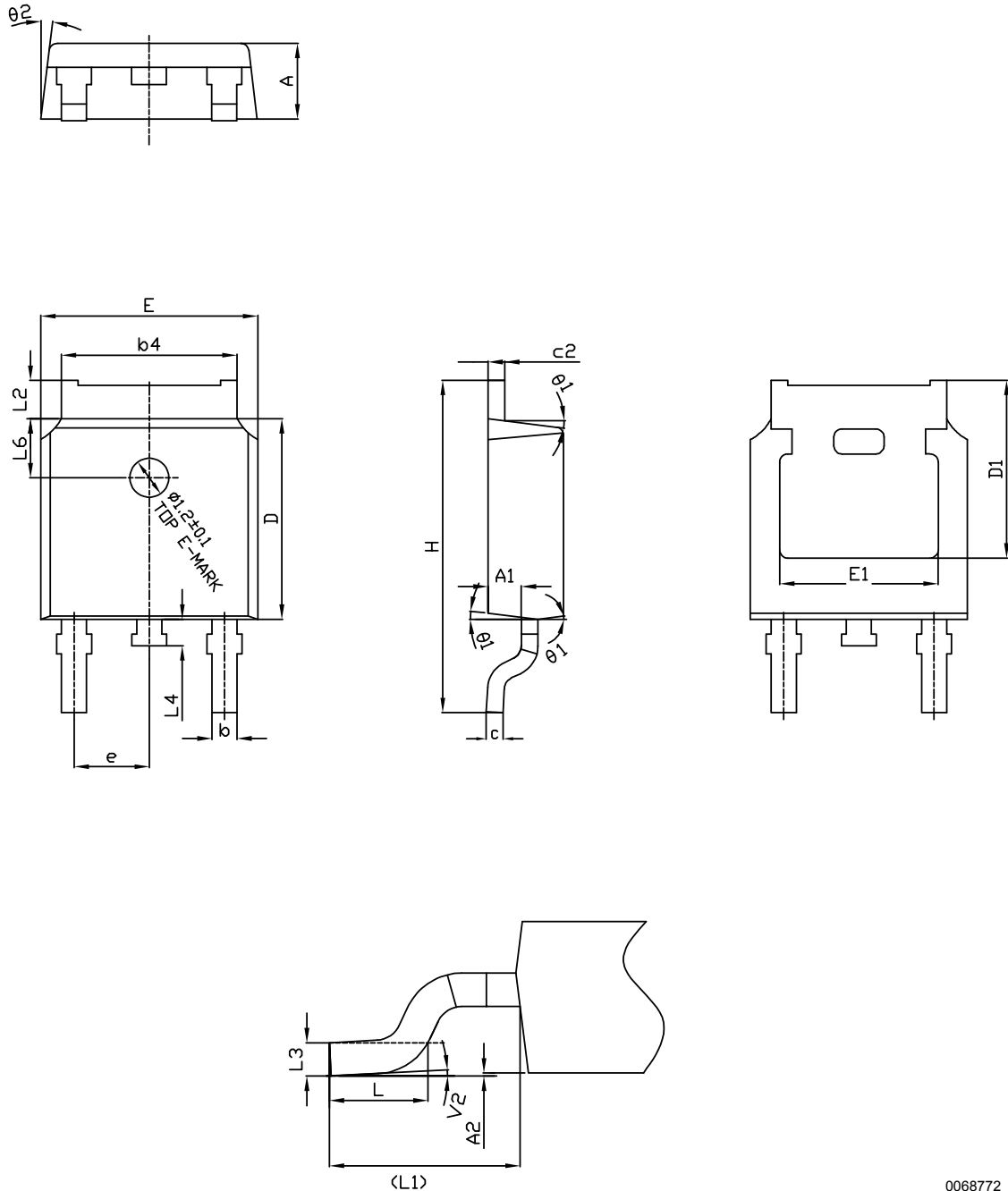
0068772_A_36

Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.3 DPAK (TO-252) type C package information

Figure 26. DPAK (TO-252) type C package outline



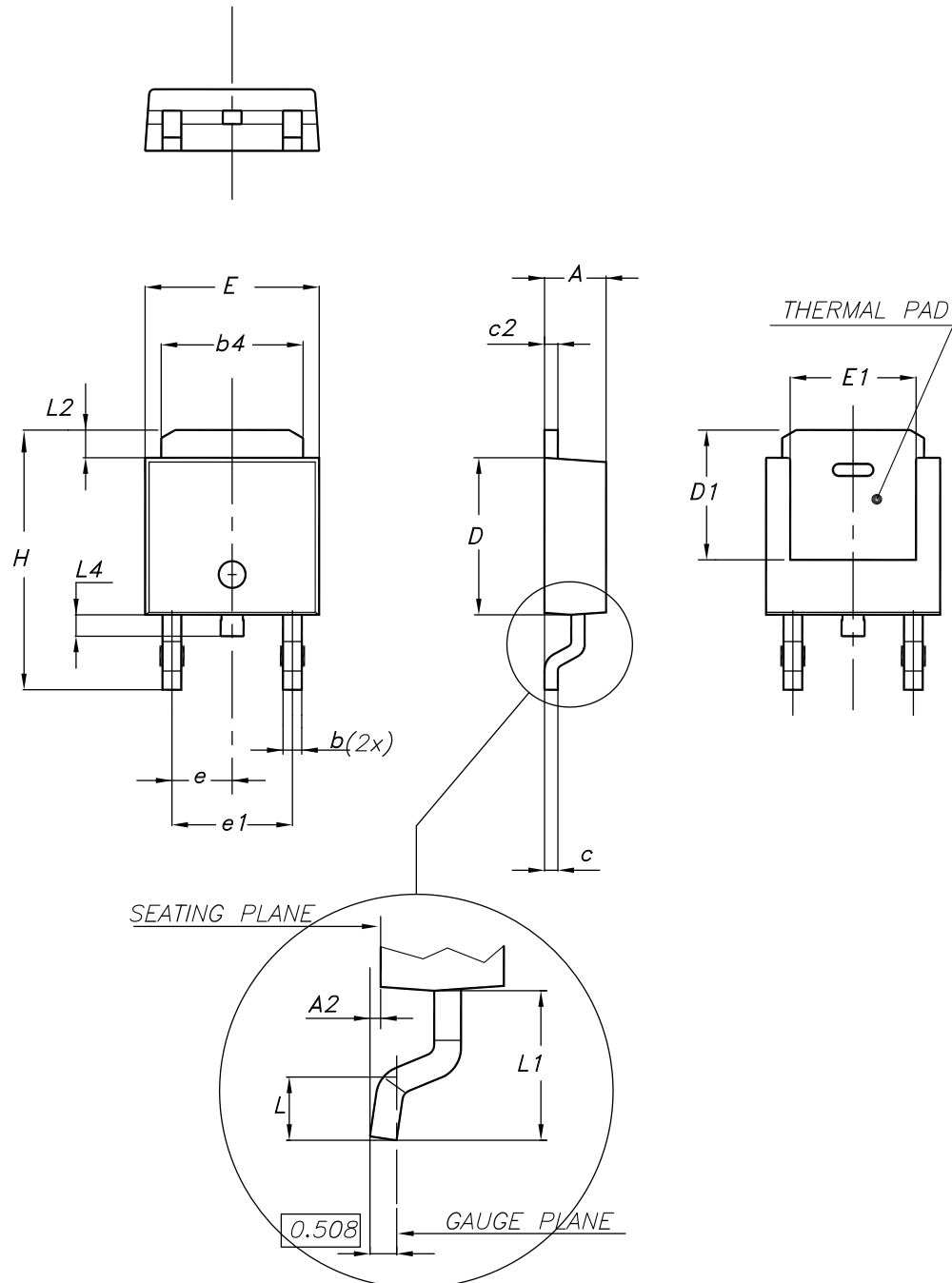
0068772_C_36

Table 10. DPAK (TO-252) type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.15	5.40	5.65
E	6.50	6.60	6.70
E1	4.70	4.85	5.00
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

4.4 DPAK (TO-252) type E package information

Figure 27. DPAK (TO-252) type E package outline

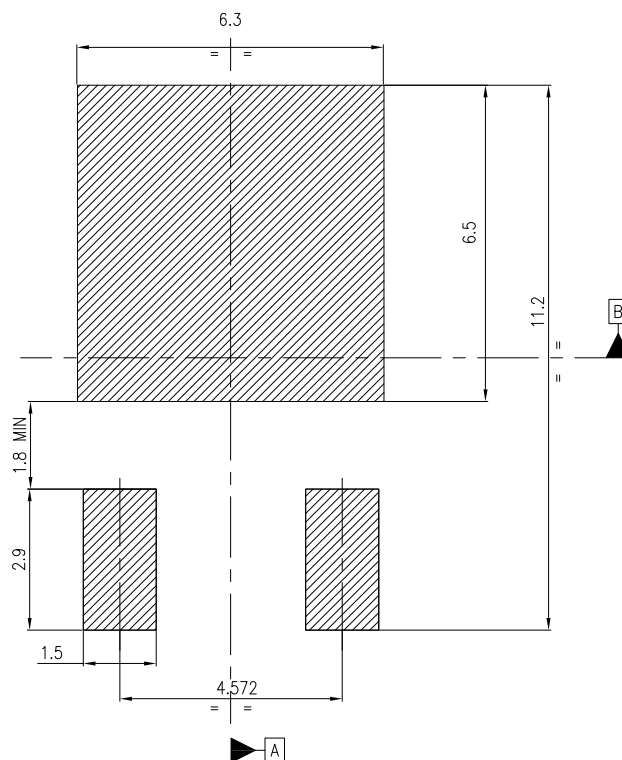


0068772_typeE_rev.36

Table 11. DPAK (TO-252) type E mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 28. DPAK (TO-252) recommended footprint (dimensions are in mm)



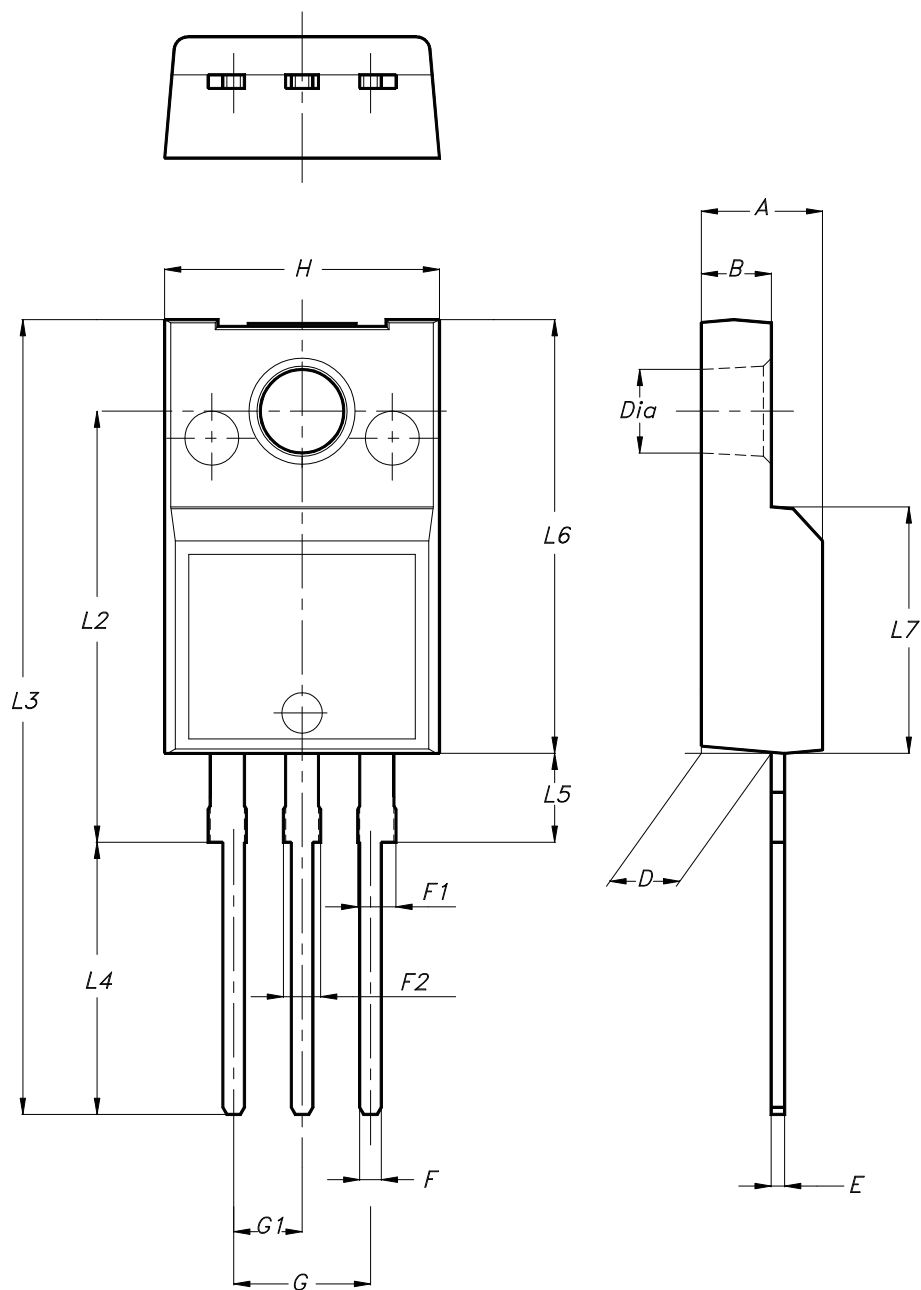
Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within $\Phi 0.05$ A B

FP_0068772_36

4.5 TO-220FP type B package information

Figure 29. TO-220FP type B package outline



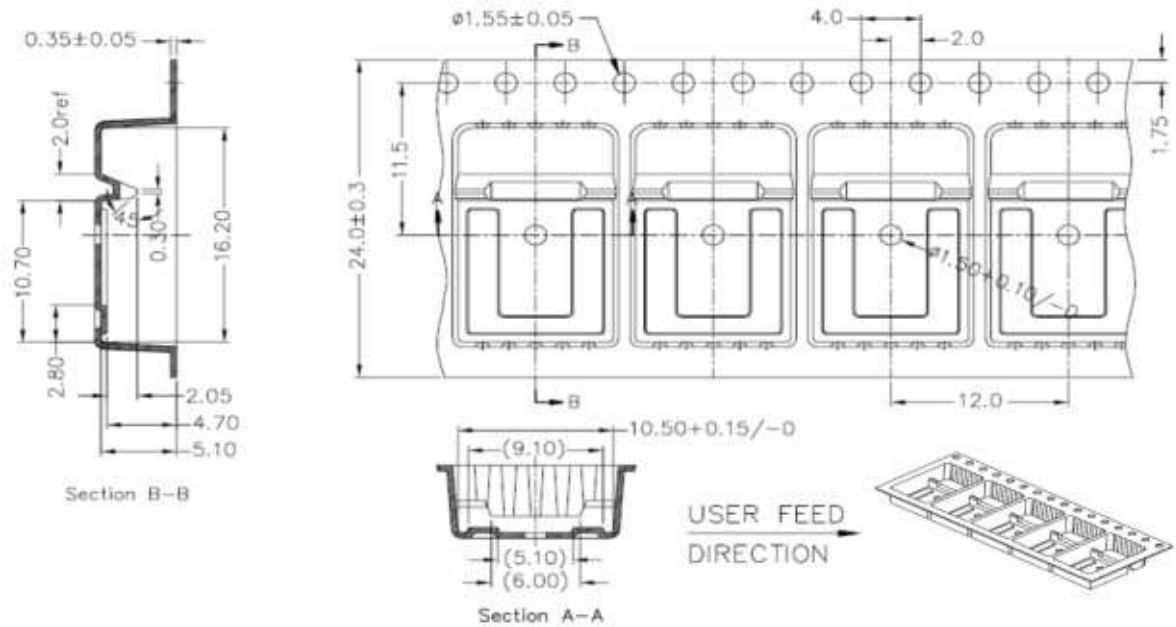
7012510_B_rev.14

Table 12. TO-220FP type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.6 D²PAK packing information

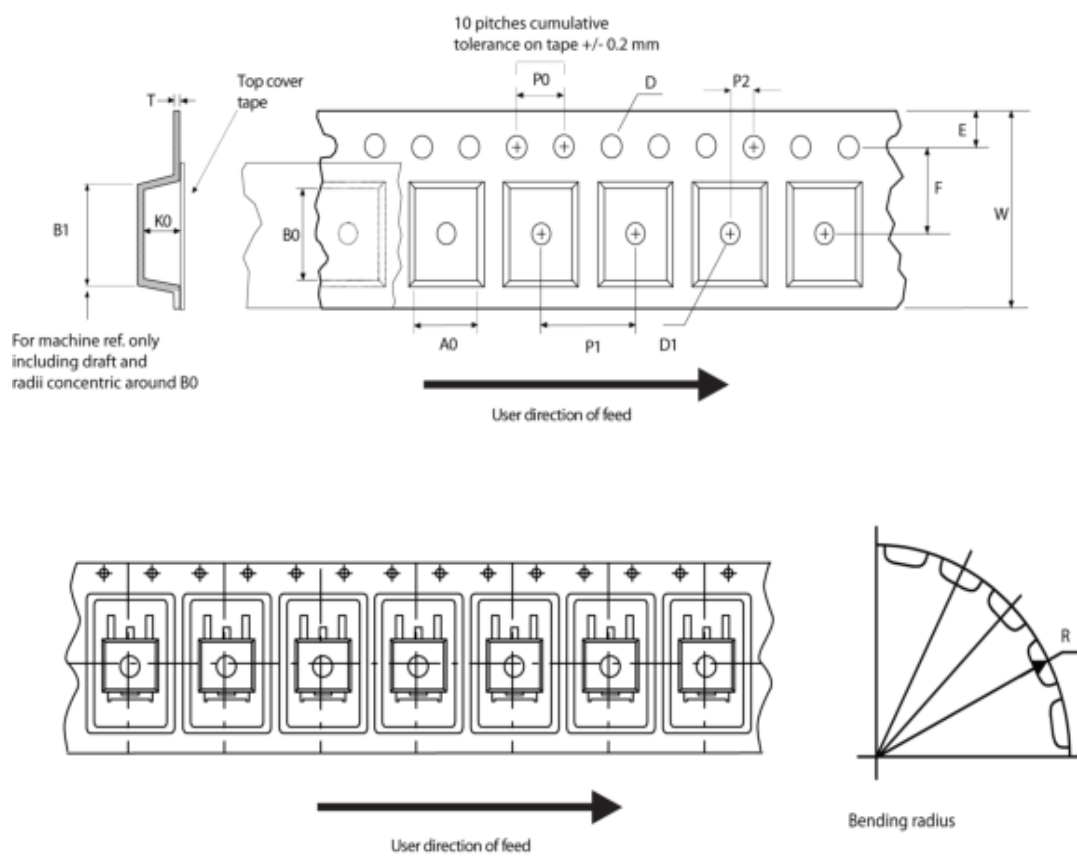
Figure 30. D²PAK tape drawing (dimensions are in mm)



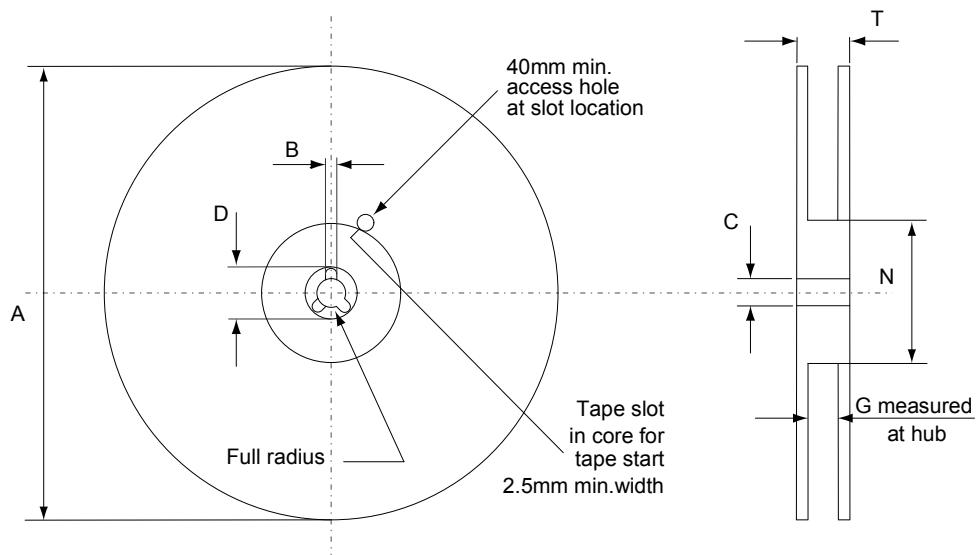
DM01095771_2

4.7 DPAK packing information

Figure 31. DPAK tape outline



AM08852v1

Figure 32. DPAK reel outline


AM06038v1

Table 13. DPAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			



5 Ordering information

Table 14. Order codes

Order codes	Marking	Package	Packing
STB8N65M5	8N65M5	D ² PAK	Tape and reel
STD8N65M5		DPAK	Tape and reel
STF8N65M5		TO-220FP	Tube

Revision history

Table 15. Document revision history

Date	Revision	Changes
23-Oct-2009	1	First release.
14-Oct-2010	2	Document status promoted from preliminary data to datasheet.
05-Jul-2011	3	<i>Table 7: Source drain diode</i> has been updated.
04-Oct-2012	4	<ul style="list-style-type: none"> – Updated: <i>Figure 1, 10, 14 and 17.</i> – Updated: <i>note1</i> and 3 below the <i>Table 2</i> – Updated the entire <i>Section 4: Package mechanical data.</i> – Updated title and description on the cover page.
29-Oct-2012	5	– Updated R_g values in <i>Table 5.</i>
03-Mar-2022	6	<p>The part numbers STI8N65M5, STP8N65M5, STU8N65M5 have been moved to a separate datasheet and the document has been updated accordingly.</p> <p>Modified R_g value in <i>Table 5. Dynamic.</i></p> <p>Updated <i>Section 4 Package information.</i></p> <p>Minor text changes.</p>
21-Aug-2025	7	<p>Updated <i>Section 4: Package information.</i></p> <p>Minor text changes.</p>

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	8
4	Package information	9
4.1	D ² PAK (TO-263) type A package information	9
4.2	DPAK (TO-252) type A package information	12
4.3	DPAK (TO-252) type C package information	14
4.4	DPAK (TO-252) type E package information	16
4.5	TO-220FP type B package information	19
4.6	D ² PAK packing information	21
4.7	DPAK packing information	22
5	Ordering information	24
	Revision history	25



IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved