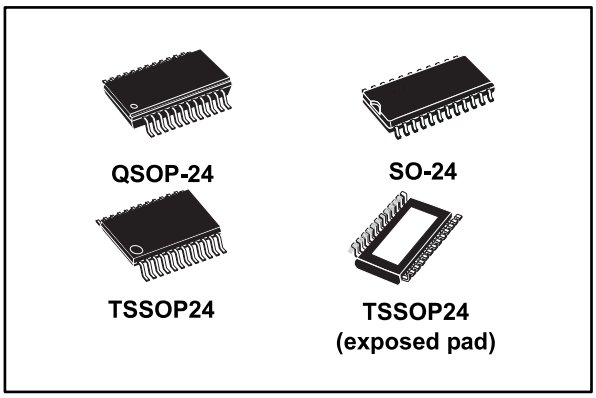
STP16DPS05

Low voltage 16-bit constant current LED sink driver with output error detection

Datasheet - production data



Features

- Low voltage power supply down to 3 V
- 16 constant current output channels
- Adjustable output current through external resistor
- Short and open output error detection
- Serial data IN/parallel data OUT
- 3.3 V micro driver-able
- Output current: 20-100 mA
- 30 MHz clock frequency
- Available in high thermal efficiency TSSOP exposed pad
- ESD protection: 2 kV HBM, 200 V MM

Description

The STP16DPS05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The device contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bit D-type storage register. In the output stage, sixteen regulated current sources were designed to provide 5-100 mA constant current to drive the LEDs.

The STP16DPS05 features open and short LED detections on the outputs. The STP16DPS05 is backward compatible with STP16C/L596.The detection circuit checks 3 different conditions that can occur on the output line: short to GND, short to V_O or open line.

The data detection results are loaded in the shift register and shifted out via the serial line output.

The detection functionality is implemented without increasing the pin count number, through a secondary function of the LATCH and output enable pin (DM1 and DM2 respectively), a dedicated logic sequence allows the device to enter or leave from detection mode. Through an external resistor, users can adjust the STP16DPS05 output current, controlling in this way the light intensity of LEDs, in addition, user can adjust LED's brightness intensity from 0% to 100% via $\overline{OE}$/DM2 pin.

The STP16DPS05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, makes the device suitable for high data rate transmission. The 3.3 V voltage supply is well useful for applications that interface any 3.3 V micro. Compared with a standard TSSOP package, the TSSOP exposed pad increases heat dissipation capability by a 2.5 factor.

Table 1: Device summary

Order code	Package	Packing
STP16DPS05MTR	SO-24 (tape and reel)	1000 parts per reel
STP16DPS05TTR	TSSOP24 (tape and reel)	2500 parts per reel
STP16DPS05XTTR	TSSOP24 exposed pad (tape and reel)	2500 parts per reel
STP16DPS05PTR	QSOP-24	2500 parts per reel

This is information on a product in full production. www.st.com

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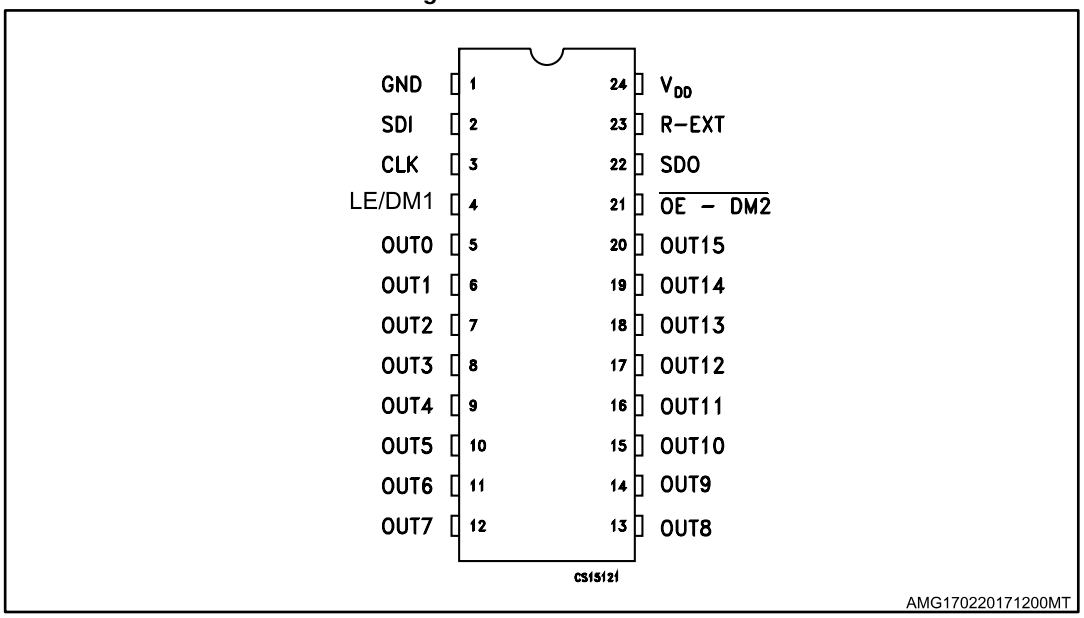
1 Summary description

Table 2: Typical current accuracy

Output voltage	Current accuracy		Output current	V_{DD}	Temperature
	Between bits	Between ICs			
≥ 1.3 V	± 1.5%	± 5%	20 to 100 mA	3.3 V to 5 V	25 °C

1.1 Pin connection and description

Figure 1: Pin connection



The exposed pad should be electrically connected to a metal land electrically isolated or connected to ground.

Table 3: Pin description

Pin n°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE/DM1	Latch input terminal - detect mode 1 (see operation principle)
5-20	$\overline{\text{OUT 0-15}}$	Output terminal
21	$\overline{\text{OE/DM2}}$	Input terminal of output enable (active low) - detect mode 1 (see operation principle)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal for an external resistor for constant current programming
24	V_{DD}	Supply voltage terminal

2 Electrical ratings

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the *Table 4: "Absolute maximum ratings"* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	100	mA
V_I	Input voltage	-0.4 to V_{DD}	V
I_{GND}	GND terminal current	1600	mA
f_{CLK}	Clock frequency	50	MHz
T_J	Junction temperature range (1)	-40 to + 170	°C

Notes:

(1) Such absolute value is achieved according the thermal shutdown.

2.2 Thermal data

Table 5: Thermal data

Symbol	Parameter		Value	Unit
T_{-OPR}	Operating temperature range		-40 to +125	°C
T_{STG}	Storage temperature range		-55 to +150	°C
R_{thJA}	Thermal resistance junction-ambient (1)	SO-24	42.7	°C/W
		TSSOP24	55	°C/W
		TSSOP24 (2) exposed pad	37.5	°C/W
		QSOP-24	55	°C/W

Notes:

(1) According with JEDEC JESD51-7.

(2) The exposed pad should be soldered directly to the PCB to obtain the thermal benefits.

2.3 Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3	-	5.5	V
V_O	Output voltage			-	20	V
I_O	Output current	OUTn	5	-	100	mA
I_{OH}	Output current	SERIAL-OUT		-	+1	mA
I_{OL}	Output current	SERIAL-OUT		-	-1	mA
V_{IH}	Input voltage		0.7 V_{DD}	-	V_{DD}+0.3	V
V_{IL}	Input voltage		-0.3	-	0.3 V_{DD}	V
t_{wLAT}	LE/DM1 pulse width	V_{DD} = 3.0 V to 5.0 V	6	-		ns
t_{wCLK}	CLK pulse width		8	-		ns
t_{wEN}	$\overline{OE}$/DM2 pulse width		100	-		ns
$t_{SETUP(D)}$	Setup time for DATA		10	-		ns
$t_{HOLD(D)}$	Hold time for DATA		5	-		ns
$t_{SETUP(L)}$	Setup time for LATCH		10	-		ns
f_{CLK}	Clock frequency	Cascade operation (1)		-	30	MHz

Notes:

(1) If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please consider the timings carefully.

3 Electrical characteristics

V_{DD} = 5 V, T_A = 25 °C, unless otherwise specified.

Table 7: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input voltage high level		0.7 V_{DD}		V_{DD}	V
V_{IL}	Input voltage low level		GND		0.3 V_{DD}	V
I_{OH}	Output leakage current	V_{OH} = 20 V			1	µA
V_{OL}	Output voltage (serial-OUT)	I_{OL} = 1 mA			0.4	V
V_{OH}	Output voltage (serial-OUT)	I_{OH} = -1 mA	V_{OH} -V_{DD} = -0.4 V			V
I_{OL1}	Output current	V_O = 0.3 V, R_{ext} = 3.9 kΩ	4.25	5	5.75	
I_{OL2}		V_O = 0.3 V, R_{ext} = 970 Ω	19	20	21	
I_{OL3}		V_O = 1.3 V, R_{ext} = 190 Ω	96	100	104	mA
ΔI_{OL1}	Output current error between bit (all output ON)	V_O = 0.3 V, R_{ext} = 3.9 kΩ		± 5	± 8	
ΔI_{OL2}		V_O = 0.3 V, R_{ext} = 970 Ω		± 1.5	± 3	%
ΔI_{OL3}		V_O = 1.3 V, R_{ext} = 190 Ω		± 1.2	± 3	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	kΩ
$R_{SIN(down)}$	Pull-down resistor		100	200	400	kΩ
$I_{DD(OFF1)}$	Supply current (OFF)	R_{ext} = 970 OUT 0 to 15 = OFF		5	6	mA
$I_{DD(OFF2)}$		R_{ext} = 240 OUT 0 to 15 = OFF		13	14	
$I_{DD(ON1)}$	Supply current (ON)	R_{ext} = 970 OUT 0 to 15 = ON		6	7	
$I_{DD(ON2)}$		R_{ext} = 240 OUT 0 to 15 = ON		13.5	14.5	
Thermal	Thermal protection (1)			170		°C

Notes:

(1) Guaranteed by design (not tested). The thermal protection switches OFF only the outputs current.

V_{DD} = 5 V, T_A = 25 °C, unless otherwise specified.

Table 8: Switching characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
t_{PLH1}	Propagation delay time, CLK- $\overline{OUTn}$, LE/DM1 = H, $\overline{OE/DM2}$ = L	V_{IH} = V_{DD} V_{IL} = GND C_L = 10 pF I_O = 20 mA V_L = 3.0 V R_{ext} = 1 KΩ R_L = 60 Ω	V_{DD} = 3.3 V	-	40 to 44	44	ns
			V_{DD} = 5 V	-	20 to 44	44	
t_{PLH2}	Propagation delay time, LE/DM1- $\overline{OUTn}$, $\overline{OE/DM2}$ = L		V_{DD} = 3.3 V	-	51	77	ns
			V_{DD} = 5 V	-	32	47	
t_{PLH3}	Propagation delay time, $\overline{OE/DM2}$ - $\overline{OUTn}$, LE = H		V_{DD} = 3.3 V	-	49 to 57	57 to 77	ns
			V_{DD} = 5 V	-	27 to 32	32 to 41	
t_{PLH}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V	-	21.5 to 22	32	ns
			V_{DD} = 5 V	-	14.5 to 15	21.5	
t_{PHL1}	Propagation delay time, CLK- $\overline{OUTn}$, LE/DM1 = H, $\overline{OE/DM2}$ = L		V_{DD} = 3.3 V	-	15 to 18	25	ns
			V_{DD} = 5 V	-	11 to 13	14.5 to 16	
t_{PHL2}	Propagation delay time, LE/DM1 $\overline{-OUTn}$, $\overline{OE/DM2}$ = L		V_{DD} = 3.3 V	-	13 to 18	18 to 25	ns
			V_{DD} = 5 V	-	9 to 12	12.5 to 15	
t_{PHL3}	Propagation delay time, $\overline{OE/DM2}$ - $\overline{OUTn}$, LE/DM1 = H		V_{DD} = 3.3 V	-	11.5 to 12	12 to 18	ns
			V_{DD} = 5 V	-	8.5 to 10	9.7 to 12	
t_{PHL}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V	-	25.5	38	ns
			V_{DD} = 5 V	-	17.5 to 20.5	25	
t_{ON}	Output rise time 10~90% of voltage waveform		V_{DD} = 3.3 V	-	34 to 20	24 to 53.5	ns
			V_{DD} = 5 V	-	12.5 to 9	9 to 18.5	
t_{OFF}	Output fall time 90~10% of voltage waveform		V_{DD} = 3.3 V	-	5.5 to 3.3	3.3 to 8.5	ns
			V_{DD} = 5 V	-	4.5to 2.8	2.8 to 6.5	
t_r	CLK rise time (1)			-		5000	ns
t_f	CLK fall time (1)			-		5000	ns

Notes:

(1) In order to achieve high cascade data transfer, please consider tr/tf timings carefully.

4 Equivalent circuit and outputs

Figure 2: OE/DM2 terminal

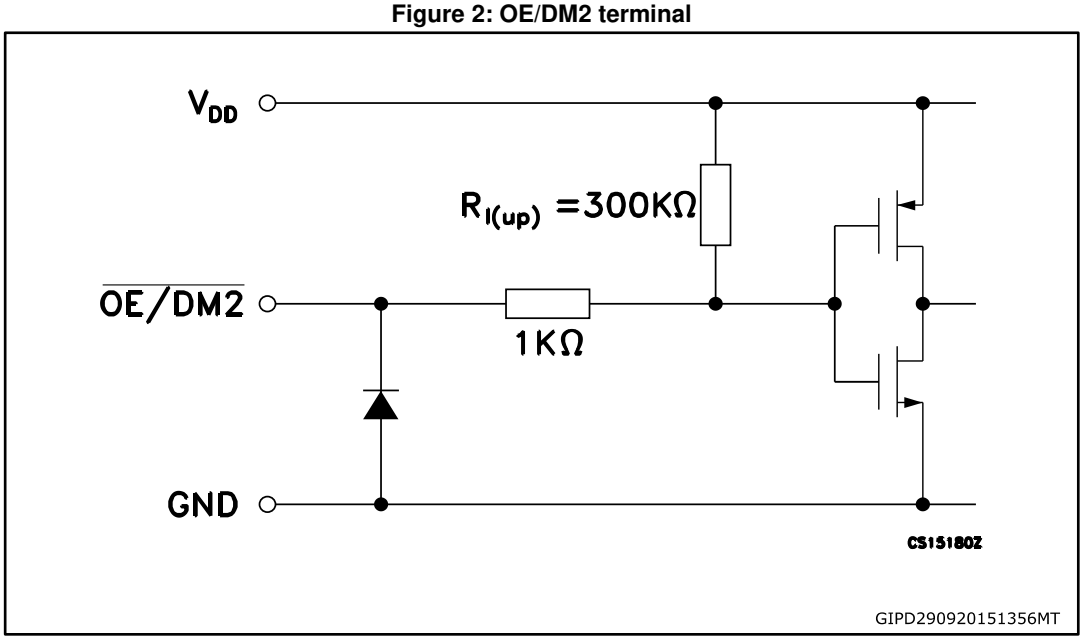


Figure 3: LE/DM1 terminal

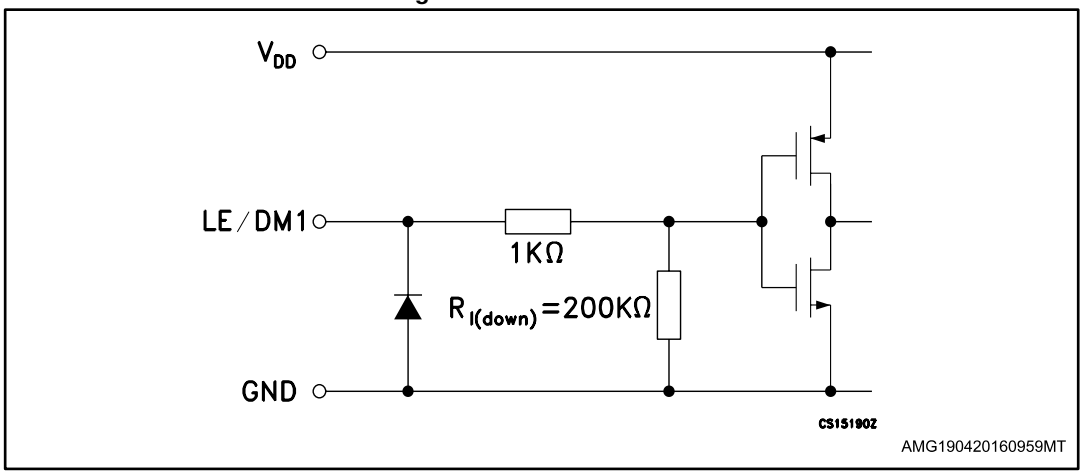


Figure 4: CLK, SDI terminal

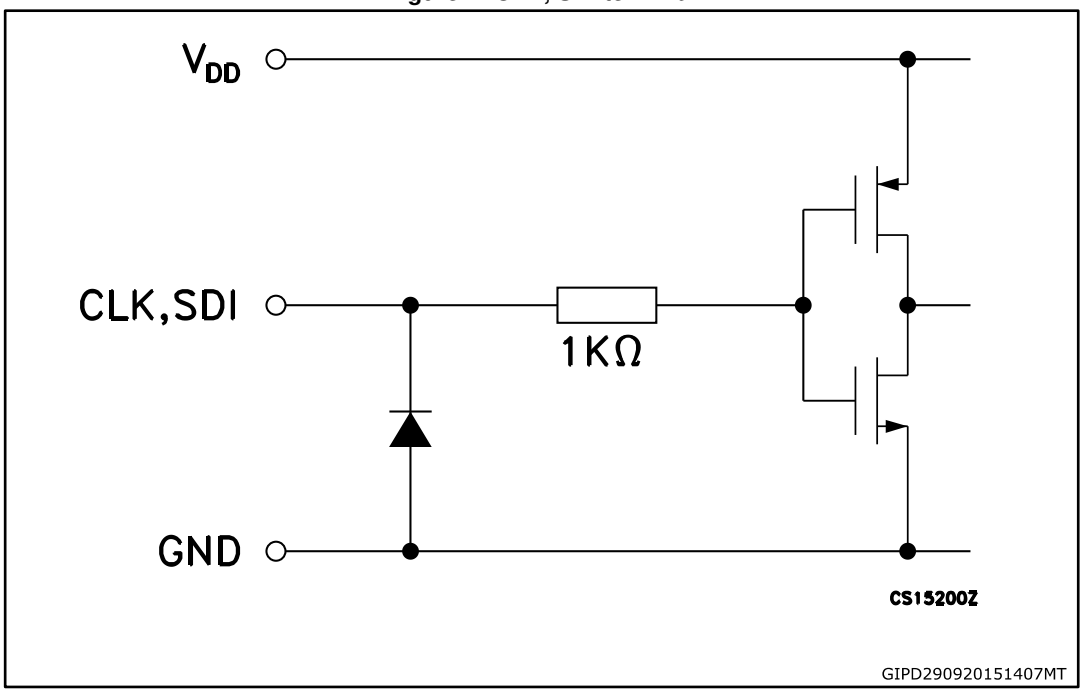


Figure 5: SDO terminal

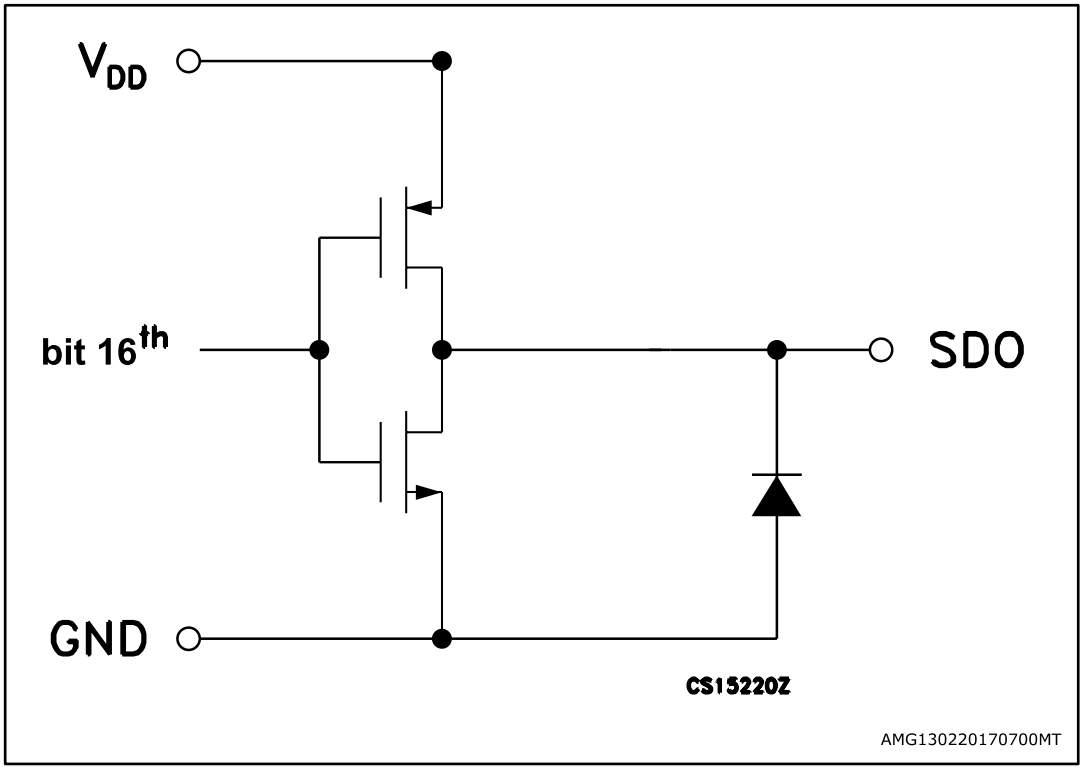
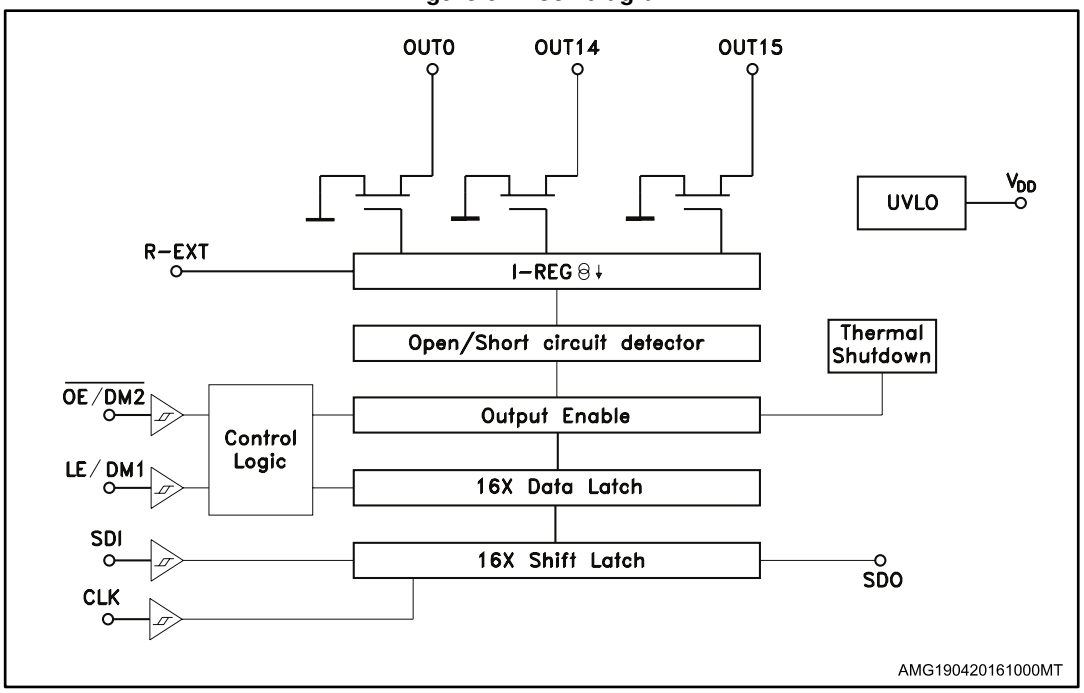


Figure 6: Block diagram



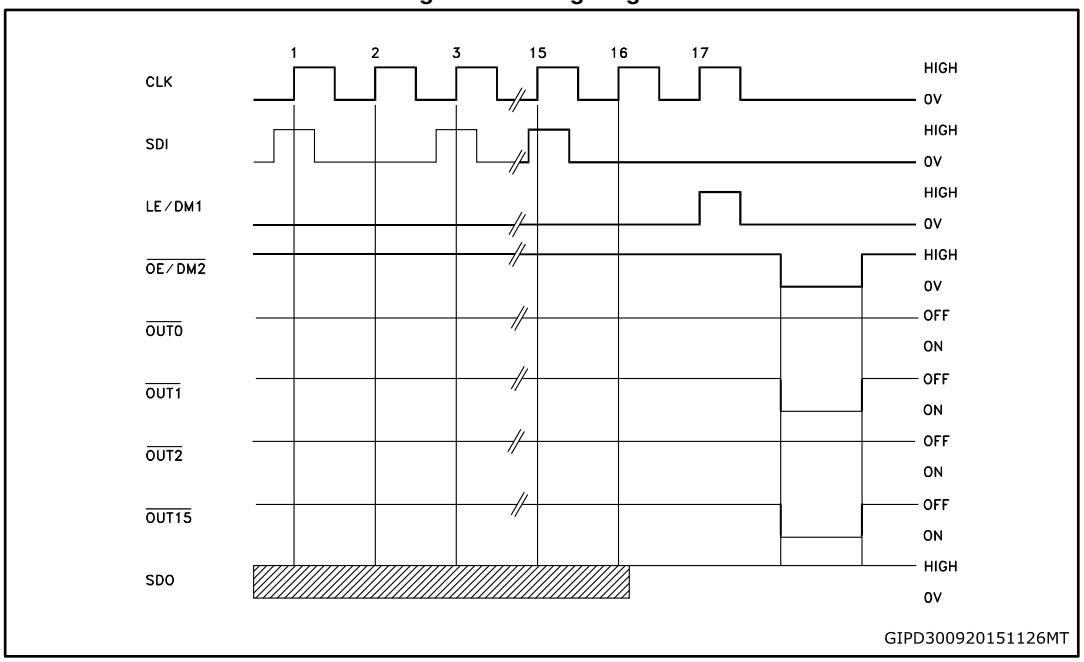
5 Timing diagrams

Table 9: Truth table

CLOCK	LE/DM1	$\overline{OE}$/DM2	SERIAL-IN	$\overline{OUT0}$ ..... $\overline{OUT7}$ ..... $\overline{OUT15}$	SDO
_|¯	H	L	Dn	Dn ..... Dn - 7 ..... Dn -15	Dn - 15
_|¯	L	L	Dn + 1	No change	Dn - 14
_|¯	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
¯|_	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
¯|_	X	H	Dn + 3	OFF	Dn - 13

OUTn = ON when Dn = H OUTn = OFF when Dn = L.

Figure 7: Timing diagram



1 Latch and output enable are level sensitive and ARE NOT synchronized with rising-or-falling edge of CLK signal.

2 When LE/DM1 terminal is low level, the latch circuits hold previous set of data.

3 When LE/DM1 terminal is high level, the latch circuits refresh new set of data from SDI chain.

4 When $\overline{OE}$/DM2 terminal is at low level, the output terminals - $\overline{Out0}$ to $\overline{Out15}$ respond to data in the latch circuits, either '1' for ON or '0' for OFF.

5 When $\overline{OE}$/DM2 terminal is at high level, all output terminals will be switched OFF.

Figure 8: Clock, serial-in, serial-out

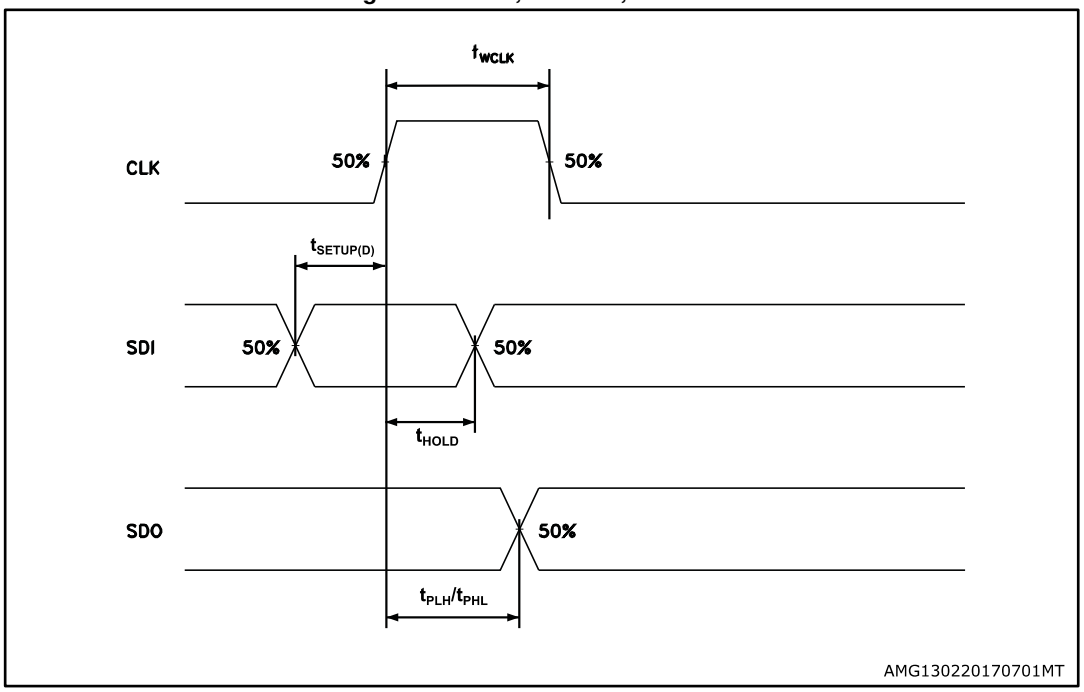


Figure 9: Clock, serial-in, latch, enable, outputs

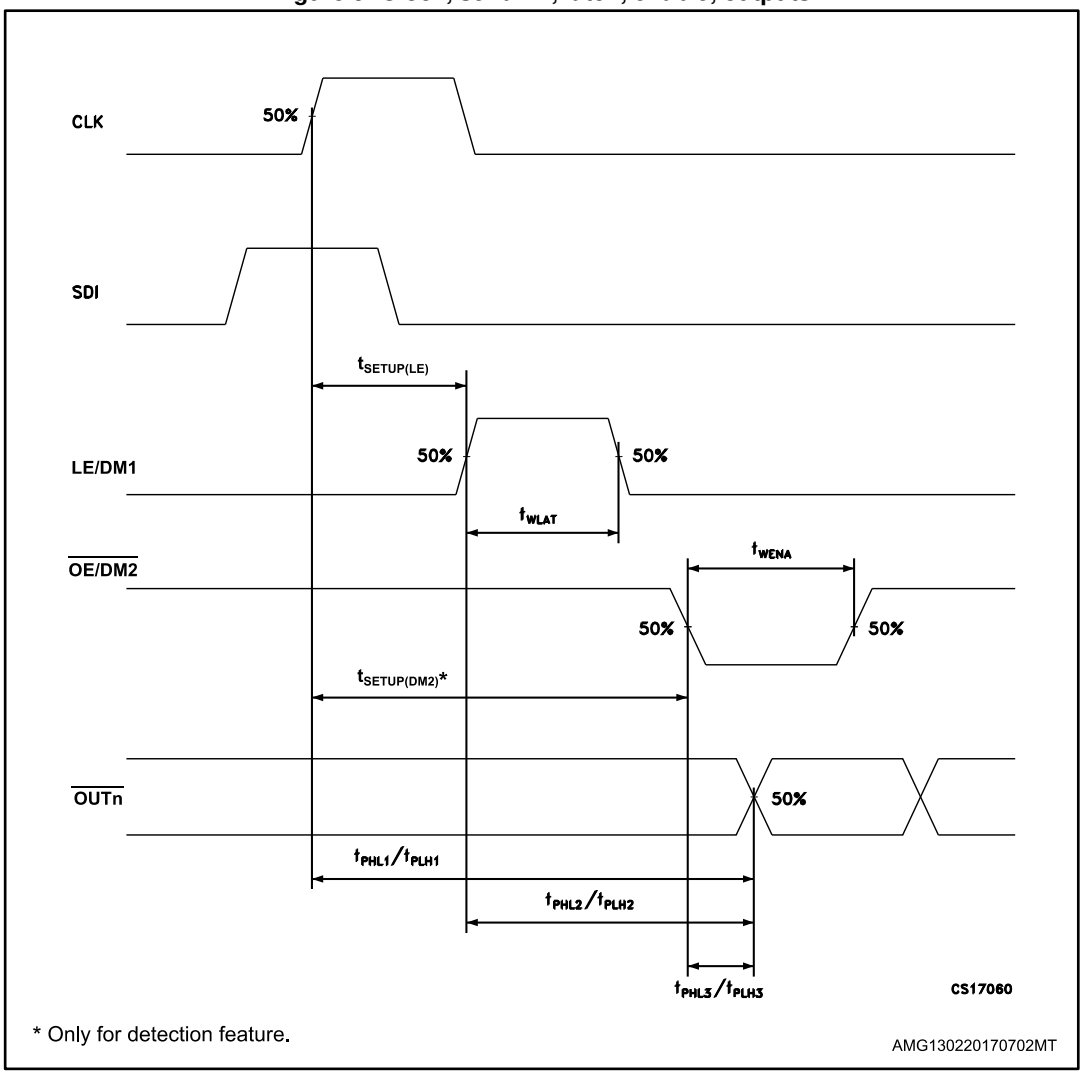
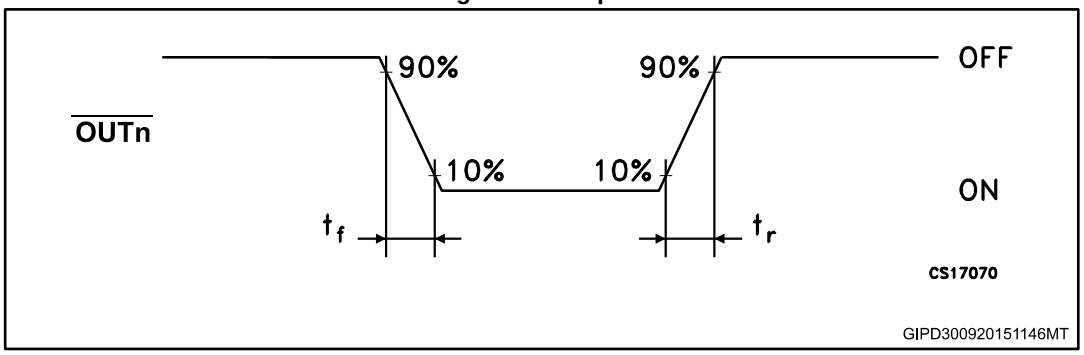


Figure 10: Outputs



6 Typical characteristics

Figure 11: Output current-R_{EXT} resistor

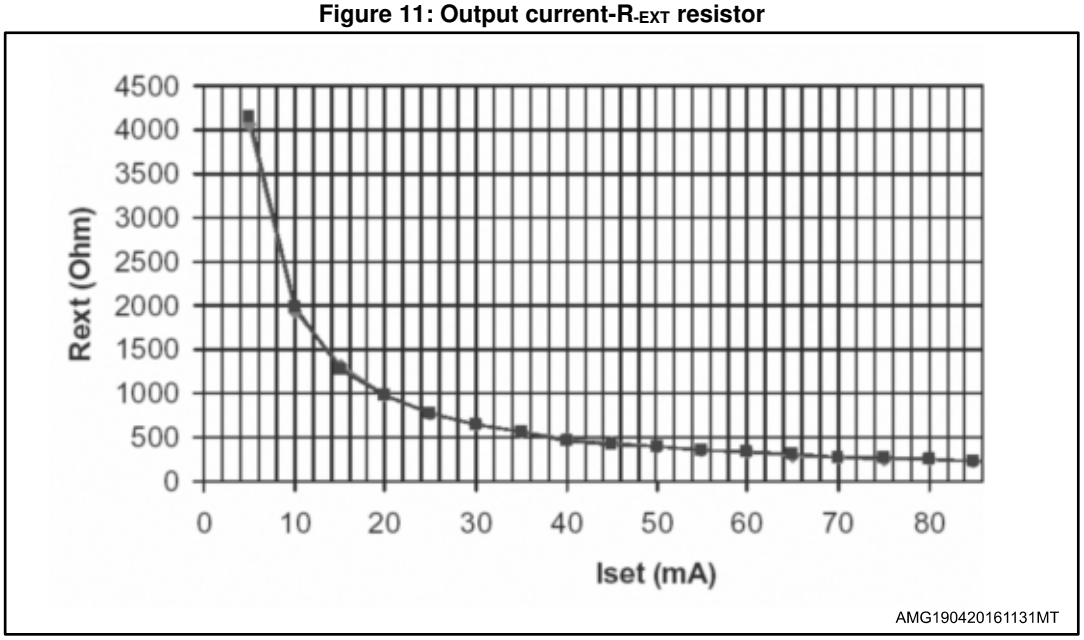


Table 10: Output current-R_{EXT} resistor

R_{EXT} (Ω)	Output current (mA)
976	20
780	25
652	30
560	35
488	40
433	45
389	50
354	55
325	60
300	65
278	70
259	75
241	80
229	85

Conditions:

temperature = 25 °C, V_{DD} = 3.3 V; 5.0 V, I_{SET} = 3 mA; 5 mA; 10 mA; 20 mA; 50 mA; 80 mA.

Figure 12: I_{SET} vs dropout voltage (V_{drop})

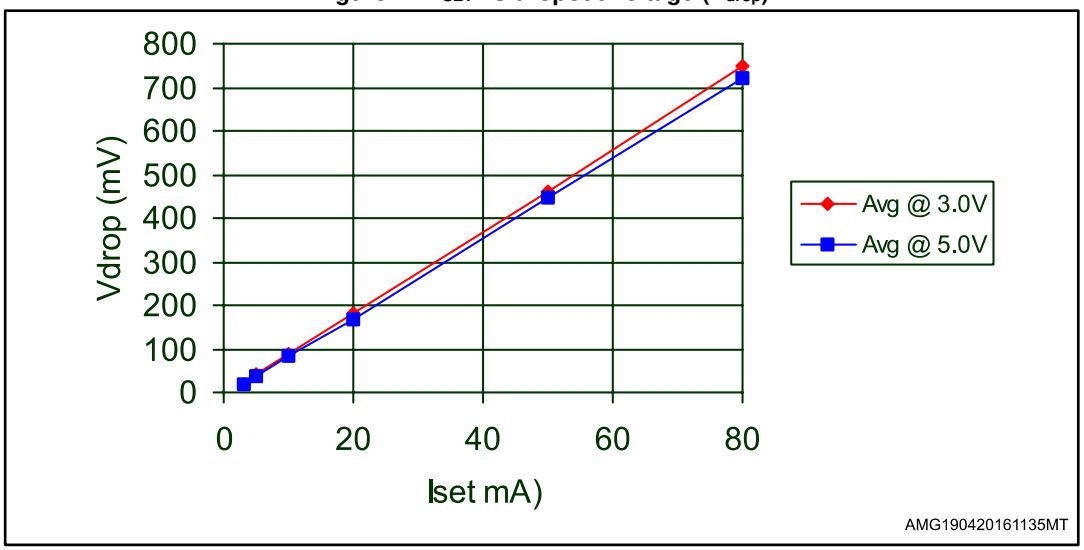
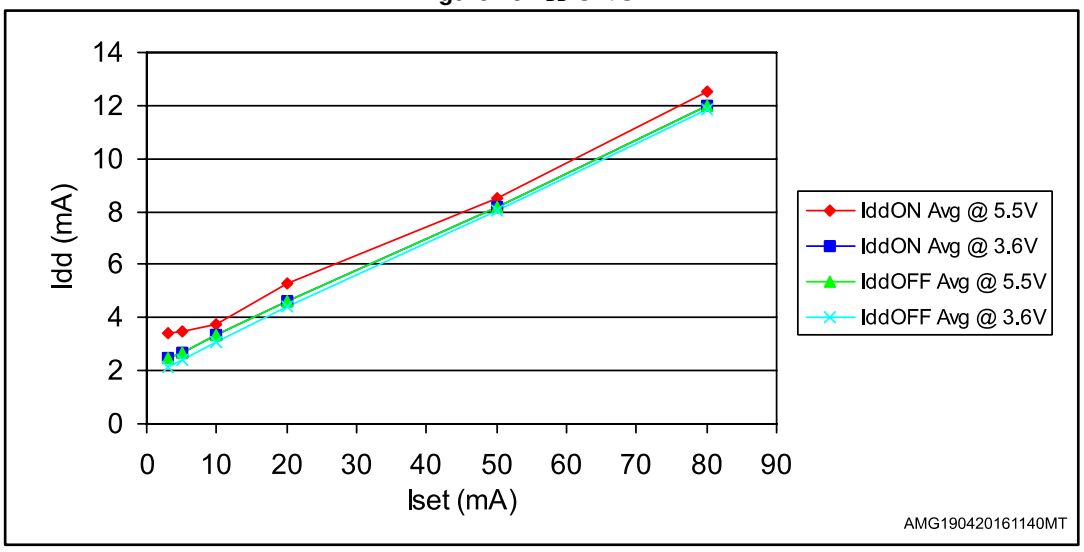


Table 11: I_{SET} vs dropout voltage (V_{drop})

Iout (mA)	Avg @ 3.0 V	Avg @ 5.0 V
3	19.33	22.66
5	36.67	40.33
10	77.33	80
20	158.67	157.33
50	406	406
80	692	668

Figure 13: I_{DD} ON/OFF



7 Detection mode functionality

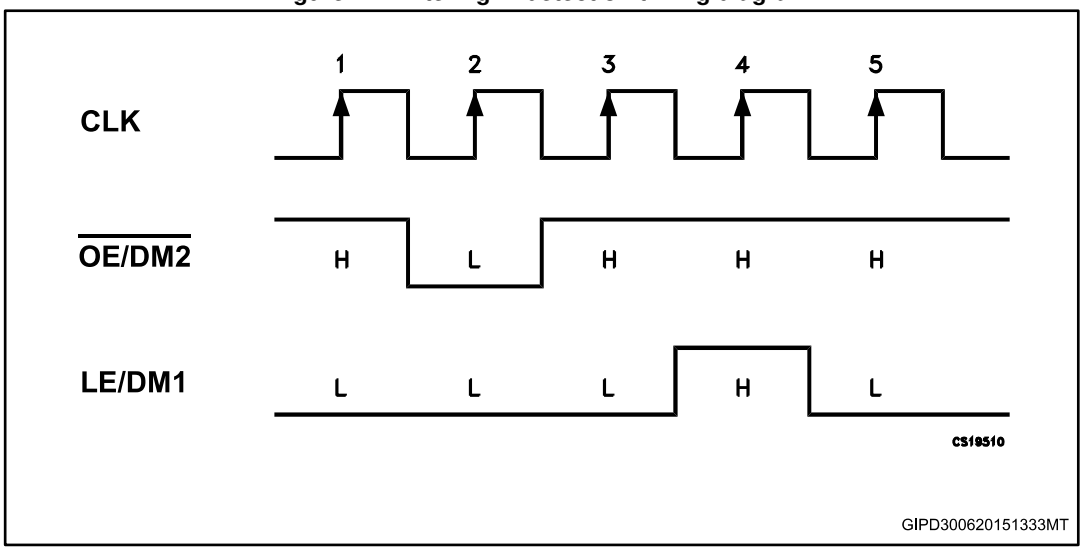
7.1 Phase one: “entering in detection mode“

From the “normal mode” condition the device can switch to the “error mode” by a logic sequence on the $\overline{\text{OE/DM2}}$ and LE/DM1 pins as showed in the following table and diagram:

Table 12: Entering in detection truth table

CLK	1°	2°	3°	4°	5°
$\overline{\text{OE/DM2}}$	H	L	H	H	H
LE/DM1	L	L	L	H	L

Figure 14: Entering in detection timing diagram

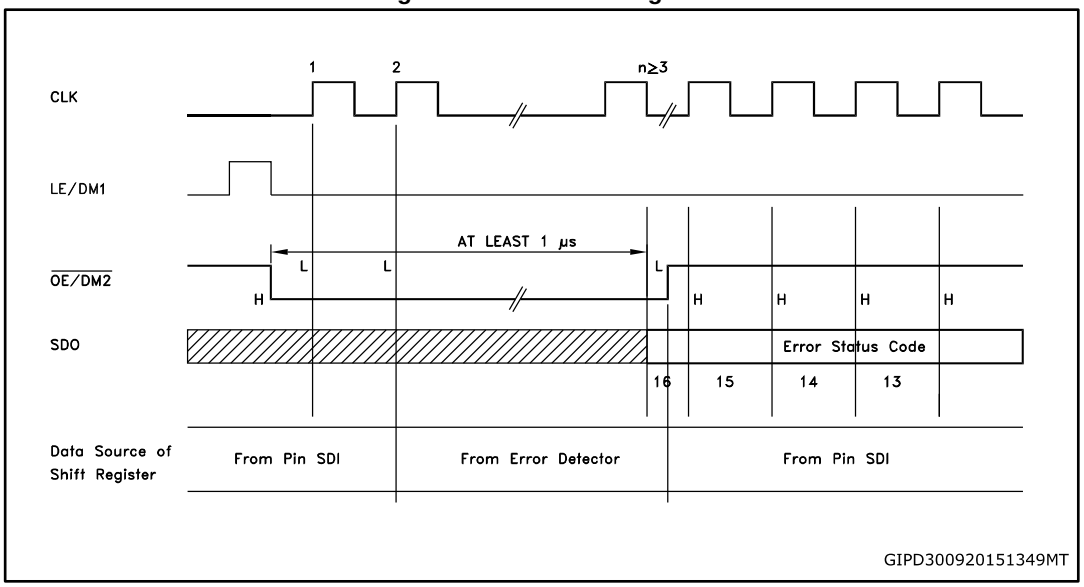


After these five CLK cycles the device goes into the “error detection mode” and at the 6th rise front of CLK the SDI data are ready for the sampling.

7.2 Phase two: “error detection”

The 16 data bits must be set “1” in order to set ON all the outputs during the detection. The data are latched by LE/DM1 and after that the outputs are ready for the detection process. When the microcontroller switches the $\overline{\text{OE/DM2}}$ to LOW, the device drives the LEDs in order to analyze if an OPEN or SHORT condition has occurred.

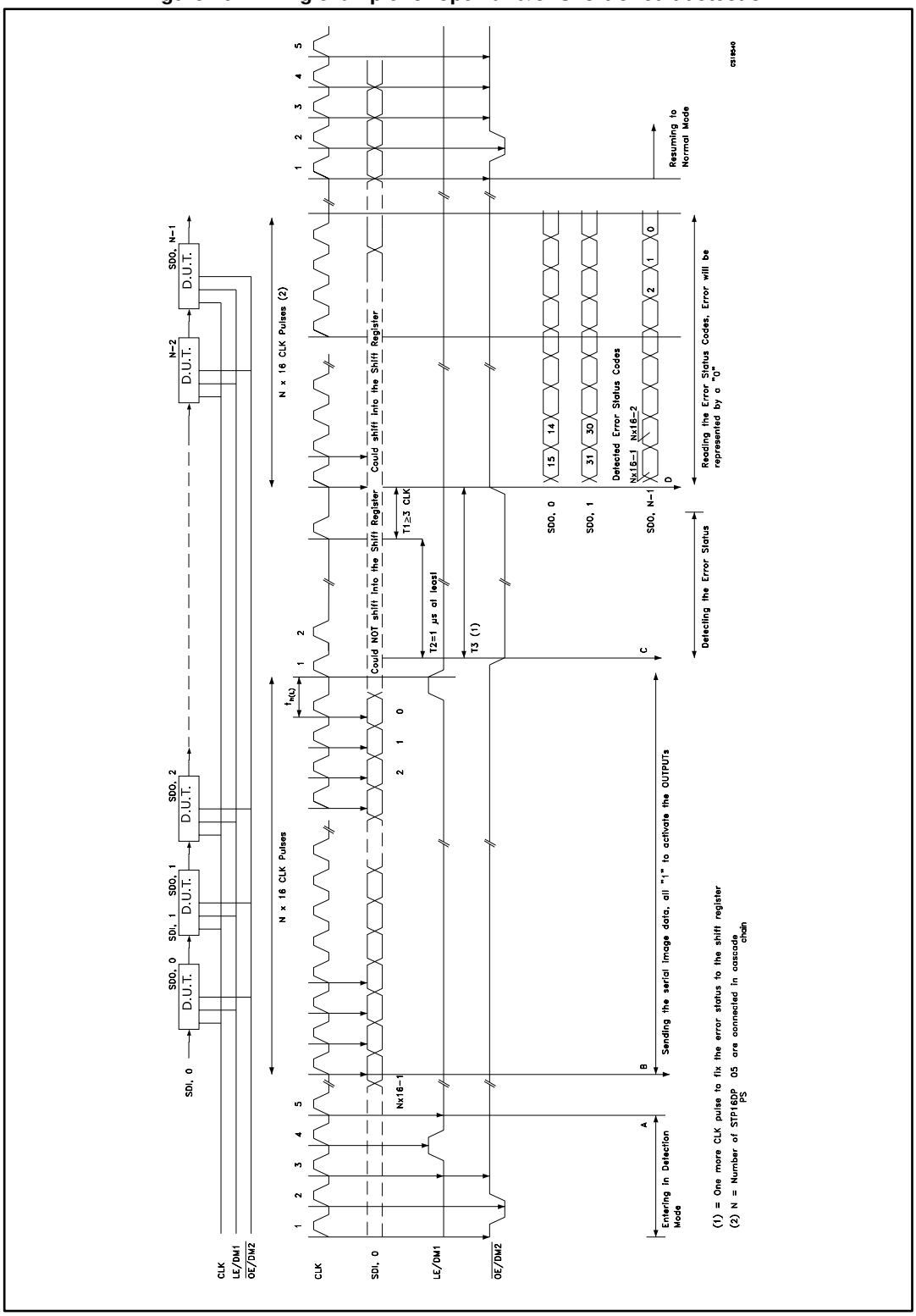
Figure 15: Detection diagram



The LEDs status will be detected at least in 1 microsecond and after this time the microcontroller sets $\overline{\text{OE/DM2}}$ in HIGH state and the output data detection result will go to the microprocessor via SDO.

Detection mode and normal mode use both the same format data. As soon as all the detection data bits are available on the serial line, the device may go back to normal mode of operation. To re-detect the status the device must go back in normal mode and reentering in error detection mode.

Figure 16: Timing example for open and/or short-circuit detection



7.3 Phase three: "resuming normal mode"

The sequence for reentering normal mode is shown in the following table:

Table 13: Resuming to normal mode timing diagram

CLK	1°	2°	3°	4°	5°
$\overline{OE}$/DM2	H	L	H	H	H
LE/DM1	L	L	L	L	L



For proper device operation the “Entering in detection” sequence must be follow by a “resume mode” sequence, it is not possible to insert consecutive equal sequence.

7.4 Error detection conditions

V_{DD} = 3.3 to 5 V temperature range -40 to 125 °C.

Table 14: Detection conditions

Configuration	Detect mode	Detection results		
SW-1 or SW-3b	Open line or output short to GND detected	==> $I_{ODEC} \leq 0.5 \times I_O$	No error detected	==> $I_{ODEC} \geq 0.5 \times I_O$
SW-2 or SW-3a	Short on LED or short to V-LED detected	==> $V_O \geq 2.4$ V	No error detected	==> $V_O \leq 2.2$ V



Where: I_O = the output current programmed by the R_{EXT}, I_{ODEC} = the detected output current in detection mode.

Figure 17: Detection circuit

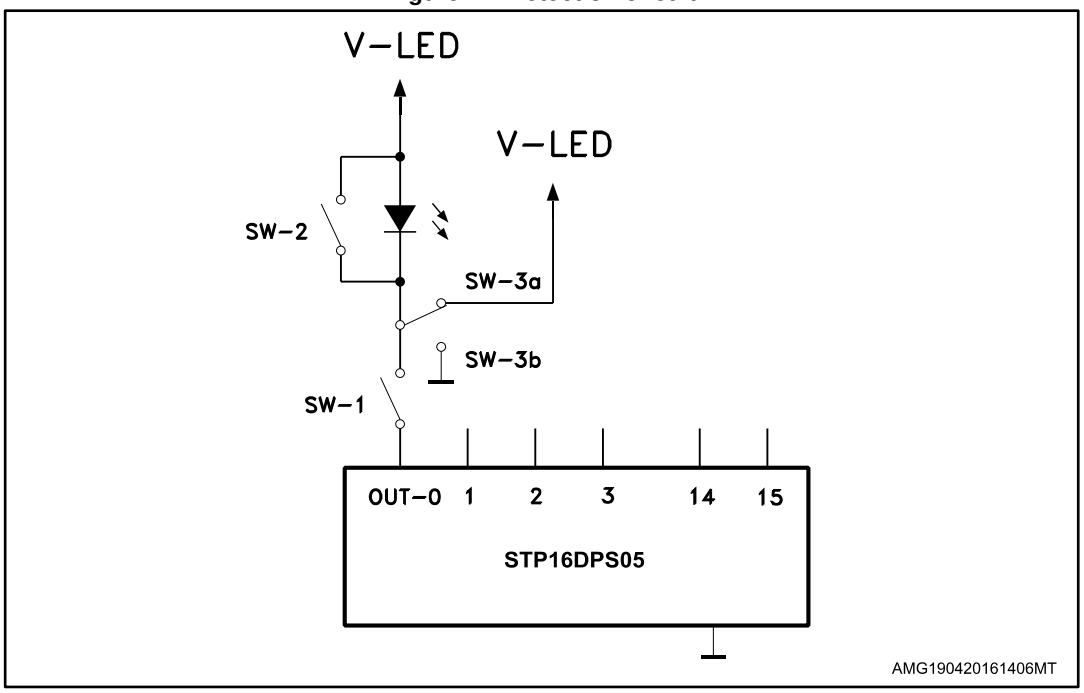
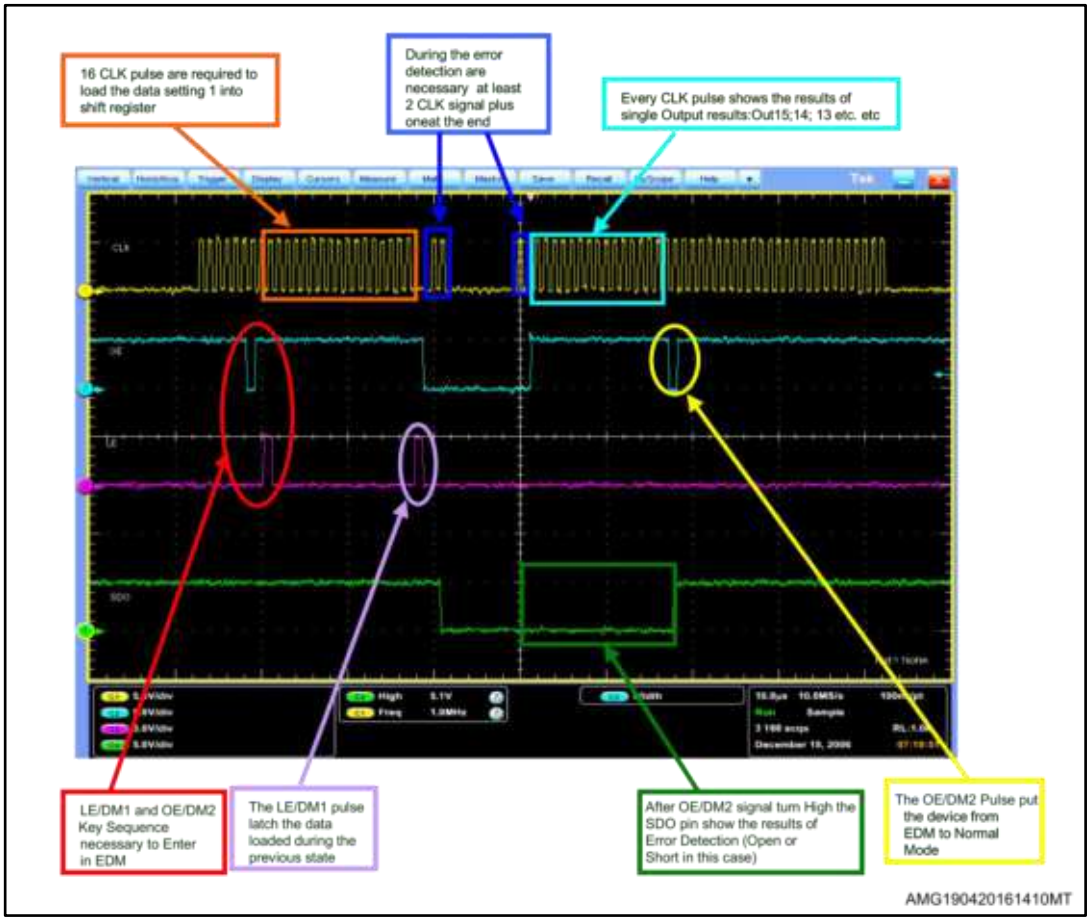
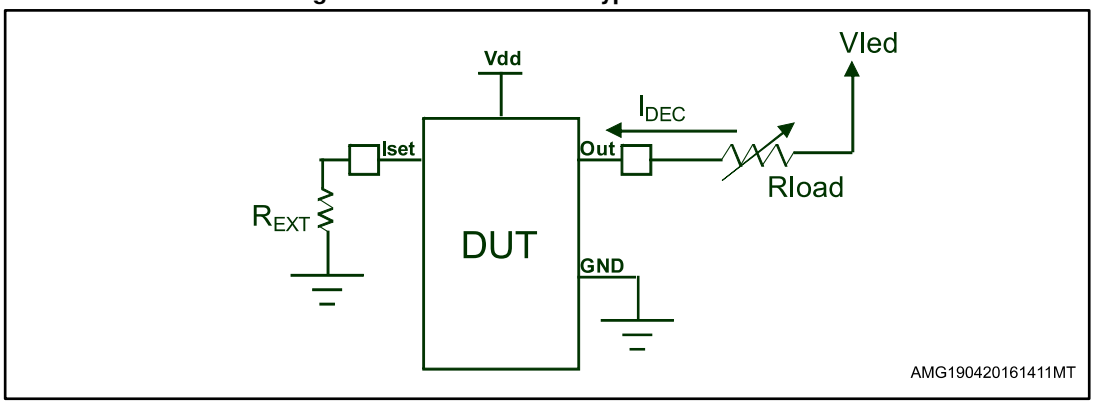


Figure 18: Error detection sequence



Typical schematic used to perform the error detection:

Figure 19: Error detection typical schematic



Using the follow formula is possible measure the Iodec.

I_{ODEC} = (Vled-Vload) / Rload.

The tables below shows the I_{ODEC} average value at 3.3 V and 5.0 V of power supply voltage.

The I_{ODEC} is the current value recognized by the devices output open error detection.

Table 15: I_{ODEC} average value at 3.3 V

Vdd (V)	Iset (mA)	R_{ext} (Ω)	Iout AVG (mA)
3.3	5	4270	2.097
	10	2056	6.79
	20	1006	10.46
	50	382	26.92
	80	251	35.03

Table 16: I_{ODEC} average value at 5 V

Vdd (V)	Iset (mA)	R_{ext} (Ω)	Iout AVG (mA)
5	5	4270	1.98
	10	2056	6.09
	20	1006	9.67
	50	382	25.54
	80	251	38.9

7.5 Auto power-saving

The auto power-saving feature minimizes the quiescent current if no active data is detected on the latches and auto powers-up the device as the first active data is latched.

Figure 20: Auto power-saving feature



Conditions:

Temp. = 25 °C, Vdd = 3.3 V, Vin = Vdd, VLed = 3.0 V, Iset = 20 mA

Ch1 (Yellow) = IDD, Ch2 (Blue) = SDI, Ch3 (Purple) = LE/DM1, Ch4 (Green) = CLK

Idd consumption:

Idd (normal operation) = 5.15 mA

pIdd (shutdown condition) = 163 µA

Figure 21: Delay LE-OUT



After 16 clock cycles without data change, device will enter in Auto power save mode as expected. Delay TLE-OUT = 1.053 µs

Conditions:

Temp. = 25 °C, Vdd = 3.3 V, Vin = Vdd, VLed = 3.0 V, Iset = 20 mA

Ch1 (Yellow) = CLK, Ch2 (Blue) = SDI, Ch3 (Purple) = LE/DM1, Ch4 (Green) = IOUT

Figure 22: Behaviour auto power saving



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When the device goes from auto power-saving to normal operating condition, the first output that switches ON shows the TON condition as seen in the plot above.

Temp. = 25°C, Vdd = 3.3 V, Vin = Vdd, VLed = 3.0 V, Iset = 20 mA

Ch1 (Yellow) = IDD, Ch2 (Blue) = SDI, Ch3 (Purple) = LE/DM1, Ch4 (Green) = CLK

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

8.1 QSOP-24 package information

Figure 23: QSOP-24 package outline

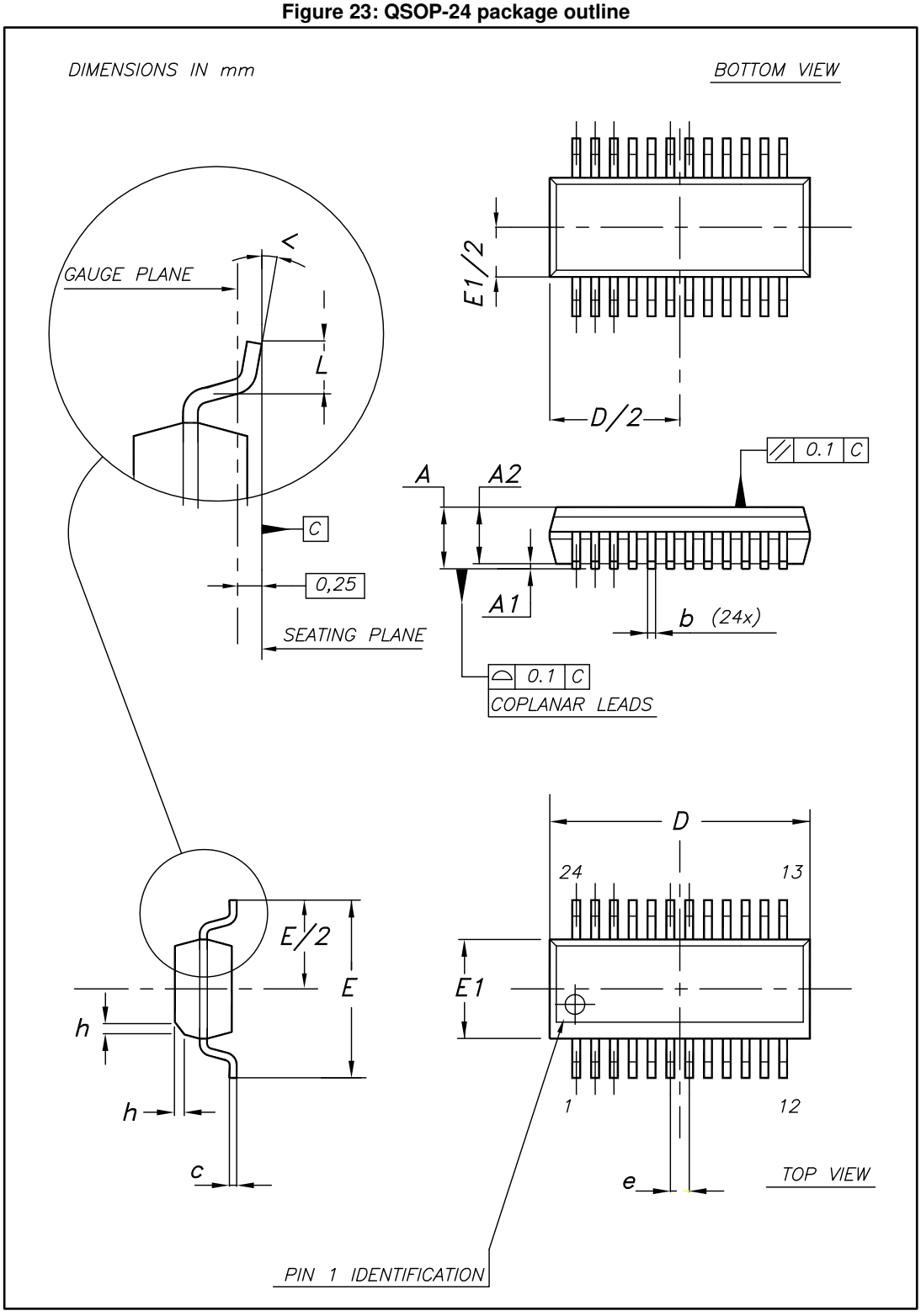


Table 17: QSOP-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.54	1.62	1.73
A1	0.10	0.15	0.25
A2		1.47	
b	0.20		0.31
c	0.17		0.254
D	8.56	8.66	8.76
E	5.80	6.00	6.20
E1	3.80	3.91	4.01
e		0.635	
L	0.40	0.635	0.89
h	0.25	0.33	0.41
<	0°		8°

8.2 TSSOP24 package information

Figure 24: TSSOP24 package outline

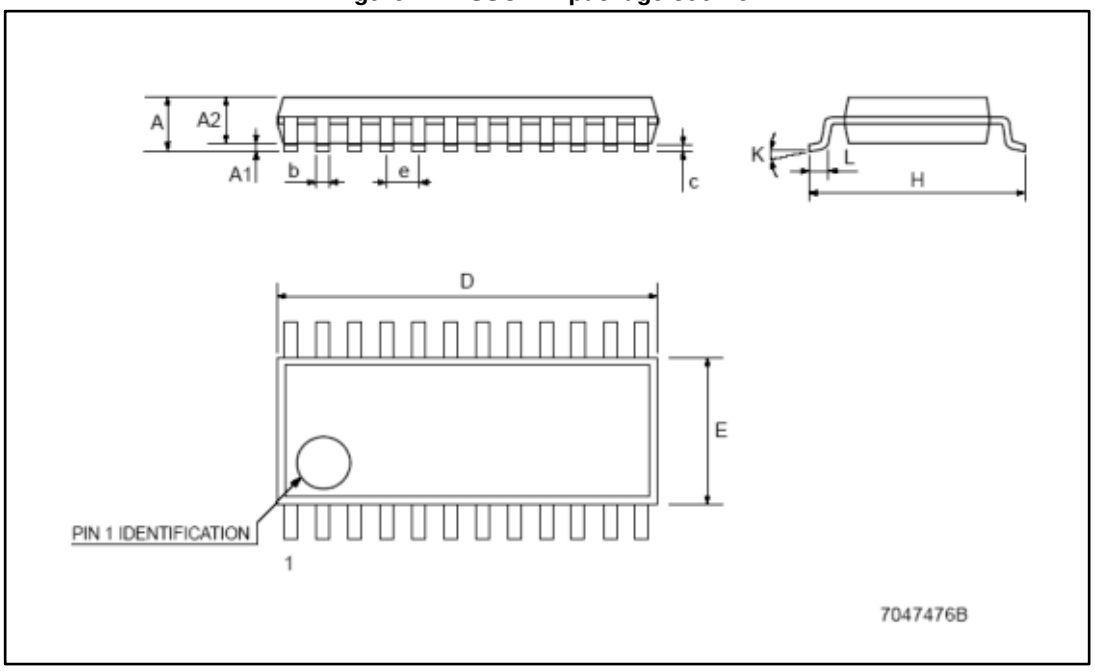


Table 18: TSSOP24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.1
A1	0.05		0.15
A2		0.9	
b	0.19		0.30
c	0.09		0.20
D	7.7		7.9
E	4.3		4.5
e		0.65 BSC	
H	6.25		6.5
K	0°		8°
L	0.50		0.70

8.3 SO-24 package information

Figure 25: SO-24 package outline

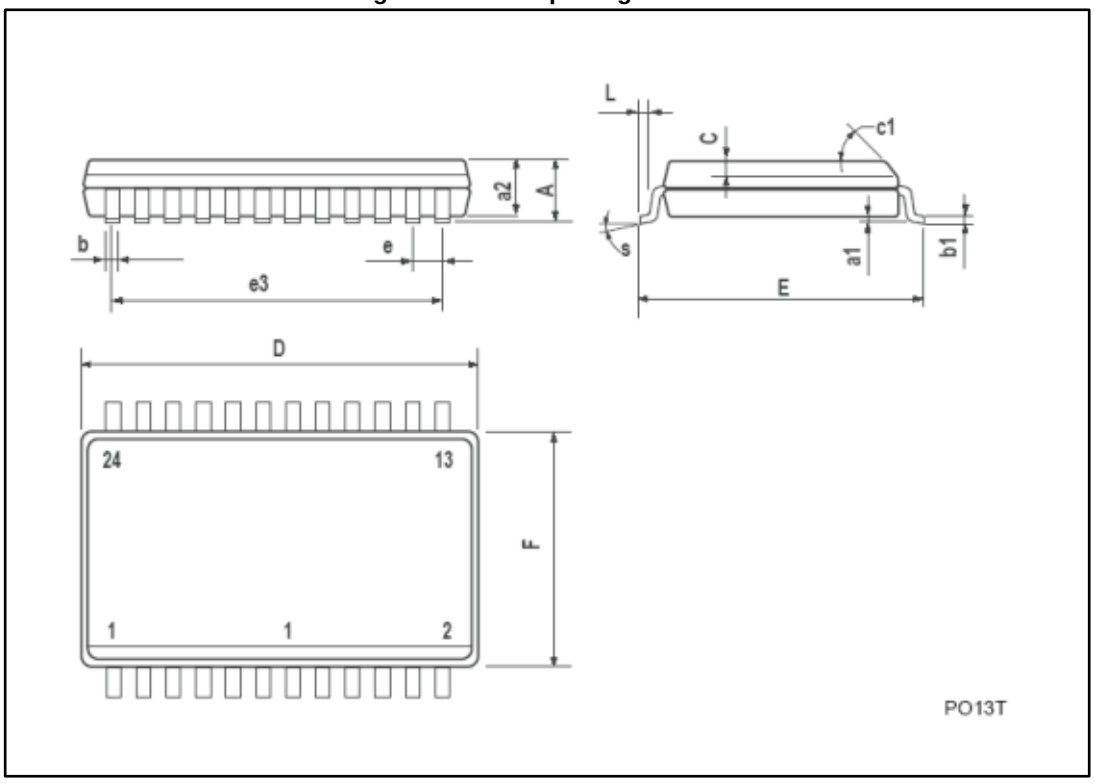


Table 19: SO-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			2.65
a1	0.1		0.2
a2			2.45
b	0.35		0.49
b1	0.23		0.32
C		0.5	
c1	45° (typ.)		
D	15.20		15.60
E	10.00		10.65
e		1.27	
e3		13.97	
F	7.40		7.60
L	0.50		1.27
S	°(max.) 8		

8.4 TSSOP exposed pad package information

Figure 26: TSSOP24 exposed pad package outline

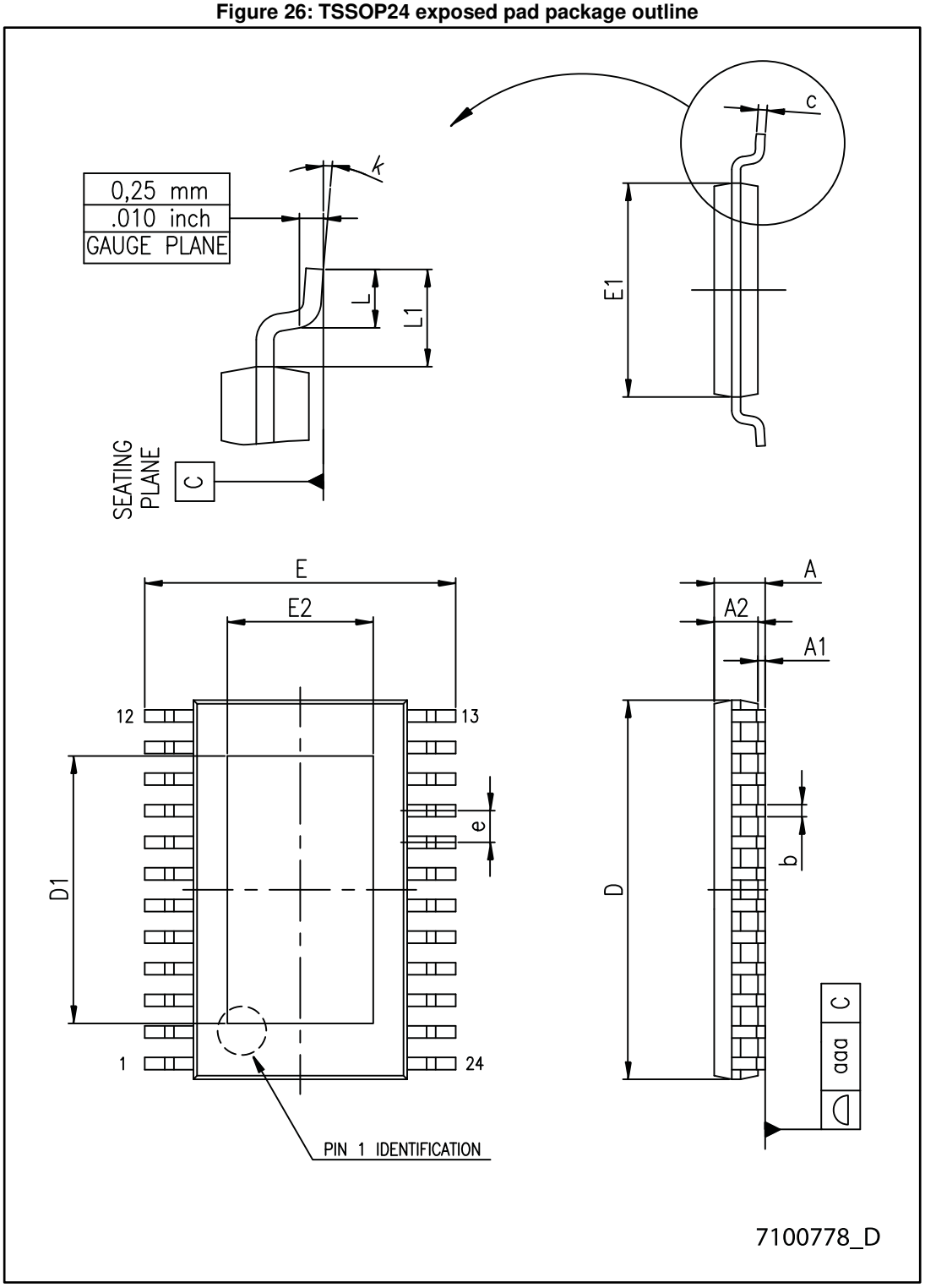


Table 20: TSSOP24 exposed pad mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
D1	4.80	5.00	5.2
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	3.00	3.20	3.40
e		0.65	
L	0.45	060	075
L1		1.00	
k	0°		8°
aaa			0.10

8.5 TSSOP24, TSSOP24 exposed pad and SO-24 packing information

Figure 27: TSSOP24, TSSOP24 exposed pad and SO-24 reel outline

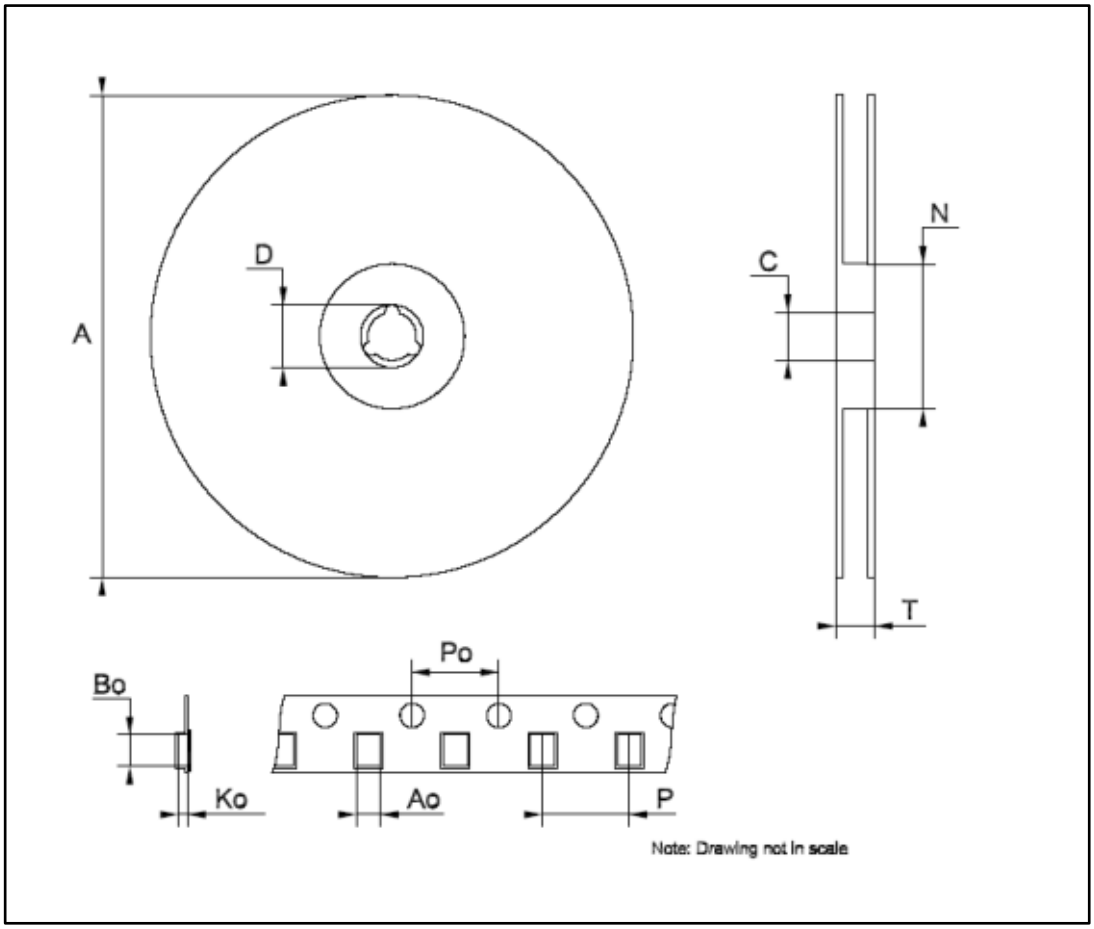


Table 21: TSSOP24 and TSSOP24 exposed pad tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	22.4
Ao	6.8	-	7
Bo	8.2	-	8.4
Ko	1.7	-	1.9
Po	3.9	-	4.1
P	11.9	-	12.1

Table 22: SO-24 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	30.4
Ao	10.8	-	11.0
Bo	15.7	-	15.9
Ko	2.9	-	3.1
Po	3.9	-	4.1
P	11.9	-	12.1

9 Revision history

Table 23: Document revision history

Date	Revision	Changes
23-Oct-2009	1	First release
22-Jan-2010	2	Updated Table 5 on page 4
13-Apr-2017	3	Updated features in cover page, *Figure 5: "SDO terminal"*, *Figure 8: "Clock, serial-in, serial-out"*, *Figure 9: "Clock, serial-in, latch, enable, outputs"* and *Section 8.1: "QSOP-24 package information"*. Minor text changes.

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