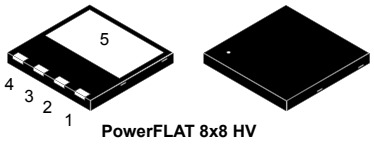
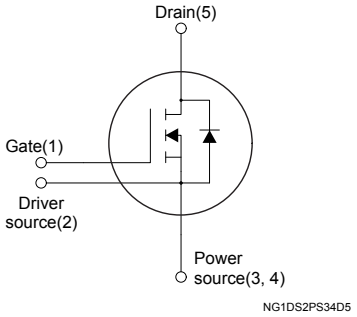
N-channel 650 V, 175 mΩ typ., 17 A MDmesh M5 Power MOSFET in a PowerFLAT 8x8 HV package



PowerFLAT 8x8 HV



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL21N65M5	650 V	190 mΩ	17 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance thanks to the extra driving source pin
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Product status link
STL21N65M5

Product summary	
Order code	STL21N65M5
Marking	21N65M5
Package	PowerFLAT 8x8 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	17	A
	Drain current (continuous) at T_C = 100 °C	11	
I_{DM}(1)	Drain current (pulsed)	68	A
P_{TOT}	Total power dissipation at T_C = 25 °C	125	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 17 A, di/dt ≤ 400 A/µs, V_{DD} = 400 V, V_{DS} (peak) < $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1	°C/W
R_{thJA}(1)	Thermal resistance, junction-to-ambient	45	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	400	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C (1)			100	
I_{GSS}	Gate body leakage current	V_{GS} = ±25 V, V_{DS}= 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 8.5 A		175	190	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1950	-	pF
C_{oss}	Output capacitance		-	46	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{o(tr)}$ (1)	Equivalent output capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	133	-	pF
$C_{o(er)}$ (2)	Equivalent output capacitance energy related		-	44	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	2.5	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 8.5 A, V_{GS} = 0 to 10 V (see Figure 15. Gate charge test circuit)	-	44	-	nC
Q_{gs}	Gate-source charge		-	12	-	nC
Q_{gd}	Gate-drain charge		-	17	-	nC

1. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*
2. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 11 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	37	-	ns
$t_{r(v)}$	Voltage rise time		-	10	-	ns
$t_{f(i)}$	Current fall time		-	12	-	ns
$t_{c(off)}$	Crossing time		-	24	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17	A
I_{SDM}(1)	Source-drain current (pulsed)		-		68	A
V_{SD}(2)	Forward on voltage	I_{SD} = 17 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/µs,	-	294		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	4		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	28		A
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/µs,	-	340		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_J = 150 °C	-	5		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	29		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

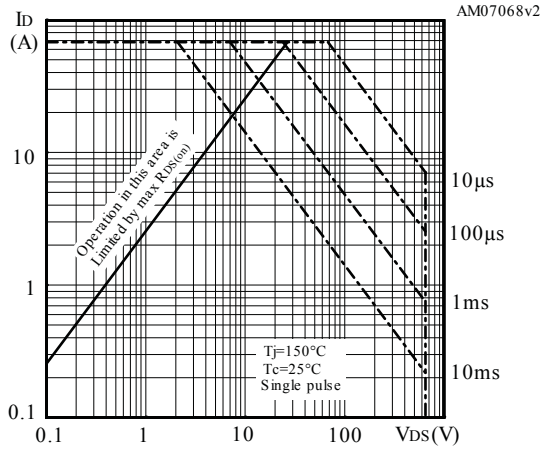


Figure 2. Normalized transient thermal impedance

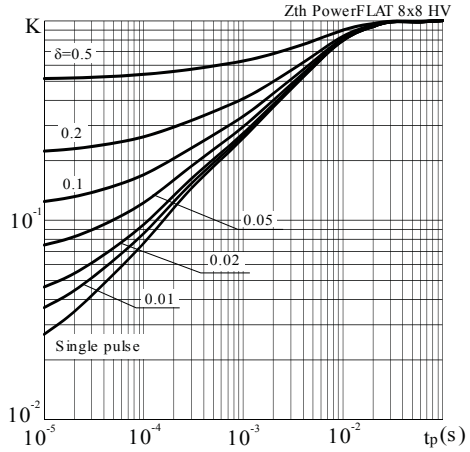


Figure 3. Typical output characteristics

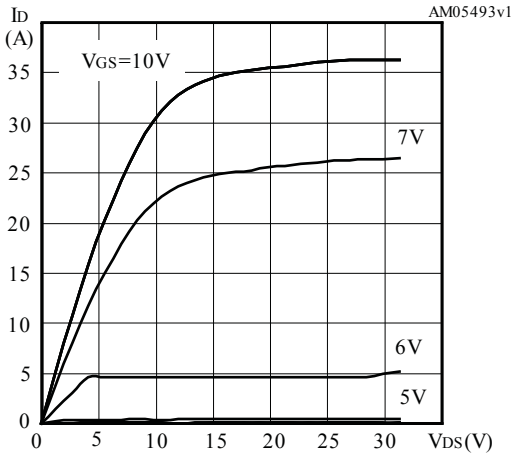


Figure 4. Typical transfer characteristics

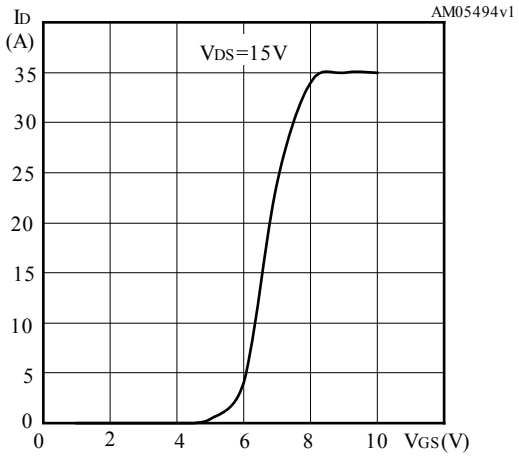


Figure 5. Typical gate charge characteristics

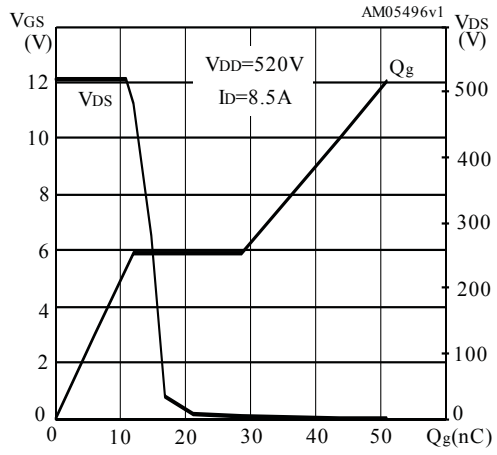


Figure 6. Typical drain-source on-resistance

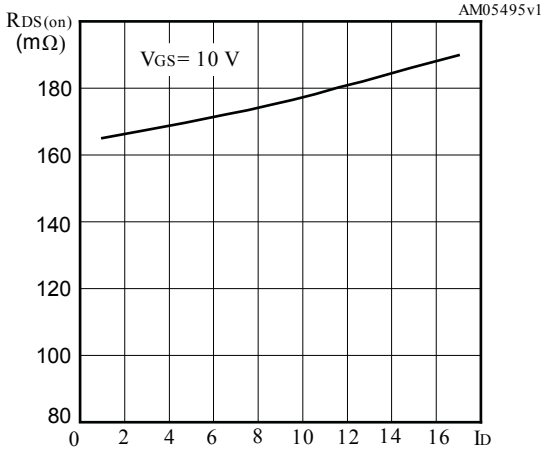


Figure 7. Typical capacitance characteristics

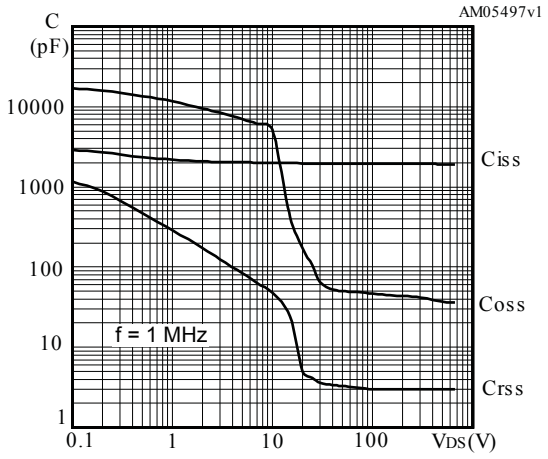


Figure 8. Typical output capacitance stored energy

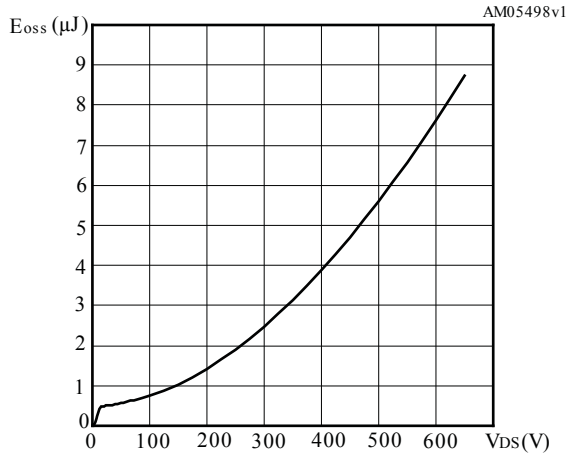


Figure 9. Normalized gate threshold vs temperature

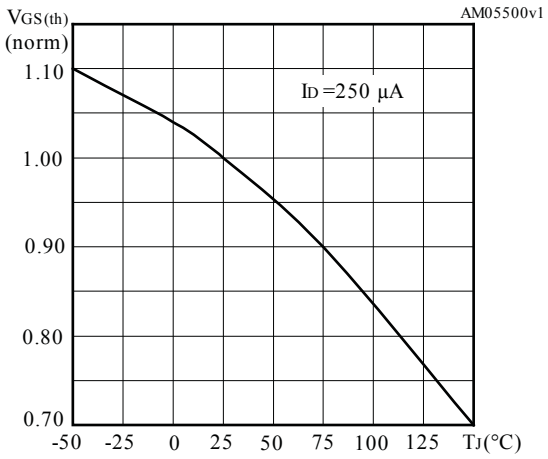


Figure 10. Normalized on-resistance vs temperature

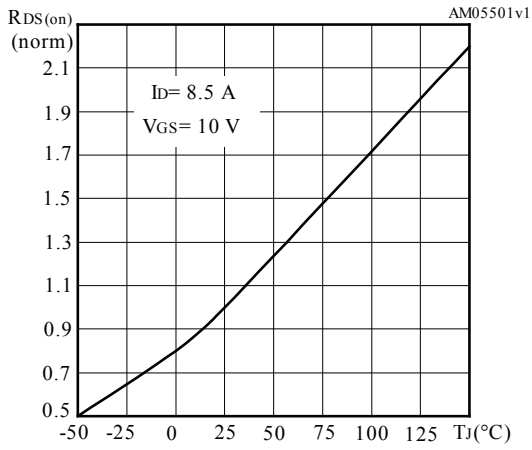


Figure 11. Typical reverse diode forward characteristics

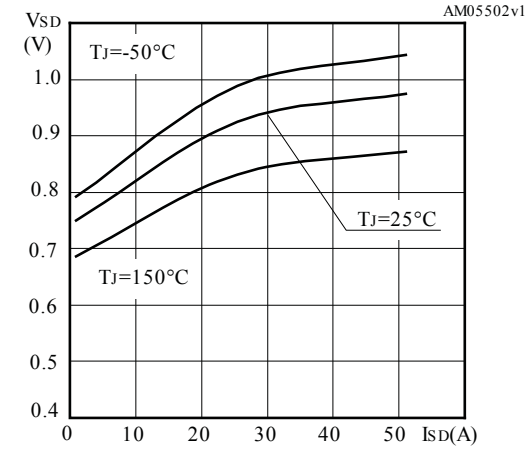


Figure 12. Normalized breakdown voltage vs temperature

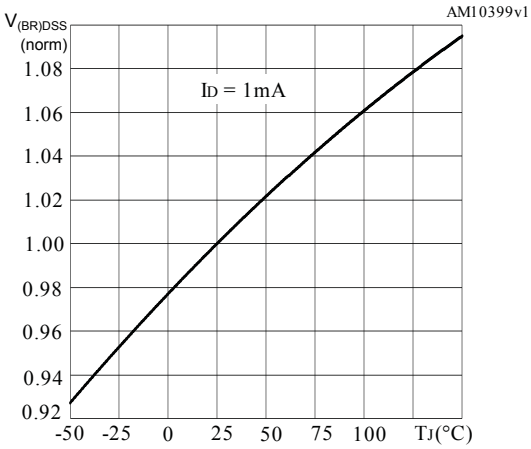
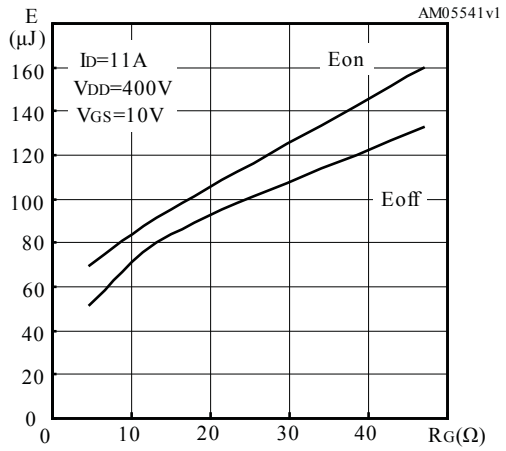


Figure 13. Typical inductive load switching energy vs gate resistance



Note: E_{on} including reverse recovery of a SiC diode.

3 Test circuits

Figure 14. Switching times test circuit for resistive load

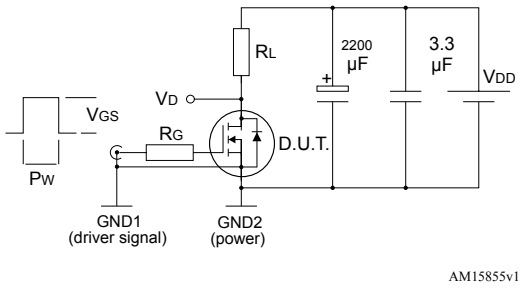


Figure 15. Gate charge test circuit

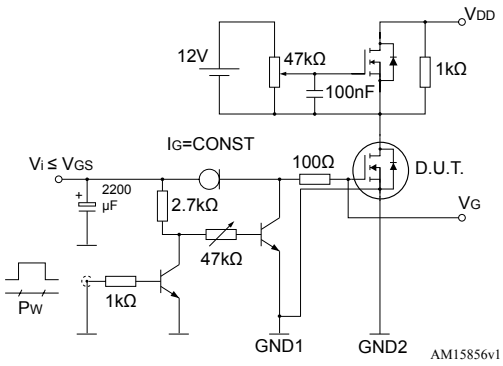


Figure 16. Test circuit for inductive load switching and diode recovery times

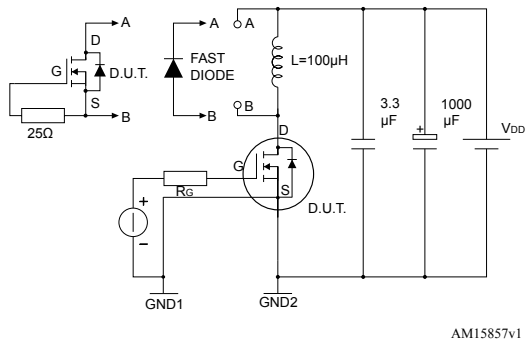


Figure 17. Unclamped inductive load test circuit

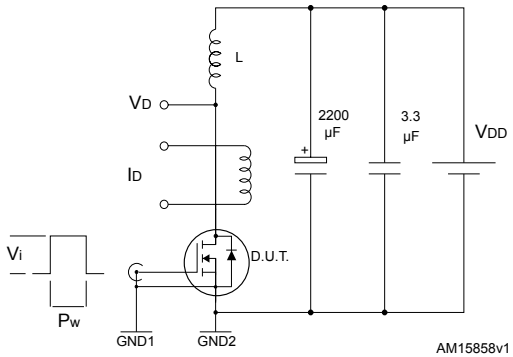


Figure 18. Unclamped inductive waveform

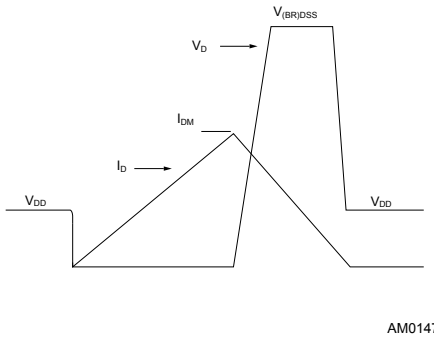
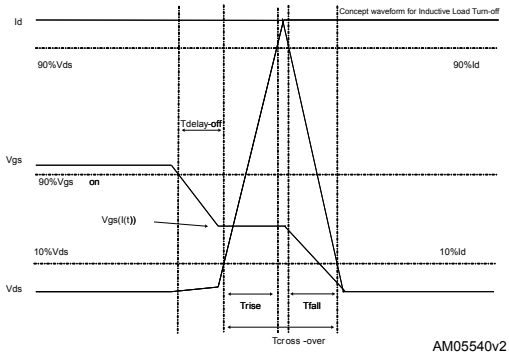


Figure 19. Switching time waveform



4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 8x8 HV type A package information

Figure 20. PowerFLAT 8x8 HV type A package outline

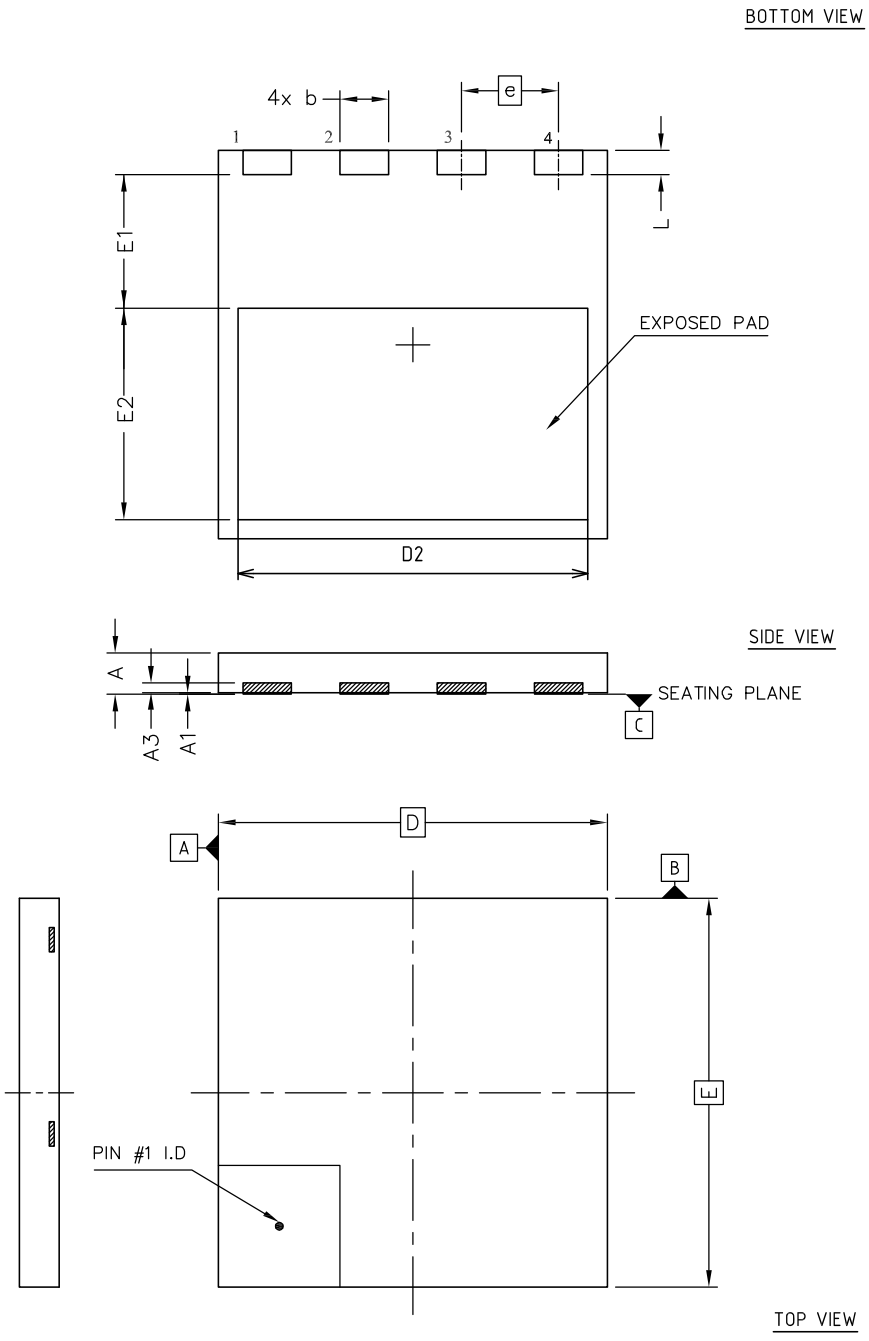
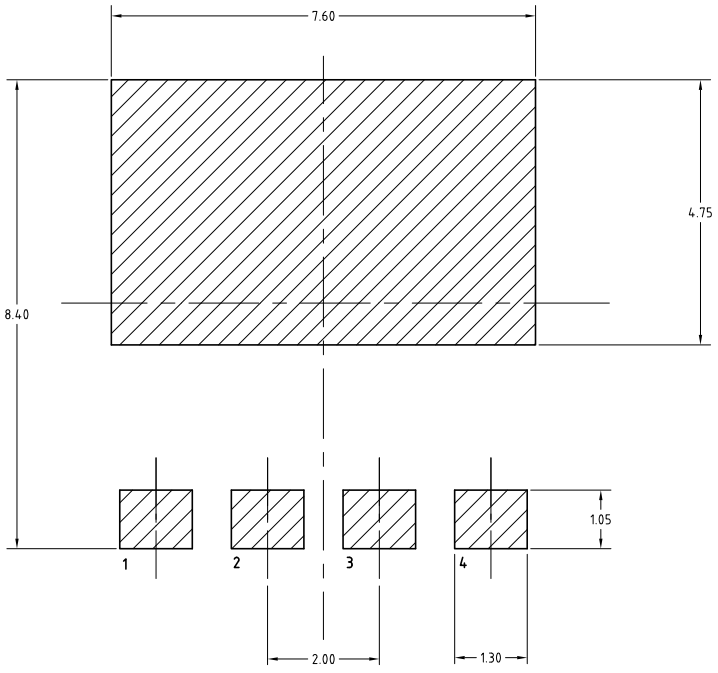


Table 8. **PowerFLAT 8x8 HV type A mechanical data**

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00 BSC	
L	0.40	0.50	0.60

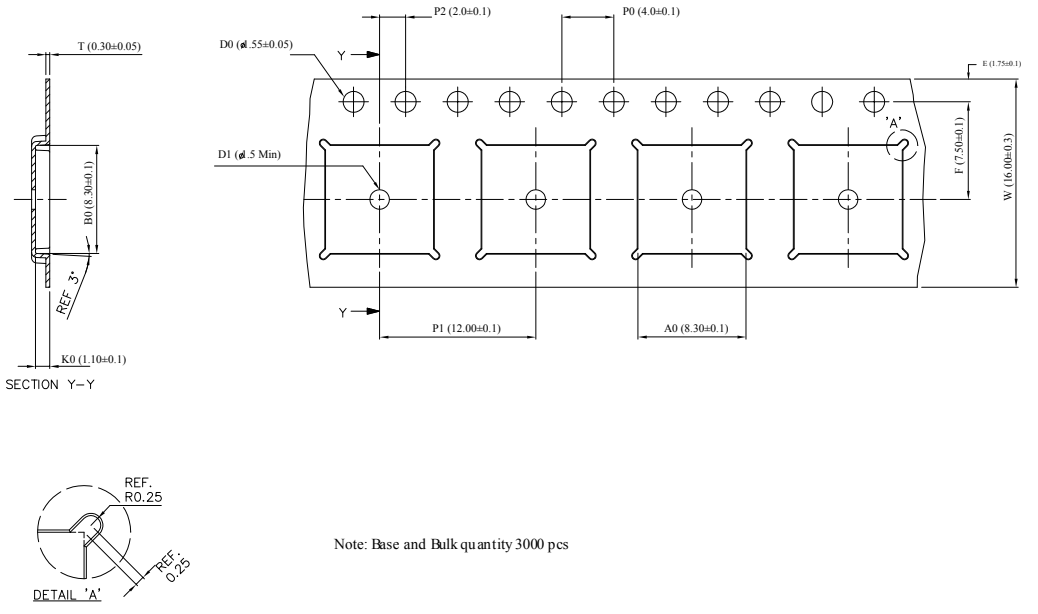
Figure 21. **PowerFLAT 8x8 HV footprint**



Note: All dimensions are in millimeters.

4.2 PowerFLAT 8x8 HV packing information

Figure 22. **PowerFLAT 8x8 HV tape**



Note: All dimensions are in millimeters.

Figure 23. **PowerFLAT 8x8 HV package orientation in carrier tape**

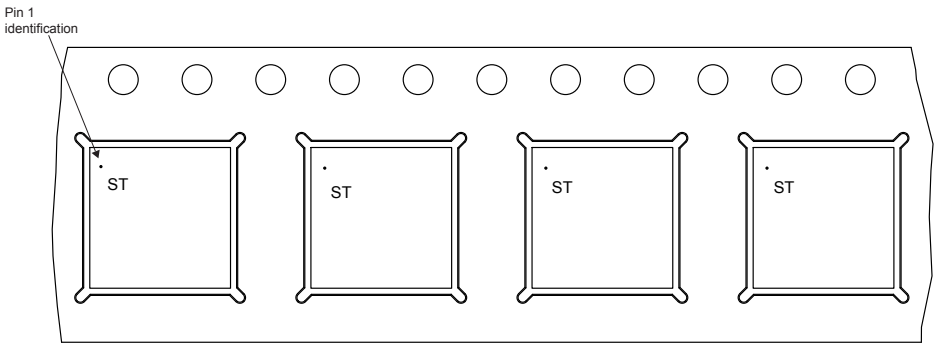
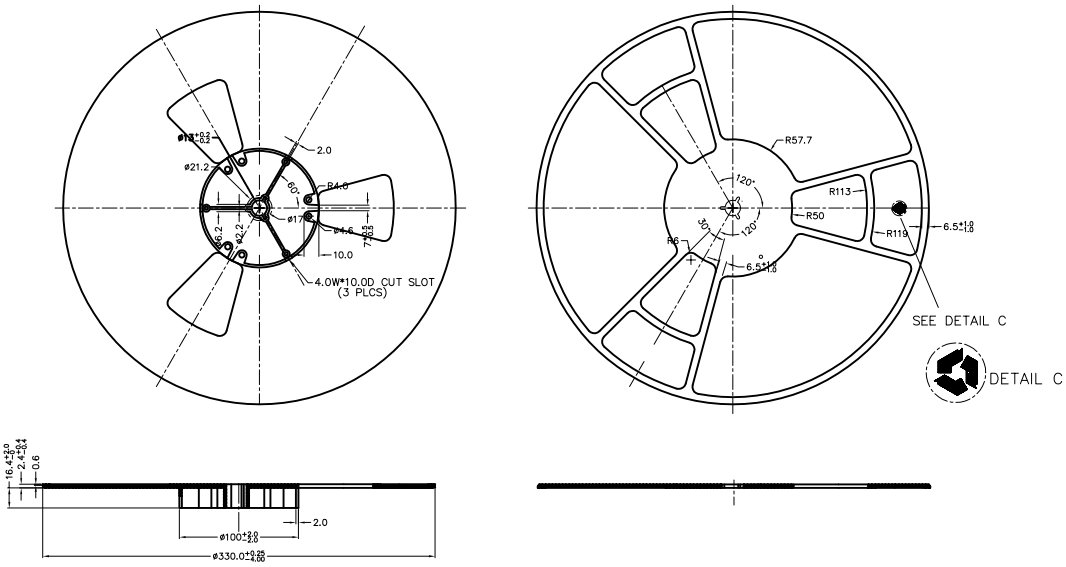


Figure 24. **PowerFLAT 8x8 HV reel**



Note: All dimensions are in millimeters.

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
28-Apr-2010	1	First release.
14-Jun-2010	2	$R_{DS(on)}$ typical value has been corrected.
14-Mar-2011	3	*Figure 2: Safe operating area*, *Figure 3: Thermal impedance* and *Figure 7: Static drain-source on-resistance* have been updated.
14-Mar-2011	4	$R_{DS(on)}$ limits in *Table 4* have been updated.
29-May-2011	5	*Section 4: Package mechanical* data has been updated. Added new section: *Section 5: Packaging mechanical data*. Minor text changes.
04-Nov-2024	6	Updated schematic on cover page. Updated Section 4.1: PowerFLAT 8x8 HV type A package information. Minor text changes.

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