STL140N4LLF5

N-channel 40 V, 2.2 mΩ typ., 32 A STripFET™ F5 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

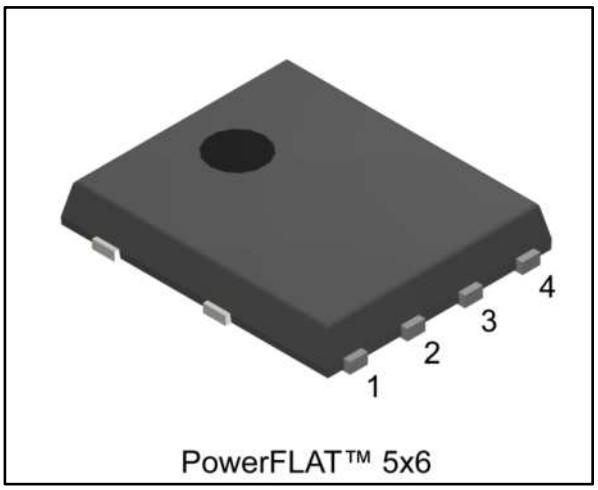
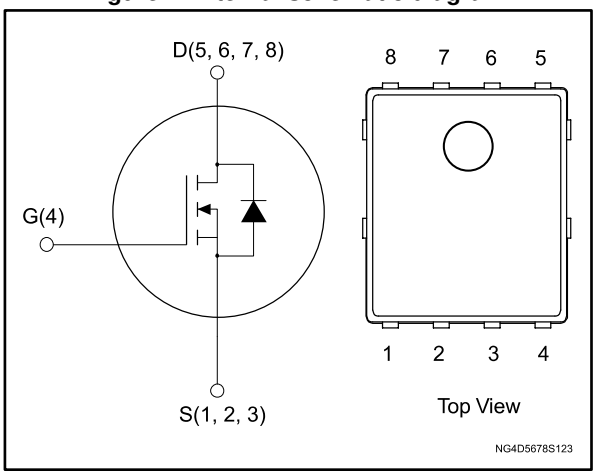


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL140N4LLF5	40 V	2.75 mΩ	32 A

- Low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This N-channel Power MOSFET is developed using the STripFET™ F5 technology and has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1: Device summary

Order code	Marking	Package	Packing
STL140N4LLF5	140N4LF5	PowerFLAT™ 5x6	Tape and reel

This is information on a product in full production.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±22	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	140	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	88	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	32	A
I_D (2)	Drain current (continuous) at T_{pcb} = 100 °C	20	A
I_{DM} (3)	Drain current (pulsed)	128	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	80	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25 °C	4	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)This value is rated according to $R_{thj\text{-}case}$.

(2)This value is rated according to $R_{thj\text{-}pcb}$.

(3)Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.56	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.3	°C/W

Notes:

(1)When mounted on FR-4 board of 1 inch², 2 oz Cu t <10 sec

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current, (pulse width limited by T_{jmax})	16	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AV}, V_{DD} = 24 V)	300	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 40 V			1	µA
		V_{GS} = 0 V, V_{DS} = 40 V, T_C= 125 °C (1)			10	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS}= ±22 V			±100	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 16 A		2.2	2.75	mΩ
		V_{GS} = 4.5 V, I_D = 16 A		2.4	3.1	mΩ

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	5900	-	pF
C_{oss}	Output capacitance		-	870	-	pF
C_{rss}	Reverse transfer capacitance		-	130	-	pF
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 32 A V_{GS}= 0 to 4.5 V, see (*Figure 14: "Test circuit for gate charge behavior"*)	-	45	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain charge		-	17	-	nC
R_G	Gate input resistance	f=1 MHz, gate DC bias = 0 V, test signal level = 20 mV, I_D = 0 A	-	1.2	-	Ω

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 15 V, I_D = 16 A, R_G = 4.7 Ω V_{GS} = 10 V, (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	19	-	ns
t_r	Rise time		-	29	-	ns
$t_{d(off)}$	Turn-off delay time		-	90	-	ns
t_f	Fall time		-	21	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Forward on voltage		-		32	A
I_{SDM}(1)	Source-drain current (pulsed)		-		128	A
V_{SD}(2)	Forward on voltage	I_{SD} = 32 A, V_{GS}=0 V	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 32 A, di/dt = 100 A/µs, V_{DD}= 25 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	44		ns
Q_{rr}	Reverse recovery charge		-	57		nC
I_{RRM}	Reverse recovery current		-	2.6		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration=300µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

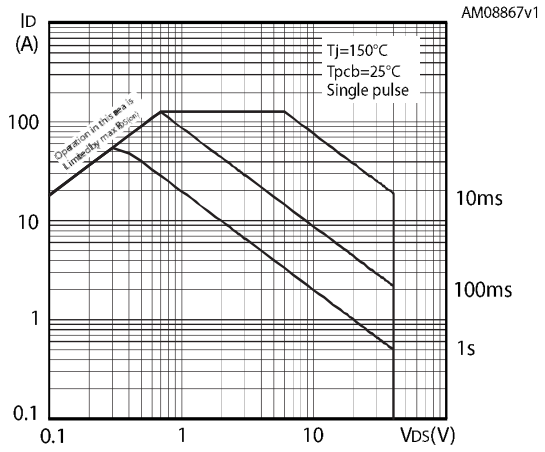


Figure 3: Thermal impedance

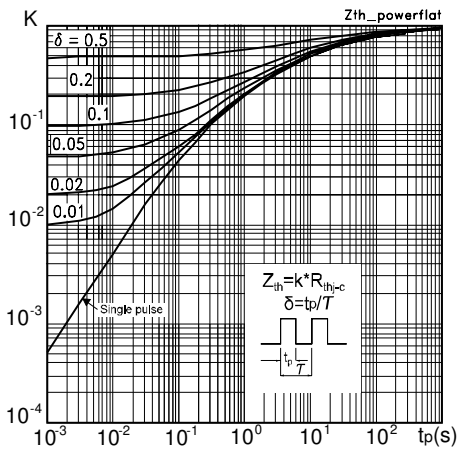


Figure 4: Output characteristics

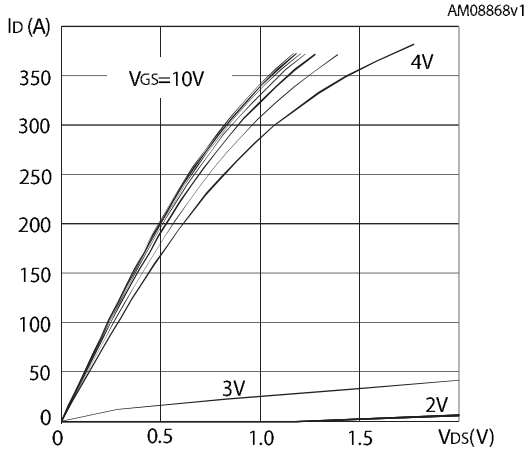


Figure 5: Transfer characteristics

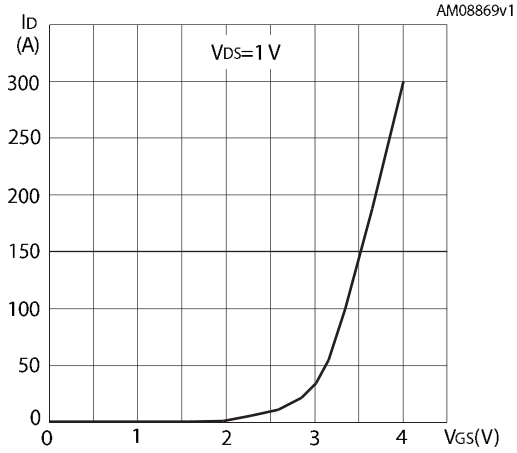


Figure 6: Gate charge vs gate-source voltage

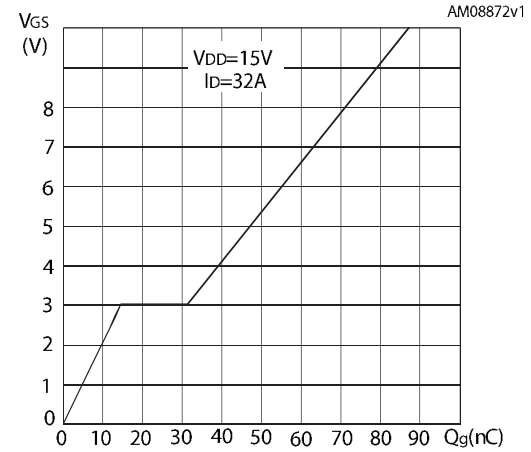


Figure 7: Static drain-source on-resistance

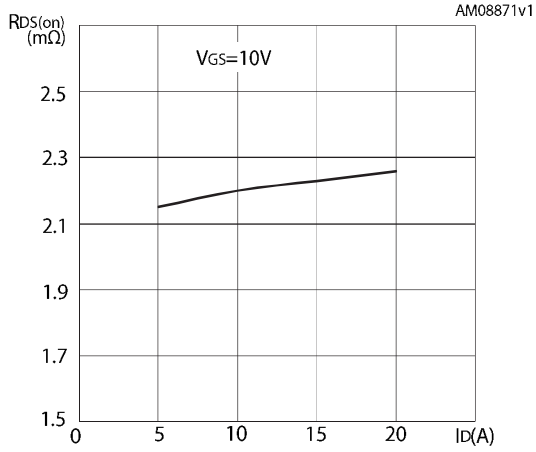


Figure 8: Capacitance variations

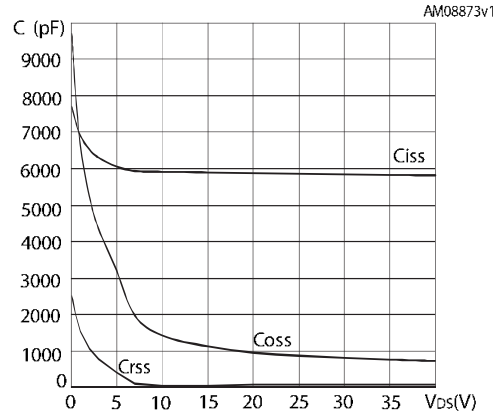


Figure 9: Normalized gate threshold voltage vs temperature

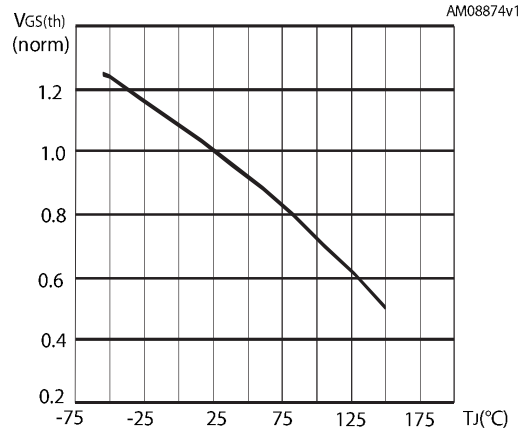


Figure 10: Normalized on-resistance vs temperature

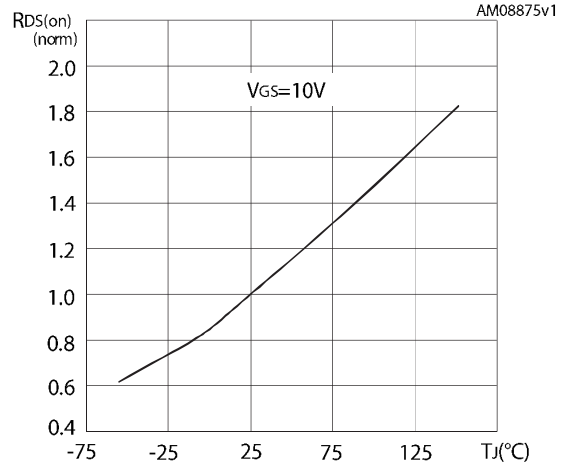


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

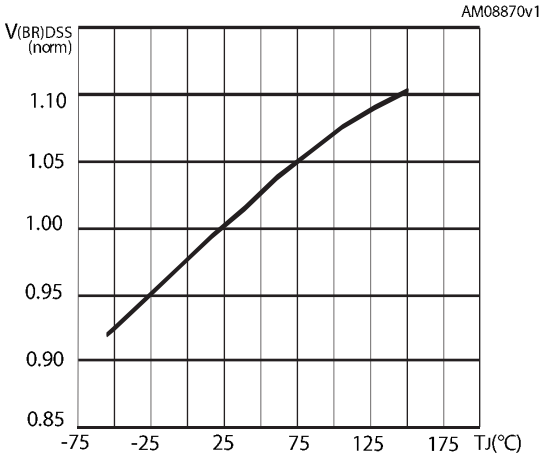
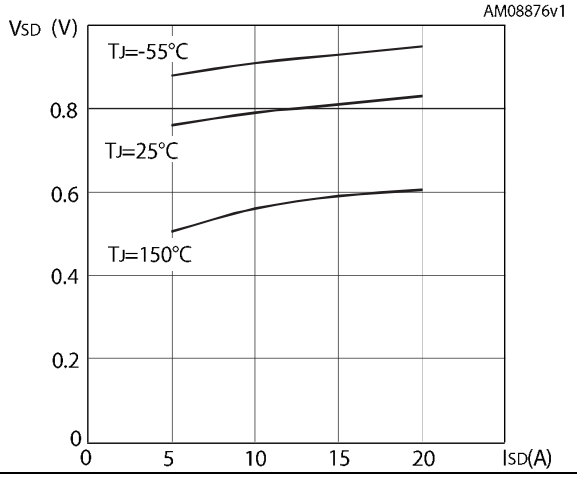


Figure 12: Source- drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

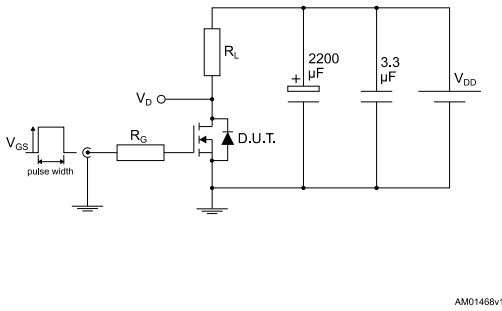


Figure 14: Test circuit for gate charge behavior

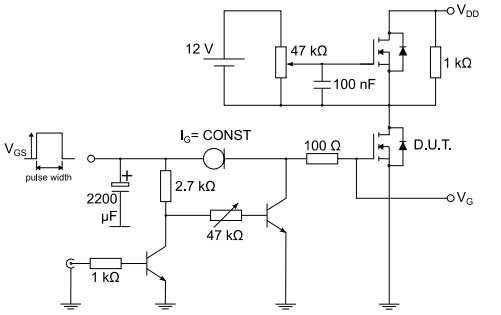


Figure 15: Test circuit for inductive load switching and diode recovery times

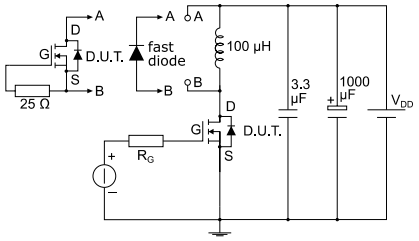


Figure 16: Unclamped inductive load test circuit

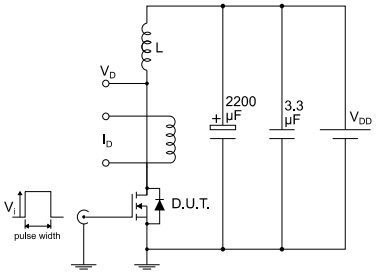


Figure 17: Unclamped inductive waveform

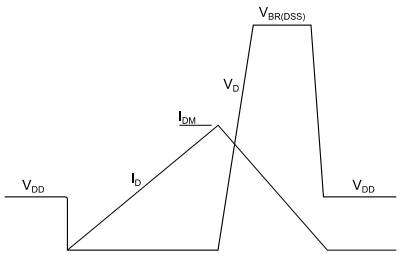
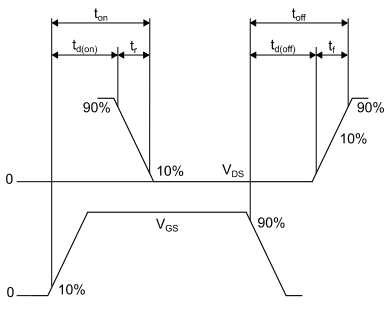


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 type C package information

Figure 19: PowerFLAT™ 5x6 type C package outline

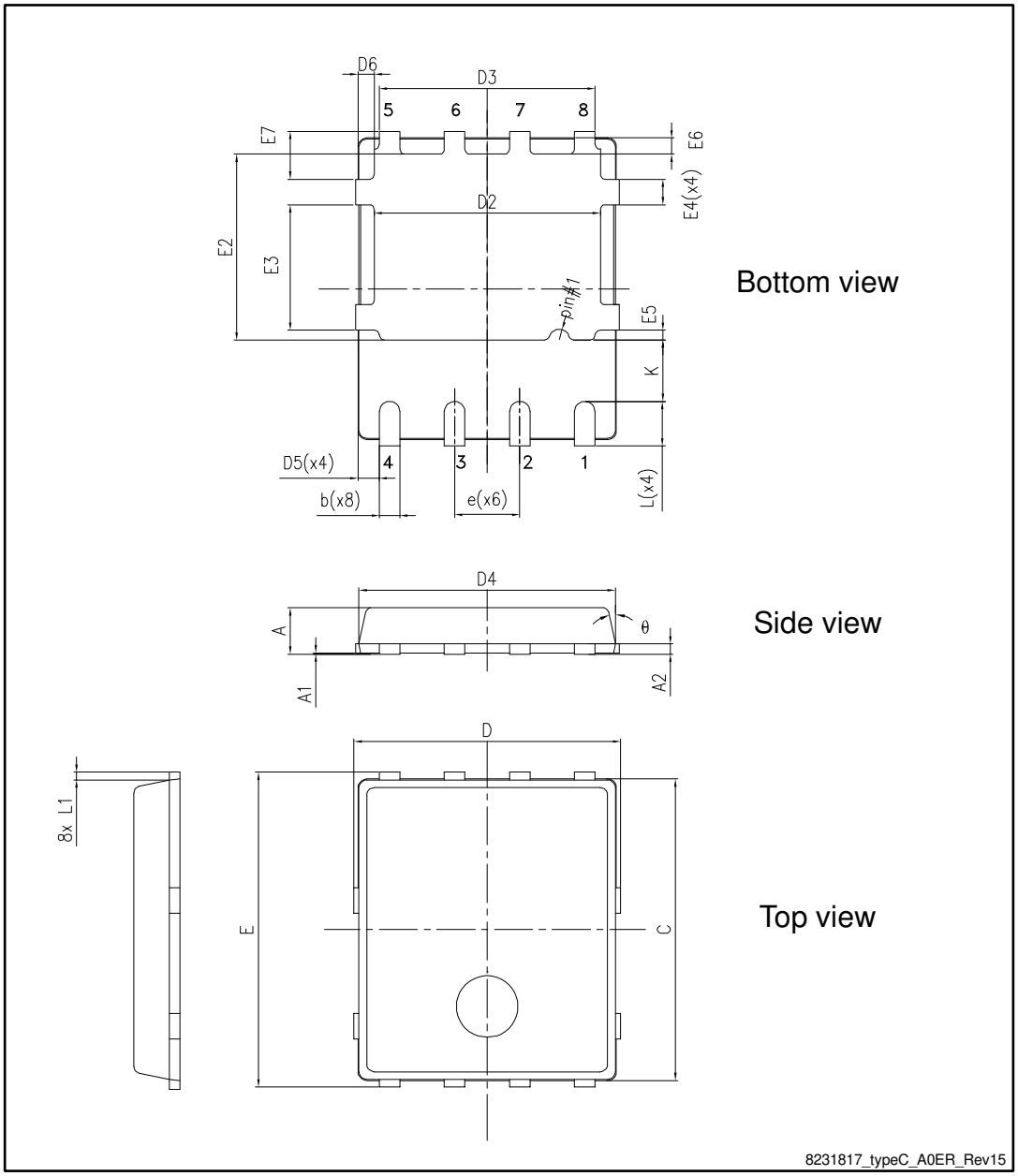
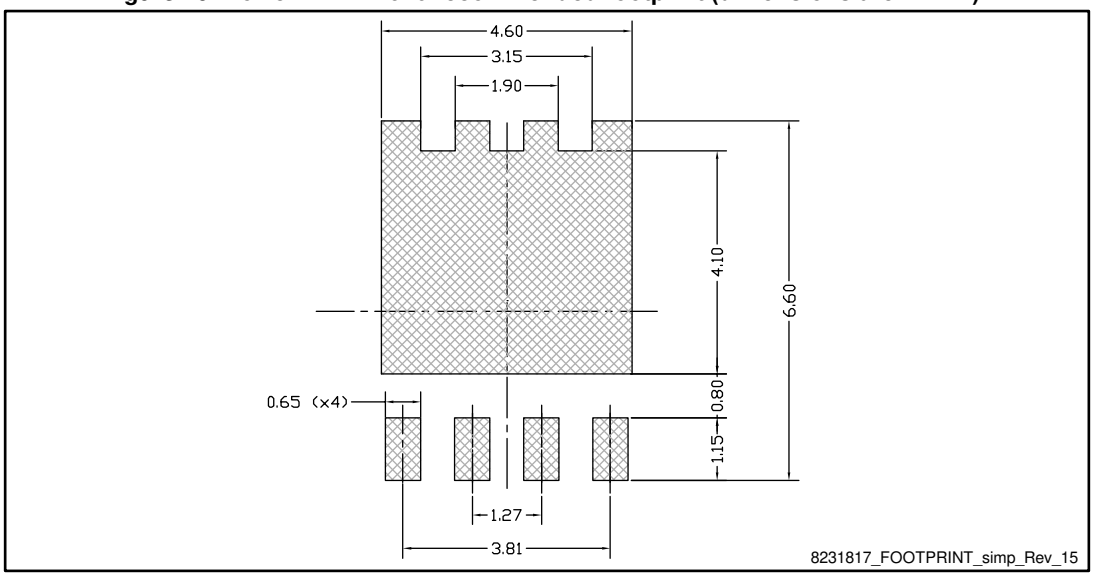


Table 9: PowerFLAT™ 5x6 type C package mechanical data

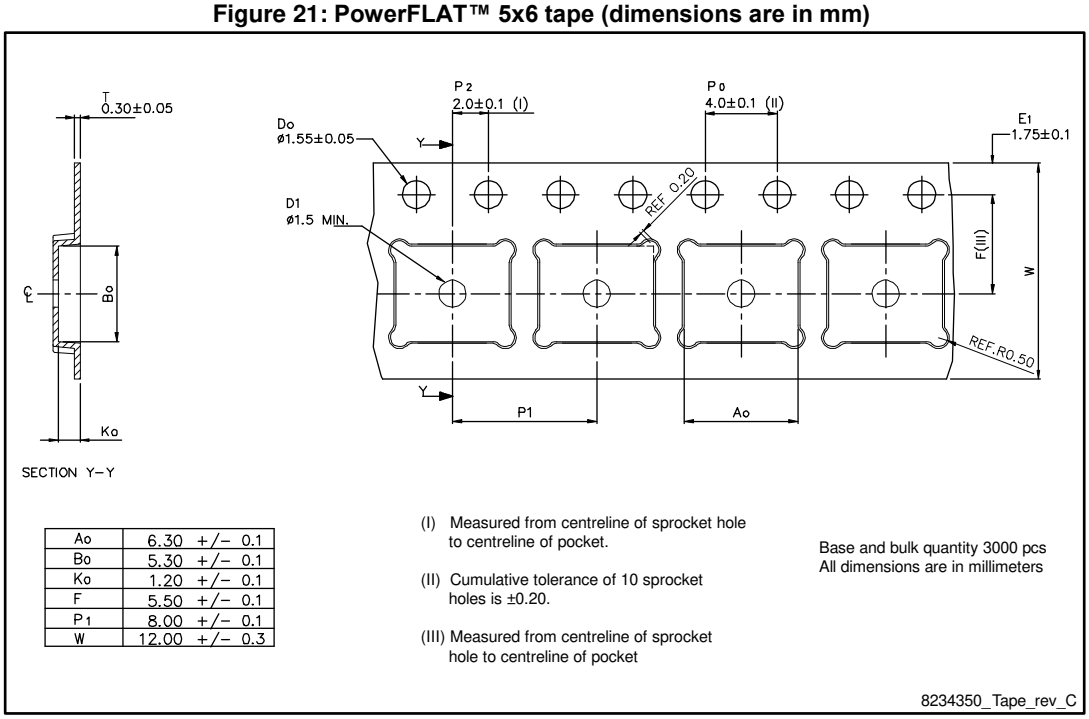
Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.725		1.025
L1	0.05	0.15	0.25
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)



Ao	6.30 +/– 0.1
Bo	5.30 +/– 0.1
Ko	1.20 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

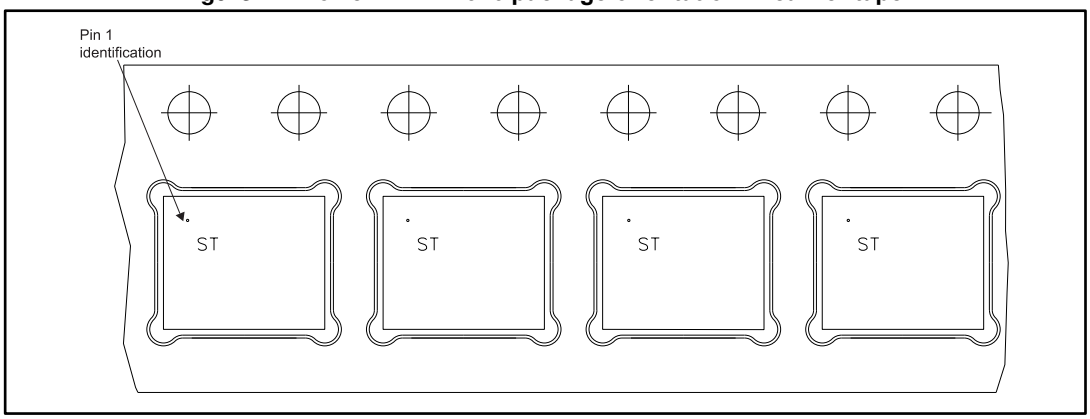
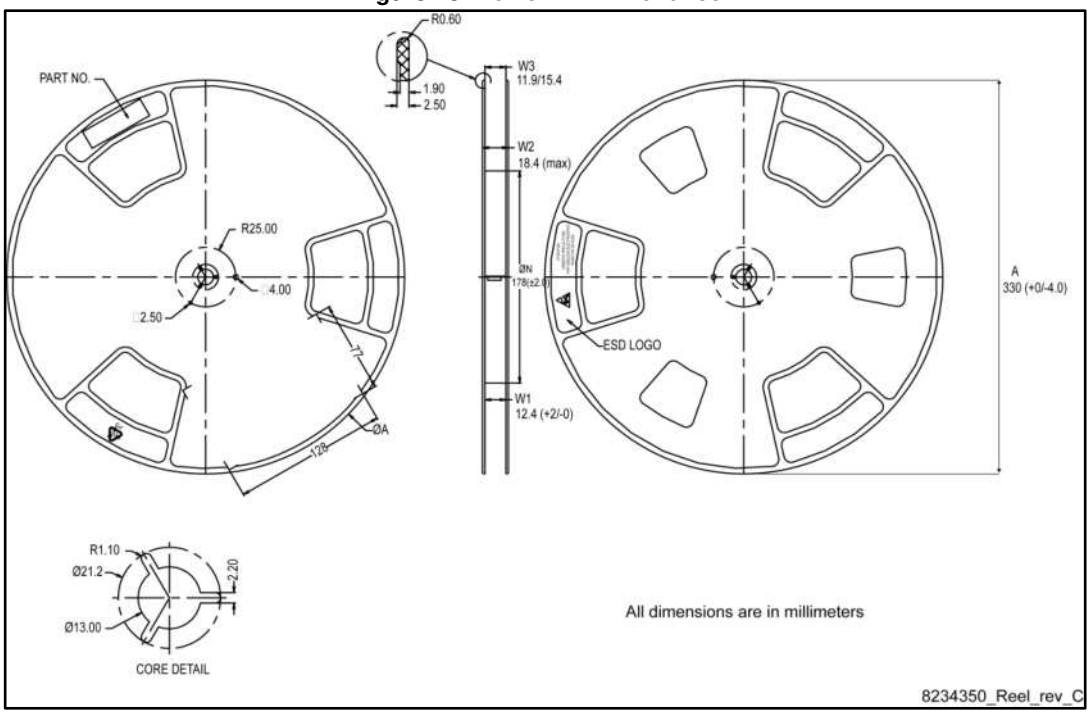


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
03-Jun-2010	1	First release.
29-Apr-2011	2	Document status promoted from preliminary data to datasheet.
10-Nov-2011	3	Section 4: Package mechanical data has been updated. Minor text changes.
08-Aug-2017	4	Modified *Table 1: "Device summary"*. Updated *Section 5: "Package information"*. Minor text changes.

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