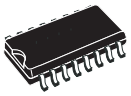
ALTAIR05T-800

Off-line all-primary sensing switching regulator

Datasheet - production data



SO16 narrow

Features

- Constant voltage and constant current output regulation (CV/CC) with no optocoupler
- Tight regulation also during heavy load transients
- 800 V avalanche rugged internal power section
- Quasi-resonant (QR) operation
- Low standby power consumption
- Automatic self-supply
- Input-voltage feedforward for mains-independent CC regulation
- Output cable drop compensation
- SO16N package

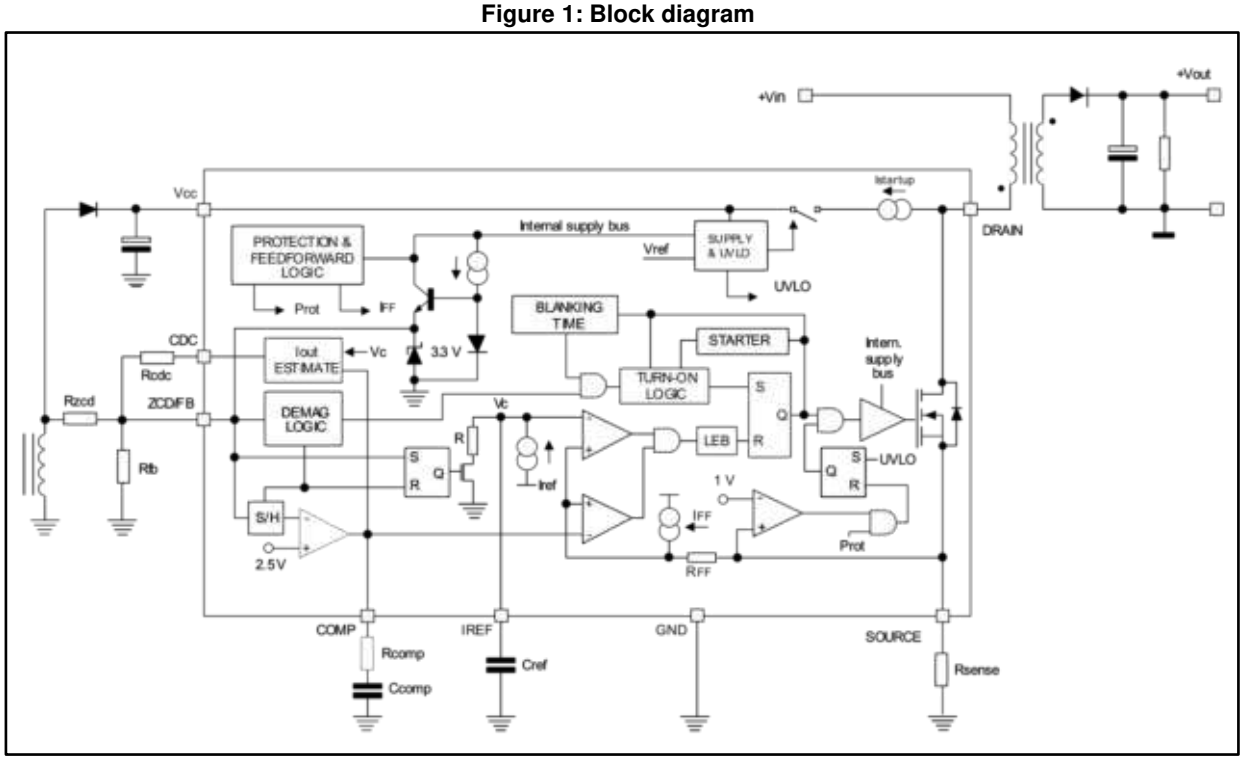
Applications

- AC-DC chargers for mobile phones and other hand-held equipments
- Compact SMPS that requires a precise current and/or voltage regulation

Description

The ALTAIR05T-800 is a high-voltage all-primary sensing switcher intended to operate directly from the rectified mains with minimum external parts. It combines a low voltage, high performance PWM controller chip and an 800 V avalanche rugged power section in the same package.

Figure 1: Block diagram



This is information on a product in full production.

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1 Device description

The device combines a low voltage PWM controller and an 800 V avalanche rugged power section in the same package.

The current-mode controller chip is specifically designed for off-line quasi-resonant flyback converters.

The device provides a constant output voltage (CV) and constant output current (CC) regulation using the primary sensing feedback. In this manner, the optocoupler, the secondary voltage reference, and the current sensor are no more necessary, even though an accurate regulation also during heavy load transients is maintained. Furthermore, the voltage drop can be compensated on the output cable so to improve CV regulation on the external accessible terminals.

Quasi-resonant operation is guaranteed by a transformer demagnetization sensing input that turns on the power section. The same input also serves to monitor the output voltage, to perform CV regulation, and to achieve mains-independent CC regulation (line voltage feedforward).

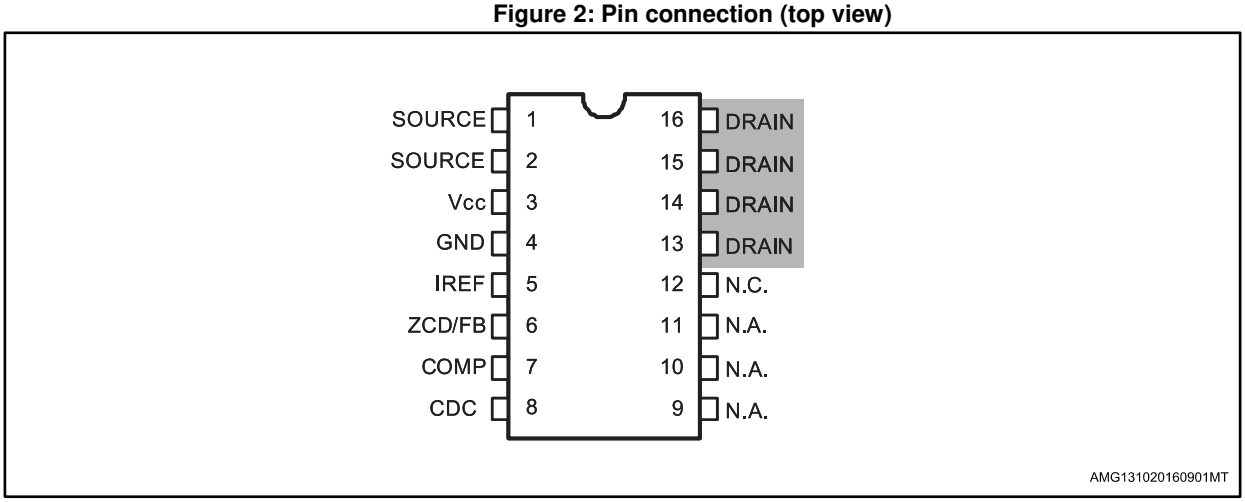
The maximum switching frequency is limited to 166 kHz, so that at medium-light load a special function automatically lowers the operating frequency still maintaining the valley switching operation. At very light load, the device enters a controlled burst-mode operation that, along with the built-in high-voltage start-up circuit and the low operating current, helps to minimize the standby power.

Although an auxiliary winding is required in the transformer to correctly perform CV/CC regulation, the chip is able to power itself directly from the rectified mains. This is useful especially during CC regulation, where the flyback voltage generated by the winding drops below UVLO threshold. However, if ultra-low no-load input consumption is required to comply with the most stringent energy-saving recommendations, then the device needs to be powered via the auxiliary winding.

In addition to these functions that optimize the power handling under different operating conditions, the device offers protection features that considerably increase safety and reliability of the end-product: auxiliary winding disconnection - or brownout - detection and shorted secondary rectifier - or saturation of the transformer. All of them are in auto-restart mode.

2 Pin connection

Figure 2: Pin connection (top view)



The copper area for heat dissipation has to be designed under the drain pins

Table 1: Pin functions

Number	Name	Function
1, 2	SOURCE	Power section source and input to the PWM comparator. The current flowing to the MOSFET is sensed through a resistor connected between the pin and GND. The resulting voltage is compared with an internal reference (0.75 V max.) to determine the MOSFET turn-off event. The pin is equipped with 250 ns blanking time after the gate-drive output goes high due to the improved noise immunity. If a second comparison level located at 1 V is exceeded, the IC is stopped and restarted after Vcc has dropped below 5 V.
3	Vcc	Supply voltage of the device. An electrolytic capacitor, connected between this pin and ground, is initially charged by the internal high-voltage start-up generator; when the device runs, the same generator keeps it charged in case the voltage supplied by the auxiliary winding is not sufficient. This feature is disabled in case a protection is tripped. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC.
4	GND	Ground. Current return for the signal part of the IC and the gate drive. All of ground connections of the bias components should be tied to a trace going to this pin and kept separate from any pulsed current return.
5	IREF	CC regulation loop reference voltage. An external capacitor has to be connected between this pin and GND. An internal circuit develops a voltage on this capacitor that is used as the reference for the MOSFET peak drain current during CC regulation. The voltage is automatically adjusted to keep the average output current constant.

Number	Name	Function
6	ZCD/FB	Demagnetization sensing of the transformer for quasi-resonant operation. Input/output voltage monitor. A negative-going edge triggers the MOSFET turn-on event. The current sourced by the pin during ON-time is monitored to get an image of the input voltage to the converter, in order to compensate the internal delay of the current sensing circuit and achieve a CC regulation independent of the mains voltage. If this current does not exceed 50 µA, either a floating pin or an abnormal low input voltage is assumed, the device is stopped and restarted after Vcc has dropped below 5 V. Besides, the pin voltage is sampled and held right at the end of the demagnetization of the transformer to get an accurate image of the output voltage to be fed to the inverting input of the internal, transconductance-type, error amplifier, whose non-inverting input is referenced to 2.5 V. Please note that the maximum $I_{ZCD/FB}$ sunk/sourced current does not have to exceed ±2 mA (AMR) in all V_{IN} range conditions (85-265 VAC). No capacitor is allowed between the pin and the auxiliary transformer.
7	COMP	Output of the internal transconductance error amplifier. The compensation network is placed between this pin and GND to achieve stability and good dynamic performance of the voltage control loop.
8	CDC	Cable drop compensation input. During CV regulation this pin, which can sink current, provides a voltage lower than the internal reference voltage (2.5 V) by an amount proportional to the DC load current. By connecting a resistor between this pin and ZCD/FB, the CV regulation setpoint is increased proportionally. This allows that the voltage drop across the output cable to be compensated and, ideally, that zero-load regulation on the externally available terminals to be achieved. Leave the pin open if the function is not used.
9 to 11	N.A.	Not available. These pins must be left not connected.
12	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
13 to 16	DRAIN	Drain connection of the internal power section. The internal high-voltage start-up generator sinks current from this pin as well. Pins connected to the internal metal frame to facilitate heat dissipation.

3 Maximum ratings

3.1 Absolute maximum ratings

Table 2: Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{DS}	1,2, 13-16	Drain-to-source (ground) voltage	-1 to 800	V
I_D	1,2, 13-16	Drain current	1	A
Eav	1,2, 13-16	Single pulse avalanche energy (Tj = 25 °C, I_D = 1 A)	50	mJ
Vcc	3	Supply voltage (Icc < 25 mA)	Self-limiting	V
$I_{ZCD/FB}$	6	Zero-current detector current	±2	mA
---	7, 8	Analog inputs and outputs	-0.3 to 3.6	V
I_{CDC}	8	Maximum sunk current	200	µA
Ptot		Power dissipation @ T_A = 50 °C	0.9	W
Tj		Junction temperature range	-40 to 150	°C
Tstg		Storage temperature	-55 to 150	°C

3.2 Thermal data

Table 3: Thermal data

Symbol	Parameter	Max. value	Unit
$R_{th\ j\text{-}pin}$	Thermal resistance, junction-to-pin	10	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance, junction-to-ambient	110	

4 Electrical characteristics

(T_J = -40 to 125 °C, Vcc = 14 V; unless otherwise specified)

Table 4: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Power section						
$V_{(BR)DSS}$	Drain-source breakdown	I_D < 100 µA; T_j = 25 °C	800			V
I_{DSS}	Off-state drain current	V_{DS} = 750 V; T_j = 125 °C (see *Figure 4: "Off-state drain and source current test circuit"* and note)			80	µA
$R_{DS(on)}$	Drain-source ON-state resistance	Id = 100 mA; Tj = 25 °C		11	14	Ω
		Id = 100 mA; Tj = 125 °C		22	28	
C_{oss}	Effective (energy-related) output capacitance	(see *Figure 3: "COSS output capacitance variation"*)				
High-voltage start-up generator						
V_{Start}	Min. drain start voltage	I_{charge} < 100 µA	40	50	60	V
I_{charge}	Vcc startup charge current	V_{DRAIN} > V_{Start}; V_{CC}< V_{CCOn} Tj = 25 °C	4	5.5	7	mA
$V_{CCrestart}$	Vcc restart voltage (Vcc falling)	*(1)*	9.5	10.5	11.5	V
		After protection tripping		5		
Supply voltage						
Vcc	Operating range	After turn-on	11.5		23	V
Vcc_{On}	Turn-on threshold	*(1)*	12	13	14	V
Vcc_{Off}	Turn-off threshold	*(1)*	9	10	11	V
V_Z	Zener voltage	Icc = 20 mA	23	25	27	V
Supply current						
$Icc_{start-up}$	Start-up current	(see *Figure 5: "Start-up current test circuit"*)		200	300	µA
Iq	Quiescent current	(see *Figure 6: "Quiescent current test circuit"*)		1	1.4	mA
Icc	Operating supply current @ 50 kHz	(see *Figure 7: "Operating supply current test circuit"*)		1.4	1.7	mA
$Iq_{(fault)}$	Fault quiescent current	During hiccup and brownout (see *Figure 8: "Quiescent current during fault test circuit"*)		250	350	µA
Start-up timer						
T_{START}	Start timer period		100	125	175	µs
$T_{RESTART}$	Restart timer period during burst mode		400	500	700	µs
Zero-current detector						
I_{ZCDb}	Input bias current	V_{ZCD} = 0.1 to 3 V		0.1	1	µA
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 1 mA	3.0	3.3	3.6	V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 1 mA	-90	-60	-30	mV

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ZCDA}	Arming voltage	Positive-going edge	100	110	120	mV
V_{ZCDT}	Triggering voltage	Negative-going edge	50	60	70	mV
I_{ZCDON}	Min. source current during MOSFET ON-time		-25	-50	-75	µA
T_{BLANK}	Trigger blanking time after MOSFET turn-off	V_{COMP} ≥ 1.3 V		6		µs
		V_{COMP} = 0.9 V		30		
Line feedforward						
R_{FF}	Equivalent feedforward resistor	I_{ZCD} = 1mA		45		Ω
Transconductance error amplifier						
V_{REF}	Voltage reference	Tj = 25°C(1)	2.46	2.5	2.54	V
		Tj = -40 to 125°C and Vcc = 12 V to 23 V (1)	2.42		2.58	
gm	Transconductance	ΔI_{COMP} = ±10 µA V_{COMP} = 1.65 V	1.3	2.2	3.2	mS
Gv	Voltage gain	Open loop		73		dB
GB	Gain-bandwidth product			500		KHz
I_{COMP}	Source current	V_{ZCD} = 2.3 V, V_{COMP} = 1.65 V	70	100		µA
	Sink current	V_{ZCD} = 2.7 V, V_{COMP} = 1.65 V	400	750		µA
V_{COMPH}	Upper COMP voltage	V_{ZCD} = 2.3 V		2.7		V
V_{COMPL}	Lower COMP voltage	V_{ZCD} = 2.7 V		0.7		V
V_{COMPBM}	Burst-mode threshold			1		V
Hys	Burst-mode hysteresis			65		mV
CDC function						
V_{CDC}	CDC voltage reference	V_{COMP} = 1.1 V, I_{CDC} = 1 µA(1)	2.4	2.5	2.6	V
Current reference						
V_{IREFx}	Maximum value	V_{COMP} = V_{COMPL}(1)	1.5	1.6	1.7	V
V_{CREF}	Current reference voltage		0.192	0.2	0.208	V
Current sense						
t_{LEB}	Leading-edge blanking		200	250	300	ns
$t_{d(H-L)}$	Delay-to-output			300		ns
V_{CSx}	Max. clamp value	dV_{cs}/d_t = 200 mV/µs (1)	0.7	0.75	0.8	V
V_{CSdis}	Hiccup-mode OCP level	(1)	0.92	1	1.08	V

Notes:

(1)Parameters tracking each other.

Figure 3: COSS output capacitance variation

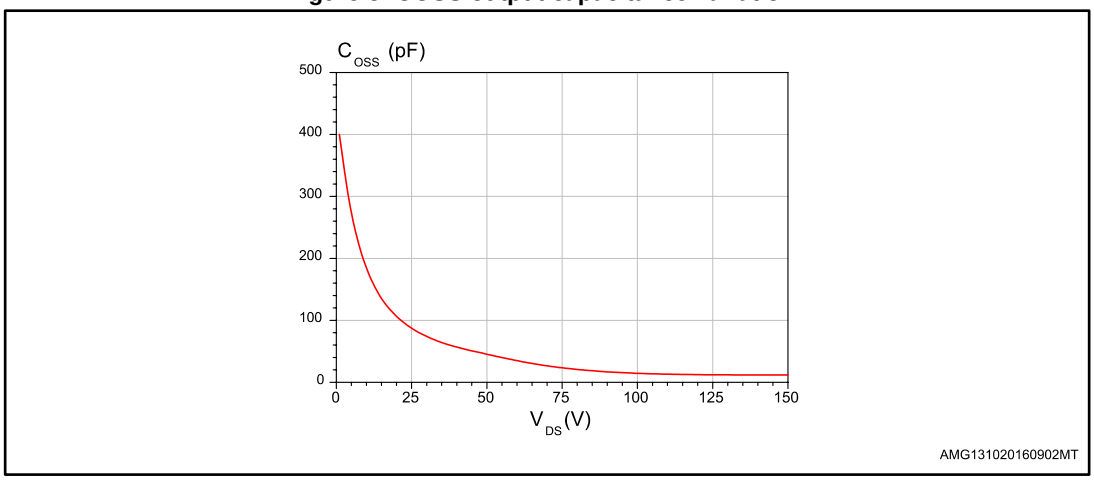
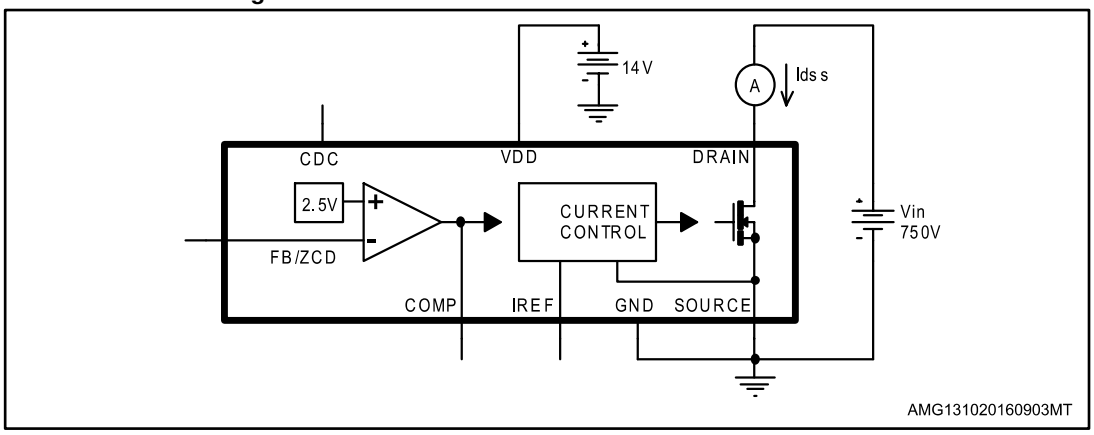


Figure 4: Off-state drain and source current test circuit



The measured I_{DSS} is the sum between the current across the start-up resistor and the off-state drain current of the MOSFET.

Figure 5: Start-up current test circuit

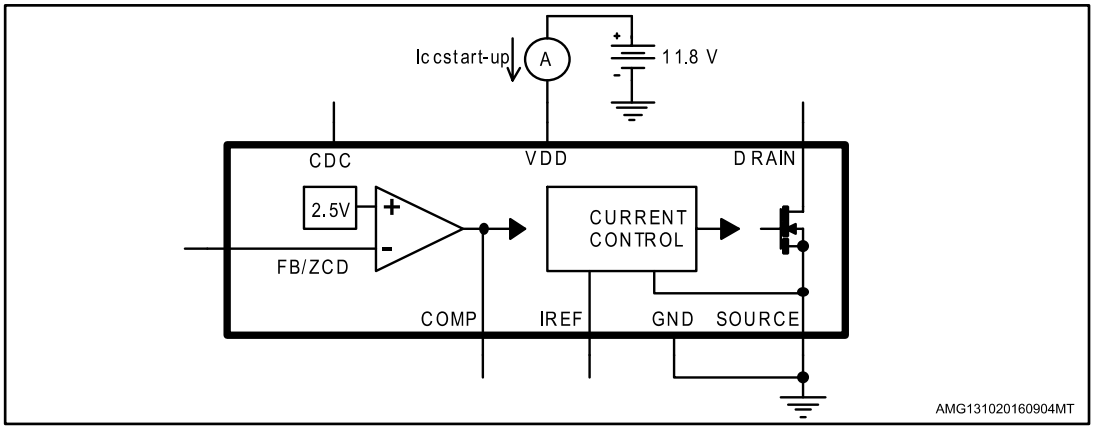


Figure 6: Quiescent current test circuit

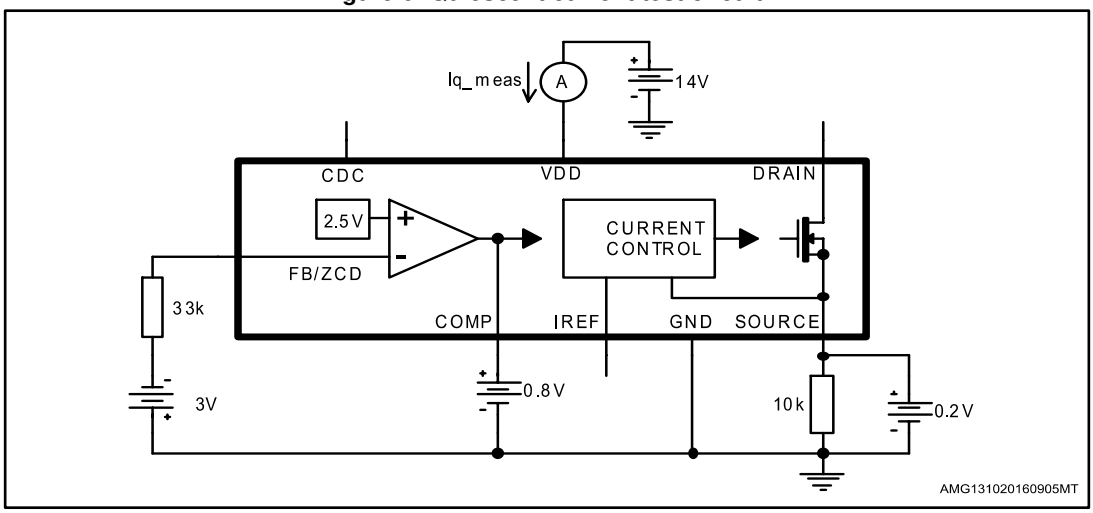
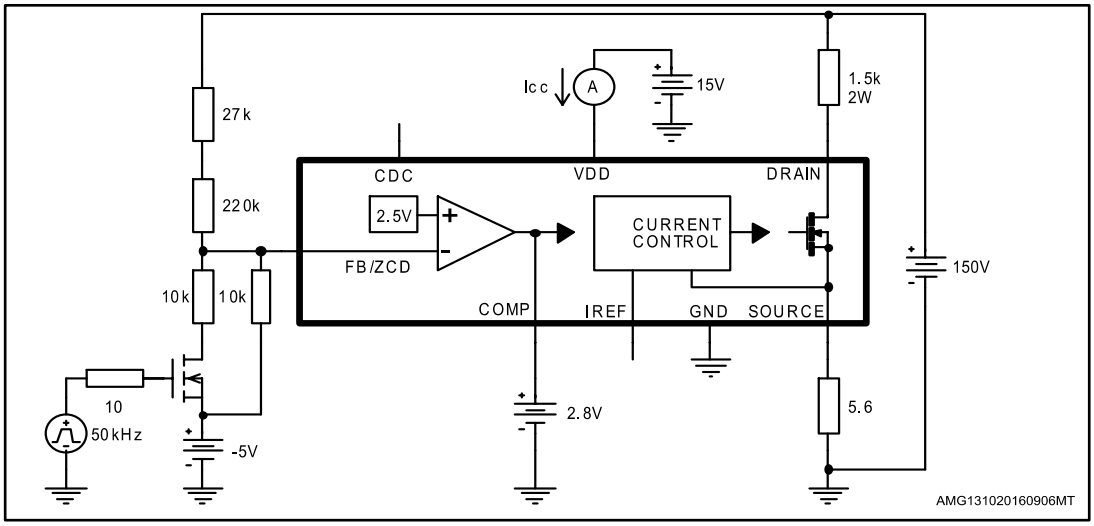
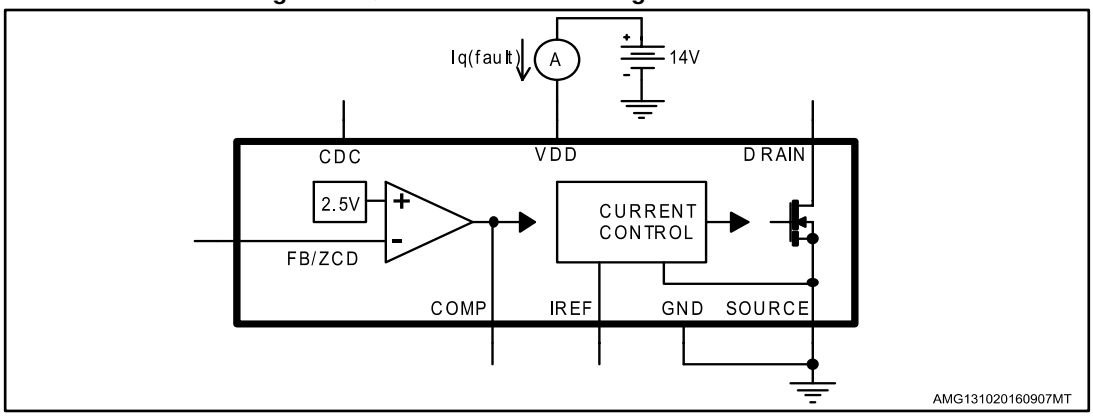


Figure 7: Operating supply current test circuit



The circuit across the ZCD pin is used for switch-on synchronization.

Figure 8: Quiescent current during fault test circuit



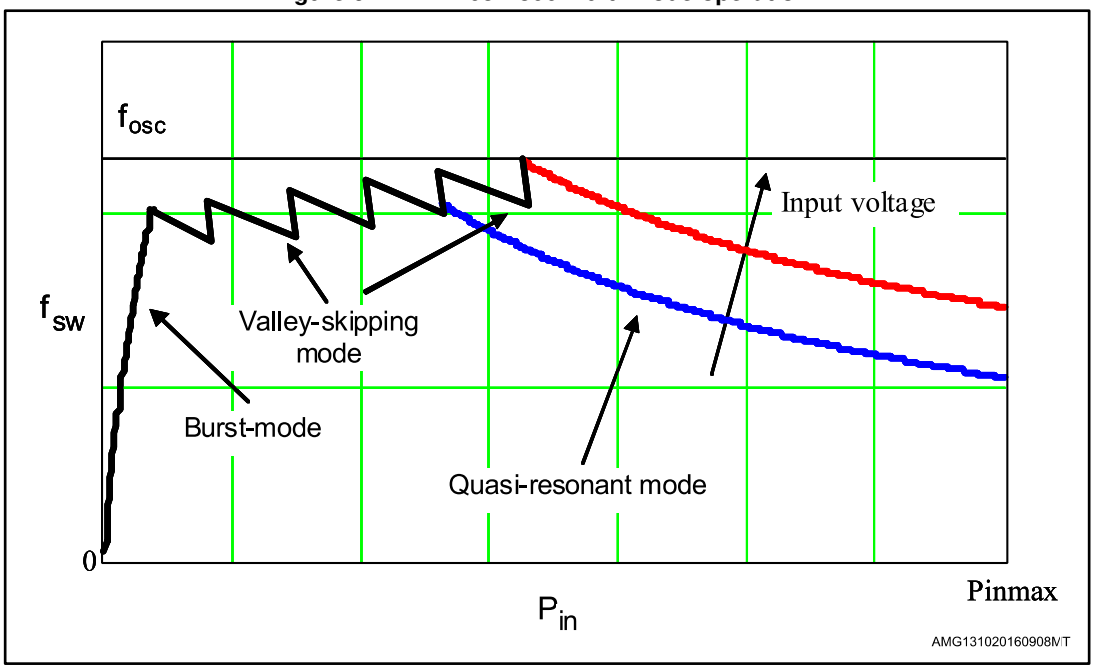
5 Application information

The device is an off-line all-primary sensing switching regulator, based on quasi-resonant flyback topology.

Depending on the load condition of the converter, the device is able to work in different modes (see *Figure 9: "ALTAIR05T-800 multi-mode operation "*):

1. QR mode at heavy load. Quasi-resonant operation lies in synchronization of the turn-on of the MOSFET to the transformer demagnetization by detecting the resulting negative-going edge of the voltage across any winding of the transformer. Therefore the system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer. As a result, the switching frequency is different for different line/load conditions (see the hyperbolic-like portion of the curves in *Figure 9: "ALTAIR05T-800 multi-mode operation "*). Minimum turn-on losses, low EMI emission and safe behavior in short-circuit are the main benefits of this kind of operation.
2. Valley-skipping mode at medium/ light load. Depending on voltage on COMP pin, the device defines the maximum operating frequency of the converter. As the load is reduced, the MOSFET turn-on event does not occur on the first valley but on the second one, the third one and so on. In this manner the switching frequency does not increase any longer (piecewise linear portion in *Figure 9: "ALTAIR05T-800 multi-mode operation "*).
3. Burst-mode with no or very light load. When the load is extremely light or disconnected, the converter enters a controlled on/off operation with constant peak current. Decreasing the load result in frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and complying with energy saving regulations or recommendations. Being the peak current very low, no issue of audible noise arises.

Figure 9: ALTAIR05T-800 multi-mode operation



5.1 Power section and gate driver

The power section guarantees safe avalanche operation within the specified energy ratings as well as high dv/dt capability. The power MOSFET has a $V_{(BR)DSS}$ of 800 V min. and a typical $R_{DS(on)}$ of 11 Ω.

The gate driver is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the power MOSFET cannot be turned on accidentally.

5.2 High-voltage start-up generator

The HV current generator is supplied through the DRAIN pin and it is enabled only if the input bulk capacitor voltage is higher than V_{start} threshold, 50 V_{DC} typically. When the HV current generator is ON, the I_{charge} current (5.5 mA typical value) is delivered to the capacitor on the V_{CC} pin.

With reference to the timing diagram of *Figure 10: "Timing diagram: normal power-up and power-down sequences"*, when power is applied to the circuit and the voltage on the input bulk capacitor is high enough, the HV generator is sufficiently biased to start operating, thus it draws about 5.5 mA (typical) from the bulk capacitor. Most of this current charges the bypass capacitor connected between the Vcc pin and ground and makes its voltage rise linearly.

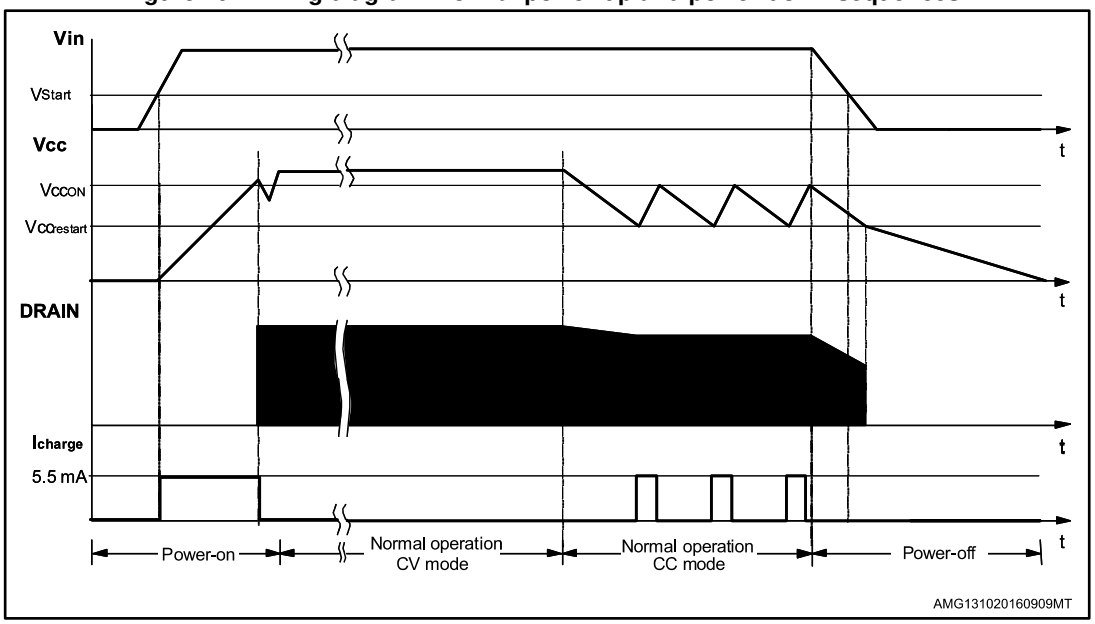
As the Vcc voltage reaches the start-up threshold (13 V typ.) the chip starts operating, the internal power MOSFET is enabled to switch and the HV generator is cut off. The IC is powered by the energy stored in the V_{cc} capacitor.

The chip is able to power itself directly from the rectified mains: when the voltage on the V_{CC} pin falls below $Vcc_{restart}$ (10.5 V typ.), during each MOSFET off-time event, the HV current generator is turned on and charges the supply capacitor until it reaches the V_{CCOn} threshold.

In this way, the self-supply circuit develops a voltage high enough to sustain the operation of the device. This feature is useful especially during CC regulation, when the flyback voltage generated by the auxiliary winding alone may not be able to keep Vcc above $V_{CCrestart}$.

At converter power-down the system loses regulation as soon as the input voltage falls below V_{Start}. This prevents restart attempts of the converter and ensures monotonic output voltage decay at system power-down.

Figure 10: Timing diagram: normal power-up and power-down sequences

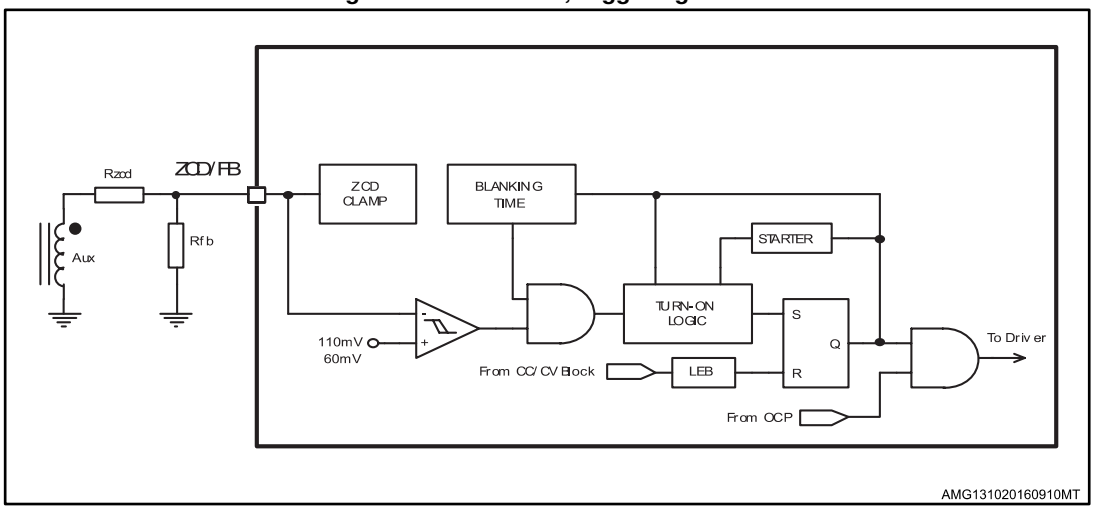


5.3 Zero-current detection and triggering block

The zero-current detection (ZCD) and triggering blocks switch on the power MOSFET if a negative-going edge falling below 50 mV is applied to the ZCD/FB pin. To do so, the triggering block must be previously armed by a positive-going edge exceeding 100 mV.

This feature is used to detect the transformer demagnetization for QR operation, where the signal for the ZCD input is obtained from the auxiliary winding of the transformer also used to supply the IC.

Figure 11: ZCD block, triggering block



The triggering block is blanked after the MOSFET turn-off to prevent any negative-going edge that follows leakage inductance demagnetization from triggering the ZCD circuit erroneously.

This blanking time is dependent on the voltage on COMP pin: it is T_{BLANK} = 30 µs for V_{COMP} = 0.9 V, and decreases almost linearly down to T_{BLANK} = 6 µs for V_{COMP} = 1.3 V.

The voltage on the pin is both top and bottom limited by a double clamp, as illustrated in the internal diagram of the ZCD block, see *Figure 11: "ZCD block, triggering block"*. The upper clamp is typically at 3.3 V, while the lower clamp is at -60 mV. The interface between the pin and the auxiliary winding is a resistor divider. Its resistance ratio as well as the individual resistance values have to be properly chosen (see "*Section 5.4: "Constant voltage operation"*" and "*Section 5.6: "Voltage feedforward block"*").

Please note that the maximum $I_{ZCD/FB}$ sunk/sourced current does not have to exceed ±2 mA (AMR) in all V_{IN} range conditions (85-265 VAC). No capacitor is allowed between ZCD pin and the auxiliary transformer.

The switching frequency is limited to 166 kHz, as the operating frequency of the converter tends to increase excessively at light load and high input voltage.

A starter block is also used to start up the system, that is, to turn on the MOSFET during the converter power-up, when no or a too small signal is available on the ZCD pin.

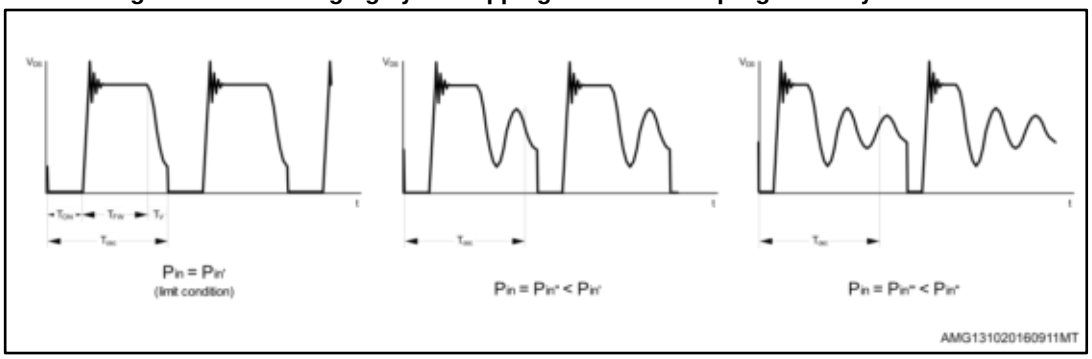
The starter frequency is 2 kHz if COMP pin is below burst mode threshold, i.e. 1 V, while it becomes 8 kHz if this voltage exceeds this value.

After the first few cycles initiated by the starter, as the voltage developed across the auxiliary winding becomes so high to arm the ZCD circuit, the turn-on of the MOSFET starts to be locked to demagnetization of the transformer, hence QR operation is set.

The starter is also active when the IC is in CC regulation and the output voltage is not so high to allow the ZCD triggering.

If the demagnetization completes, hence a negative-going edge appears on the ZCD pin, after a time exceeding time T_{BLANK} from the previous turn-on, the MOSFET is turned on again, with some delay to ensure minimum voltage at turn-on. If, instead, the negative-going edge appears before T_{BLANK} has elapsed, it is ignored and only the first negative-going edge after T_{BLANK} turns on the MOSFET. In this way one or more drain ringing cycles are skipped ("valley-skipping mode", *Figure 12: "Drain ringing cycle skipping as the load is progressively reduced"*) and the switching frequency is prevented from exceeding $1/T_{BLANK}$.

Figure 12: Drain ringing cycle skipping as the load is progressively reduced



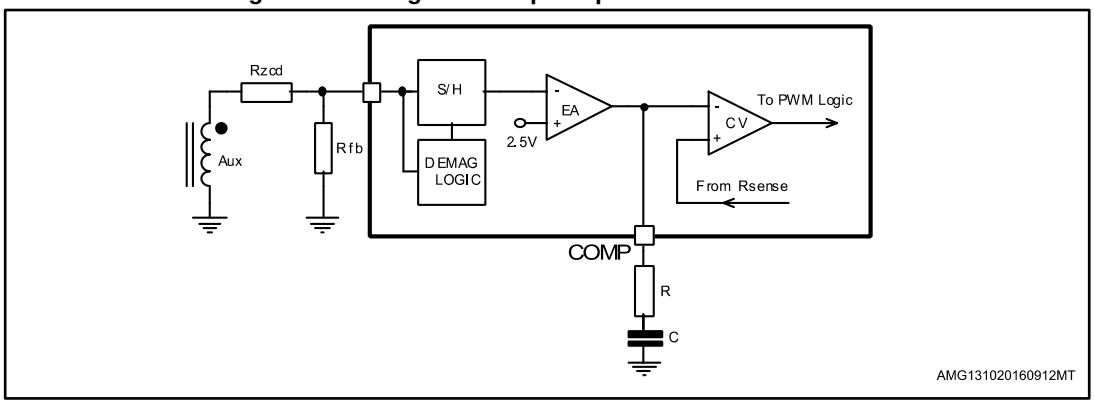
Note that when the system operates in valley skipping-mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the OFF-time of the MOSFET changes with discrete steps of one ringing cycle, while the OFF-time needed for cycle-by-cycle energy balance may fall in between. Thus one or some longer switching cycles are compensated by one or some shorter cycles and vice versa. However, this mechanism is absolutely normal and there is no appreciable effect on the performance of the converter or on its output voltage.

5.4 Constant voltage operation

The IC is specifically designed to work in primary regulation and the output voltage is sensed through a voltage partition of the auxiliary winding, just before the auxiliary rectifier diode.

Figure 13: "Voltage control principle: internal schematic" shows the internal schematic of the constant voltage mode and the external connections.

Figure 13: Voltage control principle: internal schematic



Due to the parasitic wire resistance, the auxiliary voltage is representative of the output just when the secondary current becomes zero. For this purpose, the signal on ZCD/FB pin is sampled and held at the end of transformer demagnetization to get an accurate image of the output voltage and it is compared with the error amplifier internal reference.

The COMP pin is used for the frequency compensation: usually, an RC network, which stabilizes the overall voltage control loop, is connected between this pin and ground.

The output voltage can be defined according to the following formula:

Equation 1

$$R_{FB} = \frac{V_{REF}}{\frac{N_{AUX}}{N_{SEC}} \cdot V_{OUT} - V_{REF}} \cdot R_{ZCD}$$

Where N_{SEC} and N_{AUX} are the numbers of secondary and auxiliary turns respectively.

The R_{ZCD} value can be defined depending on the application parameters (see *Section 5.6: "Voltage feedforward block"*).

5.5 Constant-current operation

Figure 14: "Current control principle" presents the principle used to control the average output current of the flyback converter.

The output voltage of the auxiliary winding is used by the demagnetization block to generate the control signal for the MOSFET switch Q1. R resistor in series absorbs a current V_C/R, where V_C is the voltage developed across the capacitor C_{REF}.

The flip-flop output is high as long as the transformer delivers current to secondary-side. This is shown in *Figure 15: "Constant current operation: switching cycle waveforms"*.

The capacitor C_{REF} has to be chosen so that its voltage V_C can be considered as a constant. Since it is charged and discharged by current in the range of some tens of µA

(I_{CREF} is typically 20 µA) at the switching frequency rate, a capacitance value in the range 4.7 to10 nF is suitable for switching frequencies of 10 kHz.

The average output current can be expressed as follows:

Equation 2

$$I_{OUT} = \frac{N_{PRI}}{N_{SEC}} \cdot \frac{V_{CREF}}{(2 \cdot R_{SENSE})}$$

Where N_{PRI} is the number of the primary turns.

This formula shows that the average output current does not depend neither on the input or the output voltage, nor on transformer inductance values. The external parameters defining the output current are the transformer ratio n and the sense resistor R_{SENSE}.

Figure 14: Current control principle

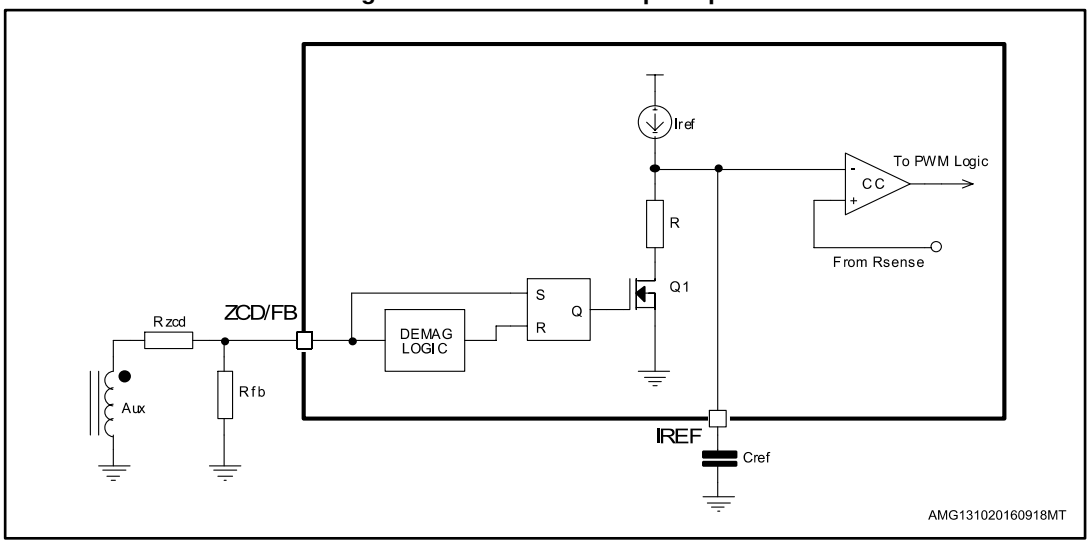
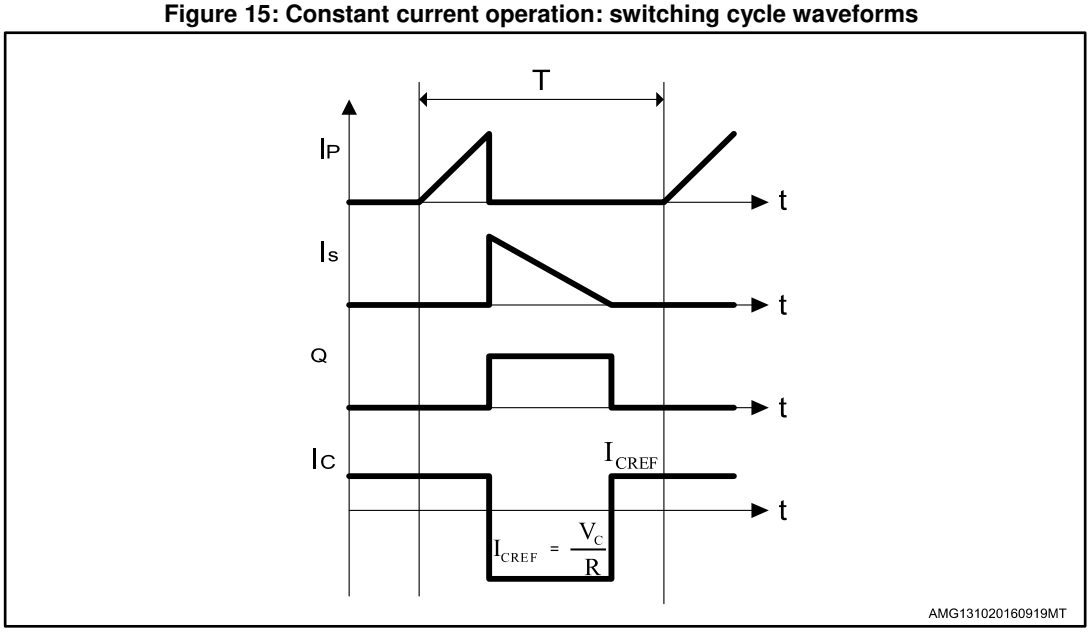


Figure 15: Constant current operation: switching cycle waveforms



5.6 Voltage feedforward block

The current control structure uses the voltage V_C to define the output current, according to **Equation 2**. Actually, the CC comparator is affected by an internal propagation delay T_d, which switches off the MOSFET with a peak current higher than the foreseen value.

This current overshoot is equal to:

Equation 3

$$\Delta I_P = \frac{V_{IN} \cdot T_d}{L_P}$$

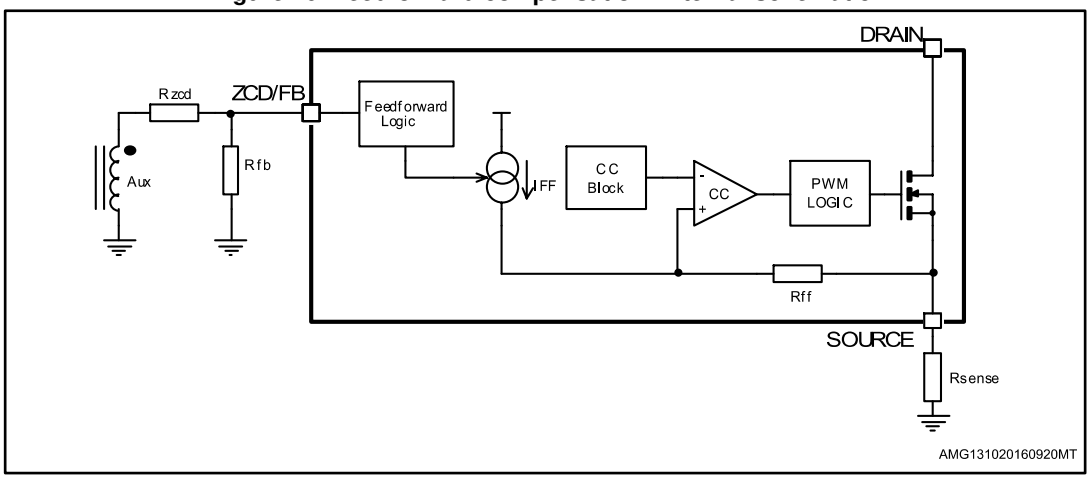
Where L_P is the primary inductance.

It introduces an error on the calculated CC setpoint, depending on the input voltage.

The device implements a line feedforward function, which solves the issue by introducing an input voltage dependent offset on the current sense signal, in order to adjust the cycle-by-cycle current limitation.

The internal schematic is shown in *Figure 16: "Feedforward compensation: internal schematic"*.

Figure 16: Feedforward compensation: internal schematic



The R_{ZCD} resistor can be calculated as follows:

Equation 4

$$R_{ZCD} = \frac{N_{AUX}}{N_{PRI}} \cdot \frac{L_P \cdot R_{FF}}{T_d \cdot R_{SENSE}}$$

In this case the peak drain current does not depend on input voltage anymore.

Concerning the R_{ZCD} value: during ON-time of the MOSFET, the current sourced by the ZCD/FB pin, I_{ZCD}, is compared with an internal reference current I_{ZCDON} (-50 µA typical).

If $I_{ZCD} < I_{ZCDON}$, the brownout function is active and the IC is shut down.

This feature is especially important when the auxiliary winding is accidentally disconnected and considerably increases safety and reliability of the end-product.

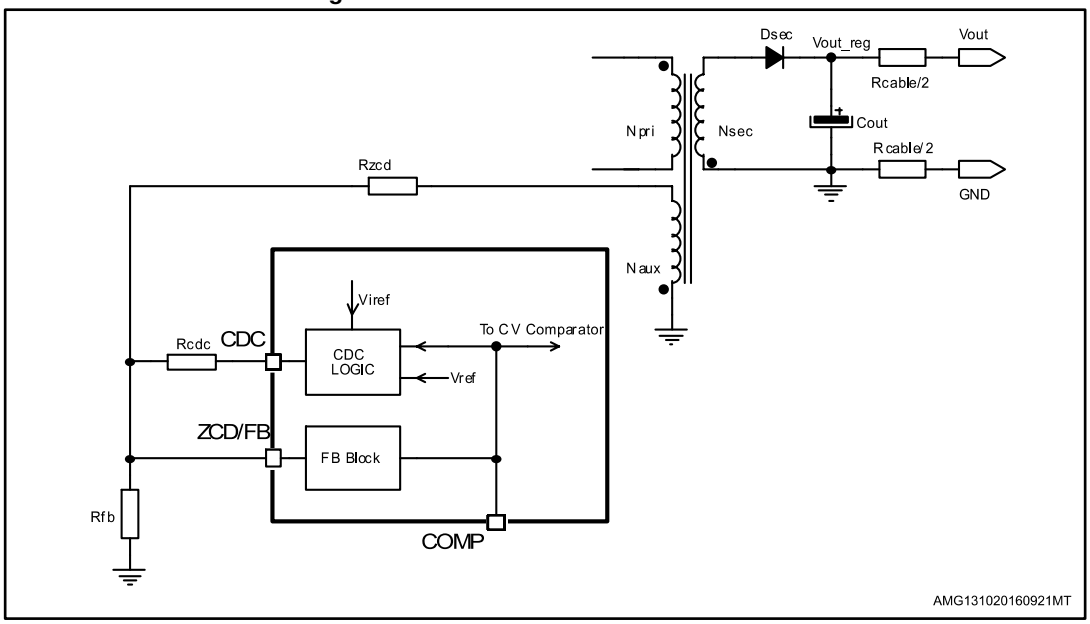
5.7 Cable drop compensation (CDC)

The voltage control loop regulates the output voltage as seen across the output capacitor.

If an output cable is used to supply the load, the voltage on the externally available terminals is dependent of the output current value. The CDC function compensates the voltage drop across the cable, so ideally zero-load regulation can be also achieved at the end of the cable.

Figure 17: "CDC block: internal schematic" presents the internal schematic.

Figure 17: CDC block: internal schematic



During CV regulation, as the CDC block is able to sink current, a resistor connected between its output and ZCD/FB pin allows the CV setpoint to be increased, by providing a voltage lower than the internal reference voltage by an amount proportional to the average load current.

If R_{CABLE} is the total cable resistance, the resistor value can be calculated by using the following equation:

Equation 5

$$R_{CDC} = \frac{2 \cdot N_{SEC}}{N_{PRI}} \cdot \frac{N_{SEC}}{N_{AUX}} \cdot \frac{R_{SENSE} \cdot R_{ZCD}}{R_{CABLE}}$$

In this equation R_{CABLE} is the total resistance of the output cable.

The CDC block acts as an outer control loop with a positive feedback that changes the CV setpoint, by affecting the stability of the overall system. In order to avoid this type of issue, the CV setpoint response time must be much lower than that of the inner voltage loop.

For this purpose the CDC block is designed with a time response of a few tens of ms. For the same reason, the minimum voltage on CDC pin is bottom limited to 2.25 V.

If the function is not required, the pin can be connected to ground or left open.

5.8 Burst-mode operation at no-load or very light load

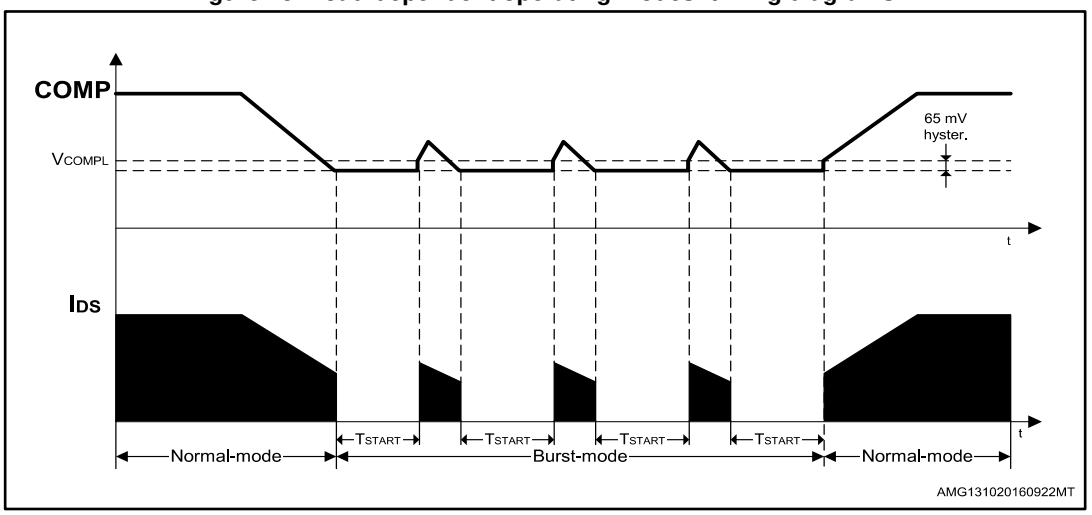
When the voltage on the COMP pin falls 65 mV below a threshold fixed internally at a value, V_{COMPBM}, the IC is disabled with the MOSFET kept in OFF-state and its consumption reduced at a lower value to minimize V_{cc} capacitor discharge.

In this condition the converter operates in burst-mode (one pulse train every T_{START} = 500 µs), with minimum energy transfer.

As a result of the energy delivery stop, the output voltage decreases: after 500 µs the controller switches on the MOSFET again and the sampled voltage on the ZCD pin is compared with the internal reference. If the voltage on the EA output, as a result of the comparison, exceeds the V_{COMPL} threshold, the device restarts switching, otherwise it stays OFF for another 500 µs period.

In this way the converter works in burst-mode with a nearly constant peak current defined by the internal disable level. Then a load decrease causes a frequency reduction, which can go down even few hundred hertz, thus minimizing all frequency-related losses and complying with energy saving regulations. This kind of operation, shown in the timing diagrams of *Figure 18: "Load-dependent operating modes: timing diagrams"*, along with the others previously described, is noise-free since the peak current is low.

Figure 18: Load-dependent operating modes: timing diagrams



5.9 Soft-start and starter block

The soft-start feature is automatically implemented by the constant current block, as the primary peak current is limited from the voltage on the C_{REF} capacitor.

During start-up, as the output voltage is zero, the IC starts in CC mode with no high peak current operations. In this way the voltage on the output capacitor increases slowly and the soft-start feature is ensured.

Actually the C_{REF} value is not important to define the soft-start time, as its duration depends on other circuit parameters, such as transformer ratio, sense resistor, output capacitors and load. The user can define the best appropriate value.

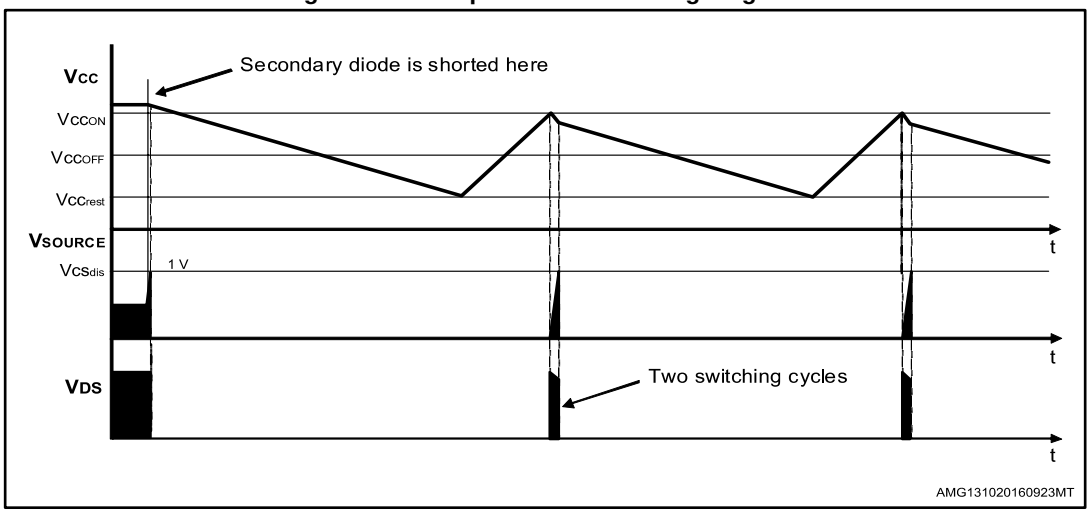
5.10 Hiccup mode OCP

The device is also protected against short-circuit of the secondary rectifier, short-circuit on the secondary winding or a hard-saturated flyback transformer. A comparator monitors continuously the voltage on the R_{SENSE} and activates a protection circuitry if this voltage exceeds 1 V.

To distinguish an actual malfunction from a disturbance (e.g. induced during ESD tests), the first time the comparator is tripped the protection circuit enters a “warning state”. If in the subsequent switching cycle the comparator is not tripped, a temporary disturbance is assumed and the protection logic is reset in its idle state; if the comparator is tripped again a real malfunction is assumed and the device is stopped.

This condition is latched as long as the device is supplied. While it is disabled, however, no energy comes from the self-supply circuit; hence the voltage on the V_{CC} capacitor decays and crosses the UVLO threshold after some time, which clears the latch. The internal start-up generator is still off, then the V_{CC} voltage still needs to go below its restart voltage before the V_{CC} capacitor is charged again and the device restarted. Ultimately, this results in a low-frequency intermittent operation (hiccup mode operation), with very low stress on the power circuit. This special condition is illustrated in the timing diagram of *Figure 19: "Hiccup mode OCP: timing diagram"*.

Figure 19: Hiccup mode OCP: timing diagram

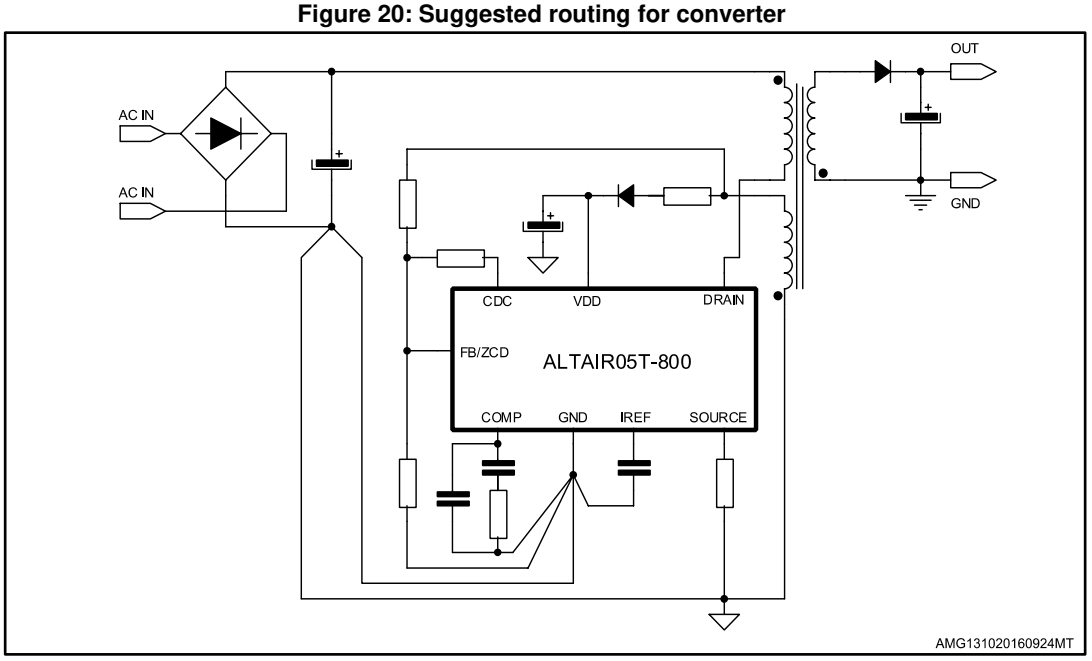


5.11 Layout recommendations

A proper printed circuit board layout is essential for the correct operation of any switch-mode converter and this is true for the ALTAIR05T-800 as well. Placing components carefully, routing traces correctly, tracing widths appropriately and compliance with isolation distances are the major issues. In particular:

- The compensation network should be connected as close as possible to the COMP pin, maintaining the trace for the GND as short as possible
- Signal ground should be routed separately from power ground and from the sense resistor trace.

Figure 20: Suggested routing for converter



6 Typical application

Figure 21: Test board schematic: 5 W wide range mains CC/CV battery charger

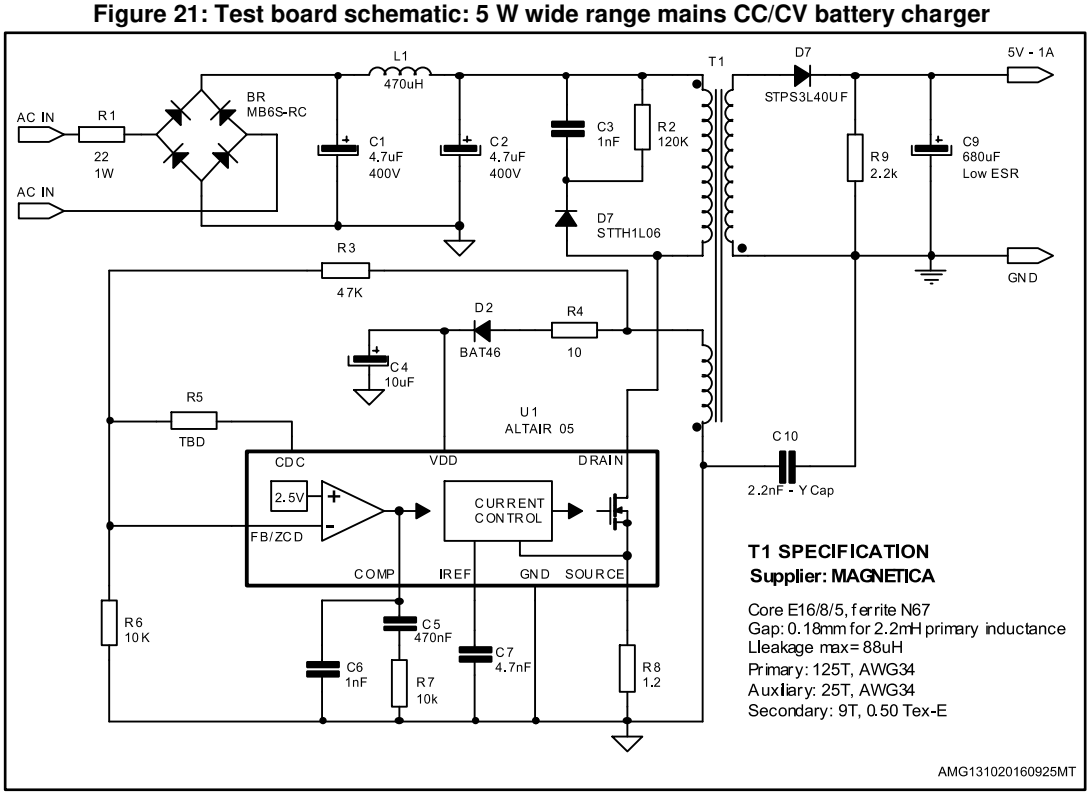


Table 5: Efficiency at 115 VAC

Load [%]	I_{OUT} [A]	V_{OUT} [V]	P_{OUT} [W]	P_{IN} [W]	Efficiency [%]
25	0.25	4.97	1.243	1.643	75.62
50	0.5	4.97	2.485	3.156	78.64
75	0.75	4.97	3.728	4.72	78.97
100	1	4.98	4.980	6.4	77.81
Average efficiency					77.79

Table 6: Efficiency at 230 VAC

Load [%]	I_{OUT} [A]	V_{OUT} [V]	P_{OUT} [W]	P_{IN} [W]	Efficiency [%]
25	0.25	4.98	1.245	1.88	66.22
50	0.5	4.97	2.485	3.349	74.18
75	0.75	4.98	3.735	4.838	77.22
100	1	4.99	4.990	6.326	78.88
Average efficiency					74.12

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

7.1 SO16N package information

Figure 22: SO16N package outline

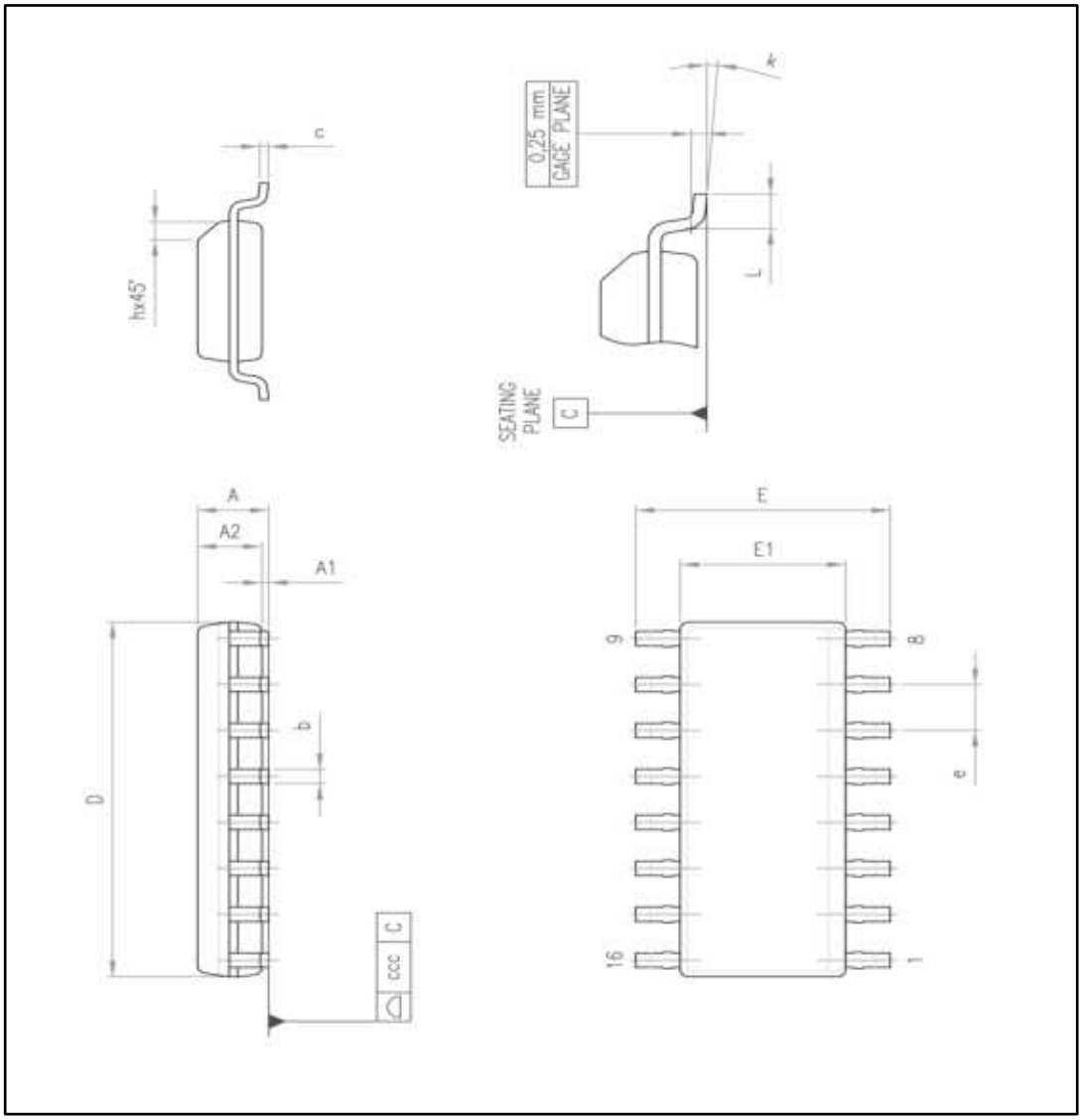


Table 7: SO16N mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

8 Order code

Table 8: Ordering information

Order code	Package	Packing
ALTAIR05T-800	SO16N	Tube
ALTAIR05T-800TR		Tape and reel

9 Revision history

Table 9: Document revision history

Date	Revision	Changes
25-Oct-2010	1	Initial release.
20-Oct-2016	2	Updated *Table 2: "Absolute maximum ratings"*, *Section 4: "Electrical characteristics"* and *Section 7: "Package information"*. Minor text changes.

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