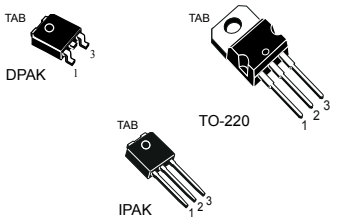
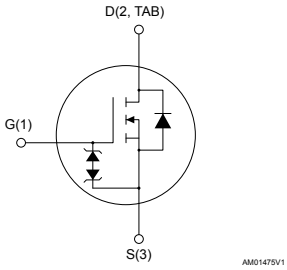
Datasheet

N-channel 525 V, 2.1 Ω typ., 2.5 A MDmesh™ K3 Power MOSFETs in DPAK, TO-220 and IPAK packages





Product status link
STD4N52K3
STP4N52K3
STU4N52K3

Features

Order code	V_{DS}	$R_{DS(on)}$max.	I_D	Package
STD4N52K3	525 V	2.6 Ω	2.5 A	DPAK
STP4N52K3			2.5 A	TO-220
STU4N52K3			2.5 A	IPAK

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

These MDmesh™ K3 Power MOSFETs are the result of improvements applied to STMicroelectronics' MDmesh™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	525	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	2.5	A
I_D	Drain current (continuous) at T_C = 100 °C	2	A
I_{DM} (1)	Drain current (pulsed)	10	A
P_{TOT}	Total dissipation at T_C = 25 °C	45	W
dv/dt (2)	Peak diode recovery voltage slope	12	V/ns
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 2.5 A, di/dt ≤ 400 A/µs, V_{DSpeak} ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220	IPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.78		2.78	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient		62.5	100	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	50			°C/W

1. *When mounted on 1inch² FR-4 board, 2 oz Cu.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} (1)	Avalanche current, repetitive or not-repetitive	1.3	A
E_{AS} (2)	Single pulse avalanche energy	110	mJ

1. *Pulse width limited by T_j max.*
2. *Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.*

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	525			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 525 V			1	µA
		V_{GS} = 0 V, V_{DS} = 525 V, T_C = 125 °C (1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 1.25 A		2.1	2.6	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	334	-	pF
C_{oss}	Output capacitance			28		
C_{rss}	Reverse transfer capacitance			5		
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 420 V, V_{GS} = 0 V	-	20	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	4	-	Ω
Q_g	Total gate charge	V_{DD} = 420 V, I_D = 2.5 A, V_{GS} = 0 to 10 V (see Figure 16. Test circuit for gate charge behavior)	-	11	-	nC
Q_{gs}	Gate-source charge			2		
Q_{gd}	Gate-drain charge			7		

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 420 V.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 260 V, I_D = 1.25 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	8	-	ns
t_r	Rise time			7		
$t_{d(off)}$	Turn-off delay time			21		
t_f	Fall time			14		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.5	A
I_{SDM} (1)	Source-drain current (pulsed)				10	
V_{SD} (2)	Forward on voltage	I_{SD} = 2.5 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 2.5 A, di/dt = 100 A/µs	-	173		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V (see Figure 17. Test circuit for inductive load switching and diode recovery times)		778		nC
I_{RRM}	Reverse recovery current			9		A
t_{rr}	Reverse recovery time	I_{SD} = 2.5 A, di/dt = 100 A/µs	-	196		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_j = 150 °C (see Figure 17. Test circuit for inductive load switching and diode recovery times)		941		nC
I_{RRM}	Reverse recovery current			10		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics curves

Figure 1. Safe operating area for DPAK/IPAK

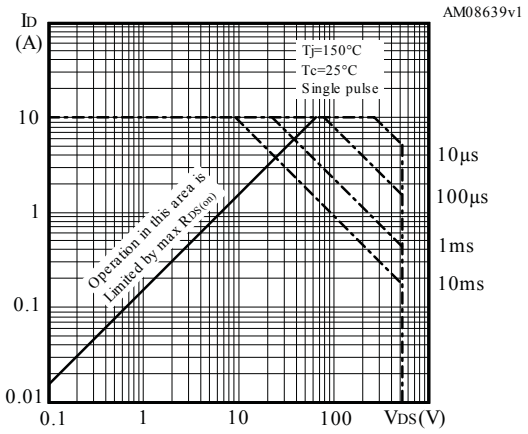


Figure 2. Thermal impedance for DPAK/IPAK

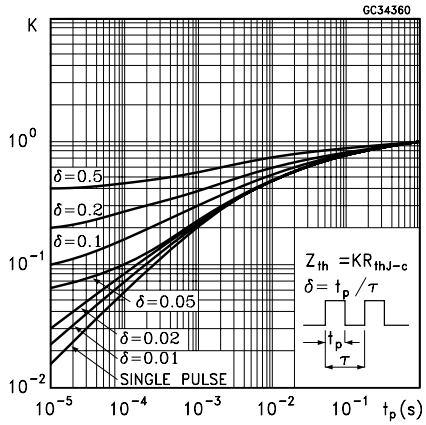


Figure 3. Safe operating area for TO-220

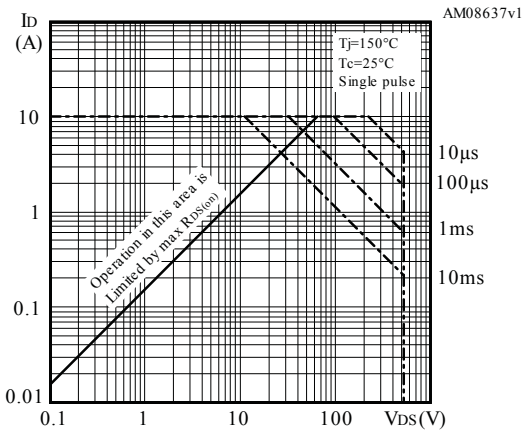


Figure 4. Thermal impedance for TO-220

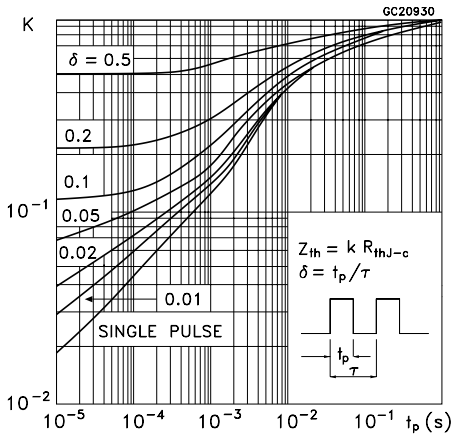


Figure 5. Output characterisics

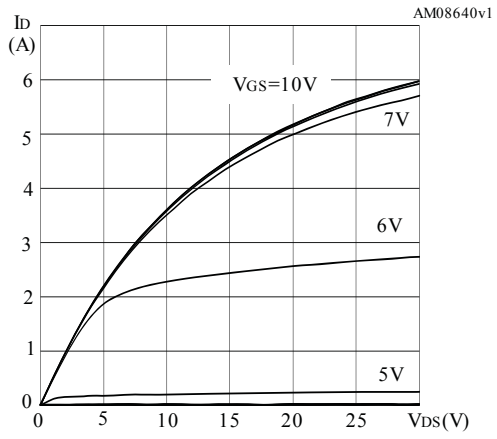


Figure 6. Transfer characteristics

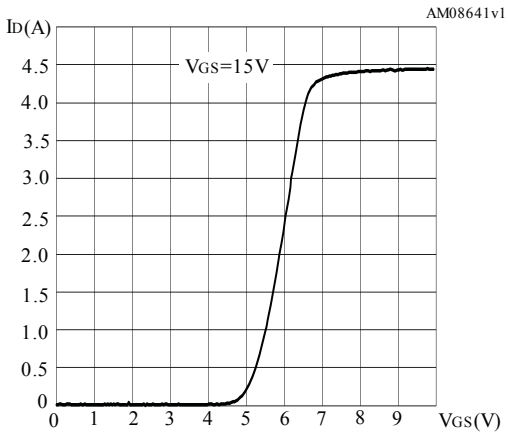


Figure 7. Normalized $V_{(BR)DSS}$ vs temperature

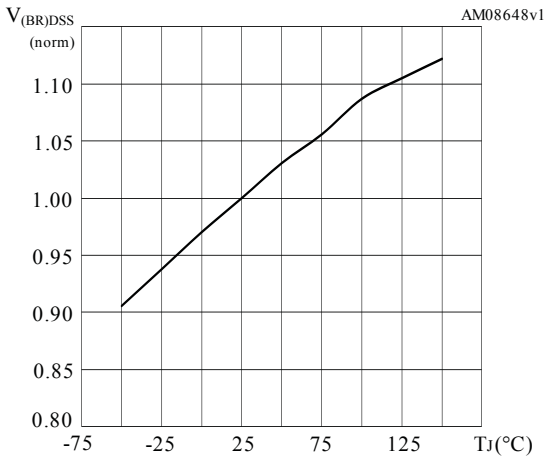


Figure 8. Static drain-source on-resistance

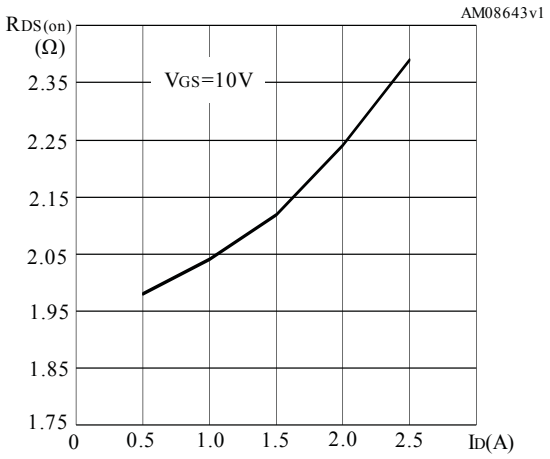


Figure 9. Gate charge vs gate-source voltage

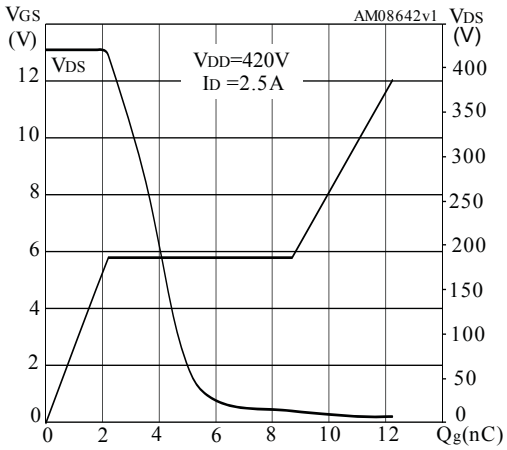


Figure 10. Capacitance variations

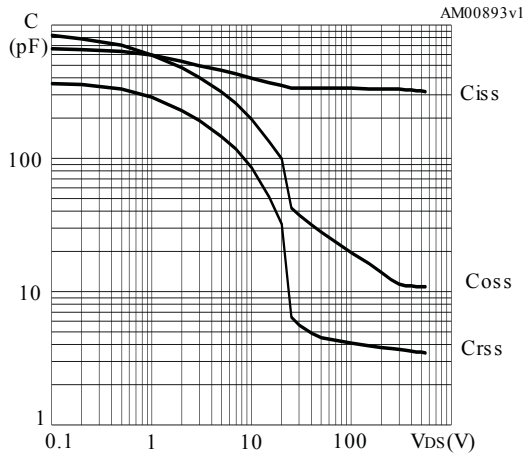


Figure 11. Normalized gate threshold voltage vs temperature

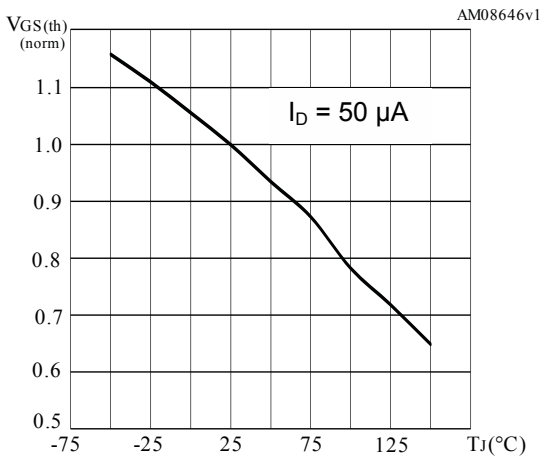


Figure 12. Normalized on-resistance vs temperature

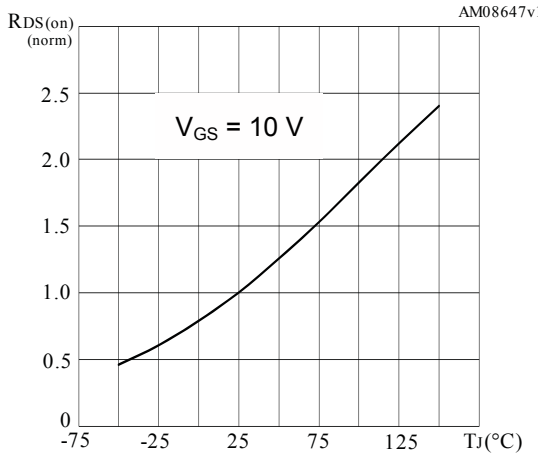


Figure 13. Source-drain diode forward characteristics

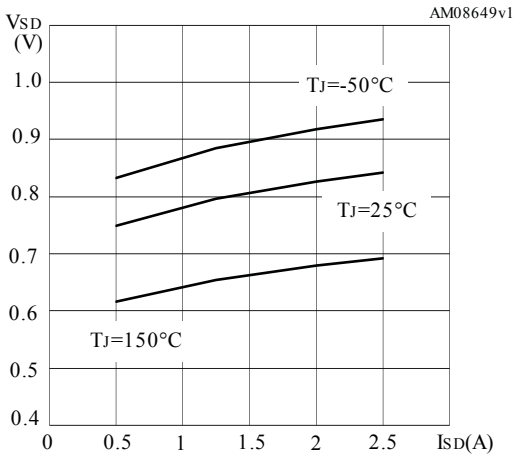
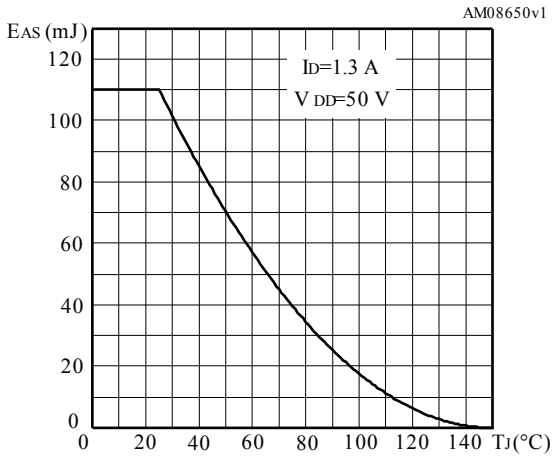


Figure 14. Maximum avalanche energy vs temperature



3 Test circuits

Figure 15. Test circuit for resistive load switching times

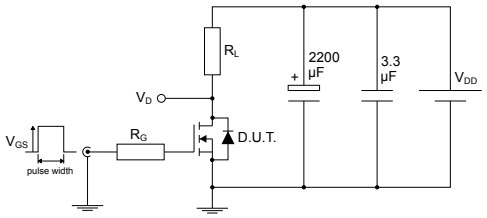


Figure 16. Test circuit for gate charge behavior

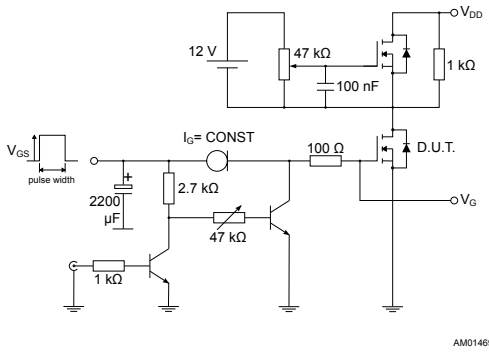


Figure 17. Test circuit for inductive load switching and diode recovery times

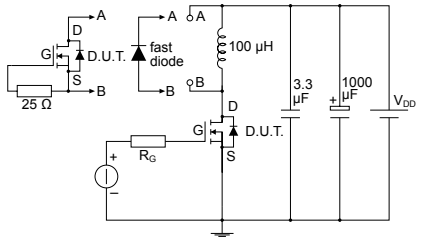


Figure 18. Unclamped inductive load test circuit

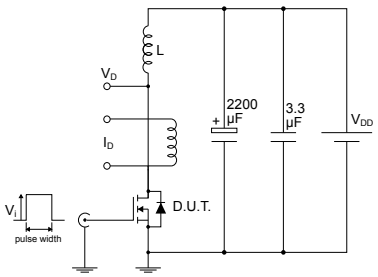


Figure 19. Unclamped inductive waveform

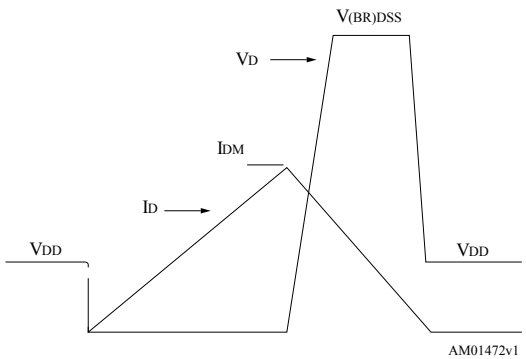
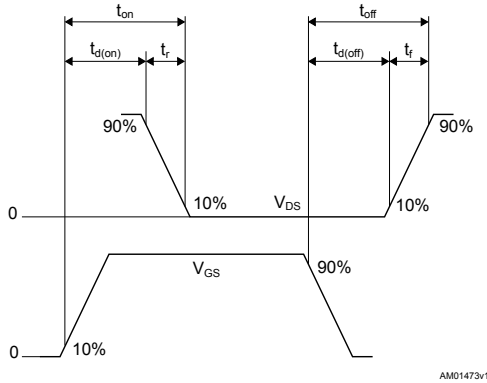


Figure 20. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 21. **DPAK (TO-252) type A package outline**

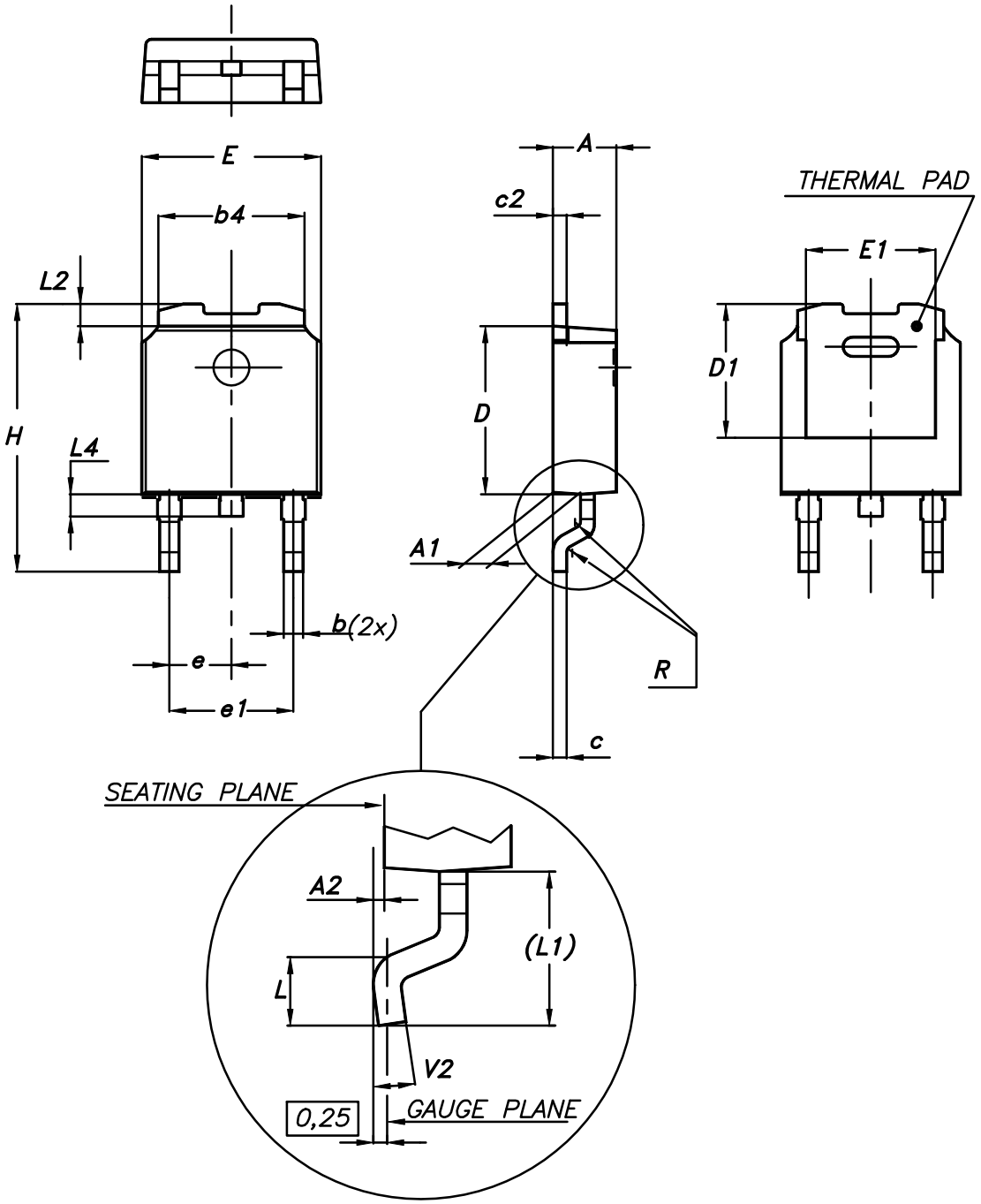


Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C package information

Figure 22. **DPAK (TO-252) type C package outline**

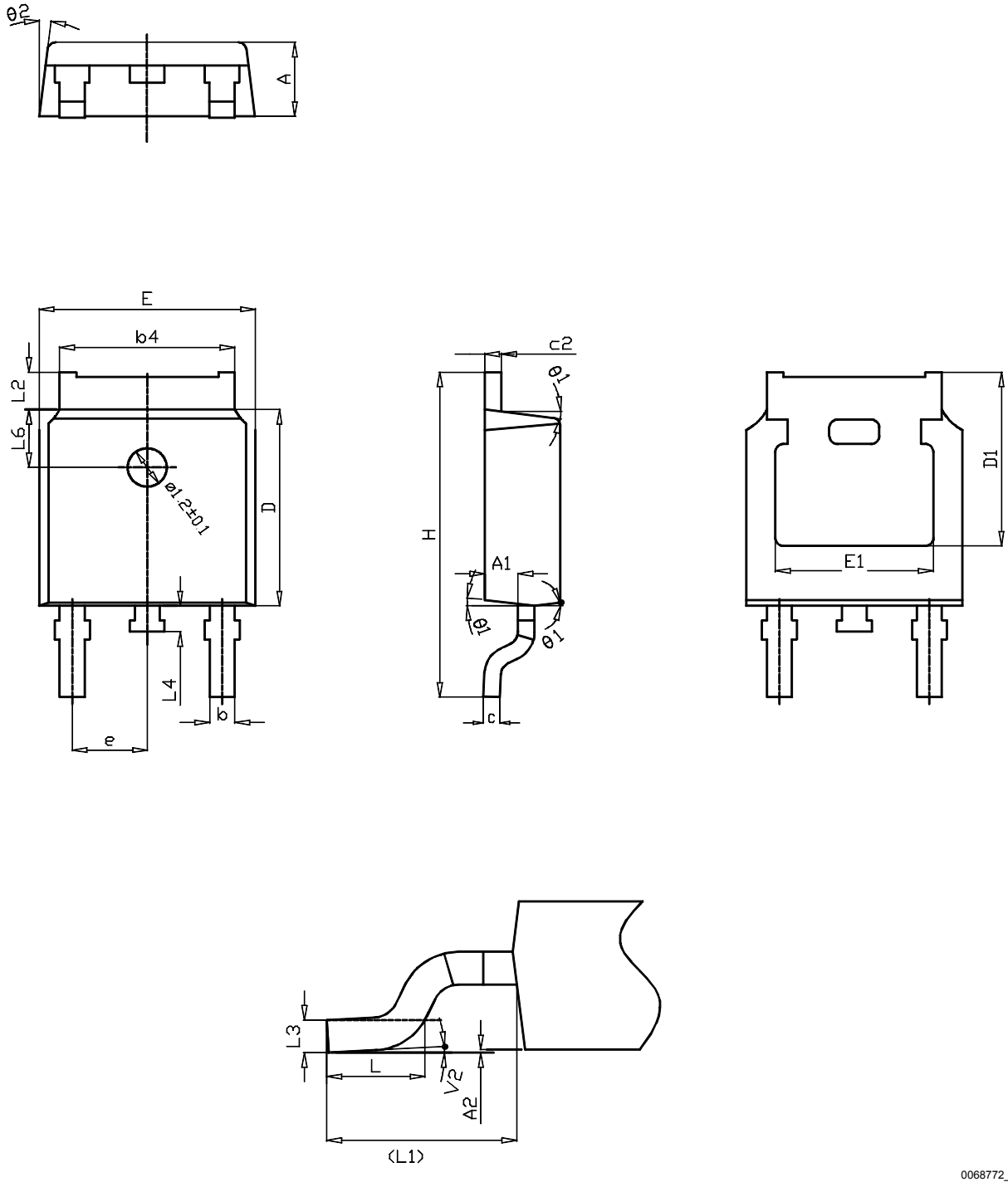
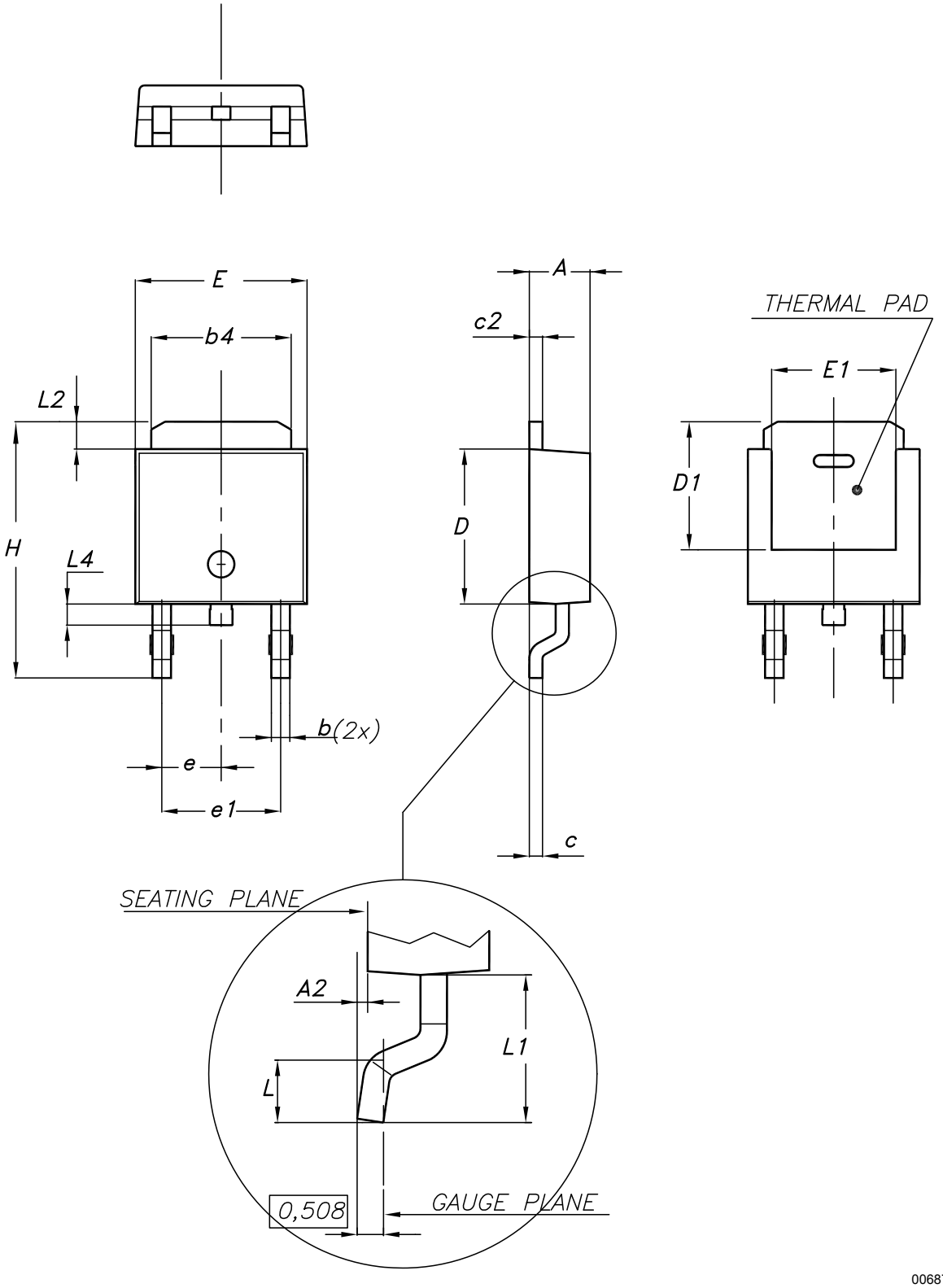


Table 10. **DPAK (TO-252) type C mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

4.3 DPAK (TO-252) type E package information

Figure 23. **DPAK (TO-252) type E package outline**

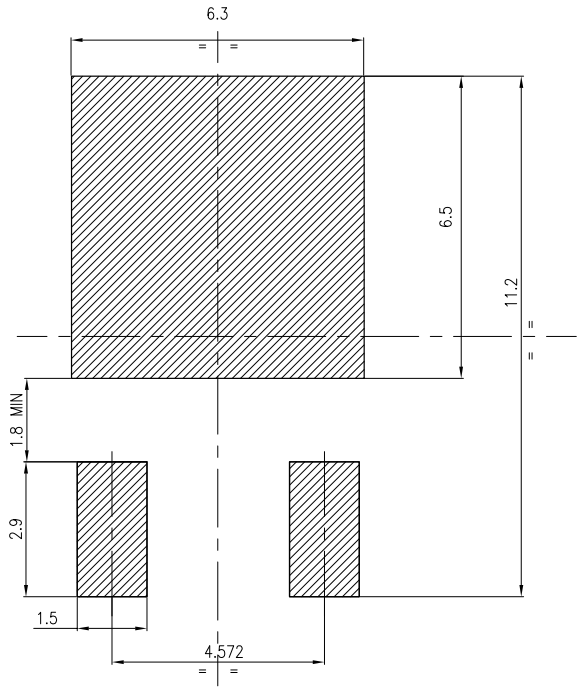


0068772_type-E_rev.25

Table 11. **DPAK (TO-252) type E mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 24. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



FP_0068772_25

4.4 DPAK (TO-252) packing information

Figure 25. **DPAK (TO-252) tape outline**

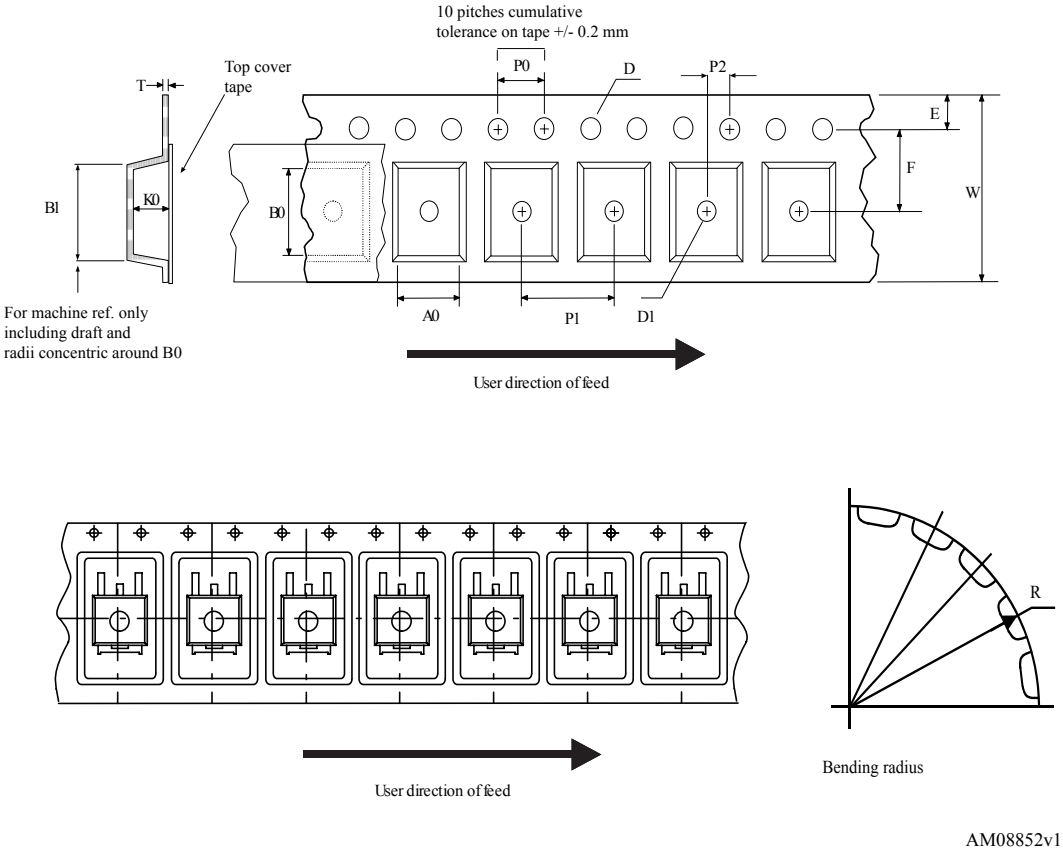
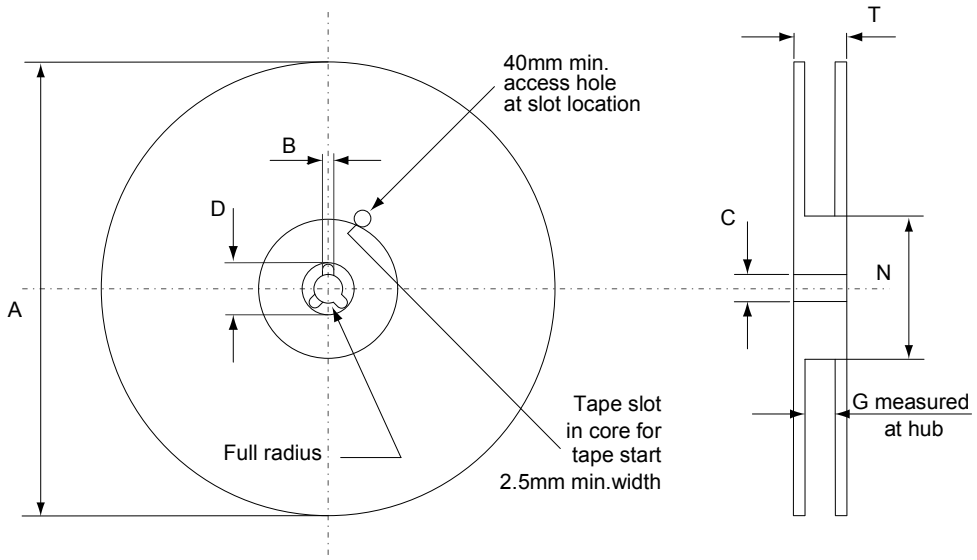


Figure 26. **DPAK (TO-252) reel outline**



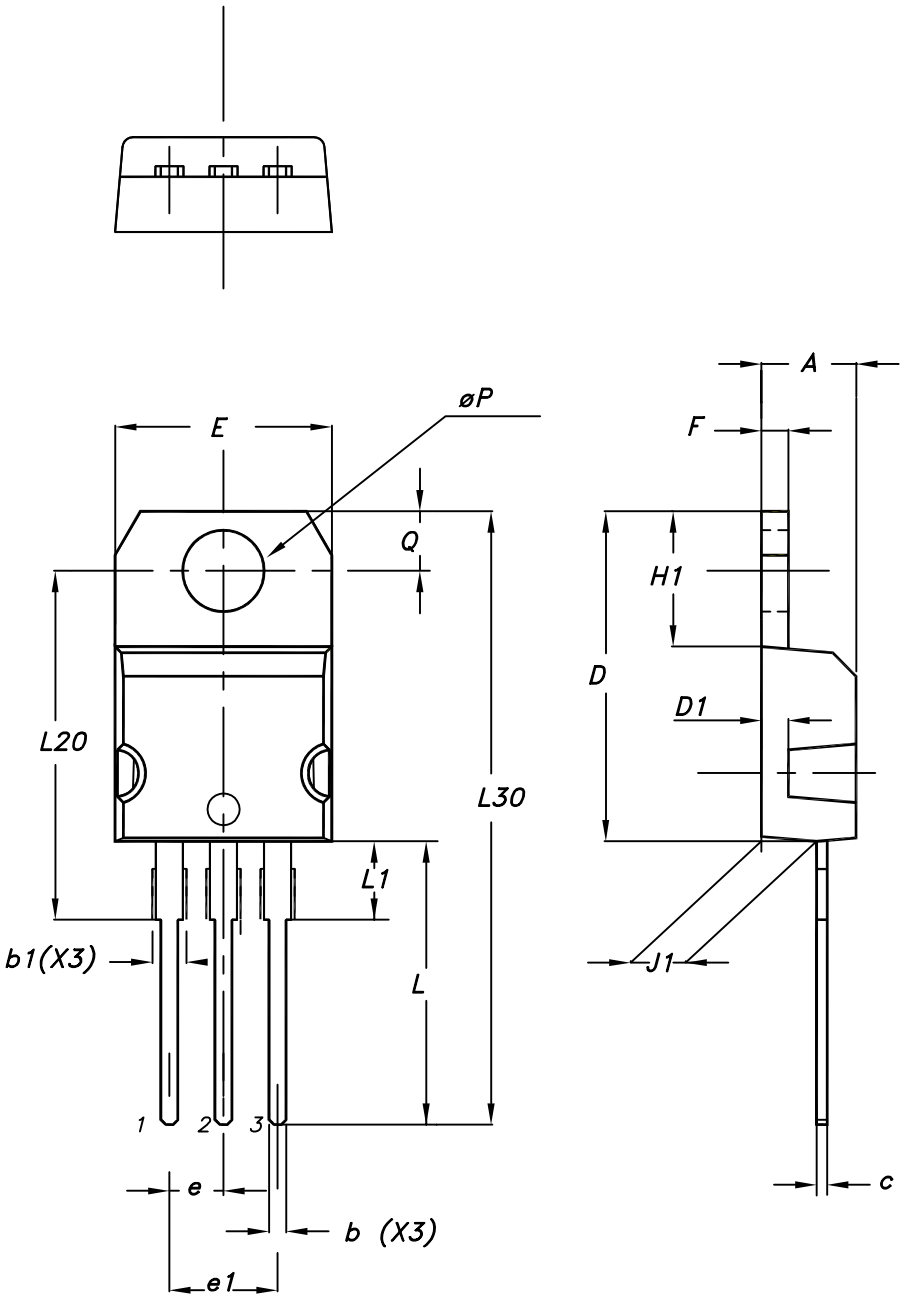
AM06038v1

Table 12. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.5 TO-220 type A package information

Figure 27. **TO-220 type A package outline**



0015988_typeA_Rev_21

Table 13. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.6 IPAK (TO-251) type A package information

Figure 28. **IPAK (TO-251) type A package outline**

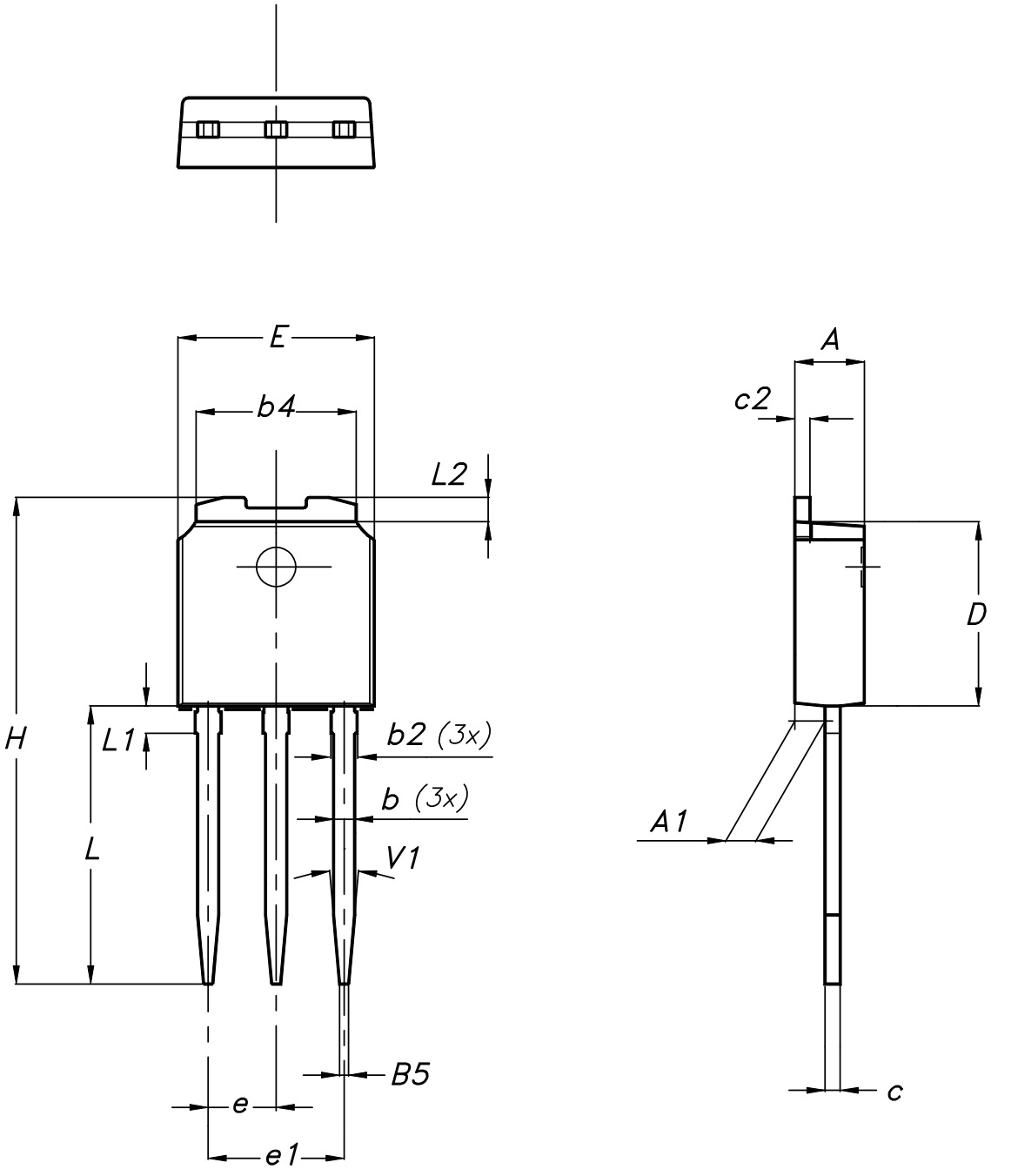
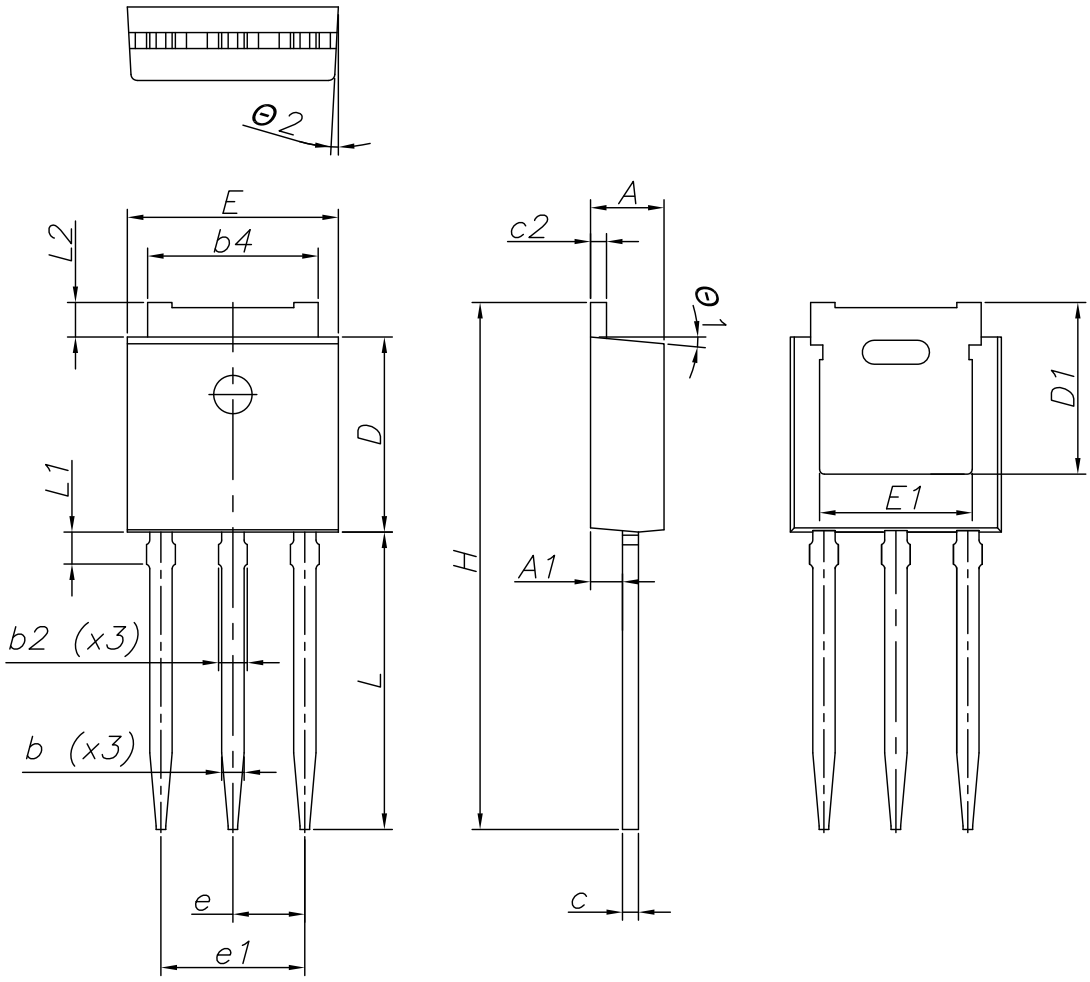


Table 14. **IPAK (TO-251) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.7 IPAK (TO-251) type C package information

Figure 29. **IPAK (TO-251) type C package outline**



0068771_IK_typeC_rev14

Table 15. **IPAK (TO-251) type C package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

5 Ordering information

Table 16. **Order codes**

Order code	Marking	Package	Packing
STD4N52K3	4N52K3	DPAK	Tape and reel
STP4N52K3		TO-220	Tube
STU4N52K3		IPAK	Tube

Revision history

Table 17. **Document revision history**

Date	Version	Changes
09-Nov-2010	1	First release
19-Feb-2013	2	Updated packages order in Table 1: Device summary. Updated Table 4: Package mechanical data and Table 5: Packaging mechanical data. Minor text changes on the cover page.
20-Aug-2018	3	The part number STF4N52K3 has been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Updated title and features in cover page. Updated Section 1 Electrical ratings, Section 2 Electrical characteristics and Section 2.1 Electrical characteristics curves. Added Section 5 Ordering information. Minor text changes.

Contents

1 **Electrical ratings** 2
2 **Electrical characteristics** 3
2.1 Electrical characteristics curves 5
3 **Test circuits** 8
4 **Package information** 9
4.1 DPAK (TO-252) type A package information 9
4.2 DPAK (TO-252) type C package information 11
4.3 DPAK (TO-252) type E package information 13
4.4 DPAK (TO-252) packing information 15
4.5 TO-220 type A package information 17
4.6 IPAK (TO-251) type A package information 19
4.7 IPAK (TO-251) type C package information 21
5 **Ordering information** 24
Revision history 25

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved