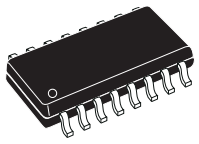
ALTAIR04-900

Off-line all-primary-sensing switching regulator

Datasheet - production data



SO16N

Features

- Optoless primary side constant voltage operations
- Adjustable and mains-independent maximum output current for safe operations during overload/short-circuit conditions
- 900 V avalanche-rugged internal power section
- Quasi-resonant valley switching operation
- Low standby consumption
- Overcurrent protection against transformer saturation and secondary diode short-circuit
- SO16N package

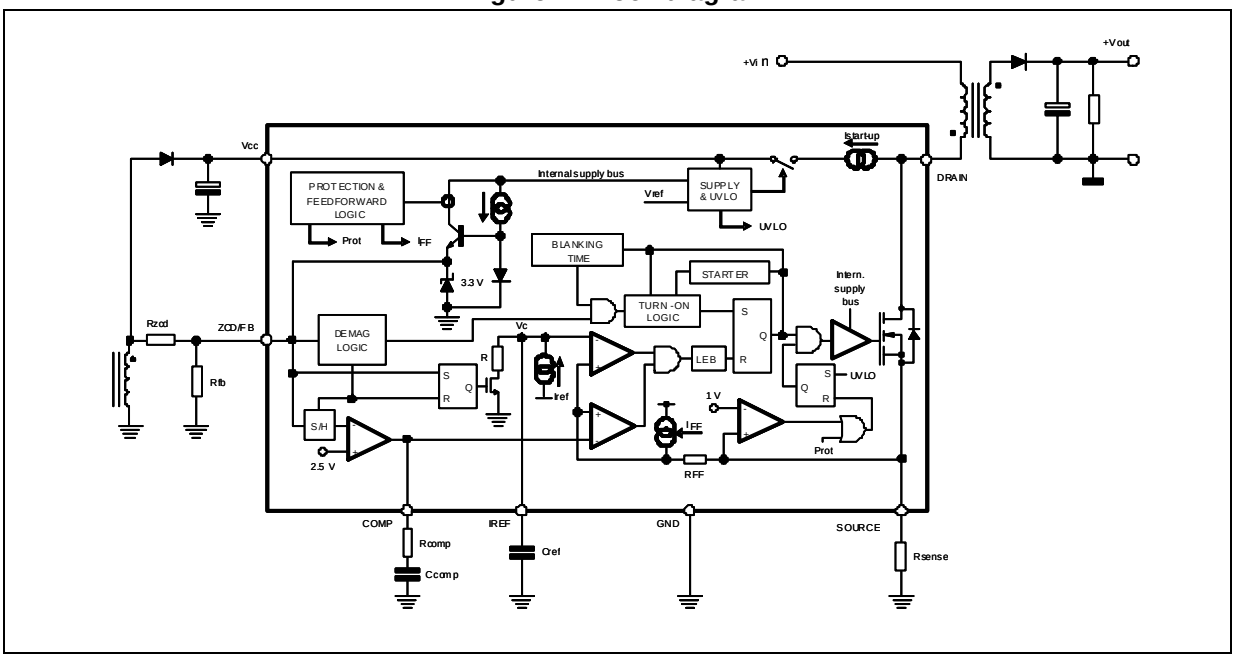
Applications

- SMPS for energy metering
- Auxiliary power supplies for 3-phase input industrial systems
- AC-DC adapters

Description

The ALTAIR04-900 is a high voltage all-primary-sensing switcher, operating directly from the rectified mains with minimum external parts. It combines a high-performance low voltage PWM controller chip and a 900 V avalanche-rugged power section in the same package.

Figure 1. Block diagram



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1 Description

This device combines two silicons in the same package: a low voltage PWM controller and a 900 V avalanche-rugged power section.

The controller is in current-mode specifically designed for off-line quasi-resonant flyback converters.

The device provides a constant output voltage using the primary-sensing feedback. This eliminates the need for the optocoupler, the secondary voltage reference, as well as the current sensor, still maintaining an accurate regulation. Besides, the maximum deliverable output current can be set so to increase the end-product safety and reliability during fault events.

Quasi-resonant operation is guaranteed by a transformer demagnetization sensing input which turns on the power section. The same input also serves the output voltage monitoring, to perform CV regulation, and to achieve mains-independent maximum deliverable output current (line voltage feed-forward).

The maximum switching frequency is top-limited 166 kHz, so that at light-to-medium load a special function automatically lowers the operating frequency still maintaining the valley switching operation. When the load is very light, the device enters a controlled burst-mode operation that, along with the built-in high voltage start-up circuit and the low operating current, minimizes the standby power.

Although an auxiliary winding is required in the transformer to correctly perform CV/CC regulation, the chip powers itself directly from the rectified mains. This is important during CC regulation, where the flyback voltage, generated by the winding, drops below UVLO threshold.

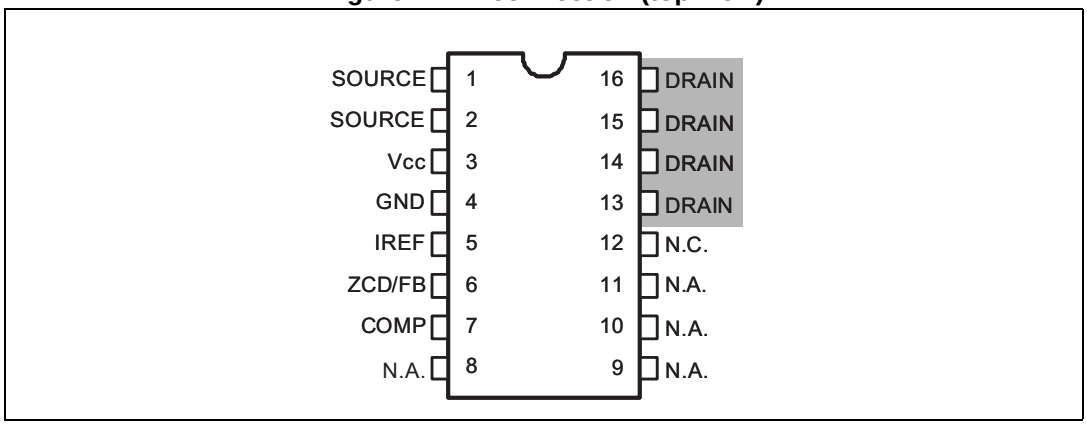
However, if ultra low no-load input consumption is required to comply with the most strict energy-saving recommendations, then the device needs to be powered by the auxiliary winding.

These functions optimize power handling under different operating conditions. The device offers protection features that, in auto restart-mode, increase end-product safety and reliability:

- Auxiliary winding disconnection, or brownout
- Detection
- Shorted secondary rectifier, or transformer saturation

2 Pin connection

Figure 2. Pin connection (top view)



Note: The copper area has to be placed under the drain pins to dissipate heat.

Table 1. Pin functions

Number	Name	Function
1, 2	SOURCE	Power section source and input to the PWM comparator. The current, flowing through MOSFET, is sensed by a resistor connected between the pin and GND. The resulting voltage is compared with an internal reference (0.75 V max.) to determine the MOSFET turn-off. The pin is equipped with 250 ns blanking time, after the gate-drive output goes high for noise immunity. If a second comparison level located at 1 V is exceeded the IC is stopped and restarted after Vcc has dropped below 5 V.
3	Vcc	Supply voltage of the device. An electrolytic capacitor, connected between this pin and ground, is initially charged by the internal high voltage start-up generator; when the device runs, the same generator keeps it charged if the voltage, supplied by the auxiliary winding, is not sufficient. This feature is disabled if a protection is tripped. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to get a clean bias voltage for the signal part of IC.
4	GND	Ground. Current return both for IC signal part and the gate-drive. All ground connections of bias components should be tied to a trace and kept separated from any pulsed current return.
5	IREF	CC regulation loop reference voltage. An external capacitor has to be connected between this pin and GND. An internal circuit develops a voltage on this capacitor used as the reference for peak drain current of the MOSFET during CC regulation. The voltage is automatically adjusted to keep the average output current constant.

Table 1. Pin functions (continued)

Number	Name	Function
6	ZCD/FB	Transformer demagnetization sensing for quasi-resonant operation. Input/output voltage monitoring. A negative-going edge triggers the MOSFET turn-on. The current sourced by the pin during on-time is monitored to compensate the internal delay of the current sensing circuit and achieve a CC regulation independent of the mains voltage. If this current does not exceed 50 µA, either a floating pin or a low input voltage is assumed, the device is stopped and restarted after Vcc has dropped below 5 V. Besides, the pin voltage is sampled-and-held right at the end of the transformer demagnetization to get an accurate image of the output voltage to be fed to the inverting input of the internal transconductance-type error amplifier, whose non-inverting input is 2.5 V. The maximum $I_{ZCD/FB}$ sunk/sourced current doesn't exceed ±2 mA (AMR) in all Vin range conditions. No capacitor is allowed between the pin and the auxiliary transformer.
7	COMP	Output of the internal transconductance error amplifier. The compensation network is placed between this pin and GND to achieve stability and good dynamic performance of the voltage control loop.
8-11	N.A	Not available. These pins must be left not connected.
12	N.C	Not internally connected.
13 to 16	DRAIN	Drain connection of the internal power section. The internal high voltage start-up generator sinks current from these pins as well. Pins are connected to the internal metal frame to facilitate heat dissipation.

3 Maximum ratings

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{DS}	1,2, 13-16	Drain-to-source (ground) voltage	-1 to 900	V
I_D	1,2, 13-16	Drain current	0.7	A
E_{av}	1,2, 13-16	Single pulse avalanche energy (T_j = 25 °C, I_D = 0.7 A)	25	mJ
Vcc	3	Supply voltage (Icc < 25 mA)	Self limiting	V
$I_{ZCD/FB}$	6	Zero-current detector current	±2	mA
V_{comp}	8	Analog input	-0.3 to 3.6	V
P_{tot}		Power dissipation @T_A = 50 °C	0.9	W
T_j		Junction temperature range	-40 to 150	°C
T_{stg}		Storage temperature	-55 to 150	°C

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj\text{-}pin}$	Thermal resistance, junction-to-pin	10	°C/W
$R_{thj\text{-}amb}$	Thermal resistance, junction-to-ambient	110	

4 Electrical characteristics

(T_J = -40 to 125 °C, Vcc = 14 V; unless otherwise specified)

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Power section						
$V_{(BR)DSS}$	Drain-source breakdown	I_D< 100 µA; T_j = 25 °C	900			V
I_{DSS}	Off-state drain current	V_{DS} = 850 V; T_j = 125 °C (See *Figure 4* and note)			80	µA
$R_{DS(on)}$	Drain-source on-state resistance	Id=250 mA; T_j = 25 °C		16	19	Ω
		Id=250 mA; T_j = 125 °C			38	
C_{oss}	Effective (energy-related) output capacitance	(See *Figure 3*)				
High voltage start-up generator						
V_{Start}	Min. drain start voltage	I_{charge} < 100 µA	40	50	60	V
I_{charge}	Vcc start-up charge current	V_{DRAIN}> V_{Start}; Vcc < Vcc_{On} T_j = 25 °C	4	5.5	7	mA
		V_{DRAIN}> V_{Start}; Vcc < Vcc_{On}	+/-10%			
$V_{CCrestart}$	Vcc restart voltage (Vcc falling)	(1)	9.5	10.5	11.5	V
		After protection tripping		5		
Supply voltage						
Vcc	Operating range	After turn-on	11.5		23	V
Vcc_{On}	Turn-on threshold	(1)	12	13	14	V
Vcc_{Off}	Turn-off threshold	(1)	9	10	11	V
V_Z	Zener voltage	Icc = 20 mA	23	25	27	V
Supply current						
$Icc_{start-up}$	Start-up current	(See *Figure 5*)		200	300	µA
Iq	Quiescent current	(See *Figure 6*)		1	1.4	mA
Icc	Operating supply current @ 50 kHz	(See *Figure 7*)		1.4	1.7	mA
$Iq_{(fault)}$	Fault quiescent current	During hiccup and brownout (See *Figure 8*)		250	350	µA
Start-up timer						
T_{START}	Start timer period		100	125	175	µs
$T_{RESTART}$	Restart timer period during burst-mode		400	500	700	µs

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Zero-current detector						
I_{ZCDb}	Input bias current	V_{ZCD} = 0.1 to 3 V		0.1	1	µA
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 1 mA	3.0	3.3	3.6	V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 1 mA	-90	-60	-30	mV
V_{ZCDA}	Arming voltage	Positive-going edge	100	110	120	mV
V_{ZCDT}	Triggering voltage	Negative-going edge	50	60	70	mV
I_{ZCDON}	Min. source current during MOSFET on-time		-25	-50	-75	µA
T_{BLANK}	Trigger blanking time after MOSFET turn-off	$V_{COMP} \geq 1.3$ V		6		µs
		V_{COMP} = 0.9 V		30		
Line feed-forward						
R_{FF}	Equivalent feed-forward resistor	I_{ZCD} = 1 mA		45		Ω
Transconductance error amplifier						
V_{REF}	Voltage reference	T_j = 25 °C (1)	2.46	2.5	2.54	V
		T_j = -40 to 125 °C and Vcc = 12 V to 23 V (1)	2.42		2.58	
gm	Transconductance	ΔI_{COMP} = ±10 µA V_{COMP} = 1.65 V	1.3	2.2	3.2	mS
Gv	Voltage gain	Open loop		73		dB
GB	Gain-bandwidth product			500		KHz
I_{COMP}	Source current	V_{ZCD} = 2.3 V, V_{COMP} = 1.65 V	70	100		µA
	Sink current	V_{ZCD} = 2.7 V, V_{COMP} = 1.65 V	400	750		µA
V_{COMPH}	Upper COMP voltage	V_{ZCD} = 2.3 V		2.7		V
V_{COMPL}	Lower COMP voltage	V_{ZCD} = 2.7 V		0.7		V
V_{COMPBM}	Burst-mode threshold			1		V
Hys	Burst-mode hysteresis			65		mV
Current reference						
V_{IREFx}	Maximum value	$V_{COMP} = V_{COMPL}$ (1)	1.5	1.6	1.7	V
G_I	Current loop gain	$V_{COMP} = V_{COMPH}$	0.5	0.6	0.7	
V_{CREF}	Current reference voltage		0.38	0.4	0.42	V
Current sense						
t_{LEB}	Leading-edge blanking		200	250	300	ns
td(H-L)	Delay-to-output			300		ns
V_{CSx}	Max. clamp value	dVcs/dt = 200 mV/µs (1)	0.7	0.75	0.8	V
V_{CSdis}	Hiccup-mode OCP level	(1)	0.92	1	1.08	V

1. Parameters track one to each other

Figure 3. C_{OSS} output capacitance variation

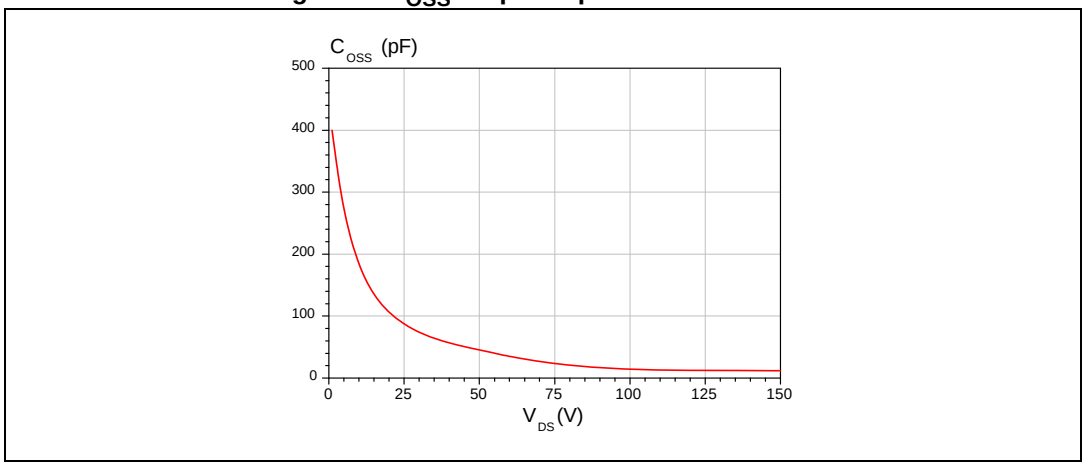
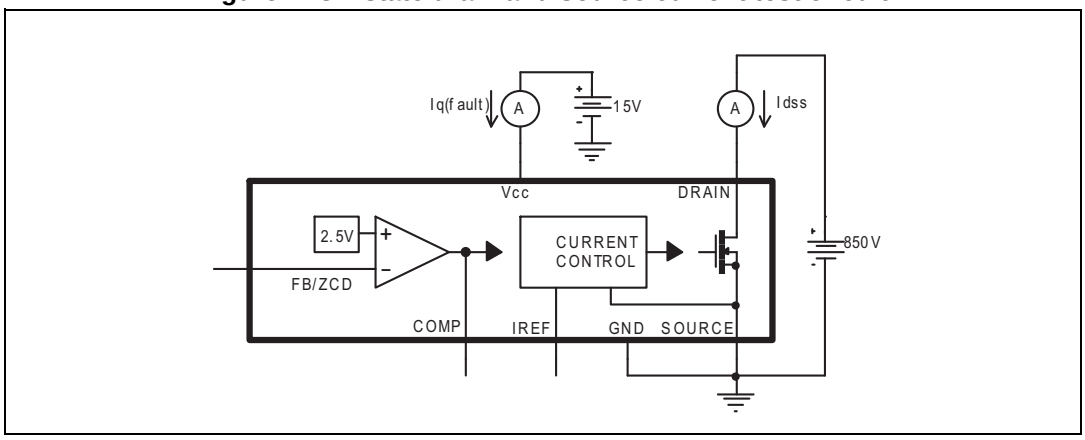


Figure 4. Off-state drain and source current test circuit



Note: The measured I_{DSS} is the sum between the current across the start-up resistor and the MOSFET off-state drain current.

Figure 5. Start-up current test circuit

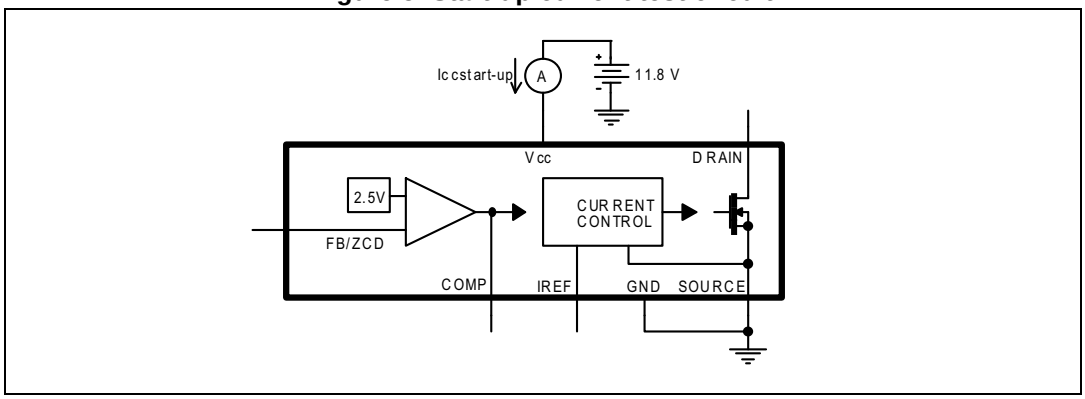


Figure 6. Quiescent current test circuit

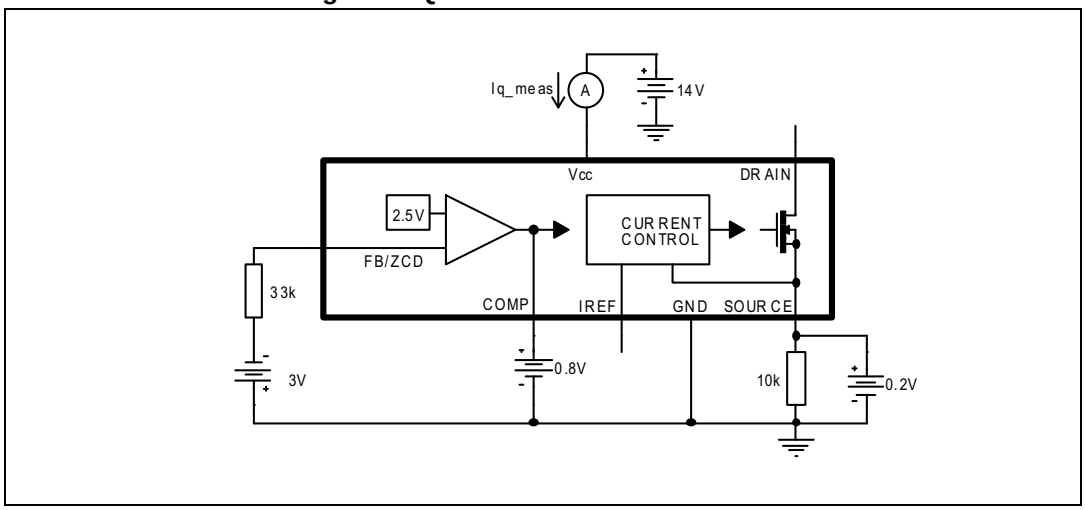
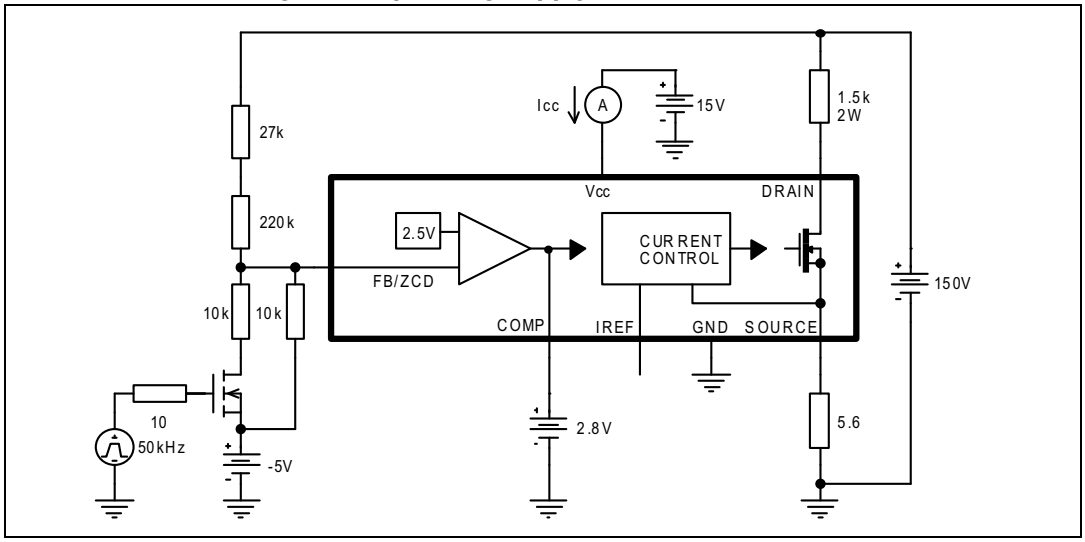
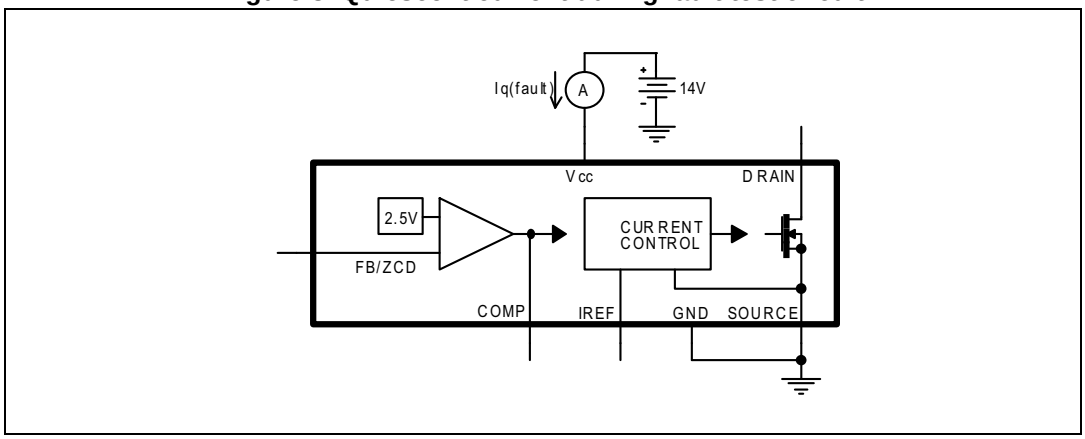


Figure 7. Operating supply current test circuit



Note: The circuit across the ZCD pin is used for the switch-on synchronization.

Figure 8. Quiescent current during fault test circuit



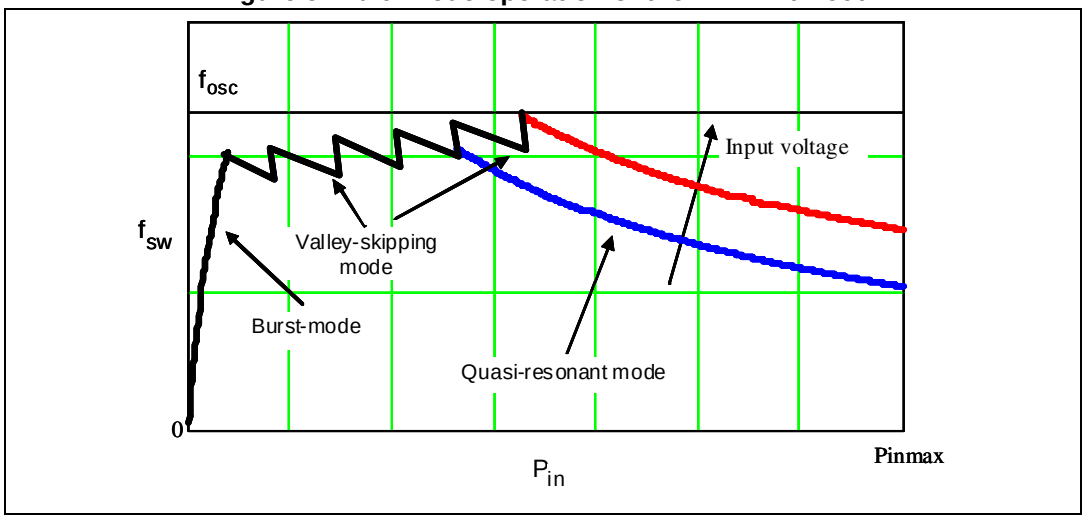
5 Application information

The device is an all-primary-sensing switching regulator, based on quasi-resonant flyback topology.

According to the load conditions of the converter, the device can work in different modes (see *Figure 9*):

1. QR-mode at heavy load. Quasi-resonant operation synchronizes MOSFET turn-on and the demagnetization of the transformer by detecting the resulting negative-going edge of the voltage across any winding of the transformer. The system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer. Therefore, the switching frequency is different according to different line/load conditions (see the hyperbolic-like portion of the curves in *Figure 9*). Minimum turn-on losses, low EMI emissions and safe behavior in short-circuit are the main benefits of this operation.
2. Valley-skipping-mode at light-to-medium load. According to voltage on COMP pin, the device defines the maximum operating frequency of the converter. As the load is reduced, MOSFET turn-on doesn't occur on the first valley but on the second one, the third one and so on. In this manner, the switching frequency doesn't rise (piecewise linear portion in *Figure 9*).
3. Burst-mode with or without very light load. When the load is extremely light or disconnected, the converter enters a controlled on/off operation with a constant peak current. Decreasing the load results even few hundred hertz minimizes all frequency-related losses and makes it easier to comply with energy saving regulations or recommendations. Being the peak current very low, no issue of audible noise arises.

Figure 9. Multi-mode operation of the ALTAIR04-900



5.1 Power section and gate driver

The power section guarantees the safe avalanche operation within the specified energy rating as well as high dv/dt capability. The MOSFET has a $V_{(BR)DSS}$ of 900 V min. and a typical $R_{DS(on)}$ of 16 Ω.

The gate driver is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common-mode EMI. Under UVLO conditions, an internal pull-down circuit holds the gate low in order to ensure that the MOSFET cannot be turned on accidentally.

5.2 High voltage start-up generator

Figure 10 shows the internal schematic of the high voltage start-up generator (HV generator). The HV current generator is supplied through the DRAIN pin and it is enabled only if the input bulk capacitor voltage is higher than V_{Start} threshold, 50 V_{DC} typically. When the HV current generator is on, the I_{charge} current (5.5 mA typical value) is delivered to the capacitor on the Vcc pin.

With reference to the timing diagram in *Figure 10*, when power is applied to the circuit and the voltage on the input bulk capacitor is high, the HV generator is sufficiently biased to start operating, thus it draws about 5.5 mA (typical) from the bulk capacitor. This current charges the bypass capacitor connected between the Vcc pin and ground and rises its voltage linearly.

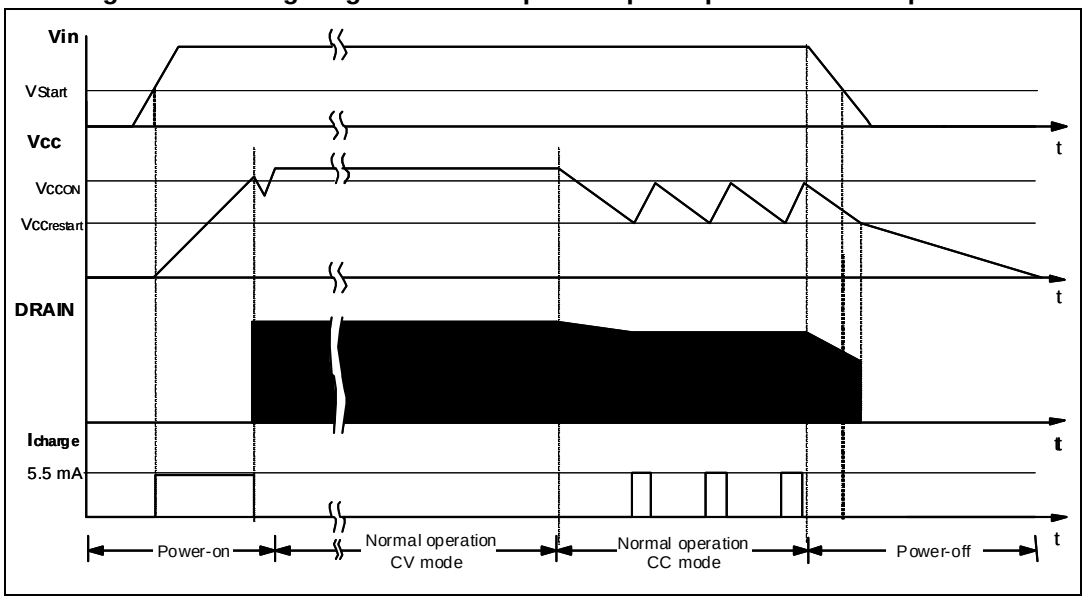
As the Vcc voltage reaches the start-up threshold (13 V typ.) the chip starts operating, the internal MOSFET is enabled to switch and the HV generator is cut off by the Vcc_OK signal asserted high. The IC is powered by the energy stored in the Vcc capacitor.

The chip powers itself directly from the rectified mains: when the voltage on the Vcc pin falls below $Vcc_{restart}$ (10.5V typ.), during each MOSFET off-time, the HV current generator turns on and charges the supply capacitor until it reaches the Vcc_{On} threshold.

In this manner, the self-supply circuit develops a high voltage to sustain the operation of the device. This feature is useful during CC regulation, when the flyback voltage generated by the auxiliary winding alone, may not be able to keep Vcc above $Vcc_{restart}$.

At converter power-down, the system loses regulation as soon as the input voltage falls below V_{Start}. This avoids converter restart attempts and assures monotonic output voltage decay at system power-down.

Figure 10. Timing diagram: normal power-up and power-down sequences

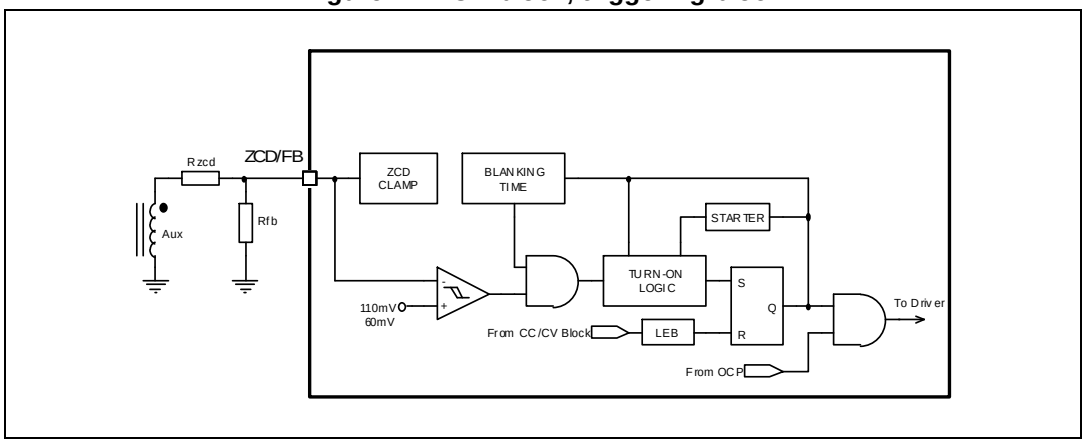


5.3 Zero-current detection and triggering block

The zero-current detection (ZCD) and triggering blocks switch on the MOSFET if a negative-going edge falling below 50 mV is applied to the ZCD/FB pin. The triggering block must be previously armed by a positive-going edge exceeding 100 mV.

This feature detects transformer demagnetization for QR operation, where the signal for ZCD input is obtained by the transformer auxiliary winding, also used to supply the IC.

Figure 11. ZCD block, triggering block



The triggering block is blanked after MOSFET turn-off to prevent any negative-going edge, following leakage inductance demagnetization, from triggering the ZCD circuit erroneously.

This blanking time is dependent on the voltage on COMP pin: it is T_{BLANK} = 30 µs for V_{COMP} = 0.9 V, and decreases almost linearly down to T_{BLANK} = 6 µs for V_{COMP} = 1.3 V.

The voltage on the pin is both top and bottom-limited by a double clamp, as illustrated in the internal diagram of ZCD block (see *Figure 11*). The upper clamp is typically 3.3 V, while the lower clamp is -60 mV. The interface between the pin and the auxiliary winding is a resistor

divider. Its resistance ratio as well as the individual resistance values have to be properly chosen (see "*Section 5.4: Constant voltage operation*" and "*Section 5.6: Voltage feed-forward block*").

The maximum $I_{ZCD/FB}$ sunk/sourced current must not exceed ±2 mA (AMR) in all Vin range conditions. No capacitor is allowed between ZCD pin and the auxiliary transformer.

The switching frequency is 166 kHz top-limited, as the converter operating frequency can increase excessively at light load and on high input voltage.

A starter block is also used to start up the system, that is, to turn on the MOSFET during the converter power-up, when any or a very small signal is available on ZCD pin.

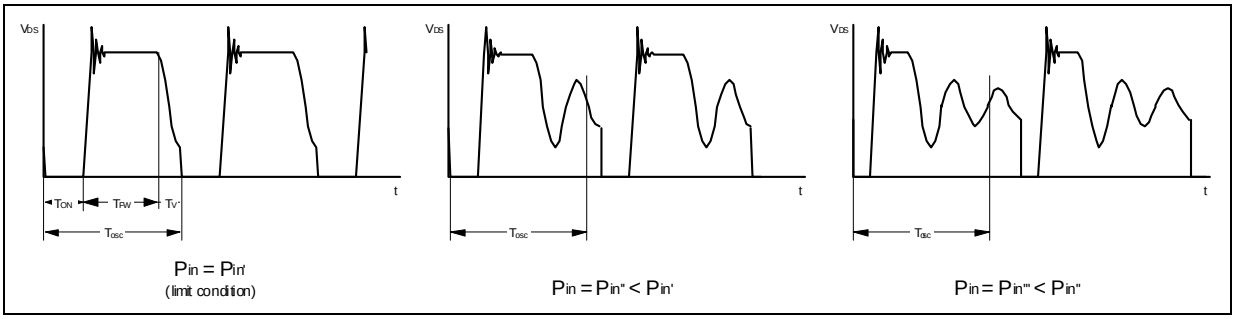
The starter frequency is 2 kHz if COMP pin is below burst-mode threshold, 1 V, while it becomes 8 kHz if this voltage exceeds this value.

After the first few cycles initiated by the starter, as the voltage developed across the auxiliary winding arms the ZCD circuit, MOSFET turn-on starts to be locked to transformer demagnetization, hence setting up QR operation.

The starter is also active when the IC is in CC regulation and the output voltage is not so high to allow the ZCD triggering.

If the demagnetization completes, hence a negative-going edge appears on ZCD pin, after a time exceeding T_{BLANK} time, the MOSFET turns on again, with some delay to assure minimum voltage at turn-on. If, instead, the negative-going edge appears before T_{BLANK} has elapsed, it is ignored and the first negative-going edge after T_{BLANK} turns on the MOSFET. Therefore one or more drain ringing cycles are skipped ("valley-skipping-mode", *Figure 12*) and the switching frequency cannot exceed $1/T_{BLANK}$.

Figure 12. Drain ringing cycle skipping as the load is progressively reduced



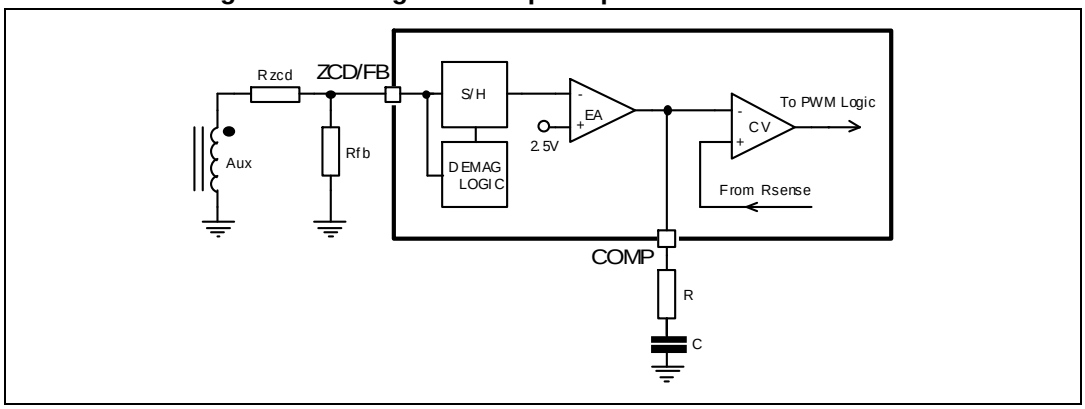
When the system operates in valley-skipping-mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the off-time of the MOSFET changes with discrete steps of one ringing cycle, while the off-time needed for cycle-by-cycle energy balance may fall in between. Thus one or more longer switching cycles are compensated by one or more shorter cycles and vice versa. However, this mechanism is absolutely normal and there is no appreciable impact on the performance of the converter or on its output voltage.

5.4 Constant voltage operation

The IC is specifically designed to work in the primary regulation and the output voltage is sensed through a voltage partition of the auxiliary winding, just before the auxiliary rectifier diode.

Figure 13 shows the internal schematic of the constant voltage-mode and the external connections.

Figure 13. Voltage control principle: internal schematic



Due to the parasitic wire resistance, the auxiliary voltage is representative of the output just when the secondary current becomes zero. For this purpose, the signal on ZCD/FB pin is sampled-and-held at the end of the transformer demagnetization to get an accurate image of the output voltage and it is compared with the error amplifier internal reference.

The COMP pin is used for the frequency compensation: usually, an RC network, which stabilizes the overall voltage control loop, is connected between this pin and ground.

The output voltage can be defined according to the following formula:

Equation 1

$$R_{FB} = \frac{V_{REF}}{\frac{N_{AUX}}{N_{SEC}} \cdot V_{OUT} - V_{REF}} \cdot R_{ZCD}$$

where N_{SEC} and N_{AUX} are the numbers of secondary and auxiliary turns respectively.

R_{ZCD} value depends on the application parameters (see "*Section 5.6: Voltage feed-forward block*").

5.5 Constant current operation

Figure 14 presents the principle used to control the average output current of a flyback converter.

The output voltage of the auxiliary winding is used by the demagnetization block to generate the control signal for the switch Q1. R resistor absorbs a current V_C/R, where V_C is the voltage developed across the capacitor C_{REF}.

The flip-flop output is high as long as the transformer delivers current on the secondary side. This is shown in *Figure 15*.

The capacitor C_{REF} has to be chosen so that its voltage V_C can be considered as a constant. Since it is charged and discharged by currents in the range of 10 µA (I_{CREF} is typically 20 µA) at the switching frequency rate, a capacitance value in the range of 4.7-10 nF suits to switching frequencies of 10 kHz.

The average output current can be expressed as follows:

Equation 2

$$I_{OUT} = \frac{N_{PRI}}{N_{SEC}} \cdot \frac{G_I \cdot V_{CREF}}{(2 \cdot R_{SENSE})}$$

where N_{PRI} is the primary turn number.

This formula shows that the average output current does not depend neither on the input or the output voltage, nor on transformer inductance values. The external parameters defining the output current, are the transformer ratio n and the sense resistor R_{SENSE}.

G_I current loop gain and V_{CREF} current reference voltage are internally defined.

Figure 14. Current control principle

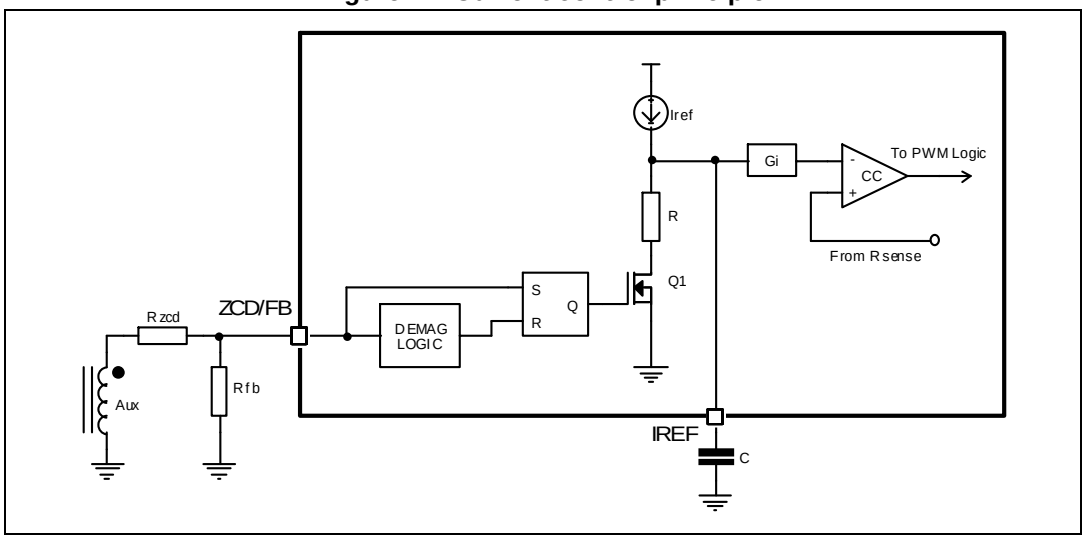
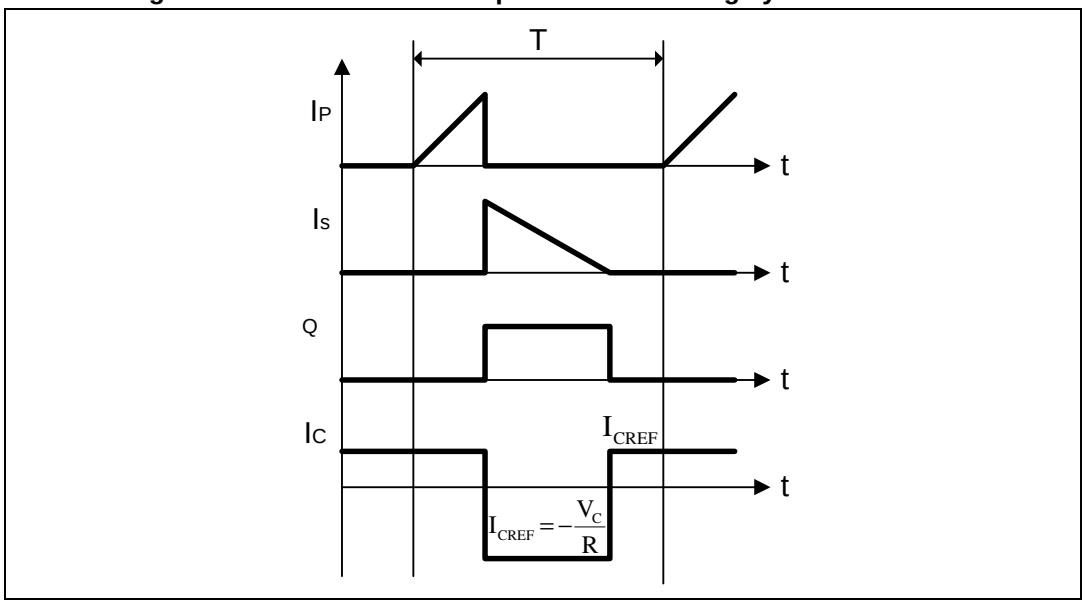


Figure 15. Constant current operation: switching cycle waveforms



5.6 Voltage feed-forward block

The current control structure uses the voltage V_C to define the output current, according to equation 2. Actually, the CC comparator is affected by T_d an internal propagation delay, which switches off the MOSFET with a peak current higher than the foreseen value.

This current overshoot is equal to:

Equation 3

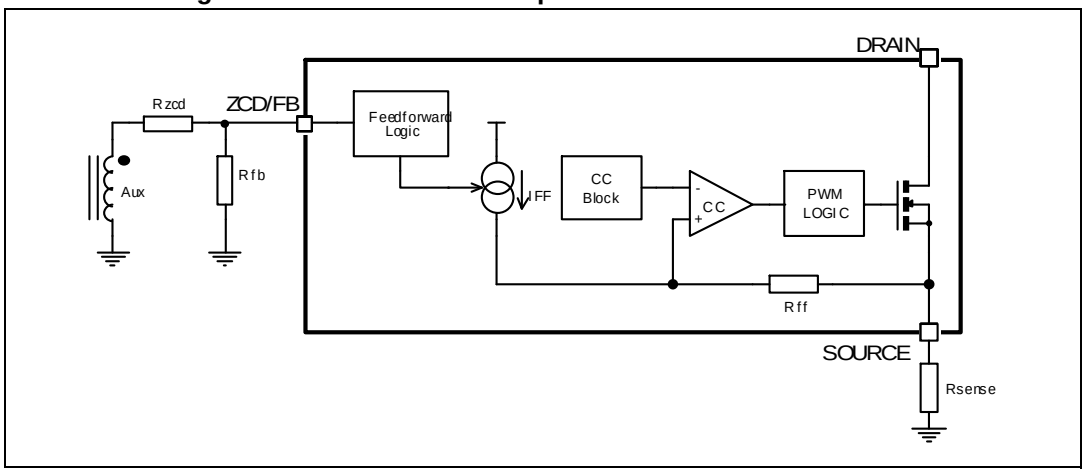
$$\Delta I_P = \frac{V_{IN} \cdot T_d}{L_P}$$

where L_P is the primary inductance and it introduces an error on the calculated CC set point, depending on the input voltage.

The device implements a line feed-forward function, which solves the issue by introducing an input offset voltage on the current sense signal, in order to adjust the cycle-by-cycle current limitation.

The internal schematic is shown in *Figure 16*.

Figure 16. Feed-forward compensation: internal schematic



R_{ZCD} resistor can be calculated as follows:

Equation 4

$$R_{ZCD} = \frac{N_{AUX}}{N_{PRI}} \cdot \frac{L_P \cdot R_{FF}}{T_d \cdot R_{SENSE}}$$

The peak drain current does not depend on the input voltage.

Concerning R_{ZCD} value: during the MOSFET on-time, the current, sourced from ZCD/FB pin, I_{ZCD}, is compared with an internal reference current I_{ZCDON} (- 50 µA typical).

If $I_{ZCD} < I_{ZCDON}$, the brownout function is active and IC shuts down.

This feature is important when the auxiliary winding is accidentally disconnected and considerably increases the end-product safety and reliability.

5.7 Burst-mode operation (no load or very light load)

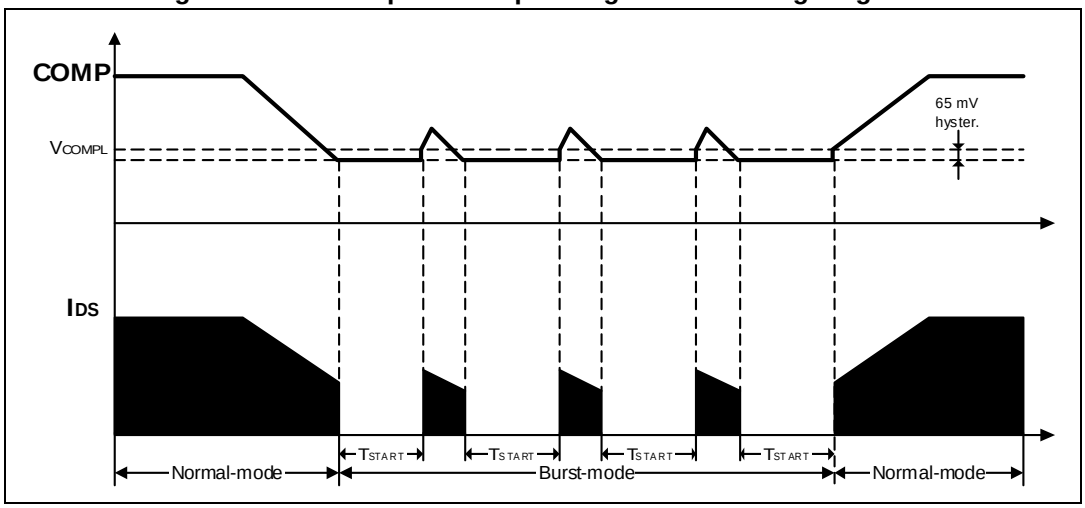
When the voltage on COMP pin falls 65 mV below a fixed threshold, V_{COMPBM}, the IC is disabled, the MOSFET is in off-state and its consumption reduced to a lower value to minimize Vcc capacitor discharge.

Due to this condition, the converter operates in burst-mode (one pulse train every T_{START} = 500 µs), with a minimum energy transfer.

Therefore, the output voltage decreases: after 500 µs the controller switches on the MOSFET again and the sampled voltage on the ZCD pin is compared with the internal reference. If the voltage on the EA output, as a result of the comparison, exceeds the V_{COMPL} threshold, the device restarts switching, otherwise it is off for another period of 500 µs.

The converter works in burst-mode with a nearly constant peak current. A load decrease causes a frequency reduction, which can go down even to few hundreds hertz, thus minimizing all frequency-related losses and meeting energy saving regulations. This kind of operation, shown in the timing diagrams (see *Figure 17*) along with the others previously described, is noise-free since the peak current is low.

Figure 17. Load-dependent operating modes: timing diagrams



5.8 Soft-start and starter block

The soft-start feature is automatically implemented by the constant current block, as the primary peak current is limited on the C_{REF} capacitor.

During the startup, as the output voltage is zero, IC starts in CC-mode without high peak current operations. The voltage on the output capacitor increases slowly and the soft-start feature is assured.

Actually the C_{REF} value is not important to define the soft-start time, as its duration depends on other circuit parameters, such as: transformer ratio, sense resistor, output capacitors and load. The user can define the best appropriate value.

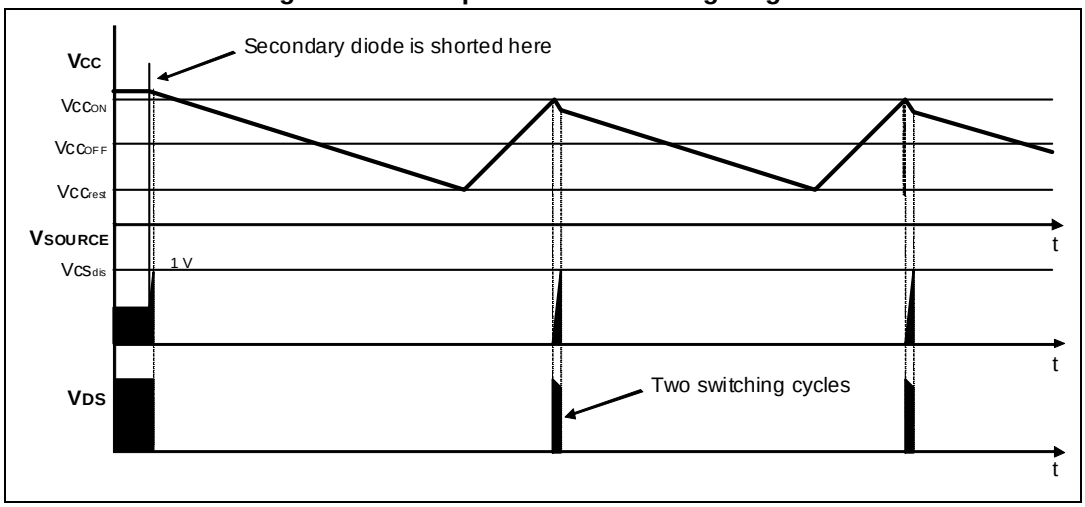
5.9 Hiccup-mode OCP

The device is also protected against short-circuit of the secondary rectifier, short-circuit on the secondary winding or a hard-saturated flyback transformer. A comparator monitors continuously the voltage on R_{SENSE} and activates a protection circuitry if this voltage exceeds 1 V.

To distinguish a malfunction from a disturbance (induced during ESD tests), the first time the comparator is tripped, the protection circuit enters a “warning state”. If in the following switching cycle the comparator is not tripped, a temporary disturbance is assumed and the protection logic is reset in its idle state; if the comparator is tripped again a real malfunction is assumed and the device stops.

This condition is latched as long as the device is supplied. Any energy comes from the self-supply circuit; hence the voltage on the Vcc capacitor decays and crosses the UVLO threshold after some time, which clears the latch. The internal start-up generator is still off, then the Vcc voltage still needs to go below its restart voltage before the Vcc capacitor is charged again and the device restarted. Finally, this results in a low-frequency intermittent operation (hiccup-mode operation), with very low stress on the power circuit. This special condition is illustrated in the timing diagram of *Figure 18*.

Figure 18. Hiccup-mode OCP: timing diagram

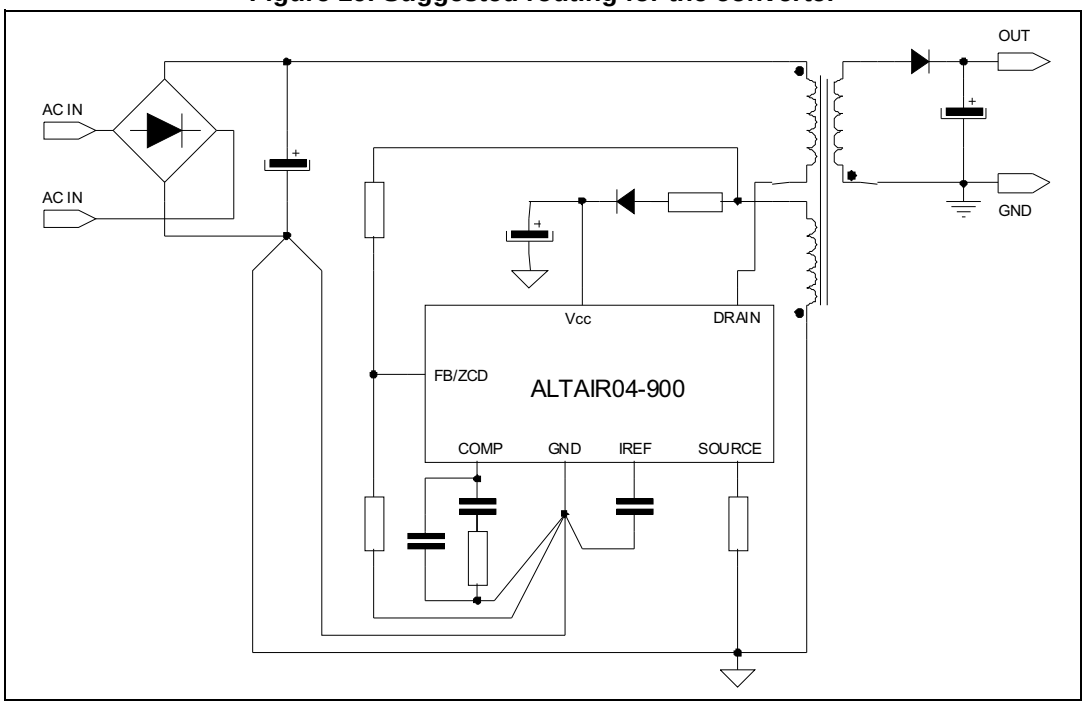


5.10 Layout recommendations

A proper printed circuit board layout is very important for the correct operation of any switch-mode converter. Placing components carefully, routing traces correctly, appropriate trace widths and compliance with isolation distances are very important matters. In particular:

- The compensation network should be connected as closer as possible to the COMP pin, keeping short the trace for the GND
- Signal ground should be routed separately from power ground, as well as from the sense resistor trace

Figure 19. Suggested routing for the converter



6 Typical applications

Figure 20. Test board schematic: 4.5 W (9 V - 500 mA) wide range mains adapter

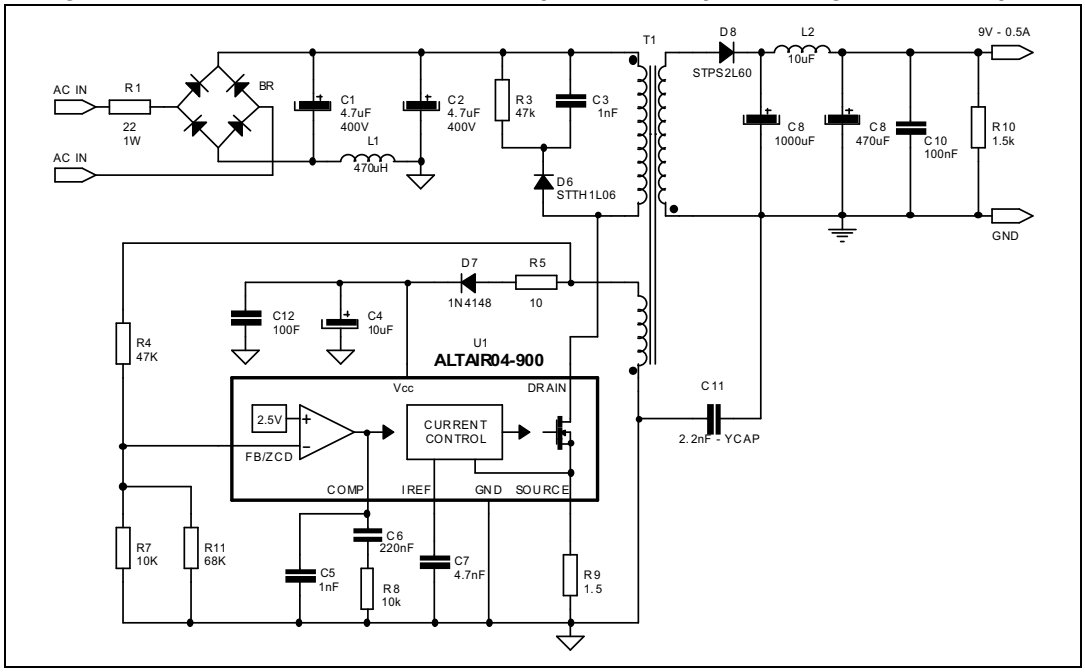
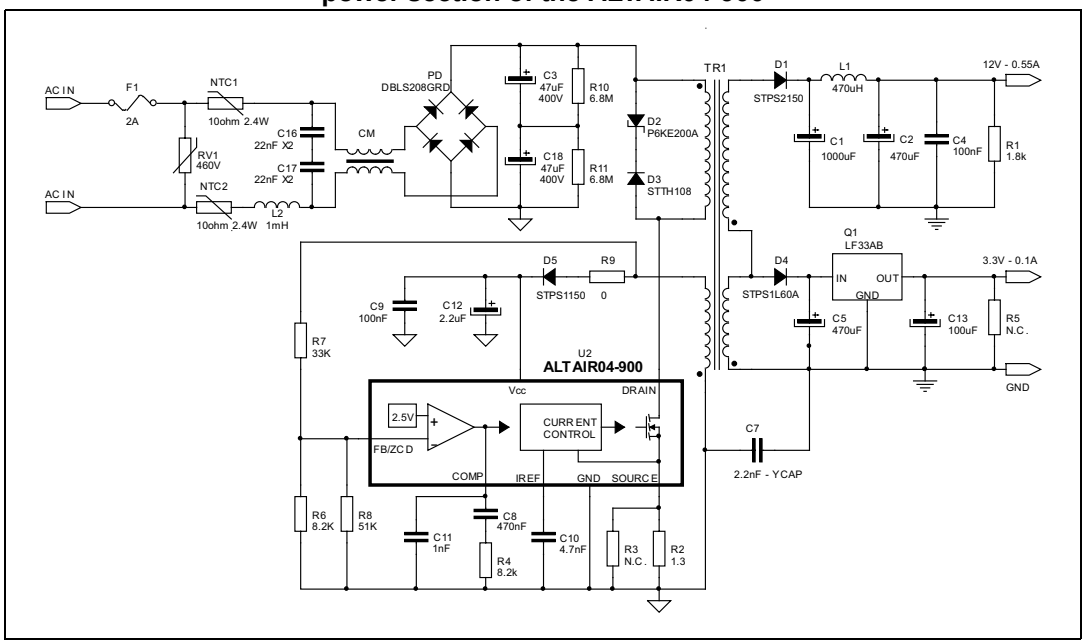


Figure 21. Electrical schematic for 440 V_{AC} input voltage option due to 900 V rated power section of the ALTAIR04-900



6.1 Test board: evaluation data

Figure 22. No-load consumption

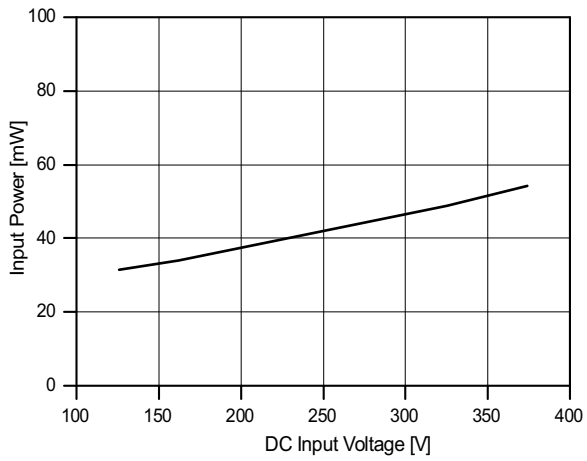


Figure 23. Efficiency at full load

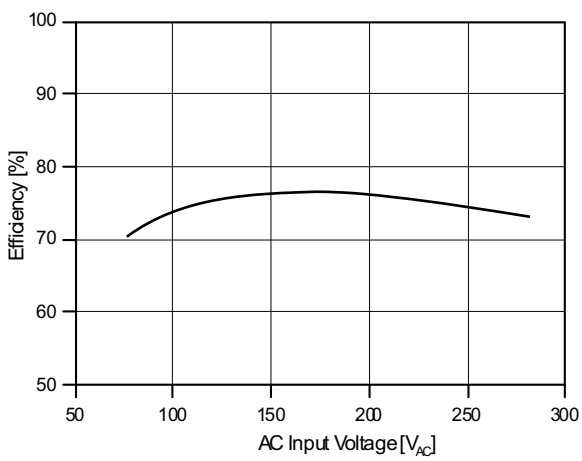


Figure 24. V-I curve @ 110 V_{AC}

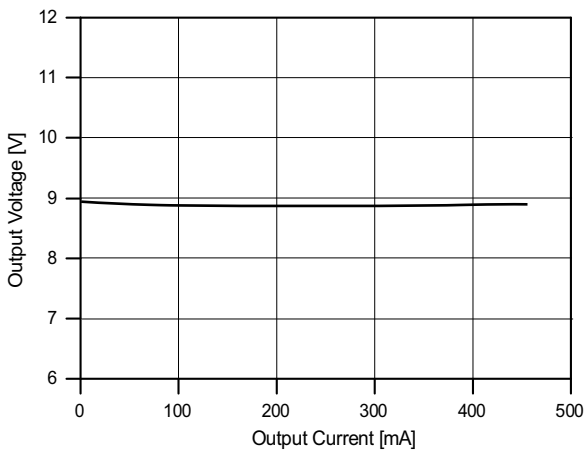
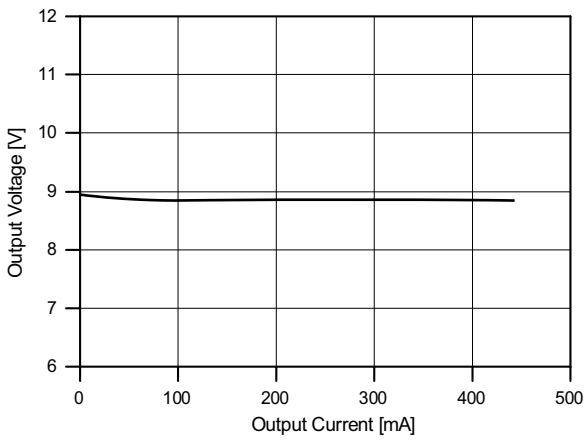
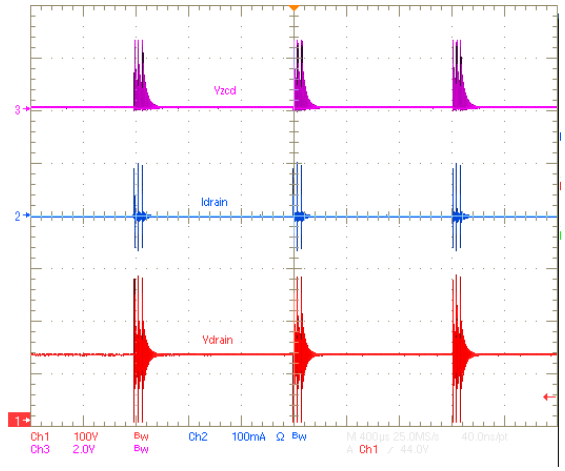


Figure 25. V-I curve @ 264 V_{AC}



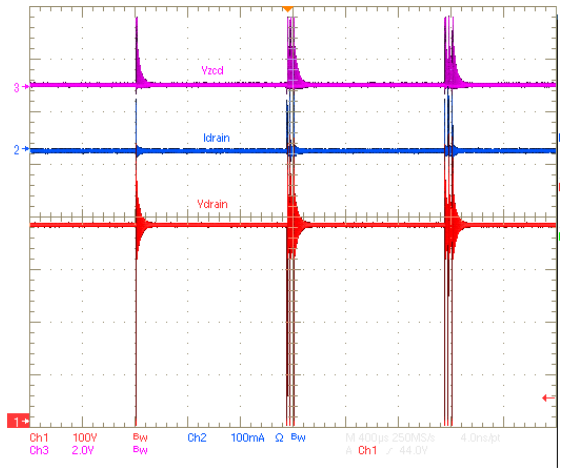
6.2 Test board: main waveforms

Figure 26. 110 V_{AC}, no-load



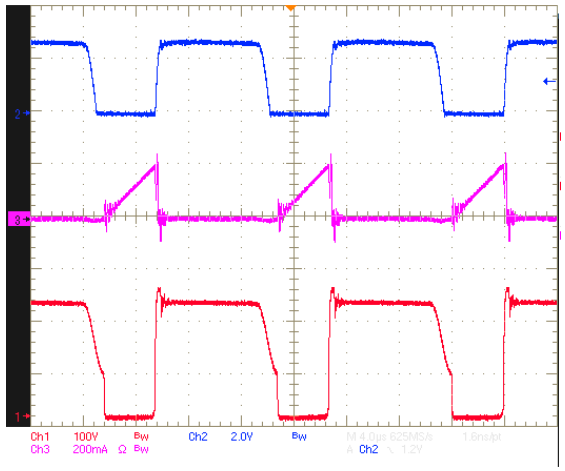
M: 400 s/div

Figure 27. 264 V_{AC}, no-load



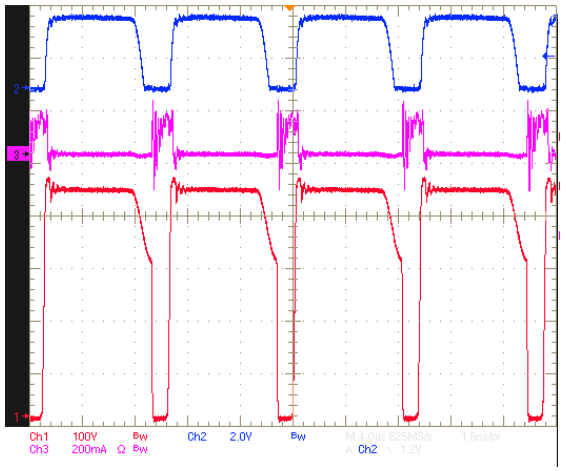
M: 400 s/div

Figure 28. 110 V_{AC}, full load



M: 400 s/div

Figure 29. 234 V_{AC}, full load



M: 400 s/div

7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 30. SO16N drawings

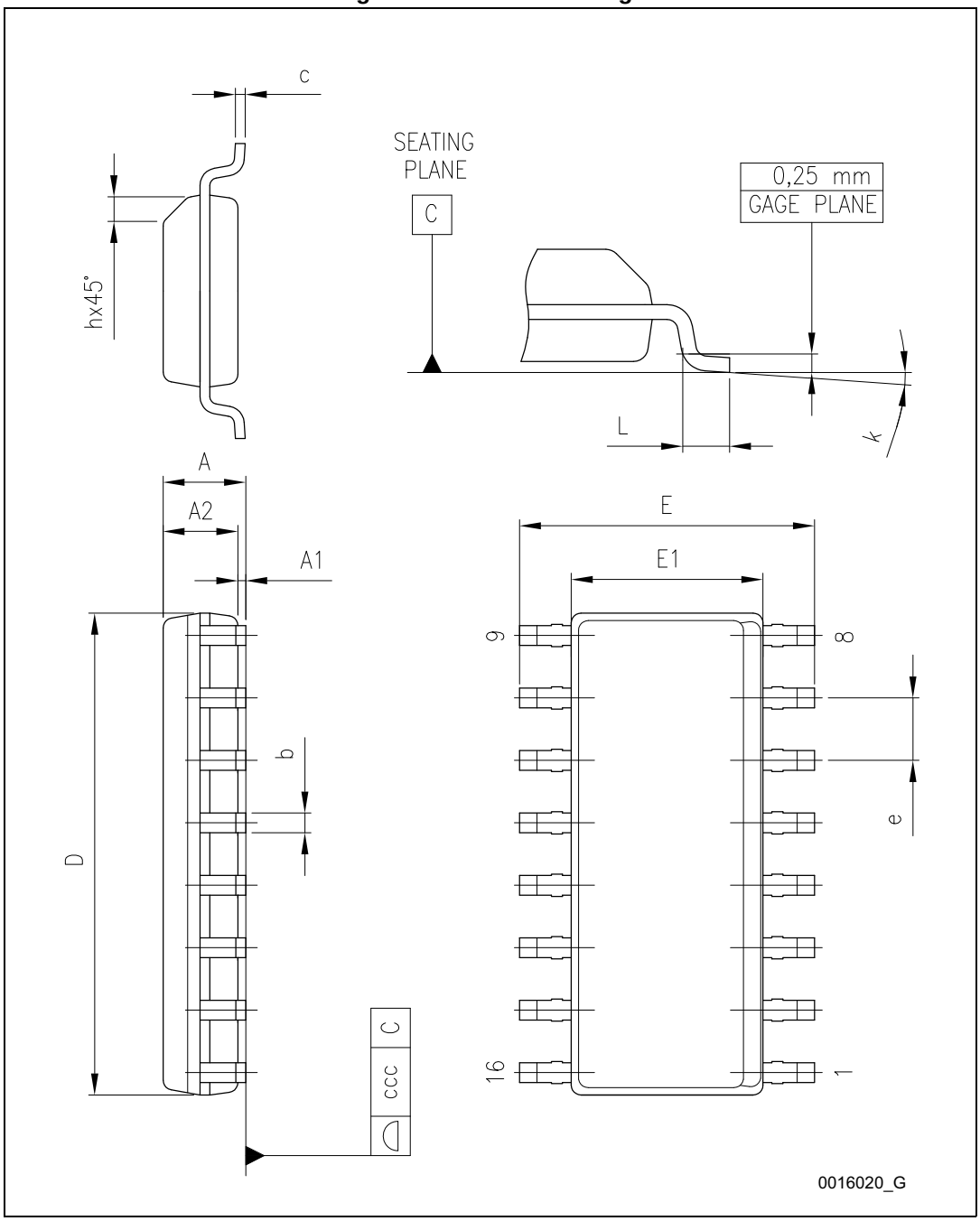
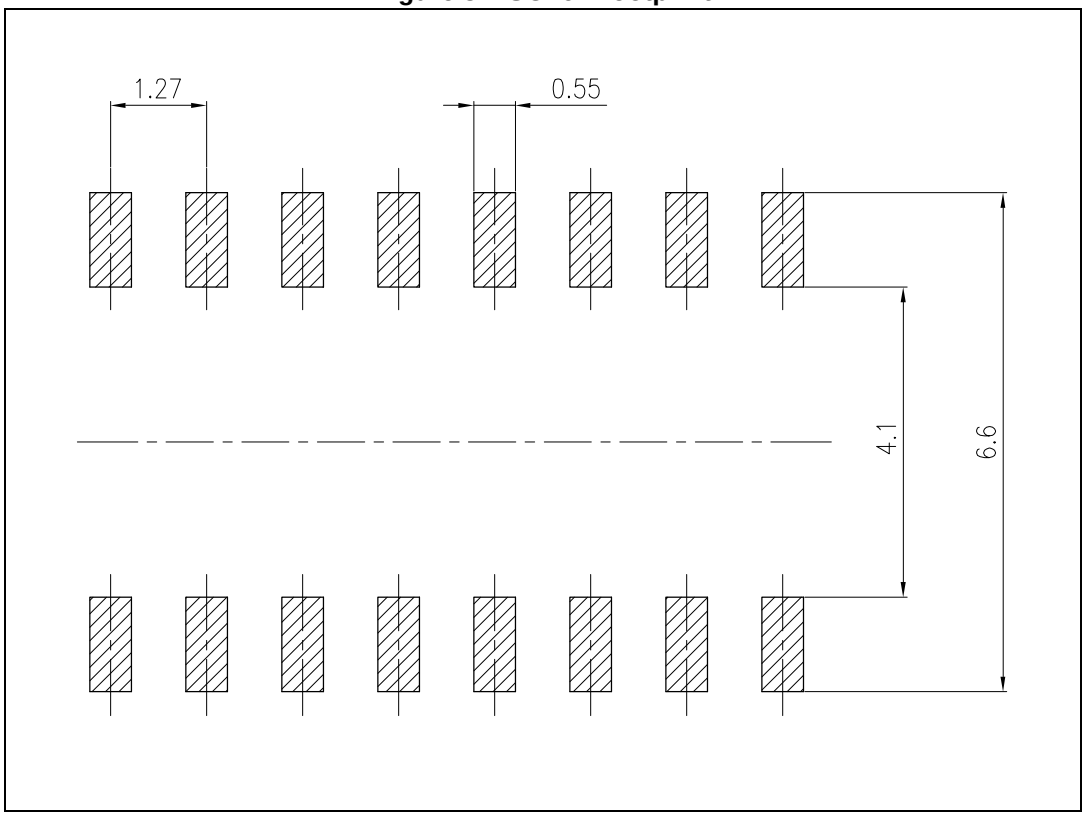


Table 5. SO16N mechanical data

Dim.	mm		
	Typ.	Min.	Max.
A	1.55	1.43	1.68
A1	0.15	0.12	0.18
A2	1.52	1.48	1.56
b	0.40	0.375	0.425
c			0.238
D	9.85	9.82	9.88
E	6.00	5.90	6.10
E1	3.90	3.87	3.93
e	1.27		
h		0.425	0.50
L	0.635	0.585	0.685
k	4	2	8
ccc			0.04

Figure 31. SO16N footprint



8 Ordering information

Table 6. Ordering information

Order codes	Package	Packaging
ALTAIR04-900	SO16N	Tube
ALTAIR04-900TR		Tape and reel

9 Revision history

Table 7. Document revision history

Date	Revision	Changes
11-Nov-2010	1	Initial release
25-Jan-2011	2	Updated *Chapter Table 4. on page 7*
07-Oct-2014	3	Updated *Table 2: Absolute maximum ratings*, *Section 4: Electrical characteristics* and *Section 7: Package mechanical data*. Minor text changes.

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