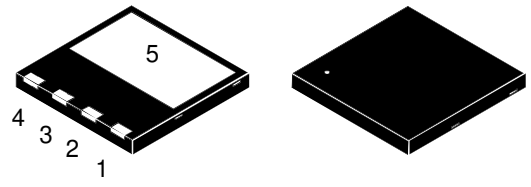
STL26NM60N

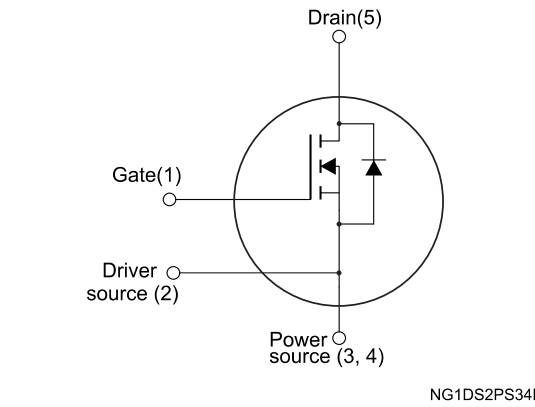
N-channel 600 V, 0.160 Ω typ., 19 A MDmesh™ II Power MOSFET in a PowerFLAT 8x8 HV package

Datasheet - production data



PowerFLAT™ 8x8 HV

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STL26NM60N	600 V	0.185 Ω	19 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL26NM60N	26NM60N	PowerFLAT™ 8x8 HV	Tape and reel

This is information on a product in full production.

www.st.com

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3 Test circuits 8
4 Package information 9
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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	19	A
I_D	Drain current (continuous) at T_C = 100 °C	12	A
I_{DM} (1)	Drain current (pulsed)	76	A
P_{TOT}	Total dissipation at T_C = 25 °C	125	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 19 A, di/dt ≤ 400 A/µs, $V_{DS(peak)}$ ≤ $V_{(BR)DSS}$, V_{DD} ≤ 80% $V_{(BR)DSS}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1	°C/W
$R_{thj\text{-}amb}$ (1)	Thermal resistance junction-ambient	45	°C/W

Notes:

(1)When mounted on 1inch² FR-4 board, 2 oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Single pulse avalanche current (pulse width limited by T_{jmax})	6	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AS}, V_{DD}=50 V)	400	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C= 125 °C (1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±0.1	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10 A		0.160	0.185	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	1800	-	pF
C_{oss}	Output capacitance		-	115	-	pF
C_{rss}	Reverse transfer capacitance		-	6	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 480 V	-	310	-	pF
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 19 A, V_{GS} = 10 V (see *Figure 14: "Gate charge test circuit"*)	-	60	-	nC
Q_{gs}	Gate-source charge		-	8.5	-	nC
Q_{gd}	Gate-drain charge		-	30	-	nC
R_G	Gate input resistance	f=1 MHz, I_D=0 A	-	2.8	-	Ω

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 10 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Switching times test circuit for resistive load"* and *Figure 18: "Switching time waveform"*)	-	13	-	ns
t_r	Rise time		-	25	-	ns
$t_{d(off)}$	Turn-off delay time		-	85	-	ns
t_f	Fall time		-	50	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		19	A
I_{SDM}(1)	Source-drain current (pulsed)		-		76	A
V_{SD}(2)	Forward on voltage	I_{SD} = 19 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 19 A, di/dt = 100 A/µs	-	370		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V (see *Figure 15: " Test circuit for inductive load switching and diode recovery times"*)	-	5.8		µC
I_{RRM}	Reverse recovery current		-	31.6		A
t_{rr}	Reverse recovery time	I_{SD} = 19 A, di/dt = 100 A/µs	-	450		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_j = 150 °C (see *Figure 15: " Test circuit for inductive load switching and diode recovery times"*)	-	7.5		µC
I_{RRM}	Reverse recovery current		-	32.5		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

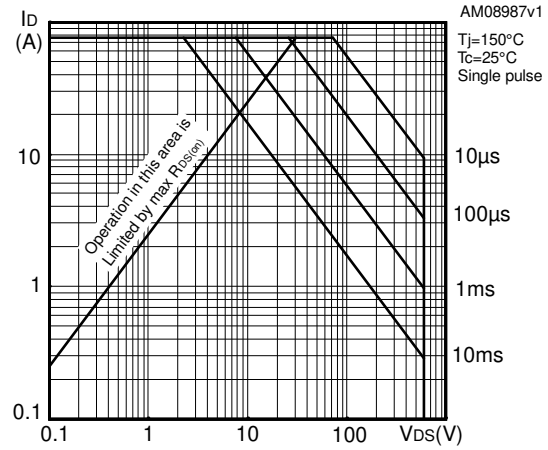


Figure 3: Thermal impedance

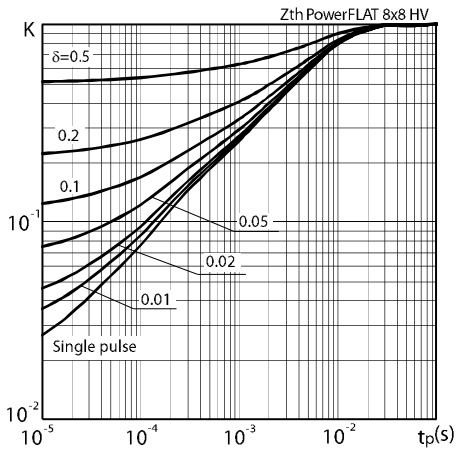


Figure 4: Output characteristics

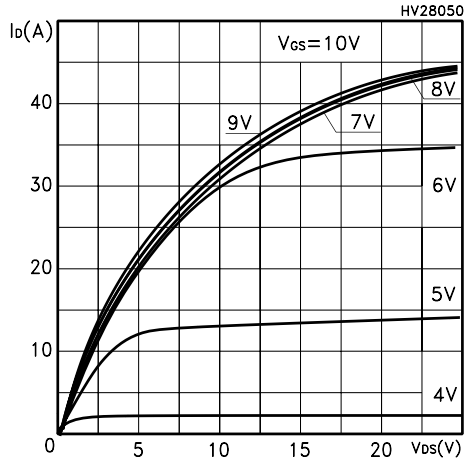


Figure 5: Transfer characteristics

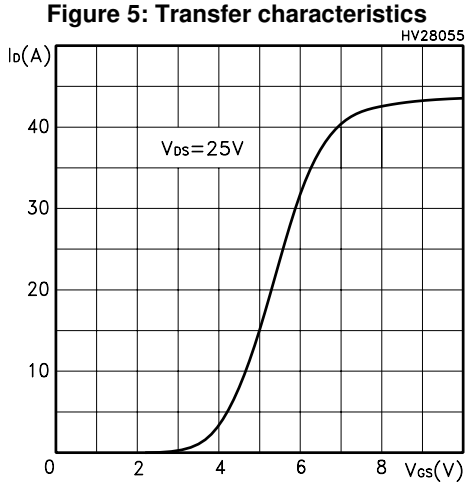


Figure 6: Gate charge vs gate-source voltage

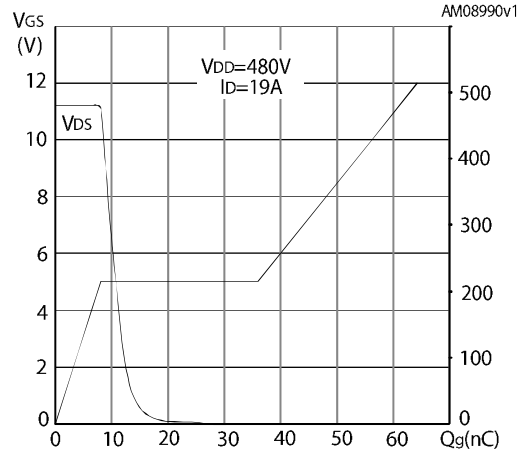


Figure 7: Static drain-source on-resistance

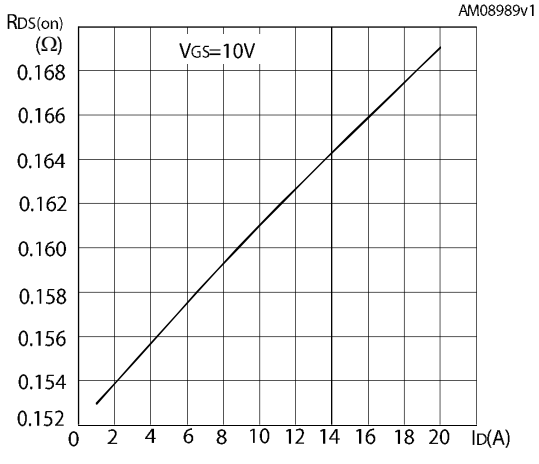


Figure 8: Capacitance variations

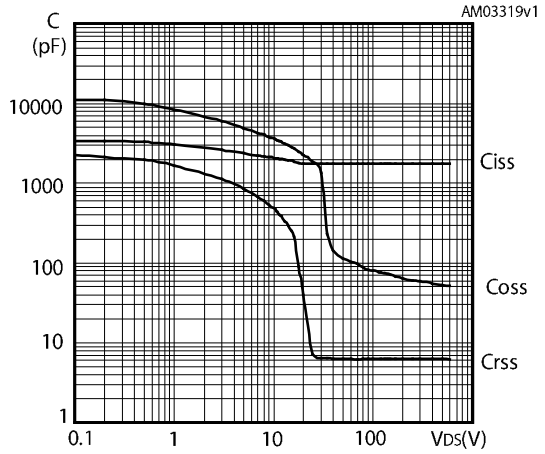


Figure 9: Source-drain diode forward characteristics

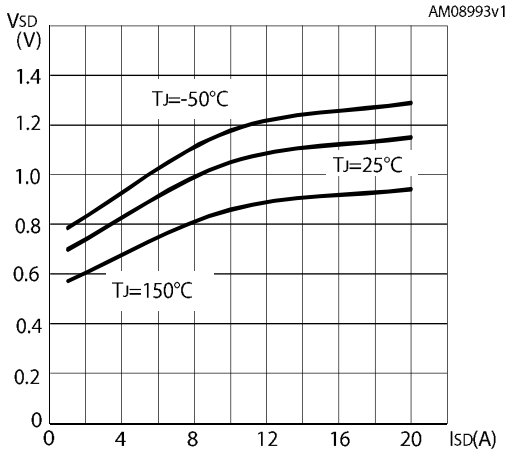


Figure 10: Normalized gate threshold voltage vs temperature

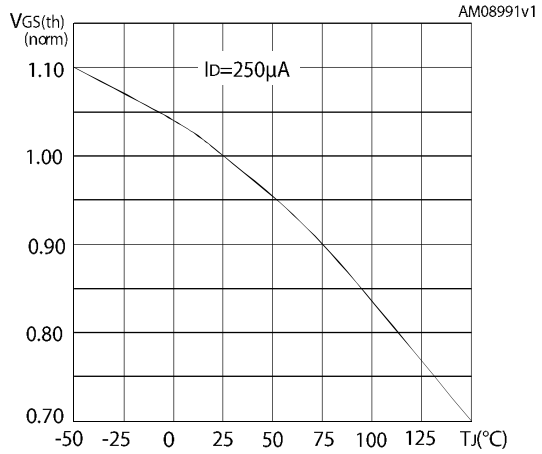


Figure 11: Normalized on-resistance vs temperature

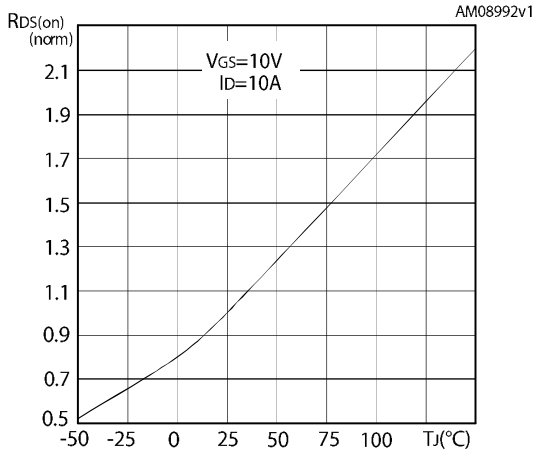
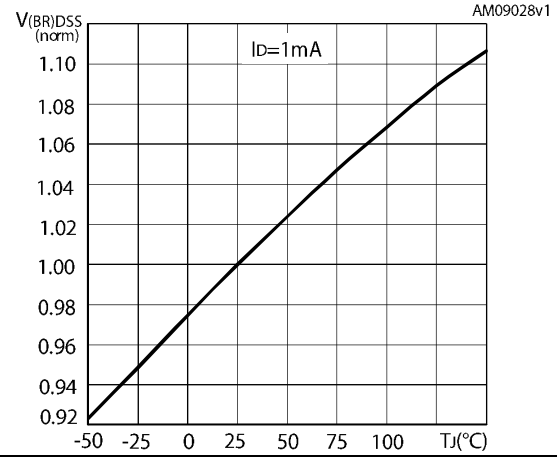


Figure 12: Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 13: Switching times test circuit for resistive load

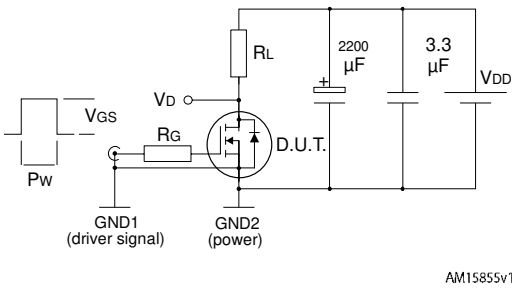


Figure 14: Gate charge test circuit

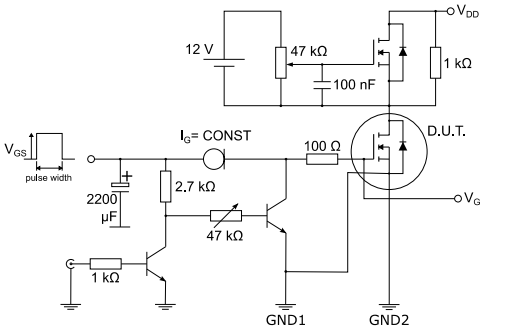


Figure 15: Test circuit for inductive load switching and diode recovery times

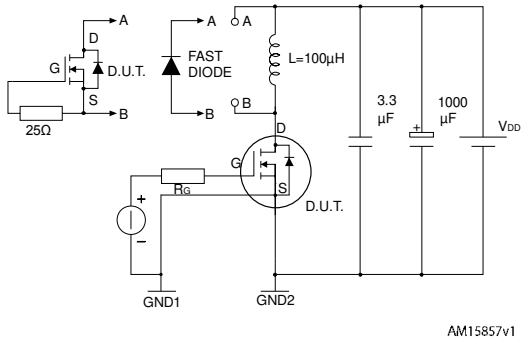


Figure 16: Unclamped inductive load test circuit

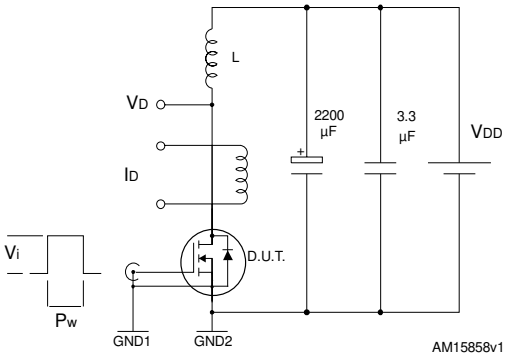


Figure 17: Unclamped inductive waveform

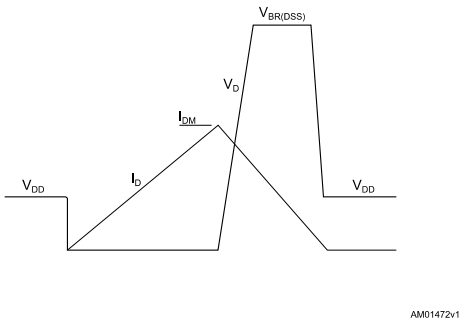
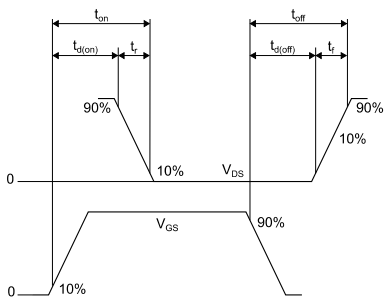


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT 8x8 HV package information

Figure 19: PowerFLAT™ 8x8 HV package outline

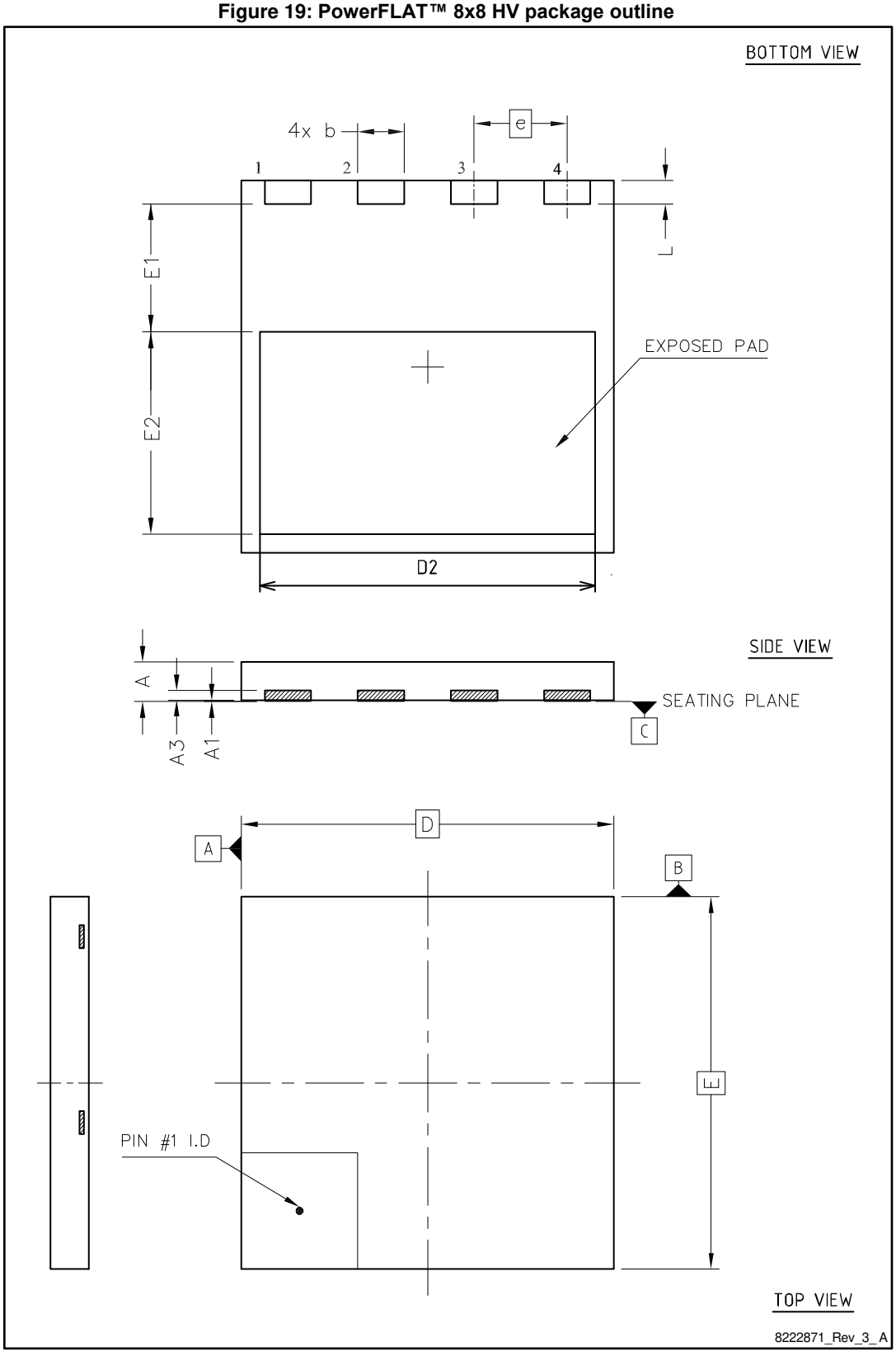
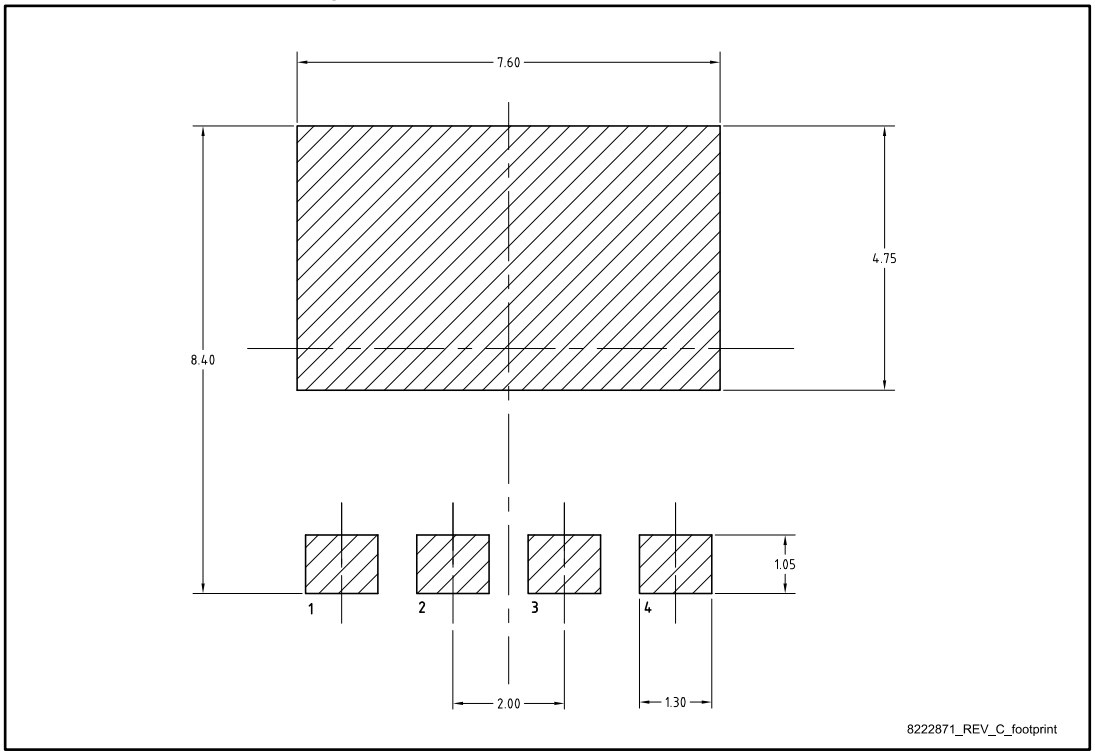


Table 9: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00	
L	0.40	0.50	0.60

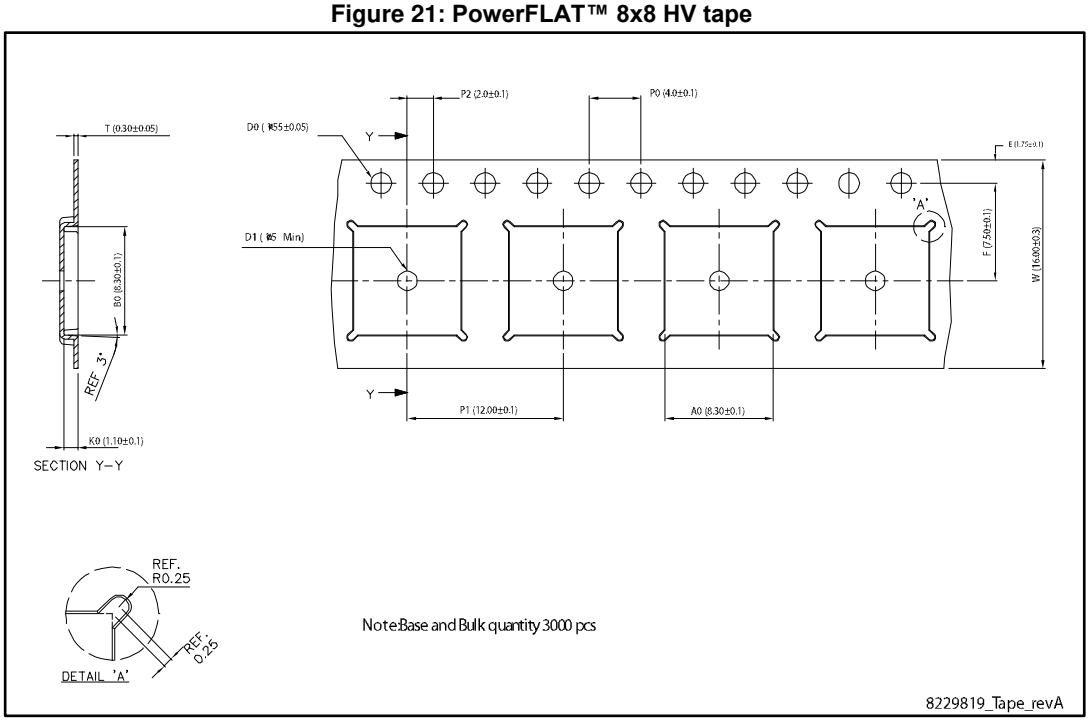
Figure 20: PowerFLAT™ 8x8 HV footprint



All dimensions are in millimeters.

4.2 PowerFLAT 8x8 HV packing information

Figure 21: PowerFLAT™ 8x8 HV tape



All dimensions are in millimeters.

Figure 22: PowerFLAT™ 8x8 HV package orientation in carrier tape

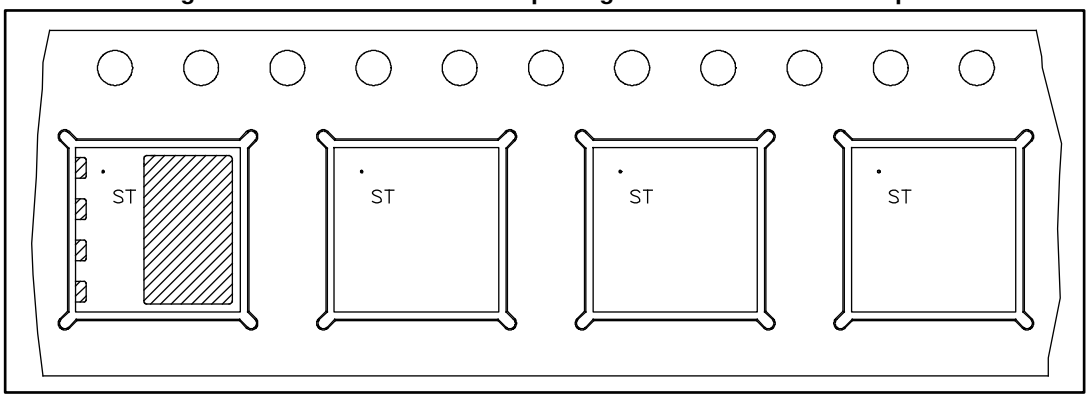
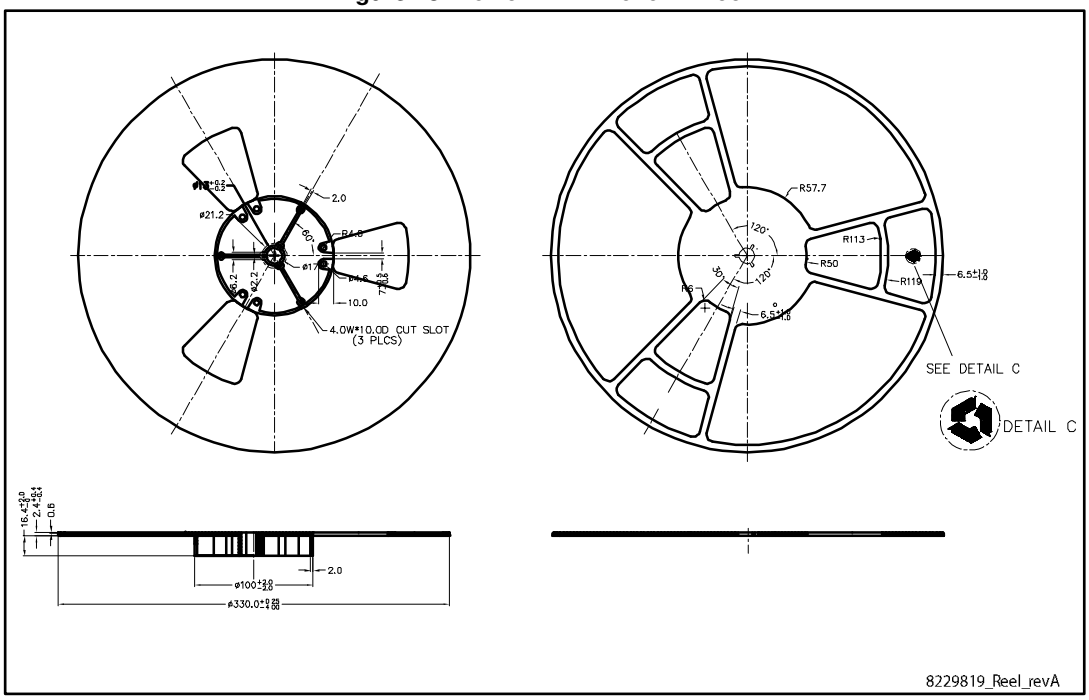


Figure 23: PowerFLAT™ 8x8 HV reel



All dimensions are in millimeters.

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
14-Feb-2011	1	First release.
03-Nov-2011	2	*Section 4: Package mechanical data* has been updated. Minor text changes.
14-Dec-2016	3	Updated title, silhouette, features, description and internal schematic diagram on cover page. Modified *Table 2: "Absolute maximum ratings"*, *Table 3: "Thermal data"*, *Table 5: "On/off states"*, *Table 6: "Dynamic"*, *Table 7: "Switching times"* and *Table 8: "Source-drain diode"*. Minor text changes.

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