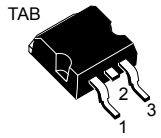
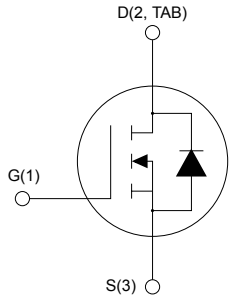
Automotive-grade N-channel 330 V, 160 mΩ typ., 18 A STripFET II Power MOSFET in a D²PAK package



D²PAK



AM01475v1_noZen

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB18NF30	330 V	180 mΩ	18 A

- AEC-Q101 qualified
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge
- 175 °C maximum junction temperature

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Product status link
STB18NF30

Product summary	
Order code	STB18NF30
Marking	18NF30
Package	D²PAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	330	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	18	A
	Drain current (continuous) at T_C = 100 °C	12	
I_{DM}(1)	Drain current (pulsed)	72	A
P_{TOT}	Total power dissipation at T_C = 25 °C	150	W
dv/dt(2)	Peak diode recovery voltage slope	10	V/ns
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 18 A, di/dt ≤ 200 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 264 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1	°C/W
R_{thJA}(1)	Thermal resistance, junction-to-ambient	30	°C/W

1. *When mounted on a standard 1 inch^2 area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	14	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	200	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	330			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 330 V			1	µA
		V_{GS} = 0 V, V_{DS} = 330 V, T_C = 125 °C(1)			50	
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 9 A		160	180	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1650	-	pF
C_{oss}	Output capacitance		-	220	-	pF
C_{rss}	Reverse transfer capacitance		-	30	-	pF
Q_g	Total gate charge	V_{DD} = 264 V, I_D = 18 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	44	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain charge		-	17	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 165 V, I_D = 9 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	20	-	ns
t_r	Rise time		-	18	-	ns
$t_{d(off)}$	Turn-off delay time		-	145	-	ns
t_f	Fall time		-	45	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
I_{SDM}(1)	Source-drain current (pulsed)		-		72	A
V_{SD}(2)	Forward on voltage	I_{SD} = 18 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs, V_{DD} = 100 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	180	400	ns
Q_{rr}	Reverse recovery charge		-	1.5		µC
I_{RRM}	Reverse recovery current		-	16		A
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_J = 150 °C (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	210		ns
Q_{rr}	Reverse recovery charge		-	1.9		µC
I_{RRM}	Reverse recovery current		-	19		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

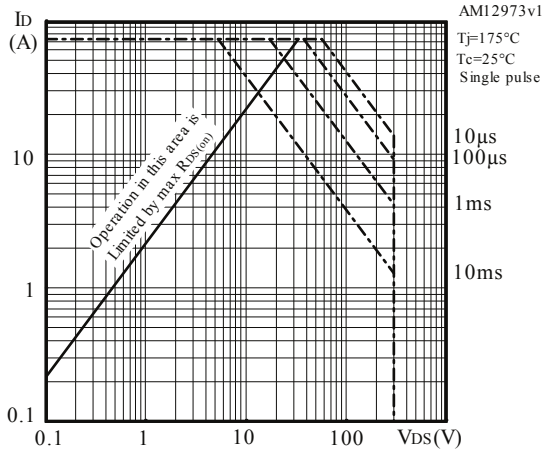


Figure 2. Normalized transient thermal impedance

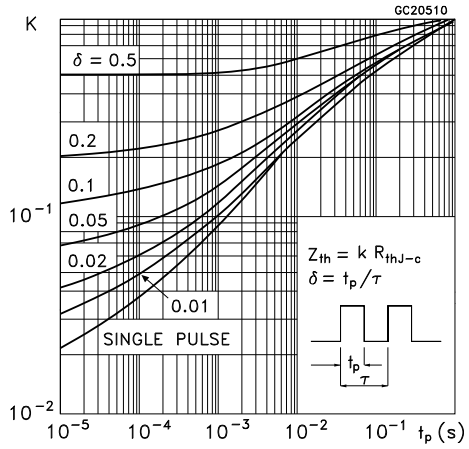


Figure 3. Typical output characterisics

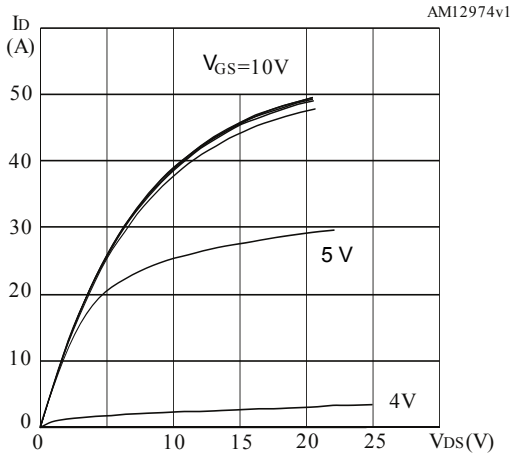


Figure 4. Typical transfer characteristics

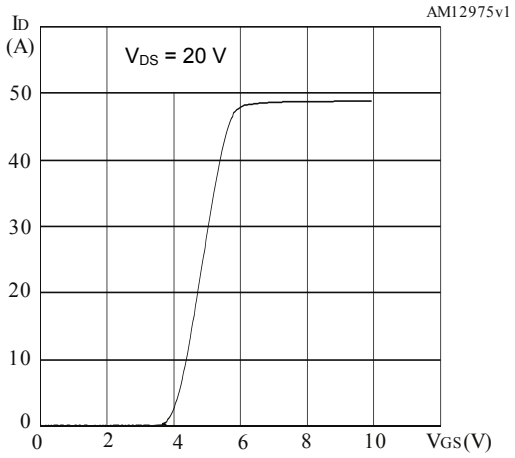


Figure 5. Normalized breakdown voltage vs temperature

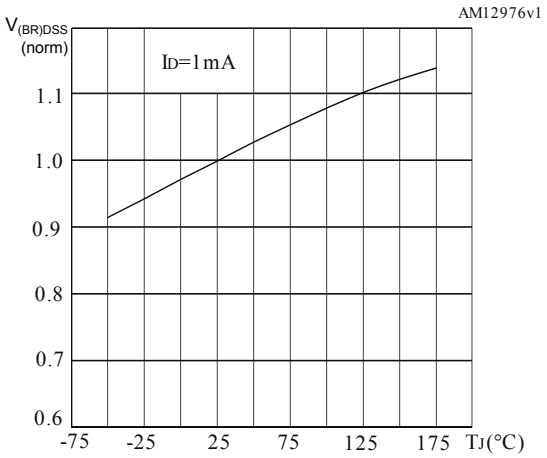


Figure 6. Typical static drain-source on-resistance

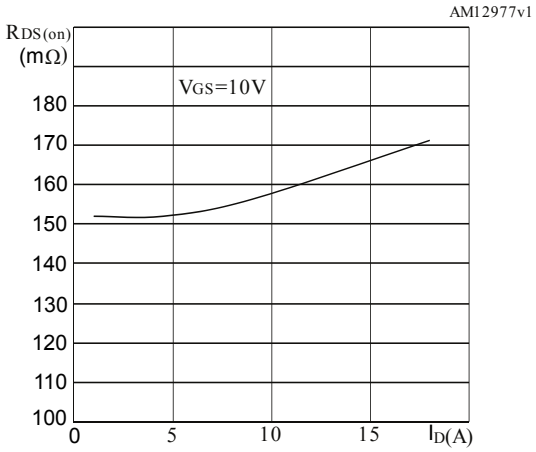


Figure 7. Typical gate charge characteristics

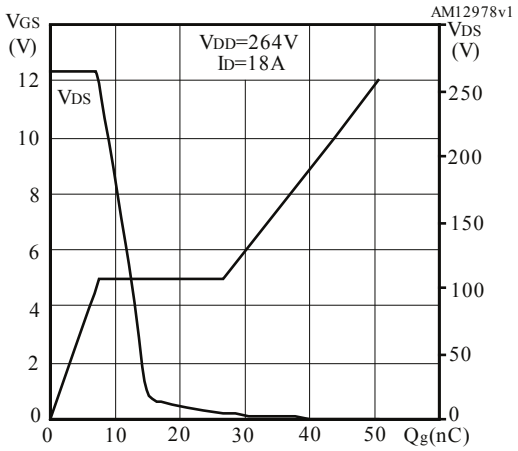


Figure 8. Typical capacitance characteristics

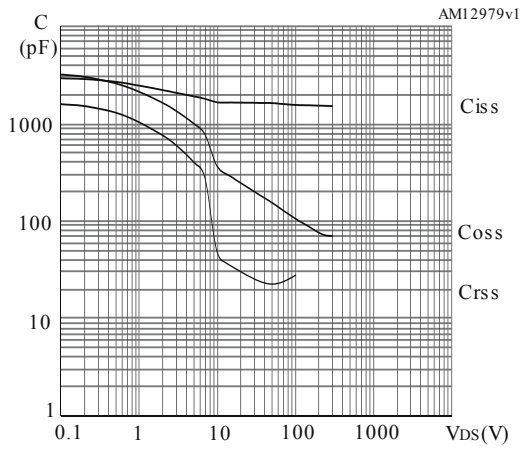


Figure 9. Normalized gate threshold vs temperature

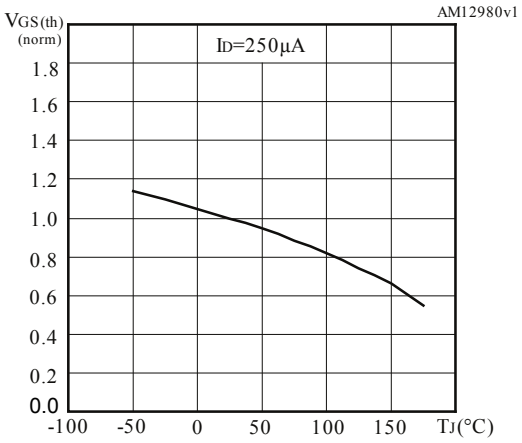


Figure 10. Normalized on-resistance vs temperature

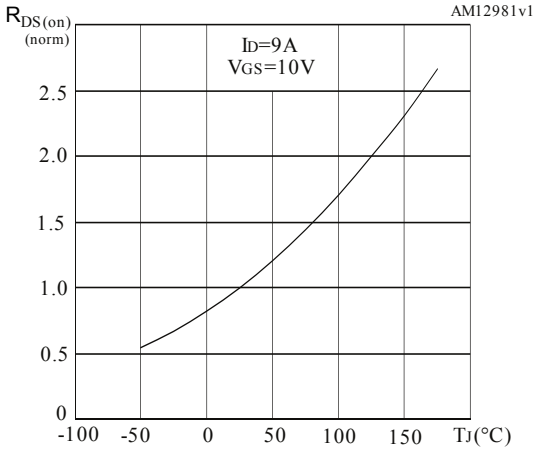
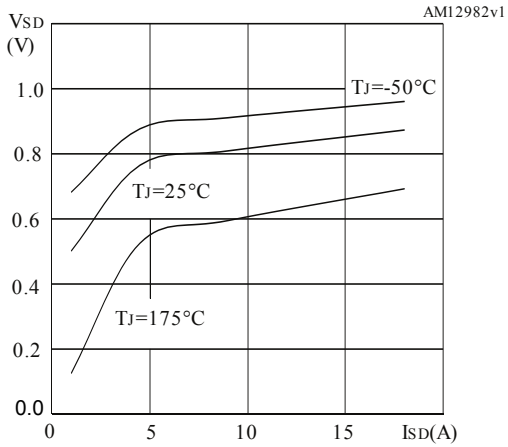
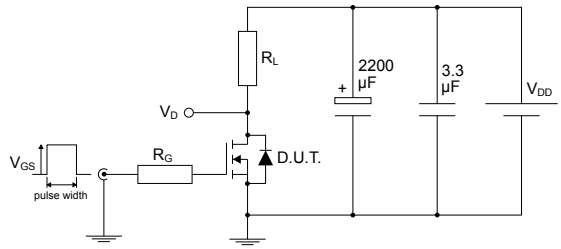


Figure 11. Typical reverse diode forward characteristics



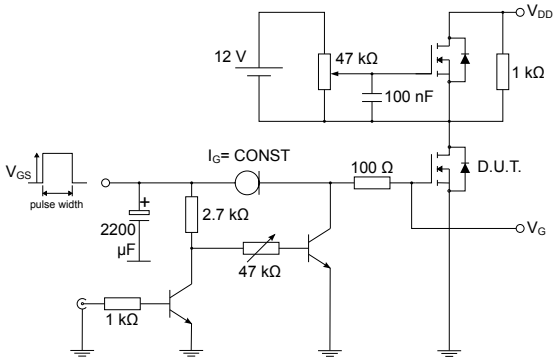
3 Test circuits

Figure 12. Test circuit for resistive load switching times



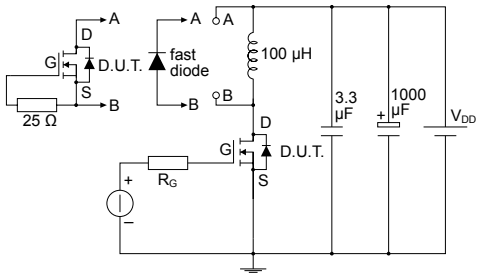
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Figure 13. Test circuit for gate charge behavior



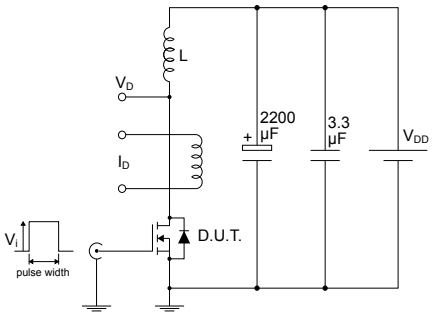
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Figure 14. Test circuit for inductive load switching and diode recovery times



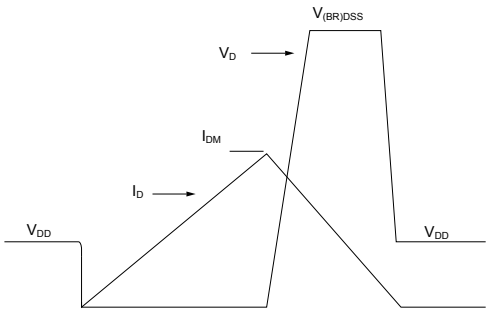
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Figure 15. Unclamped inductive load test circuit



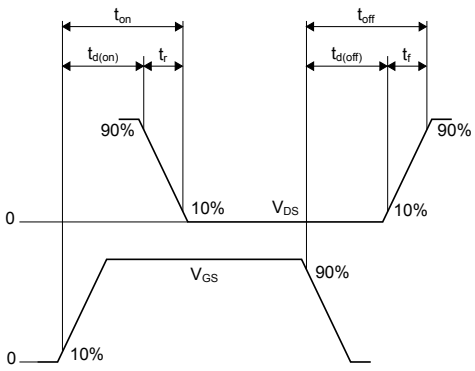
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Figure 16. Unclamped inductive waveform



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Figure 17. Switching time waveform



AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 18. **D²PAK (TO-263) type A package outline**

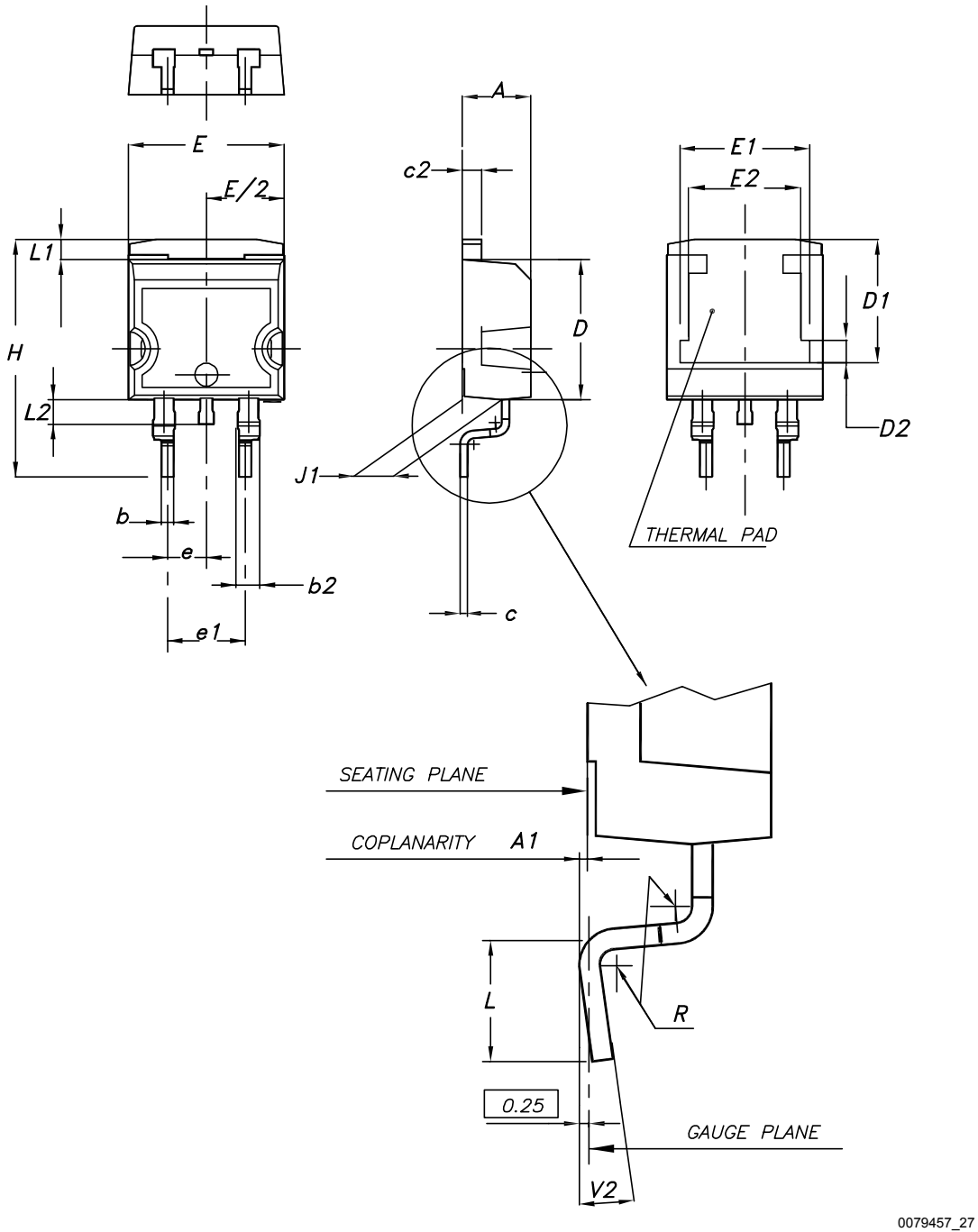
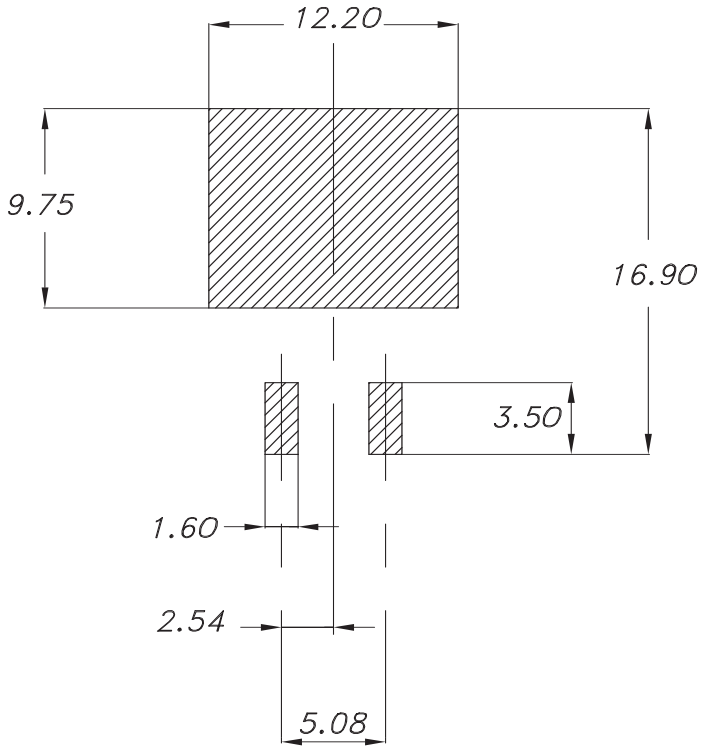


Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

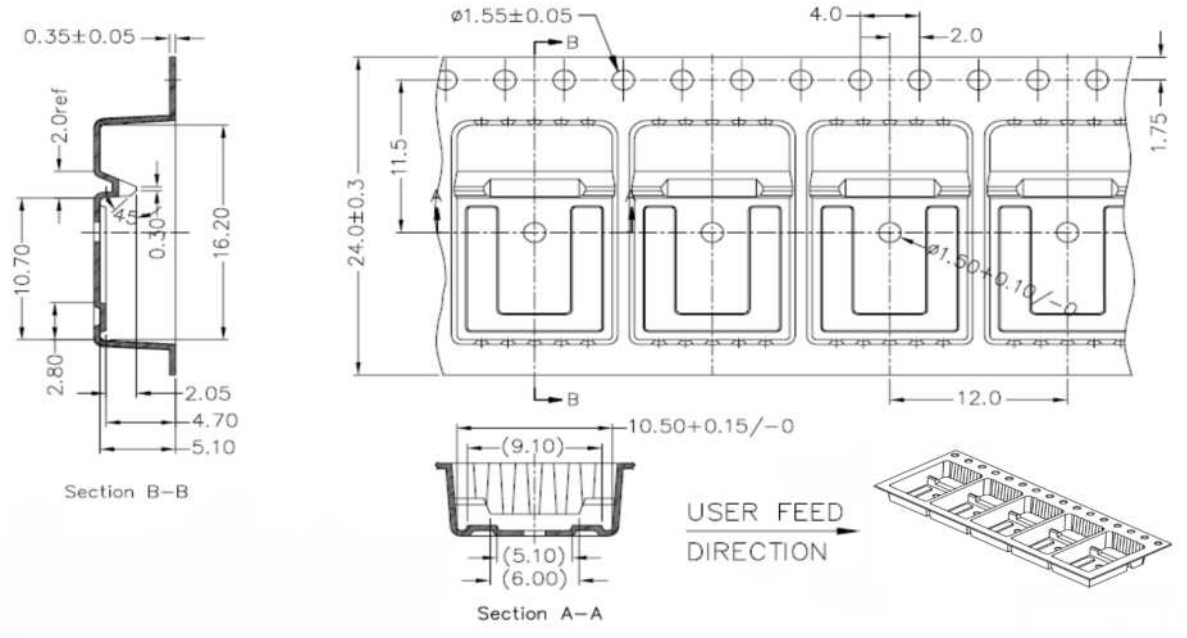
Figure 19. D²PAK (TO-263) recommended footprint (dimensions are in mm)



0079457_Rev27_footprint

4.2 D²PAK packing information

Figure 20. D²PAK tape drawing (dimensions are in mm)



DM01095771_2

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
13-Jan-2012	1	First release.
23-May-2012	2	Section *2.1: Electrical characteristics (curves)* has been added. Document status promoted from preliminary data to production data.
06-Aug-2013	3	– Updated: *Section 4: Package mechanical data* – Updated: *Figure 13, 14, 15* and *16* – Added: dv/dt in *Table 2* – Minor text changes
25-Jul-2025	4	Updated Section 4: Package information. Minor text changes.

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