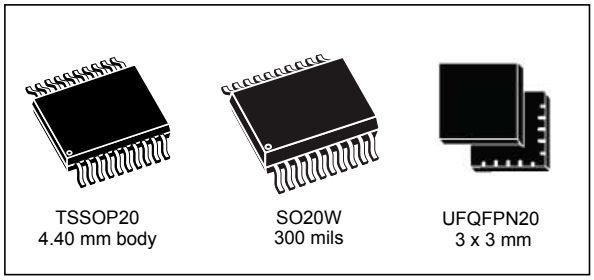
STM8SPLNB1

DiSEqC™ slave microcontroller for SaTCR based LNBs and switchers

Datasheet - production data

Features

- Clock, reset and supply management
  - Reduced power consumption,
  - Safe power on/off management by low voltage detector (LVD),
  - 2.95 to 5.5 V operating voltage,
  - Internal 16MHz oscillator.
- Communication interface
  - Two DiSEqC™ communication interfaces,
  - Four I^2C communication interfaces I/O ports.
- 4 output pins for control of a legacy matrix.

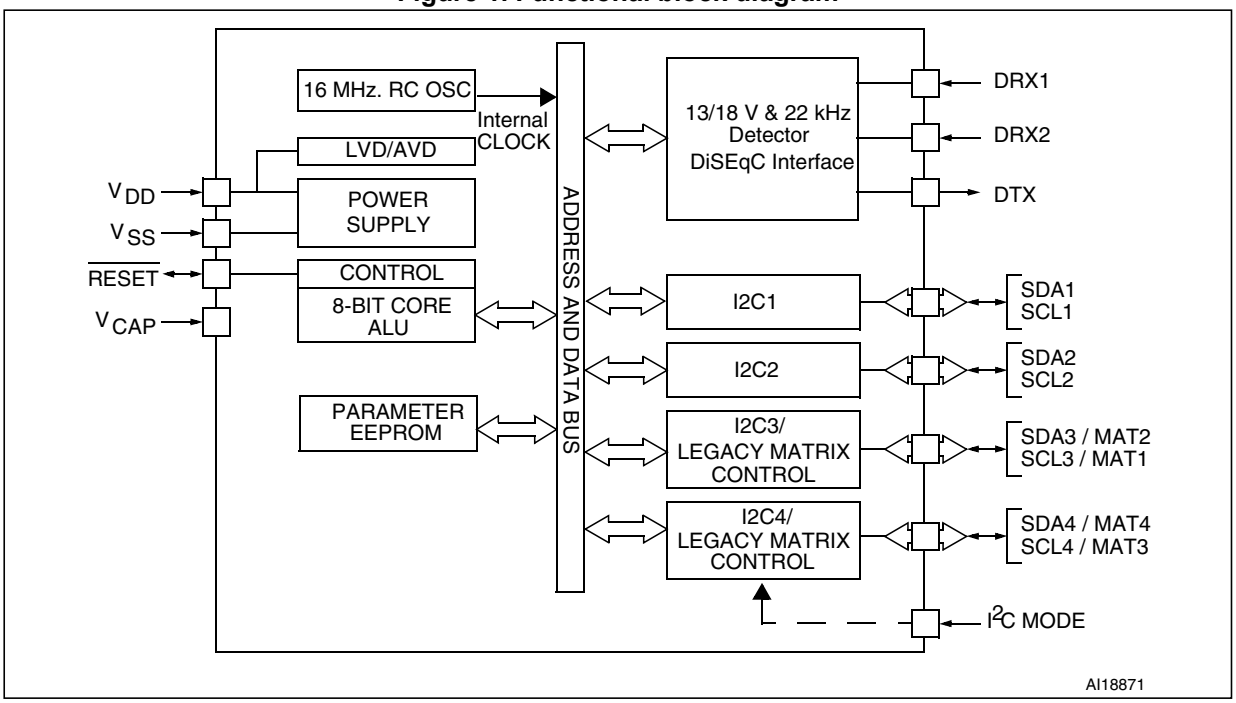


It is a complete hardware and firmware solution for system designers who require an implementation overview of the LNB device control according to DiSEqC standard (Digital Satellite Equipment Control).

Description

The STM8SPLNB1 is an 8-bit microcontroller dedicated to DiSEqC slave operation in SaTCR based LNBs (Low Noise Block) and switchers.

Figure 1. Functional block diagram



This is information on a product in full production. www.st.com

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1 Device description

1.1 Implementation

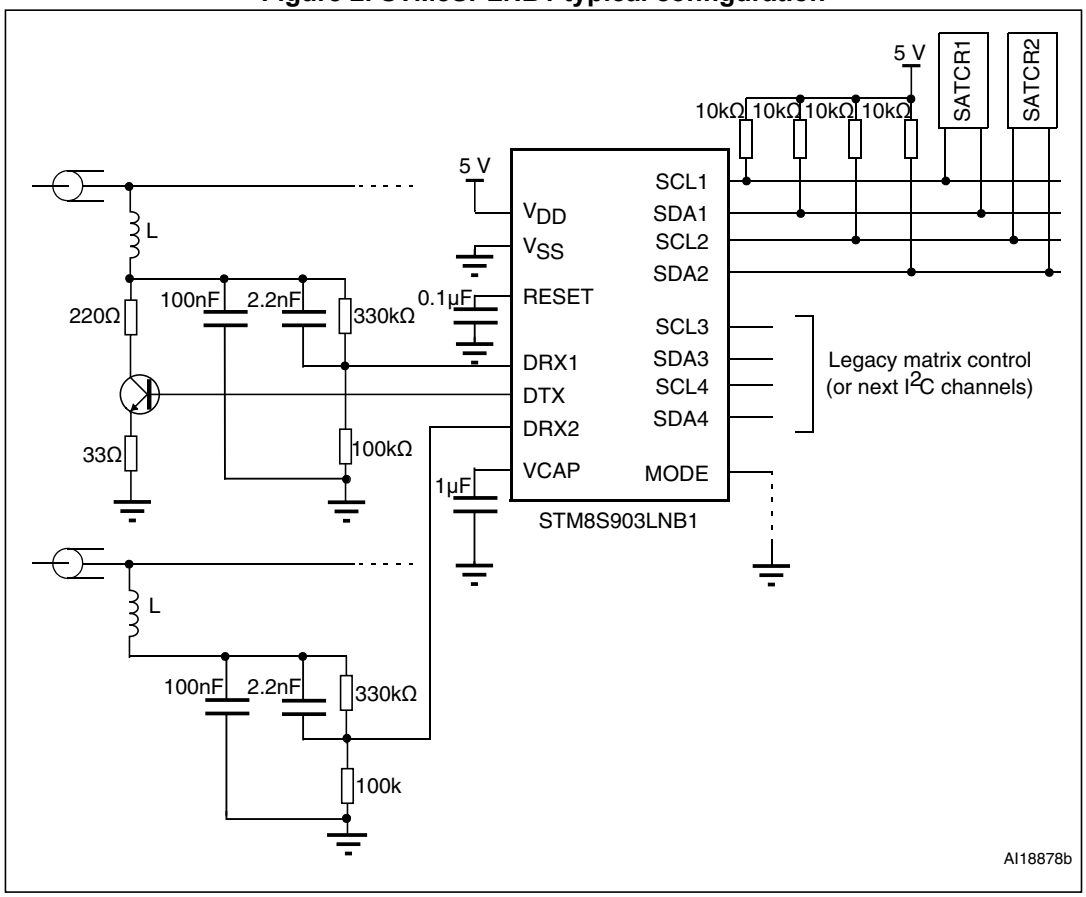
STM8SPLNB1 device is receiving DiSEqC signal on the coaxial cable, decoding and processing the DiSEqC commands. As a result, legacy matrix or I^2C lines are controlled. The STM8SPLNB1 device can also send DiSEqC answer back to master through coaxial cable.

STM8SPLNB1 is designed for usage with LNB devices with I^2C bus control and/or direct pins control (see *Figure 2: STM8SPLNB1 typical configuration*). SaTCR1 device is typically used in LNB application (see *www.st.com* for more SaTCR1 information).

Behavior of STM8SPLNB1 devices can be modified through a set of configuration parameters which are stored in device data EEPROM memory. Configuration is done also through specific DiSEqC commands. After final configuring the device can be locked to given configuration (vendor configuration).

Figure 2: STM8SPLNB1 typical configuration shows the recommended configuration for the hardware connections for LNB control with STM8SPLNB1 devices.

Figure 2. STM8SPLNB1 typical configuration



1. Power supply must have level 5V +/- 10% for correct operation.

1.1.1 Pins description

Figure 3. TSSOP20/SO20W pinout

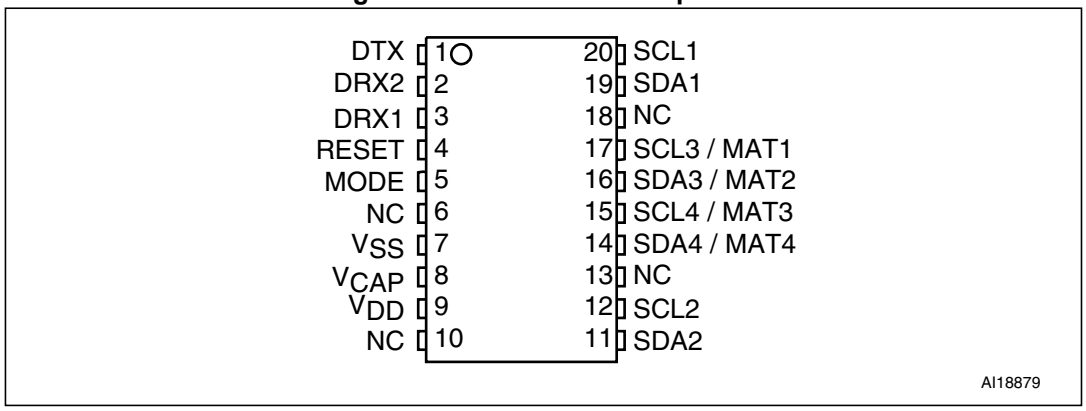


Figure 4. UFQFPN20 pinout

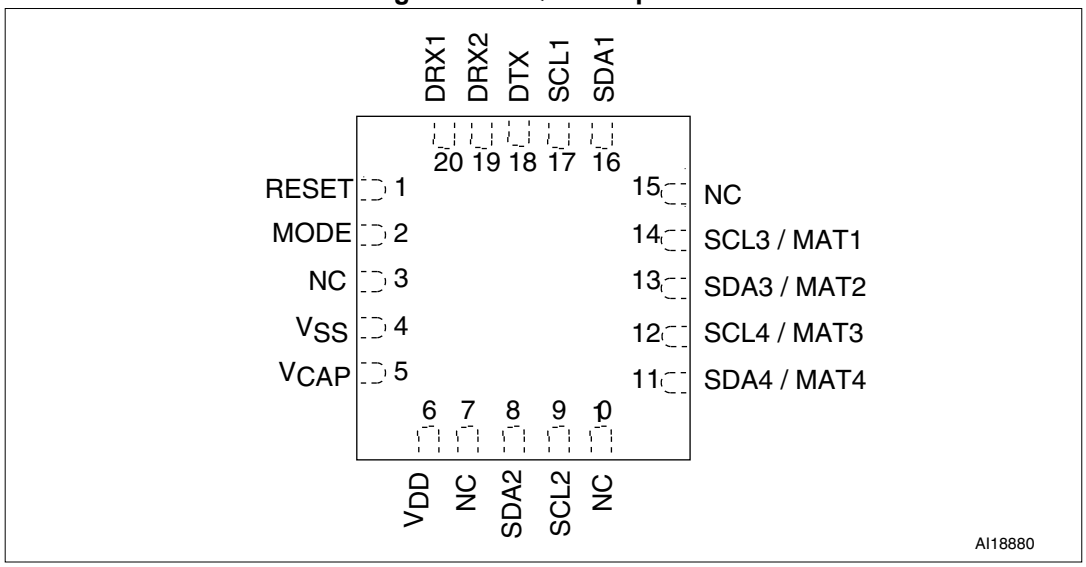


Table 1. STM8SPLNB1 pins description

pin no. TSSOP20 /SO20W	pin no. UFQFPN20	pin name	description	note
9	6	V_{DD}	+5 V power supply	+/- 10 % tolerance
7	4	V_{SS}	ground	_
4	1	RESET	device reset	0.1 µF capacitor to ground (active low)
8	5	V_{CAP}	filtering capacitor	1 µF capacitor to ground
3	20	DRX1	DiSEqC receive data input 2	HF signal after low pass filtering
2	19	DRX2	DiSEqC receive data input 2	HF signal after low pass filtering - secondary channel (less priority - see later description)

Table 1. STM8SPLNB1 pins description (continued)

pin no. TSSOP20 /SO20W	pin no. UFQFPN20	pin name	description	note
1	18	DTX	DiSEqC transmit data output	22 kHz modulation signal - need coupling to HF signal
20	17	SCL1	I^2C clock output	I^2C master channel 1 clock output
19	16	SDA1	I^2C data input/output	I^2C master channel 1 data input/output
12	9	SCL2	I^2C clock output	I^2C master channel 2 clock output
11	8	SDA2	I^2C data input/output	I^2C master channel 2 data input/output
17	14	SCL3	I^2C clock output	I^2C master channel 3 clock output
16	13	SDA3	I^2C data input/output	I^2C master channel 3 data input/output
15	12	SCL4	I^2C clock output	I^2C master channel 4 clock output
14	11	SDA4	I^2C data input/output	I^2C master channel 4 data input/output
5	2	MODE	I^2C addressing mode select	Selection of I^2C addressing mode - see note (2) under *Table 2: SaTCRs implementation - ST7LNB1 compatible mode* (pin has internal pull-up)

2 STM8SPLNB1 operation

STM8SPLNB1 has 8 output pins which can work as 4 I^2C master channels. Each I^2C channel can address 2 LNB devices (2 different I^2C addresses: 0xC8 and 0xCA) - see *Table 2: SaTCRs implementation - ST7LNB1 compatible mode* and *Table 3: SaTCRs implementation - incremental order mode* for assignment of given SaTCR to given I^2C bus and address.

Assignment depends from *I^2C addressing mode* EEPROM parameter - see *Table 14: STM8SPLNB1 EEPROM parameters*. As a convention, SaTCR1 must be associated to the BPF having the lowest center frequency of the application, SaTCR2 to the BPF having the next higher center frequency and so on.

Table 2. SaTCRs implementation - ST7LNB1 compatible mode

SatCR number	SaTCR(1)	SaTCR address	I^2C number
0	SaTCR1	0xC8	I^2C1
1	SaTCR2	0xCA	
2	SaTCR3	0xC8	I^2C2
3	SaTCR4	0xCA	
4	SaTCR5	0xC8	I^2C3
5	SaTCR6	0xCA	
6	SaTCR7	0xC8	I^2C4
7	SaTCR8/ legacy SaTCR (for wide RF band applications)	0xCA	

1. Selection of ST7LNB1 compatible mode: *pin MODE* (see *Table 1: STM8SPLNB1 pins description*) must be grounded and I2C addressing mode EEPROM parameter (see *Table 14: STM8SPLNB1 EEPROM parameters*) must be set to 0. Otherwise (e.g. pin MODE is left open or I2C addressing mode EEPROM parameter is set to 1) is used incremental order mode.

Table 3. SaTCRs implementation - incremental order mode

SatCR number	SaTCR(1)	SaTCR address	I^2C number
0	SaTCR1	0xC8	I^2C1
1	SaTCR2	0xCA	I^2C2
2	SaTCR3	0xC8	I^2C3
3	SaTCR4	0xCA	I^2C4
4	SaTCR5	0xCA	I^2C1
5	SaTCR6	0xC8	I^2C2
6	SaTCR7	0xCA	I^2C3
7	SaTCR8/ legacy SaTCR (for wide RF band applications)	0xC8	I^2C4

1. Selection of incremental order mode: *pin MODE* (see *Table 1: STM8SPLNB1 pins description*) is left open or I2C addressing mode EEPROM parameter (see *Table 14: STM8SPLNB1 EEPROM parameters*) is set to 1.

Another option is to decrease number of I^2C channels and use the remaining pins for legacy matrix LNB control - e.g. to have 2 I^2C channels (4 pins) and 4 legacy matrix output pins - see *Table 16: Application types*.

Operation mode and device behavior depends from final hardware configuration. This behavior is selected through configuration parameters - see *Table 14: STM8SPLNB1 EEPROM parameters*.

Note: Advantage of using incremental order mode is in applications with up to 4 SaTCRs - which is common in practice. Then each SaTCR owns one I^2C bus. I2C communication with another SaTCRs is running on different I^2C bus - so it does not disturb HF signal on given SaTCR (SaTCR is sensitive to I^2C bus signal transients).
Advantage of using ST7LNB1 compatible mode is in applications where is used SaTCRs control together with legacy matrix outputs (MAT1-MAT4) - see Section 1.1.1: Pins description. In this case there remains free only 2 I^2C buses for SaTCRs control (MAT1-MAT4 pins occupy I^2C3 and I^2C4 bus). In ST7LNB1 compatible mode 2 I^2C buses can address up to 4 SaTCRs - 2 SaTCRs per I^2C bus. Disadvantage is the I^2C bus disturbance to SaTCR which is not addressed - shared I^2C bus (HF filters on I^2C buses is recommended).

2.1 Supported DiSEqC commands

In the following *Table 4: STM8SPLNB1 DiSEqC™ supported commands* are listed DiSEqC commands supported by STM8SPLNB1. For more details about commands, refer to the *DiSEqC™ slave microcontroller specifications* at www.eutelsat.com.

Table 4. STM8SPLNB1 DiSEqC™ supported commands

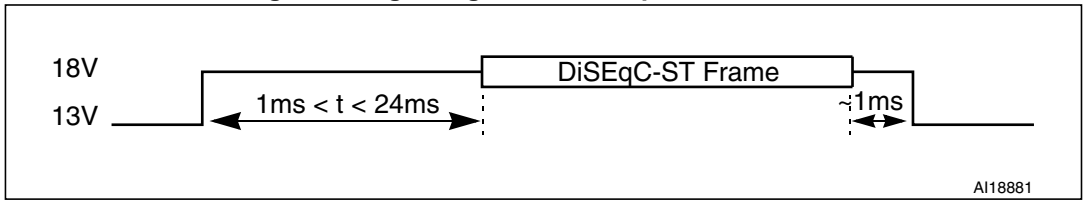
command number	command name	function
0x00	RESET	Reset DiSEqC™ microcontroller
0x0D	config read	Read configuration parameters from EEPROM
0x0F	config write	Write configuration parameters to EEPROM
0x38	write to port	DiSEqC 1.0: Write to port group command - Legacy commands
0x5A	operation command	DiSEqC-ST normal operation commands: ODU_Changechannel or ODU_SatCROFF
0x5B	installation command	DiSEqC-ST installation commands: ODU_Config, ODU_EEPvar.LOFREQ or ODU_SatCRxON

2.2 DiSEqC commands details

2.2.1 Command signaling

To be detected, the DiSEqC-ST commands must be sent after a voltage change from 13 to 18 V. A delay time between 4 ms and 24 ms must be respected before sending the DiSEqC-ST commands (see *Figure 5: Signaling of the DiSEqC-ST command*).

Figure 5. Signaling of the DiSEqC-ST command



2.2.2 Command 0x0F

STM8SPLNB1 devices are shipped to customers with a default parameter values. These parameters can be updated using a dedicated 0x0F DiSEqC command. This command has the following format where “[data]” is the parameter value to be programmed at the “[index]” location as described in *Table 14: STM8SPLNB1 EEPROM parameters*.

Table 5. Command 0x0F format

frame	DiSEqC™ address	command	data1	data2
0xE0/0xE2	[device address]	0x0F	[index]	[data]

Note: The special command E0 xx 0F FF FF protects the EEPROM data from any subsequent write access (where xx is the corresponding DiSEqC slave address).

2.2.3 Command 0x0D

This command is dedicated for reading configuration parameters. This command has the following format where the “[index]” is location to be read as shown in *Table 14: STM8SPLNB1 EEPROM parameters*.

Table 6. Command 0x0D format

frame	DiSEqC™ address	command	data1
0xE2	[device address]	0x0D	[index]

The format of the reply frame from slave has format according *Table 7: Reply to command 0x0D format* where “[data]” is the byte read from EEPROM.

Table 7. Reply to command 0x0D format

frame	data1
0xE4	[data]

2.2.4 Command 0x38

This command is used to write to port group command - legacy support.

For application supporting the legacy (except for application number 1), the backwards signaling (13/18 V, 22 kHz tone) is recognized until a valid DiSEqC 1.0 command is detected.

The following *Table 8: Command 0x38 format* presents the truth table for the legacy commands.

Table 8. Command 0x38 format

command	equivalent backward signalling	selected feed	band	polarity	satellite
E0 xx 38 F0	13V / 0kHz	0	Low	Vertical	A
E0 xx 38 F1	13V / 22kHz	1	High	Vertical	A
E0 xx 38 F2	18V / 0kHz	2	Low	Horizontal	A
E0 xx 38 F3	18V / 22kHz	3	High	Horizontal	A

2.2.5 Command 0x5A

This command is used during LNB (or switched) normal operation (default operation after configuration). Command 0x5A is DiSEqC command (see *Table 9: Command 0x5A format*) with two data bytes. In dependence from those data bytes are performed two subcommands which descriptions are in *Table 10: Subcommands 0x5A format - ODU_SaTCR_Op*.

Table 9. Command 0x5A format

frame	DiSEqC™ address	command	data1	data2
0xE0/0xE2	[device address]	0x5A	[data1](1)	[data2](1)

1. See *Table 10: Subcommands 0x5A format - ODU_SaTCR_Op* for details.

Table 10. Subcommands 0x5A format - ODU_SaTCR_Op

subcommand	data1			data2	description
	[7:5]	[4:2]	[1:0]	[7:0]	
ODU_ChangeChannel	SaTCR(1)	Feed(2)	Tun[9:8](3)	Tun[7:0](3)	This command is used for the channel selection.
ODU_PowerOff	SaTCR(1)	0		0x00	This command is used to put a SaTCR in low power mode.

1. SaTCR number - see *Table 2: SaTCRs implementation - ST7LNB1 compatible mode*.
2. Feed parameter - see *Table 11: Feeds* and *Table 15: Truth table for support of 8 RF inputs*.
3. Tuning word - see notes in *Table 14: STM8SPLNB1 EEPROM parameters* for description.

Table 11. Feeds(1)

Feed	RF input		
	Band	Polarization	Satellite
0	Low	Vertical	A
1	High	Vertical	A
2	Low	Horizontal	A
3	High	Horizontal	A
4	Low	Vertical	B
5	High	Vertical	B
6	Low	Horizontal	B
7	High	Horizontal	B

1. Applications supporting legacy are limited to one satellite only (satellite A - see *Table 8: Command 0x38 format*).

2.2.6 Command 0x5B

This command is used only during LNB (or switched) installation/configuration. Command 0x5B is DiSEqC command (see *Table 12: Command 0x5B format*) with two data bytes. In dependence from those data bytes are performed three subcommands which descriptions are in *Table 13: Subcommands 0x5B format - ODU_SaTCR_Inst*.

Table 12. Command 0x5B format

frame	DiSEqC™ address	command	data1	data2
0xE0/0xE2	[device address]	0x5B	[data1](1)	[data2](1)

1. See *Table 13.: Subcommands 0x5B format - ODU_SaTCR_Inst* for details.

Table 13. Subcommands 0x5B format - ODU_SaTCR_Inst

Subcommand	data1			data2	description
	[7:5]	[4:2]	[1:0]	[7:0]	
ODU_Config	SaTCR(1)	0	1	AppliNum(2)	This command is sent by the STB in order to set the STM8SPLNB1 application number. If the data2 value corresponds to the STM8SPLNB1 AppliNum, then the STM8SPLNB1 commands SaTCR indicated in data1 to send a tone having frequency: F = BPF(4), else: F = (BPF + 20 MHz).
ODU_Lofreq	SaTCR(1)	0	2	LOfreqNum(3)	This command is sent by the STB in order to set the L.O. frequencies present in the LNB. If the data2 value corresponds to the STM8SPLNB1 LOfreqNum, then the STM8SPLNB1 commands SaTCR indicated in data1 to send a tone having frequency: F = BPF(4), else: F = (BPF + 20 MHz).
ODU_SaTCRxSignalOn	xxh	0		xxh	When receiving this command the STM8SPLNB1 commands all connected SaTCRs to send a tone in order to indicate their respective BPF(4) center frequencies.

1. SaTCR number - see *Table 2: SaTCRs implementation - ST7LNB1 compatible mode*
2. See *Table 17: DiSEqC Applications* for details.
3. See *Table 18: Local oscillator frequencies* for details.
4. BPF is bandpass center frequency for a given SaTCR - see *Table 14: STM8SPLNB1 EEPROM parameters* for details.

3 Configuration parameters

STM8SPLNB1 devices are compliant with the Eutelsat DiSEqC slave microcontroller specifications version 1.0, but they are not scanning the control pins to determine the slave configuration. Instead this are the slave configuration parameters stored in EEPROM memory and must be programmed for each specific application through programming parameters in STM8SPLNB1 data EEPROM memory.

The EEPROM parameters described are the default configurations in our firmware. Custom configurations can be programmed at factory on request according customer requirements (FastROM process available). Customer can reprogram all EEPROM parameters through DiSEqC command - see *Section 2.2.2: Command 0x0F*.

3.1 Configuration parameters

The slave configuration parameters for STM8SPLNB1 are listed in *Table 14: STM8SPLNB1 EEPROM parameters*:

Table 14. STM8SPLNB1 EEPROM parameters

index	parameter	description	default value
00	Slave Address	DiSEqC slave address(1)	0x11
01	SaTCR1 BPF (lsb)	(2)	0x5D
02	SaTCR1 BPF (msb)		0x02
03	SaTCR2 BPF (lsb)		0xC6
04	SaTCR2BPF (msb)		0x02
05	SaTCR3 BPF (lsb)		0x48
06	SaTCR3 BPF (msb)		0x03
07	SaTCR4 BPF (lsb)		0xFC
08	SaTCR4 BPF (msb)		0x03
09	SaTCR5 BPF (lsb)		0xFF
0A	SaTCR5BPF (msb)		0xFF
0B	SaTCR6 BPF (lsb)		0xFF
0C	SaTCR6 BPF (msb)		0xFF
0D	SaTCR7 BPF(lsb) / legacy SaTCR Low band (msb)	(3)	0xFF
0E	SaTCR7 BPF(msb) / legacy SaTCR Low band (lsb)		0xFF
0F	SaTCR8 BPF(lsb) / legacy SaTCR High band (msb)		0xFF
10	SaTCR8 BPF(msb) / legacy SaTCR High band (lsb)		0xFF
11	Applitype	Application type number (refer to *Table 16.*)	0x00

Table 14. STM8SPLNB1 EEPROM parameters (continued)

index	parameter	description	default value
12	AppliNum	Application number (refer to *Table 17: DiSEqC Applications*)	0x04
13	High L.O freq Number	Refer to *Table 18: Local oscillator frequencies*	0x04
14	Low L.O freq Number	Refer to *Table 18: Local oscillator frequencies*	0x02
15	SaTCR1 matrix truth table	(4)	0xAC
16			0x35
17	SaTCR2 matrix truth table		0x59
18			0x6A
19	SaTCR3 matrix truth table		0x56
1A			0x9A
1B	SaTCR4 matrix truth table		0x95
1C			0xA6
1D	SaTCR5 matrix truth table		0xFF
1E			0xFF
1F	SaTCR6 matrix truth table		0xFF
20			0xFF
21	SaTCR7 matrix truth table		0xFF
22			0xFF
23	SaTCR8 matrix truth table / legacy matrix		0xFF
24			0xFF
25	SaTCRs GAIN(5)	SaTCRs 1 to 4 Gain	0xFF
26		SaTCRs 5 to 8 Gain	0xFF
27	SaTCRs number	(6)	0x04
28	I^2C addressing mode	defines SaTCRs assignment to I^2C bus(7)	0x00
29	Software Version Number	version number identification	0x15
2A	Reserved	(8)	0x00
2B			0x00

1. Address 0x00 is also recognized as valid address.
2. SaTCRx BPF = BPFx center frequency [MHz]/2.

3. When an application supports the wide RF band only one local oscillator with a frequency FLO is present in the LNB. In this case the selection of the high or the low band for the legacy output is performed by a dedicated SaTCR.

Two parameters are needed for the band selection:
- The tuning word for the low band selection = [(FLO (MHz) - FLow (MHz))/4] - 350: where FLow corresponds to the Low LO frequency.
- The tuning word for the high band selection = [(FLO (MHz) - FHigh (MHz))/4] - 350: where FHigh corresponds to the High band LO frequency.

Example: in a wide band application with FLO= 13250 MHz, for emulating a low band local oscillator at 9750 MHz, index 0x0D and index 0x0E must be loaded with the decimal value dec [0D:0E] = round ((13250-9750)/4) - 350 = 525.

4. Matrix truth table for SaTCRx or legacy:
1) If 4 RF inputs are implemented then the matrix truth table has coding on 2 bytes: “aaaabbbbccccdddd” where:
aaaa = selection of Feed1 on SaTCRx, aaaa = [MAT4, MAT3, MAT2, MAT1]
bbbb = selection of Feed0 on SaTCRx, bbbb = [MAT4, MAT3, MAT2, MAT1]
cccc = selection of Feed3 on SaTCRx, cccc = [MAT4, MAT3, MAT2, MAT1]
dddd = selection of Feed2 on SaTCRx,dddd = [MAT4, MAT3, MAT2, MAT1]

2) If 8 RF inputs are implemented then the truth table given in *Table 15: Truth table for support of 8 RF inputs* is used.

5. To enable the support of 8 RF inputs: the value ‘0x0000’ has to be programmed in index 15h and 16h. SaTCRs gain value: it has the following format on two bytes: “AaBbCcDd EeFfGgHh” where Aa= gain for SaTCR1, Bb = gain for SaTCR2, Cc= gain for SaTCR3, Dd=gain for SaTCR4, Ee= gain for SaTCR5, Ff= gain for SaTCR6, Gg= gain for SaTCR7, Hh=gain for SaTCR8 or legacy SaTCR. Upper case letters and upper case letters indicate LNA and IF gain, respectively.

6. SaTCRs number does not include the legacy SaTCR for the wide RF band applications.

7. Defines assignment of SaTCR to I^2C bus. 1 = incremental order mode, 0 = ST7LNB1 compatible mode or incremental order mode in dependency from MODE pin (see *Table 1: STM8SPLNB1 pins description*) state. See notes under *Table 2: SaTCRs implementation - ST7LNB1 compatible mode* and *Table 3: SaTCRs implementation - incremental order mode* for details in assignment.

8. Reserved bytes: do not write to this location.

Table 15. Truth table for support of 8 RF inputs

Feed	MAT1	MAT2	MAT3	MAT4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0

Table 16. Application types

number	application type	description
0	SaTCR control(1) (see *Figure 6: SaTCR control configuration*)	– Control through I^2C of up to 8 SaTCRs

Table 16. Application types (continued)

number	application type	description
1	SaTCR and legacy (standard RF band) (see *Figure 7: SaTCR control and legacy configuration (standard RF band)*)	– Control through I^2C up to 4 SaTCRs – Control of a legacy matrix using up to 4 pins
2	SaTCR and legacy (wide RF band) (see *Figure 8: SaTCR control and legacy configuration (wide RF band)*)	– Control though I^2C of up to 6 SaTCRs + legacy – Control of a dedicated SaTCR for the legacy support

1. This application could support up to 8 RF feeds. (applications 1 and 2 are limited to 4 RF feeds).

Figure 6. SaTCR control configuration

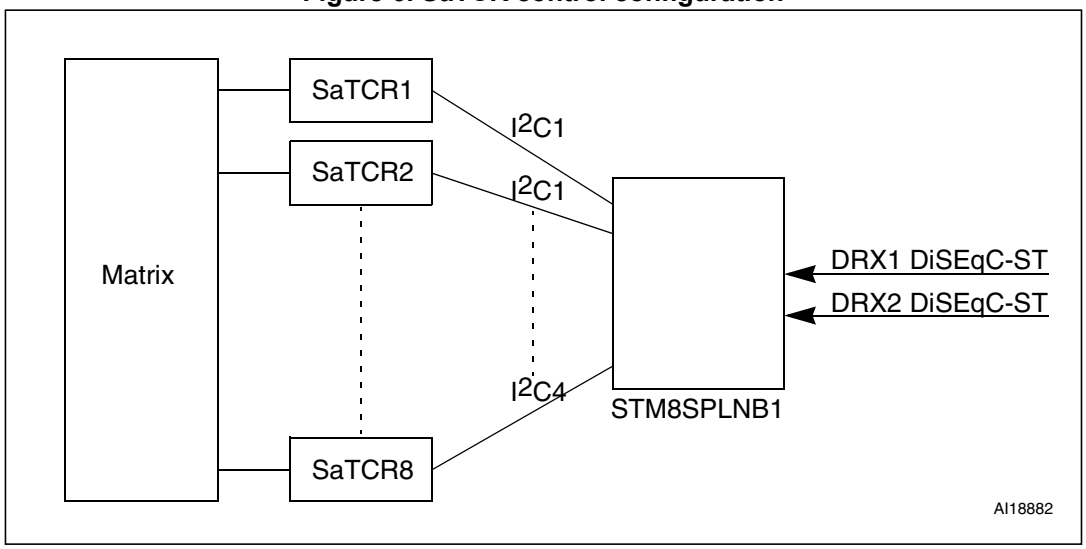


Figure 7. SaTCR control and legacy configuration (standard RF band)

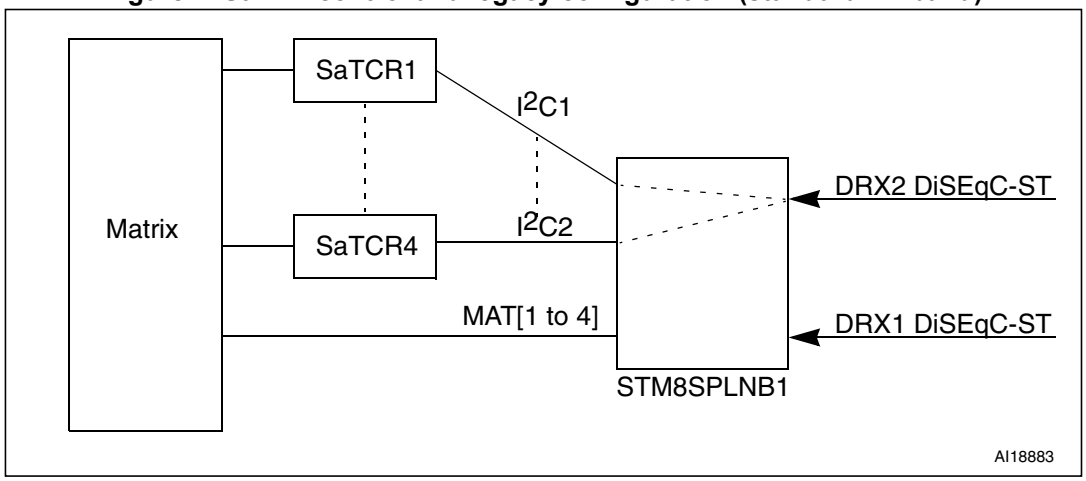


Figure 8. SaTCR control and legacy configuration (wide RF band)

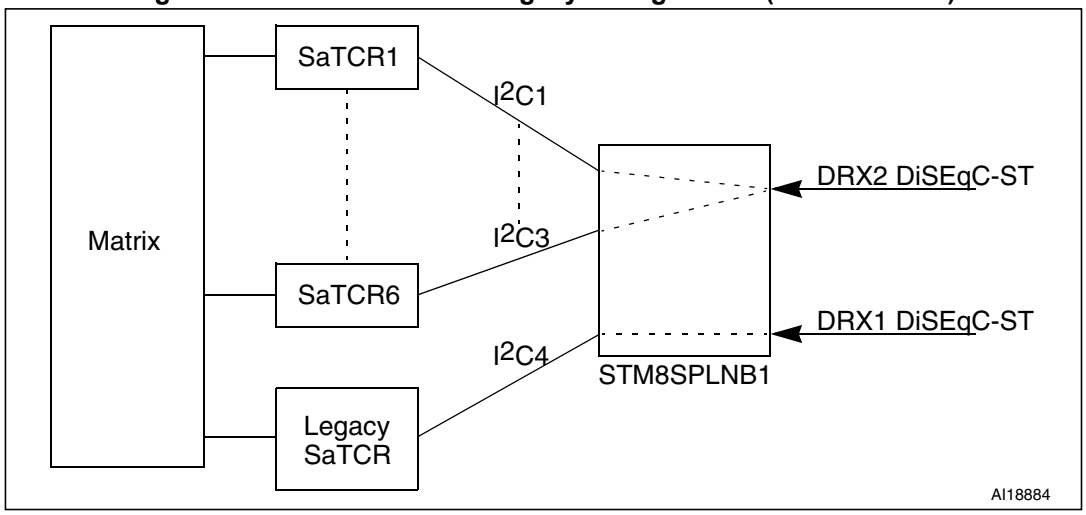


Table 17. DiSEqC Applications

Application number	Application description
0x01	Single SatCR and legacy (standard RF band)
0x02	Twin SatCR (standard RF band)
0x03	Twin SatCR and legacy (standard RF band)
0x04	Quad SatCR (standard RF band)
0x05	Double Twin SatCR (standard RF band)
0x06	Twin SatCR (wide RF band)
0x07	Twin SatCR and legacy (wide RF band)
0x08	Quad SatCR (wide RF band)
0x09	8 SatCR (standard RF band)
0x0A	6 SatCR (standard RF band)
0x0B	Quad SatCR and legacy (standard RF band)
0x0C - 0xFF	reserved

Table 18. Local oscillator frequencies

LofreqNum (hex)		Local oscillator frequency
Standard RF band	0x00	none
	0x01	not known
	0x02	9.750 GHz
	0x03	10.000 GHz
	0x04	10.600 GHz
	0x05	10.750 GHz
	0x06	11.000 GHz
	0x07	11.250 GHz
	0x08	11.475 GHz
	0x09	20.250 GHz
	0x0A	5.150 GHz
	0x0B	1.585 GHz
	0x0C	13.850 GHz
	0x0D	not allocated
	0x0E	not allocated
	0x0F	not allocated
Wide RF band	0x10	not allocated
	0x11	10.000 GHz
	0x12	10.200 GHz
	0x13	13.250 GHz
	0x14	13.450 GHz
	0x15 - 0x1F	not allocated

4 Electrical characteristics

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

4.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3 Σ).

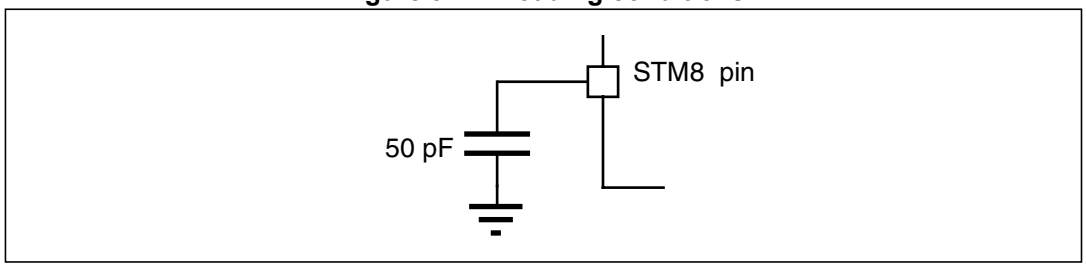
4.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5 V. They are given only as design guidelines and are not tested.

4.1.3 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the following figure.

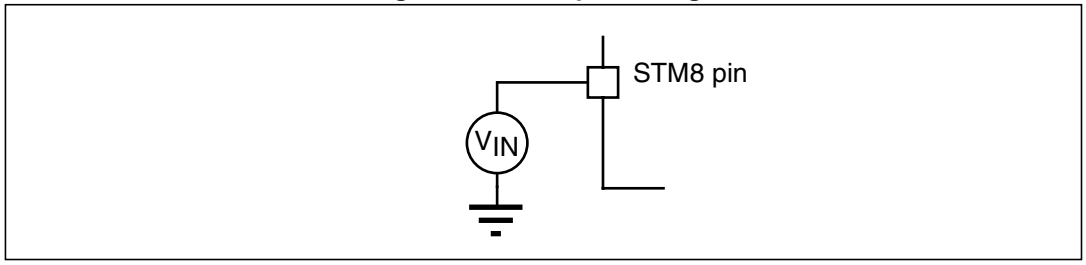
Figure 9. Pin loading conditions



4.1.4 Pin input voltage

The input voltage measurement on a pin of the device is described in the following figure.

Figure 10. Pin input voltage



4.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage	-0.3	6.5	V
V_{IN}	Input voltage on any pin	V_{SS} - 0.3	V_{DD} + 0.3	
V_{ESD}	Electrostatic discharge voltage	See *: Absolute maximum ratings (electrical sensitivity)*		

Table 20. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(2)	80	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	- 20	
$I_{INJ(PIN)}$(3)(4)	Injected current on NRST pin	± 4	
	Injected current on any other pin(5)	± 4	
$\Sigma I_{INJ(PIN)}$(3)	Total injected current (sum of all I/O and control pins)(5)	± 20	

1. Data based on characterization results, not tested in production.
2. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
4. Negative injection disturbs the analog performance of the device.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	

4.3 Operating conditions

4.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	-	0	16	MHz
V_{DD}	Standard operating voltage	-	2.95	5.5	V
V_{CAP}(1)	C_{EXT}: capacitance of external capacitor	-	470	3300	nF
	ESR of external capacitor	at 1 MHz(2)	-	0.3	Ω
	ESL of external capacitor		-	15	nH
P_D(3)	Power dissipation at T_A = 85 °C	TSSOP20	-	238	mW
		SO20W	-	220	
		UFQFPN20	-	220	
T_A	Ambient temperature	Maximum power dissipation	-40	85	°C
T_J	Junction temperature range	-	-40	105	

1. Care should be taken when selecting the capacitor, due to its tolerance, as well as the parameter dependency on temperature, DC bias and frequency in addition to other factors. The parameter maximum value must be respected for the full application range.
2. This frequency of 1 MHz as a condition for V_{CAP} parameters is given by design of internal regulator.
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$ (see *5.3: Thermal characteristics*)

Table 23. Operating conditions at power-up/power-down

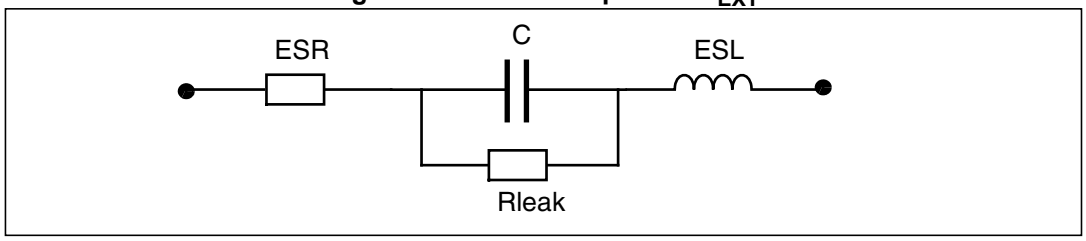
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	2	-	-	µs/V
	V_{DD} fall time rate(1)	-	2	-	-	
t_{TEMP}	Reset release delay	V_{DD} rising	-	-	1.7	ms
V_{IT+}	Power-on reset threshold	-	2.6	2.7	2.85	V
V_{IT-}	Brown-out reset threshold	-	2.5	2.65	2.8	
$V_{HYS(BOR)}$	Brown-out reset hysteresis	-	-	70	-	mV

1. Reset is always generated after a t_{TEMP} delay. The application must ensure that V_{DD} is still above the minimum operating voltage (V_{DD} min.) when the t_{TEMP} delay has elapsed.

4.3.2 V_{CAP} external capacitor

Stabilization for the internal voltage regulator is achieved connecting an external capacitor C_{EXT} to the V_{CAP} pin (see *Figure 2: STM8SPLNB1 typical configuration*). C_{EXT} is specified in *Table 22: General operating conditions*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 11. External capacitor C_{EXT}



1. ESR is the equivalent series resistance and ESL is the equivalent inductance.

4.3.3 Supply current characteristics

Total current consumption in run mode

The MCU is placed under the following conditions:

– All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)

Subject to general operating conditions for V_{DD} and T_A.

Table 24. Total current consumption at V_{DD} = 5 V

Symbol	Parameter	Conditions		Typ	Max(1)	Unit
$I_{DD(RUN)}$	Supply current in run mode	f_{CPU} = 16 MHz, V_{DD} = 5V	HSI RC osc. (16 MHz)	4.7	5.8	mA
		f_{CPU} = 16 MHz, V_{DD} = 3.3V	HSI RC osc. (16 MHz)	4.7	5.8	
$I_{DD(R)}$	Supply current in reset state(2)	V_{DD} = 5 V	-	400	-	µA

1. Data based on characterization results, not tested in production.
2. Characterized with all I/Os tied to V_{SS}.

Table 25. Output driving current

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level	I_{IO} = 10 mA, V_{DD} = 5 V	-	2	V
		I_{IO} = 4 mA, V_{DD} = 3.3 V	-	1(1)	
V_{OH}	Output high level	I_{IO} = 10 mA, V_{DD} = 5 V	2.8	-	
		I_{IO} = 4 mA, V_{DD} = 3.3 V	2.1(1)	-	

1. Data based on characterization results, not tested in production

4.3.4 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

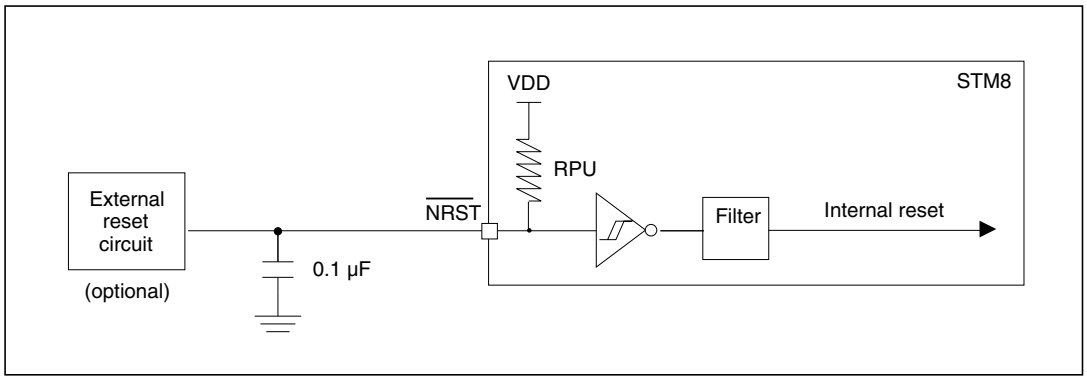
Table 26. RESET pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(RST)}$	RESET Input low level voltage (1)	-	-0.3 V		0.3 x V_{DD}	V
$V_{IH(RST)}$	RESET Input high level voltage (1)	-	0.7 x V_{DD}		V_{DD} + 0.3	
$R_{PU(RST)}$	RESET Pull-up resistor (2)	-	30	55	80	kΩ

1. Data based on characterization results, not tested in production.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.

The reset network shown in the following *Figure 12.* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in the *Table 26.: RESET pin characteristics*. Otherwise the reset is not taken into account internally.

Figure 12. Recommended reset pin protection



4.3.5 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709 (EMC design guide for STMicrocontrollers).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the application.

1. Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values.

Table 27. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25 °C, f_{CPU} = 16 MHz (HSI clock), conforming to IEC 1000-4-2	2/B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}= 3.3 V, T_A = 25 °C, f_{CPU} = 16 MHz (HSI clock), conforming to IEC 1000-4-4	4/A

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 28. EMI data

Symbol	Parameter	Conditions			Unit
		General conditions	Monitored frequency band	f_{CPU} (1)	
				16 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V T_A = 25 °C LQFP32 package Conforming to SAE J 1752/3	0.1 MHz to 30 MHz	3	dBµV
			30 MHz to 130 MHz	10	
			130 MHz to 1 GHz	7	
	SAE EMI level		SAE EMI level	2.5	

1. Data based on characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU, and DLU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). One model can be simulated: Human body model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 29. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25 °C, conforming to JESD22-A114	A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A LQFP32 package = 25 °C, conforming to SD22-C101	IV	1000	

1. Data based on characterization results, not tested in production

Static latch up

Two complementary static tests are required on ten parts to assess the latch up performance:

- A supply overvoltage (applied to each power supply pin)
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch up standard. For more details, refer to the application note AN1181.

Table 30. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch up class	$T_A = 25$ °C	A
		$T_A = 85$ °C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

5 Package information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.2 Package mechanical data

5.2.1 TSSOP package mechanical data

Figure 13. 20-pin, 4.40 mm body, 0.65 mm pitch

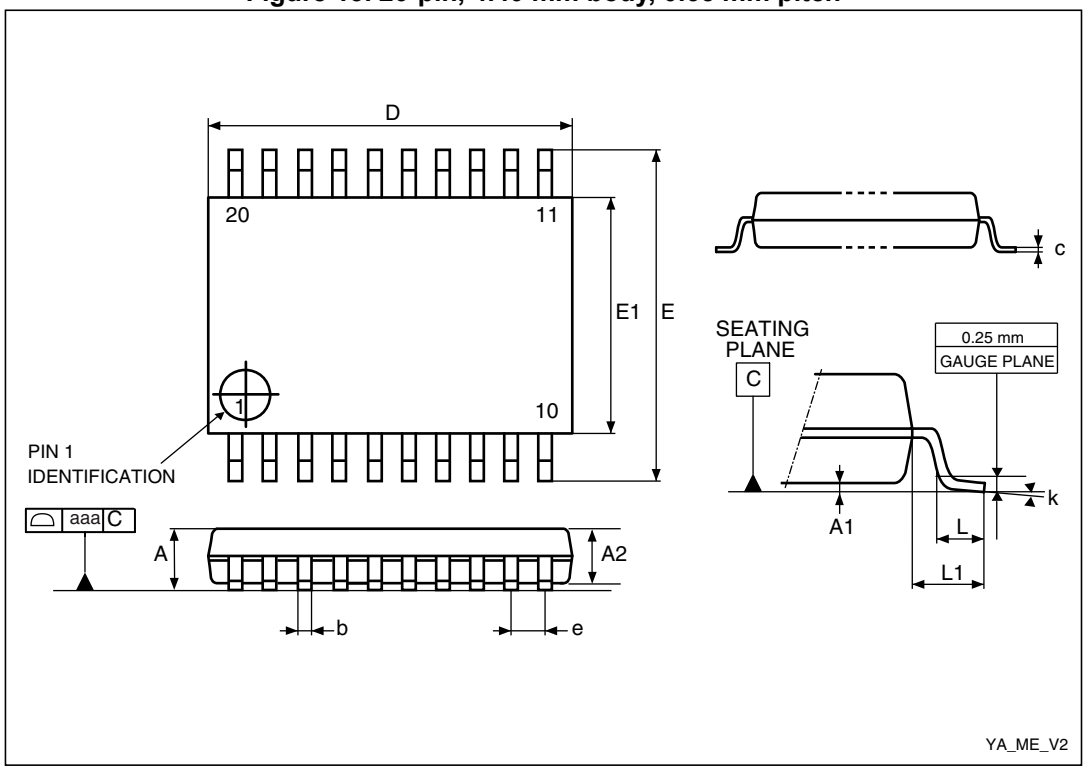


Table 31. 20-pin, 4.40 mm body, 0.65 mm pitch mechanical data

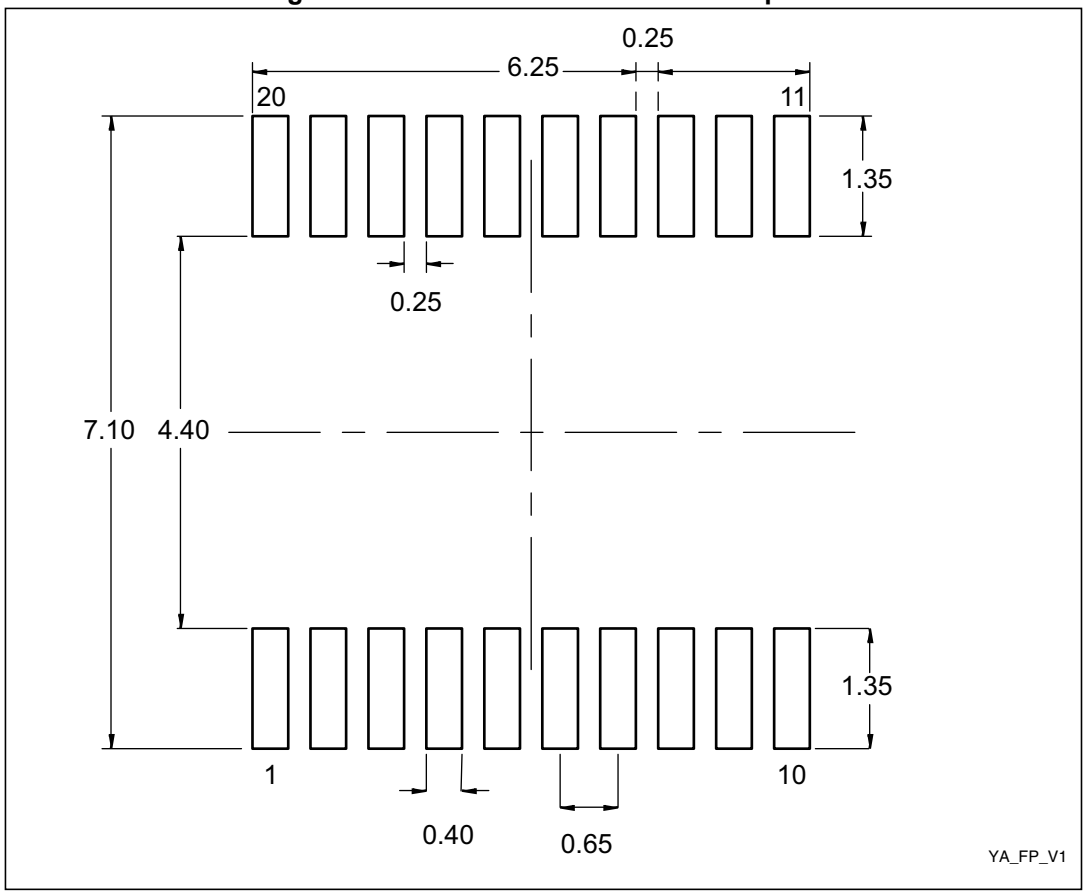
Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D[2]	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1[3]	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

Table 31. 20-pin, 4.40 mm body, 0.65 mm pitch mechanical data (continued)

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
k	0.0°	-	8.0°	0.0°	-	8.0°
aaa	0.100			0.0039		

1. Values in inches are converted from mm and rounded to 4 decimal digits
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 14. TSSOP20 recommended footprint



5.2.2 SO20W package mechanical data

Figure 15. 20-pin, plastic small outline (300 mils) package

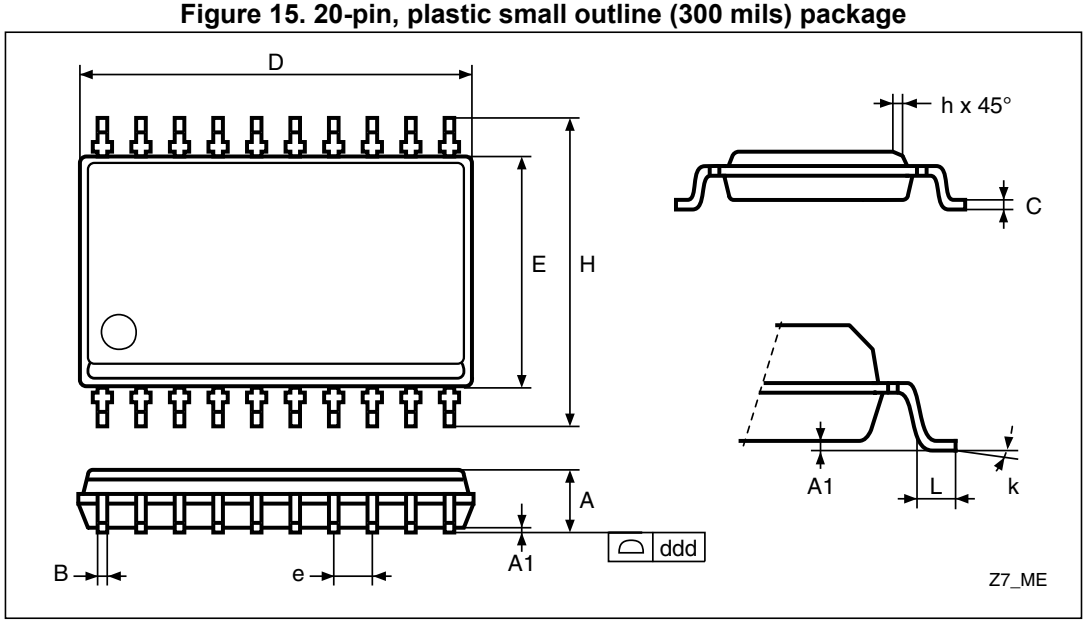


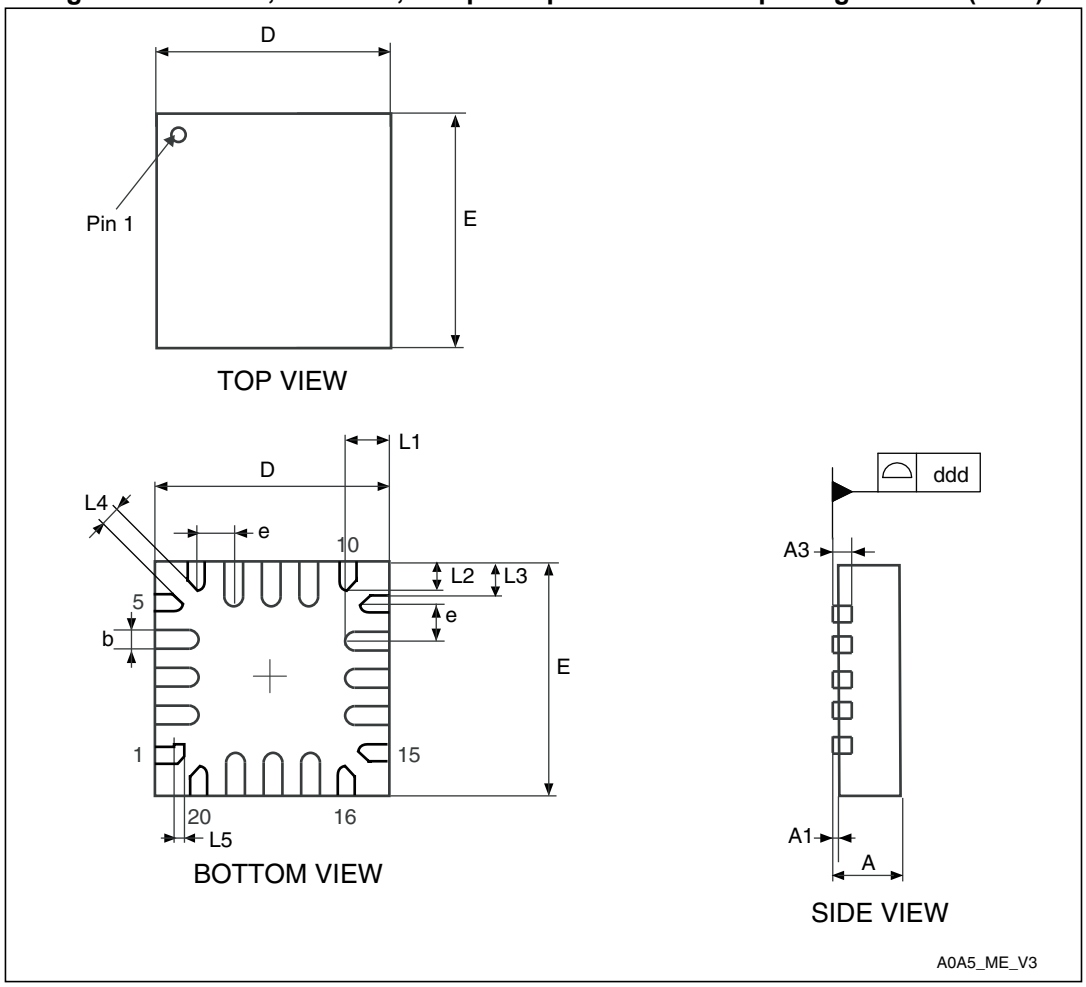
Table 32. 20-pin, plastic small outline (300 mils) mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	2.350	-	2.650	0.0925	-	0.1043
A1	0.100	-	0.300	0.0039	-	0.0118
B	0.330	-	0.510	0.0130	-	0.0201
C	0.230	-	0.320	0.0091	-	0.0126
D	12.600	-	13.000	0.4961	-	0.5118
E	7.400	-	7.600	0.2913		0.2992
e	-	1.270	-	-	0.0500	-
H	10.000	-	10.650	0.3937	-	0.4193
h	0.250	-	0.750	0.0098	-	0.0295
L	0.400	-	1.270	0.0157	-	0.0500
k	0.0°	-	8.0°	0.0°	-	8.0°
-	Tolerance (mm)			Tolerance (inches)		
ddd	0.100			0.0039		

1. Values in inches are converted from mm and rounded to 4 decimal digits

5.2.3 UFQFPN package mechanical data

Figure 16. 20-lead, ultra thin, fine pitch quad flat no-lead package outline (3 x 3)



1. Drawing is not to scale

Table 33. 20-lead, ultra thin, fine pitch quad flat no-lead package (3 x 3) package mechanical data

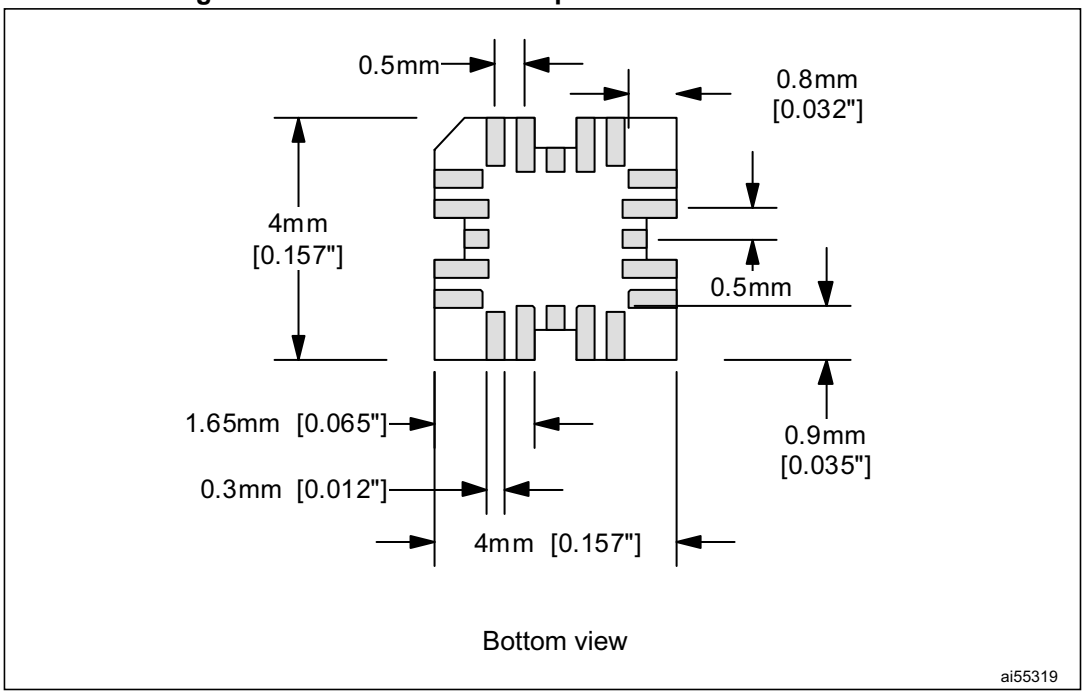
Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
D	-	3.000	-	-	0.1181	-
E	-	3.000	-	-	0.1181	-
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
e	-	0.500	-	-	0.0197	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157

Table 33. 20-lead, ultra thin, fine pitch quad flat no-lead package (3 x 3) package mechanical data (continued)

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
L3	-	0.375	-	-	0.0148	-
L4	-	0.200	-	-	0.0079	-
L5	-	0.150	-	-	0.0059	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
ddd		0.050			0.0020	

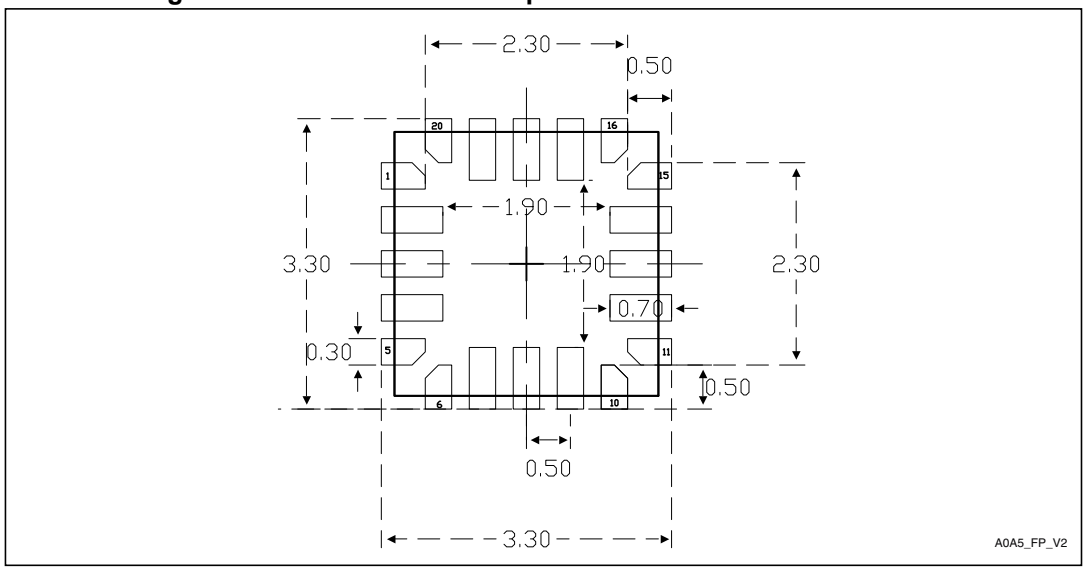
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 17. Recommended footprint for on-board emulation



1. Drawing is not to scale

Figure 18. Recommended footprint without on-board emulation



1. Drawing is not to scale
2. Dimensions are in millimeters

5.3 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 22: General operating conditions*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 34. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient TSSOP20 - 4.4 mm	84	°C/W
	Thermal resistance junction-ambient SO20W - (300 mils)	91	
	Thermal resistance junction-ambient UFQFPN20 - 3 x 3 mm	90	

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

5.3.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

6 Ordering information

6.1 STM8SPLNB1 DiSEqC™ SLAVE microcontroller option list

(Last update: Sept 2010)

Customer	.....
Address	.....
Contact	.....
Phone no.	.....
Reference FASTROM Code	FASTROM code name is assigned by STMicroelectronics

Conditioning (check only one option):

Tape & reel [ ] or Tube/Tray[ ]

Package type (check only one option):

TSSOP20 [ ] or SO20W [ ] or UFQFPN20 [ ]

EEPROM Parameters:

(any modified default settings [DEF] should be written in the Custom boxes [CUST])

INDEX	PARAMETER	DEF	CUST
00	Slave Address	11h	[h]
01	SaTCR1 BPF (lsb)	5Dh	[h]
02	SaTCR1 BPF (msb)	02h	[h]
03	SaTCR2 BPF (lsb)	C6h	[h]
04	SaTCR2BPF (msb)	02h	[h]
05	SaTCR3 BPF (lsb)	48h	[h]
06	SaTCR3 BPF (msb)	03h	[h]
07	SaTCR4 BPF (lsb)	FCh	[h]
08	SaTCR4 BPF (msb)	03h	[h]
09	SaTCR5 BPF (lsb)	FFh	[h]
0A	SaTCR5BPF (msb)	FFh	[h]
0B	SaTCR6 BPF (lsb)	FFh	[h]
0C	SaTCR6 BPF (msb)	FFh	[h]
0D	SaTCR7 BPF(lsb)/Legacy, SaTCR Low band(msb)	FFh	[h]
0E	SaTCR7 BPF(msb)/Legacy, SaTCR Low band (lsb)	FFh	[h]
0F	SaTCR8 BPF(lsb)/Legacy, SaTCR High band (msb)	FFh	[h]

10	SaTCR8 BPF(msb)/Legacy, SaTCR High band (lsb)	FFh	[h]
11	Applitype	00h	[h]
12	AppliNum	04h	[h]
13	High L.O freq Number	04h	[h]
14	Low L.O freq Number	02h	[h]
15	SaTCR1 matrix truth table	ACh	[h]
16		35h	[h]
17	SaTCR2 matrix truth table	59h	[h]
18		6Ah	[h]
19	SaTCR3 matrix truth table	56h	[h]
1A		9Ah	[h]
1B	SaTCR4 matrix truth table	95h	[h]
1C		A6h	[h]
1D	SaTCR5 matrix truth table	FFh	[h]
1E		FFh	[h]
1F	SaTCR6 matrix truth table	FFh	[h]
20		FFh	[h]
21	SaTCR7 matrix truth table	FFh	[h]
22		FFh	[h]
23	SaTCR8 matrix truth table	FFh	[h]
24	Legacy matrix	FFh	[h]
25	SaTCRs GAIN	FFh	[h]
26		FFh	[h]
27	SaTCRs number	04h	[h]
28	I2C addressing mode	00h	[h]
29	Software version	15h	[h]

(Please refer to *Table 14: STM8SPLNB1 EEPROM parameters* in the datasheet for full descriptions and notes of EEPROM Parameters)

Comments	.....
Notes	.....
Date	.....
Signature	.....

Appendix A DiSEqC™ protocol basics

For better understanding the document is here small overview of DiSEqC™ protocol (Digital Satellite Equipment Control).

A.1 Physical layer

The DiSEqC™ message is transferred between master and slave(s) through existing coaxial cable which delivers also the HF signal. The slave device(s) can be also powered through the same coaxial cable from master.

A.1.1 DC voltage on coaxial cable

Powering of the slave devices is performed by applying DC voltage on HF signal. The voltage level should be from 13 V to 18 V. Slave device uses this voltage for powering itself after some voltage regulator (e.g. +5 V regulator).

The voltage level also signalizes different DiSEqC™ state. There exists 2 states:

- 13 V voltage level
- 18 V voltage level

Those states are used in DiSEqC™ protocol signalization - horizontal or vertical polarization selection.

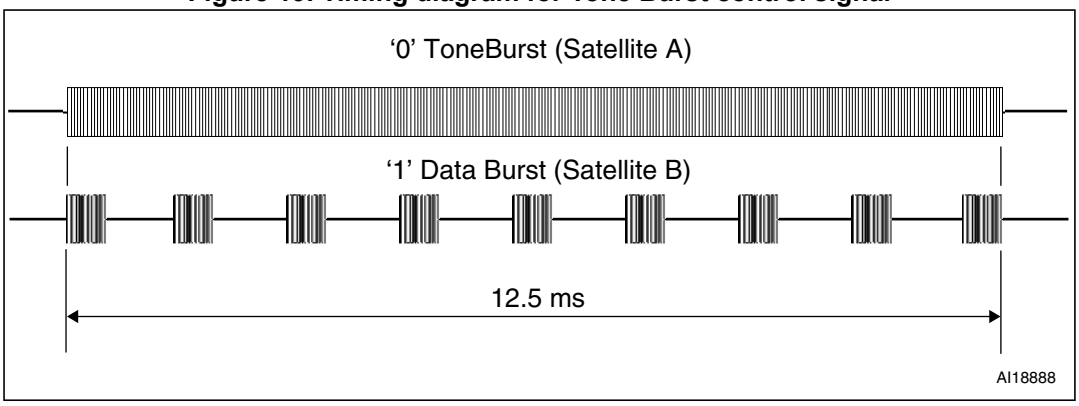
A.1.2 22 kHz signal on coaxial cable

To the signal on coaxial cable - HF signal and DC voltage - can be modulated 22 kHz signal. Presence of 22 kHz signal signalizes different state and is used in DiSEqC™ protocol signalization. Amplitude of 22 kHz signal is around 0.5 Vpp (peak to peak).

22 kHz tone presence selects *High frequency band* and no tone selects *Low frequency band*.

Satellite selection (satellite A or B) is made also according 22 kHz tone. If 22 kHz tone is transmitted continuously then *satellite A* is selected. If 22 kHz tone is transmitted in burst sequence then *satellite B* is selected (duration of this selection is 12.5 ms).

Figure 19. Timing diagram for Tone Burst control signal



A.1.3 Data transfer on coaxial cable

The 22 kHz signal is also used for data communication through coaxial cable (bidirectional transfer). In this case is used amplitude modulation of 22 kHz signal.

Bit “logical 0” coding:

- 1.0 ms 22 kHz signal
- 0.5 ms no signal

Bit “logical 0” coding:

- 0.5 ms 22 kHz signal
- 1.0 ms no signal

By this modulation is transferred full DiSEqC™ message (8 bits per byte + parity, several bytes in message - see *A.1: Physical layer*).

Figure 20. DiSEqC™ bit modulation

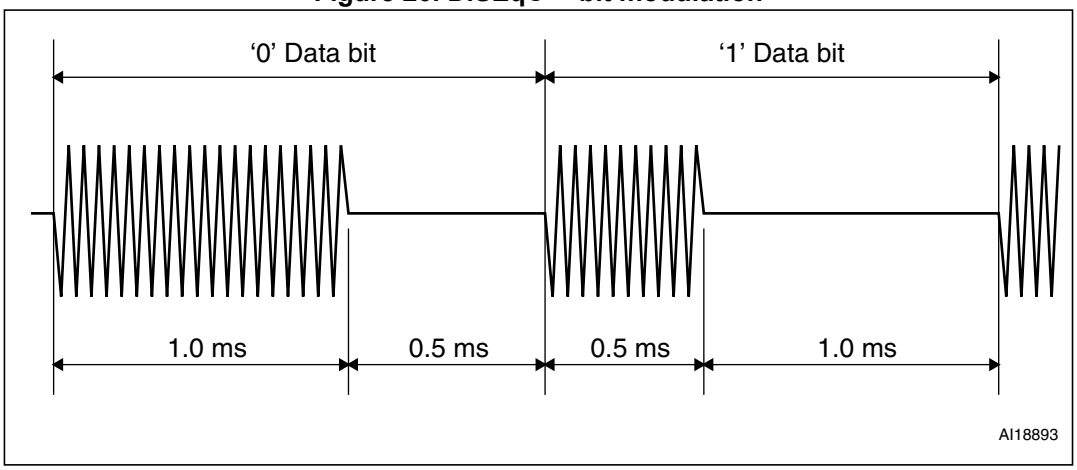
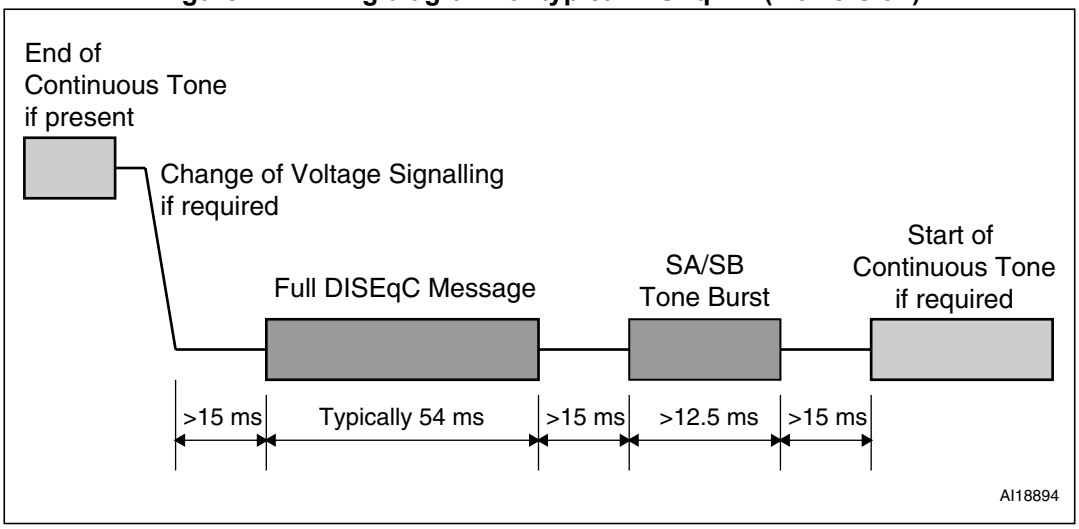


Figure 21. Timing diagram for typical DiSEqC™ (1.0 version)



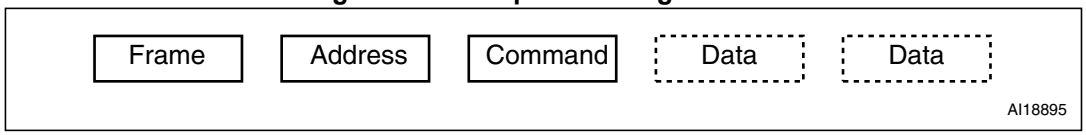
For more detailed information about DiSEqC™ protocol - see *DiSEqC™ bus functional specifications* and *DiSEqC™ slave microcontroller specifications.* Refer to www.eutelsat.com.

A.2 Protocol layer

The DiSEqC™ messages are transferred in packets. One packet consists from several bytes - each byte has 8 bits followed by parity bit (odd).

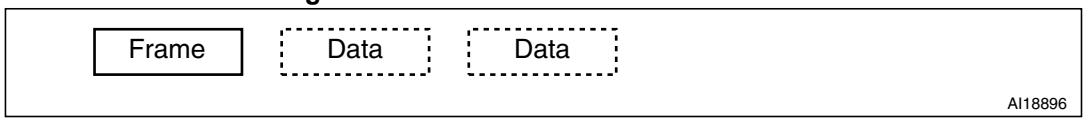
The full DiSEqC™ message contains a frame byte, an address byte, a command byte which can be followed by several data bytes.

Figure 22. DiSEqC™ message format



When host is requesting an answer from the slave (microcontroller) then the answer consists from frame byte which can be followed by several data bytes

Figure 23. Microcontroller answer format.



The frame byte identifies the direction, reply requirements and error status - see following *Table 35.*

Table 35. DiSEqC™ frame byte definition

Frame byte	definition
0xE0	Command from master, no reply required, first transmission
0xE1	Command from master, no reply required, repeated transmission
0xE2	Command from master, reply required, first transmission
0xE3	Command from master, reply required, repeated transmission
0xE4	Reply from slave, OK, no errors found
0xE5	Reply from slave, command not supported
0xE6	Reply from slave, parity error, repeat requested
0xE7	Reply from slave, command not recognized, repeat necessary

The address byte identifies the receiver. There also exist address groups (families). The family address is valid for all devices with similar (family) function - all given family devices receive message. Address families are described in *DiSEqC™ slave microcontroller specifications*. Universal (broadcast) address is 0x00 - all devices should receive messages with this address.

Command byte describes given command for device - according this command the device selects method for data processing.

Optional data bytes are data for given command. Data in answer (from slave) specify required information. There is specified data byte format only for 3 required bytes from slave:

- Status byte (bus collision, reset status, standby status, supply voltage)
- Configuration byte (more detailed information about current slave configuration)
- Switches byte (describes status of the committed switches)

For more information about format of those 3 data bytes refer to *DiSEqC™ slave microcontroller specifications* available at www.eutelsat.com (and *Table 4: STM8SPLNB1 DiSEqC™ supported commands*).

7 Revision history

Table 36. Document revision history

Date	Revision	Changes
28-Jul-2011	1	Initial release.
08-Sep-2011	2	Updated RESET capacitor value in *Figure 2: STM8SPLNB1 typical configuration*. Updated AppliNum and SaTCRs number parameters. Added note on V_{CAP} parameter in *Table 22: General operating conditions*.
03-Nov-2011	3	Updated datasheet description. Updated conditions and notes related to V_{CAP} parameter in *Table 22: General operating conditions*.
11-Jun-2012	4	Updated typical and maximum values of R_{PU} in *Table 26: RESET pin characteristics*. Modified *Figure 16: 20-lead, ultra thin, fine pitch quad flat no-lead package outline (3 x 3)* to add package top view.
18-Dec-2014	5	Updated: – *Section 5.2.1: TSSOP package mechanical data*, – *Section 5.2.2: SO20W package mechanical data*, – *Section 5.2.3: UFQFPN package mechanical data*.

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