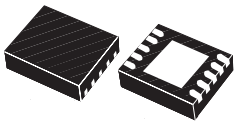
STEF12

Datasheet

Electronic fuse for 12 V line



DFN10L (3x3 mm)

Maturity status link
STEF12

Features

- Continuous current (typ): 3.6 A
- N-channel on-resistance (typ): 53 mΩ
- Enable/Fault functions
- Output clamp voltage (typ): 15 V
- Undervoltage lockout
- Short-circuit limit
- Overload current limit
- Controlled output voltage ramp
- Thermal latch (typ): 165 °C
- Operating junction temp. - 40 °C to 125 °C
- Available in DFN10 (3x3 mm) package
- UL2367 Recognized - File N. E468771

Applications

- Hard disk drives
- Solid state drives (SSD)
- Hard disk and SSD arrays
- Set-top boxes
- DVD and Blu-ray disc drivers

Description

The STEF12 is an integrated electronic fuse optimized for monitoring output current and input voltage. Connected in series to a 12 V rail, it is capable of protecting the electronic circuitry on its output from overcurrent and overvoltage. The device has a controlled delay and turn-on time.

When an overload condition occurs, the STEF12 limits the output current to a predefined safe value. If the anomalous overload condition persists it goes into an open state, disconnecting the load from the power supply. If a continuous short-circuit is present on the board, when power is re-applied the E-fuse initially limits the output current to a safe value and then again goes into an open state.

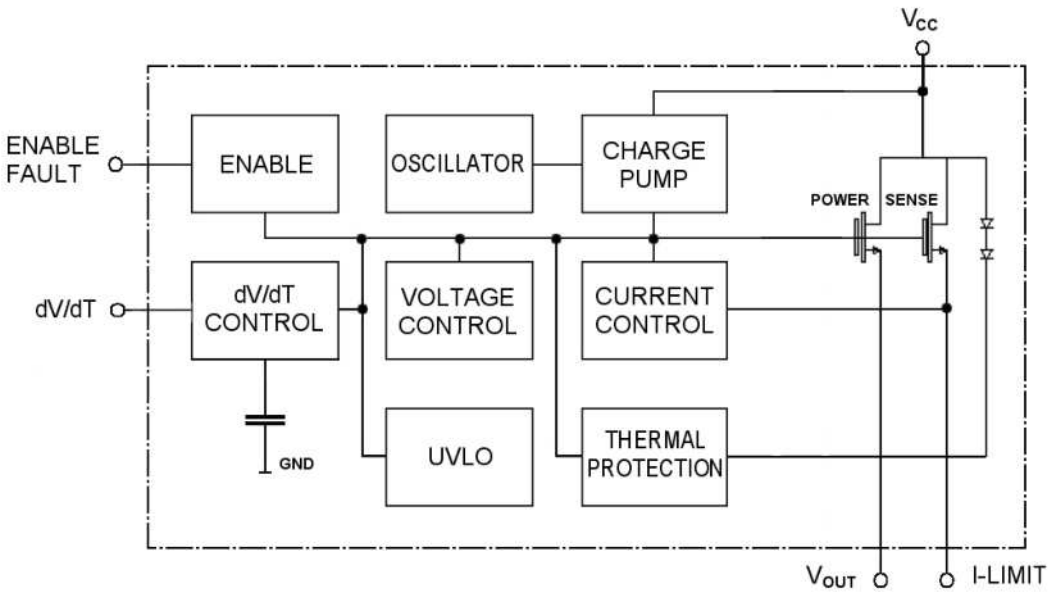
The device is equipped with a thermal protection circuit. The intervention of the thermal protection is signal led to the board monitoring circuits through a signal on the Fault pin.

Unlike the mechanical fuses, which must be physically replaced after a single event, the Efuse does not degrade in its performance after short-circuit/thermal protection interventions and it is reset either by recycling the supply voltage or using the Enable pin.

The companion chip for the 5 V power rails is also available with part number STEF05.

1 Device block diagram

Figure 1. **Block diagram**



2 Pin configuration

Figure 2. Pin connection (top view)

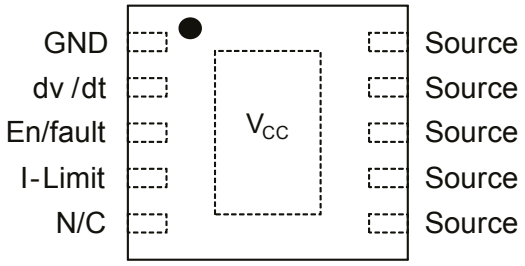


Table 1. Pin description

Pin n°	Symbol	Note
1	GND	Ground pin
2	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn-on. The internal capacitor allows a ramp-up time of around 1 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional capacitor is not required, this pin should be left open.
3	En/Fault	The Enable/Fault pin is a tri-state, bi-directional interface. During normal operation the pin must be left floating, or it can be used to disable the output of the device by pulling it to ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin goes into an intermediate state to signal a monitor circuit that the device is in thermal shutdown. It can be connected to another device of this family to cause a simultaneous shutdown during thermal events.
4	I-Limit	A resistor between this pin and the Source pin sets the overload and short-circuit current limit levels. Don't leave this pin unconnected.
5	NC	Not connected
6 to 10	V_{OUT}/Source	Connected to the source of the internal power MOSFET and to the output terminal of the fuse
11	V_{CC}	Exposed pad. Positive input voltage must be connected to V_{CC}.

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Positive power supply voltage (steady state)	-0.3 to 18	V
	Positive power supply voltage (max 100 ms)	-0.3 to 25	
V_{OUT}/source	(max 100 ms)	-0.3 to V_{CC}+0.3	V
I-Limit	(max 100 ms)	-0.3 to 25	V
En/Fault		-0.3 to 7	V
dv/dt		-0.3 to 7	V
T_{op}	Operating junction temperature range	-40 to 125	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering) 10 sec	260	°C

1. *The thermal limit is set above the maximum thermal rating. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	52.7	°C/W
R_{thJC}	Thermal resistance junction-case	17.4	°C/W

Table 4. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection	HBM	2	kV
		MM	200	V
		CDM	500	V

4 Electrical characteristics

Table 5. Electrical characteristics V_{CC} = 12 V, V_{EN} = 3.3 V, C_I = 10 µF, C_O = 47 µF, T_J = 25 °C (unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Under/Overvoltage protection						
V_{Clamp}	Output clamping voltage	V_{CC} = 18 V	13.8	15	16.2	V
V_{UVLO}	Undervoltage lockout	Turn-on, voltage rising	7.7	8.5	9.3	V
V_{Hyst}	UVLO hysteresis			0.80		V
Power MOSFET						
t_{dly}	Delay time	Enabling of chip to I_D = 100 mA with a 1 A resistive load		350		µs
R_{DSon}	On-resistance	(1)	35	53	70	mΩ
		-40 °C < T_J < 125 °C (2)			82	
V_{OFF}	Off state output voltage	V_{CC} = 18 V, V_{GS} = 0, R_L= infinite		40	100	mV
I_D	Continuous current	0.5in^2 pad, T_A = 25 °C (1)		3.6		A
		Minimum copper, T_A = 80 °C		1.7		
Current limit						
I_{Short}	Short-circuit current limit	R_{Limit} = 22 Ω	3.3	4.4	5.5	A
I_{Lim}	Overload current limit	R_{Limit} = 22 Ω		4.4		A
dv/dt circuit						
dv/dt	Output voltage ramp time	Enable to V_{OUT} = 11.7 V, No $C_{dv/dt}$	0.5	0.9	2.6	ms
Enable/Fault						
V_{IL}	Low level input voltage	Output disabled	0.35	0.58	0.81	V
$V_{I(INT)}$	Intermediate level input voltage	Thermal fault, output disabled	0.82	1.4	1.95	V
V_{IH}	High level input voltage	Output enabled	1.96	2.64	3.3	V
$V_{I(MAX)}$	High state maximum voltage		3.4	4.3	5.4	V
I_{IL}	Low level input current (sink)	V_{Enable} = 0 V		-10	-30	µA
I_I	High level leakage current for external switch	V_{Enable} = 3.3 V			1	µA
	Maximum fan-out for fault signal	Total numbers of chips that can be connected to this pin for simultaneous shutdown			3	Units
Total device						
I_{Bias}	Bias current	Device operational		1.5	2	mA
		Thermal shutdown		1		
V_{min}	Minimum operating voltage				7.6	V
Thermal latch						
T_{SD}	Shutdown temperature	(1)		165		°C

1. *Pulse test: Pulse width = 300 µs, Duty cycle = 2%.*
2. *Guaranteed by design, but not tested in production.*

5 Typical application

Figure 3. **Application circuit**

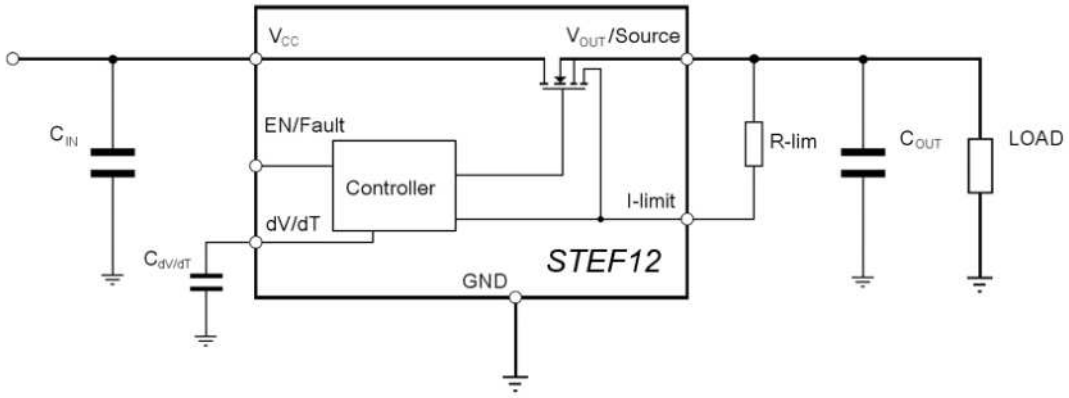
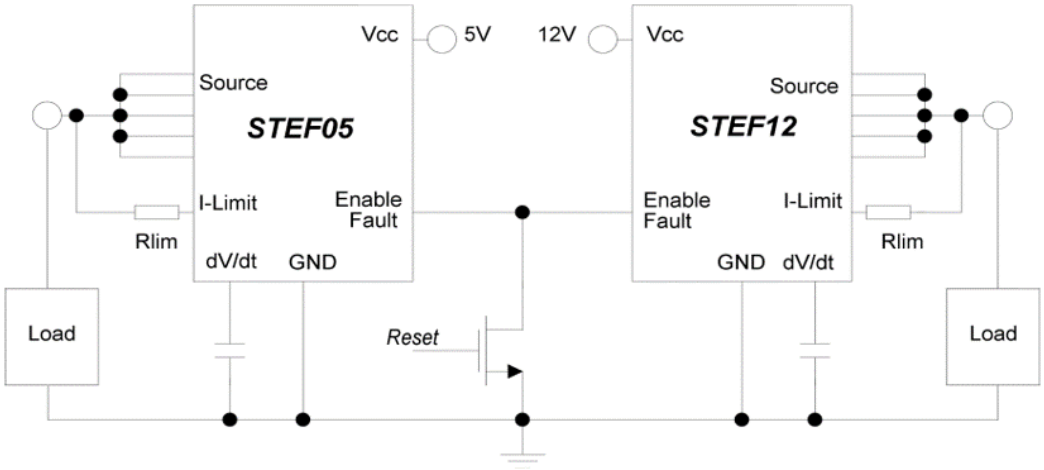


Figure 4. **Typical HDD application circuit**



5.1 Operating modes

5.1.1 Turn-on

When the input voltage is applied, the Enable/Fault pin goes up to the high state, enabling the internal control circuitry.

After an initial delay time of typically 350 µs, the output voltage is supplied with a slope defined by the internal dv/dt circuitry. If no additional capacitor is connected to dv/dt pin, the total time from the Enable signal going high and the output voltage reaching the nominal value is around 1 ms (refer to Figure 5, Figure 15).

5.1.2 Normal operating condition

The STEF12 E-fuse behaves like a mechanical fuse, buffering the circuitry on its output with the same voltage shown at its input, with a small voltage fall due to the N-channel MOSFET R_{DSOn}.

5.1.3 Output voltage clamp

This internal protection circuit clamps the output voltage to a maximum safe value, typically 15 V, if the input voltage exceeds this threshold.

5.1.4 Current limiting

When an overload event occurs, the current limiting circuit reduces the conductivity of the power MOSFET, in order to clamp the output current at the value selected externally by means of the limiting resistor R_{Limit} (Figure 3).

5.1.5 Thermal shutdown

If the device temperature exceeds the thermal latch threshold, typically 165 °C, the thermal shutdown circuitry turns the power MOSFET off, thus disconnecting the load. The EN/Fault pin of the device is automatically set at an intermediate voltage, in order to signal the overtemperature event. In this condition the E-fuse can be reset either by cycling the supply voltage or by pulling down the EN pin below the V_{il} threshold and then releasing it.

5.2 R limit calculation

As shown in Figure 3, the device uses an internal N-channel sense FET with a fixed ratio, to monitor the output current and limit it at the level set by the user.

The R_{Limit} value for achieving the requested current limitation can be estimated by using the following theoretical formula, together with the graph in Figure 13.

$$R_{Limit} = \frac{95}{I_{Short}} \quad (1)$$

5.3 $C_{dv/dt}$ calculation

Connecting a capacitor between the $C_{dv/dt}$ pin and GND allows the modification of the output voltage ramp-up time.

Given the desired time interval Δt during which the output voltage goes from zero to its maximum value, the capacitance to be added on the $C_{dv/dt}$ pin can be calculated using the following theoretical formula:

$$C_{dv/dt} = 3.92 \times 10^{-8} \Delta t - 35.3 \times 10^{-12} \quad (2)$$

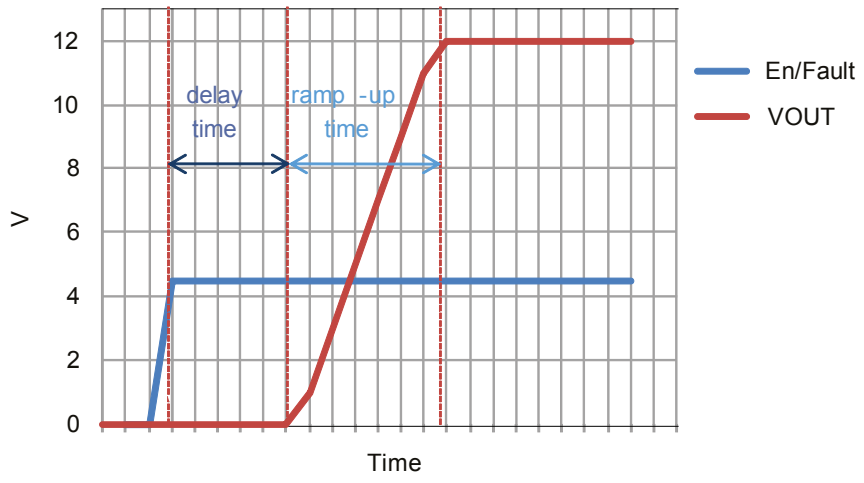
Where $C_{dv/dt}$ is expressed in Farads and the time in seconds.

The addition of an external $C_{dv/dt}$ influences also the initial delay time, defined as the time between the Enable signal going high and the start of the V_{OUT} slope (figure below).

The contribution of the external capacitor to this time interval can be estimated by using the following theoretical formula:

$$delay\ time\ [s] = 35 \times 10^{-5} + 71 \times 10^{5} \times C_{dv/dt}\ [F] \quad (3)$$

Figure 5. Delay time and V_{OUT} ramp-up time



5.4 Enable/Fault pin

The Enable/Fault pin has the dual function of controlling the output of the device and, at the same time, of providing information about the device status to the application.

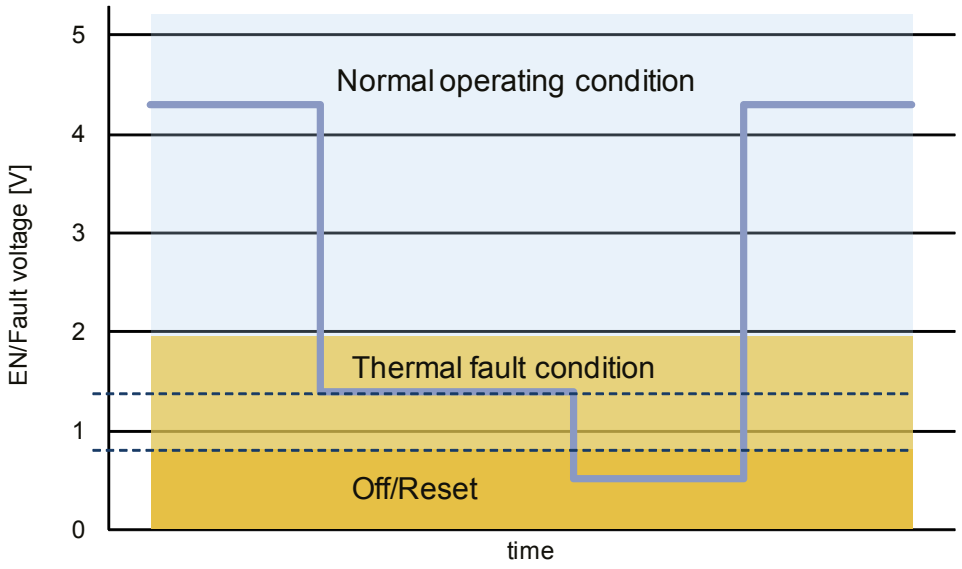
When it is used as a standard Enable pin, it should be connected to an external open-drain or open-collector device. In this case, when it is pulled at low logic level, it turns the output of the E-Fuse off.

If this pin is left floating, since it has internal pull-up circuitry, the output of the E-Fuse is kept ON, in normal operating conditions.

In case of thermal fault, the pin is pulled to an intermediate state (figure below). This signal can be provided to a monitor circuit, informing it that a thermal shutdown has occurred, or it can be directly connected to the Enable/Fault pins of other STEFxx devices on the same application in order to achieve a simultaneous enable/disable feature.

When a thermal fault occurs, the device can be reset either by cycling the supply voltage or by pulling down the Enable pin below the V_{il} threshold and then releasing it.

Figure 6. Enable/Fault pin status



6 Typical characteristics

The following plots are referred to the typical application circuit and, unless otherwise noted, at T_A = 25 °C.

Figure 7. Clamping voltage vs. temperature

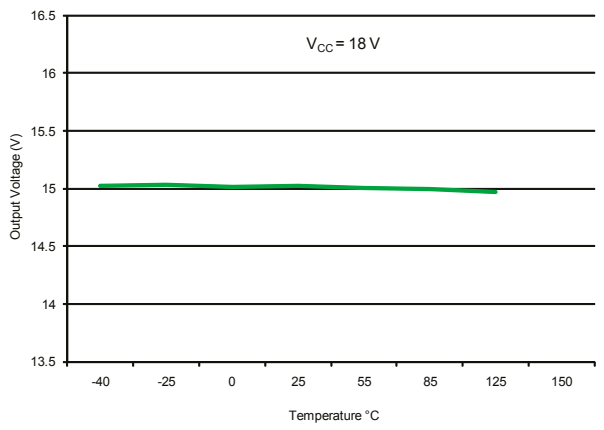


Figure 8. UVLO voltage vs. temperature

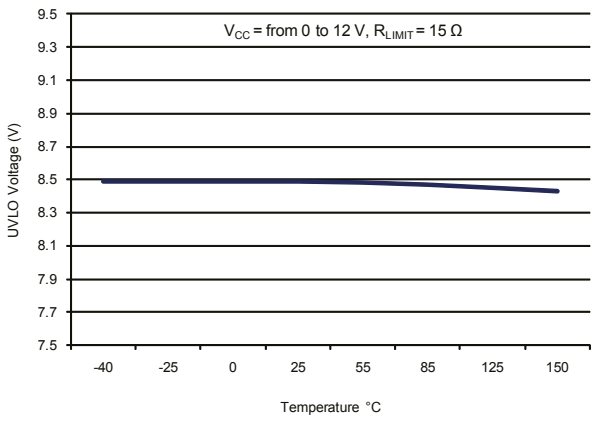


Figure 9. UVLO hysteresis vs. temperature

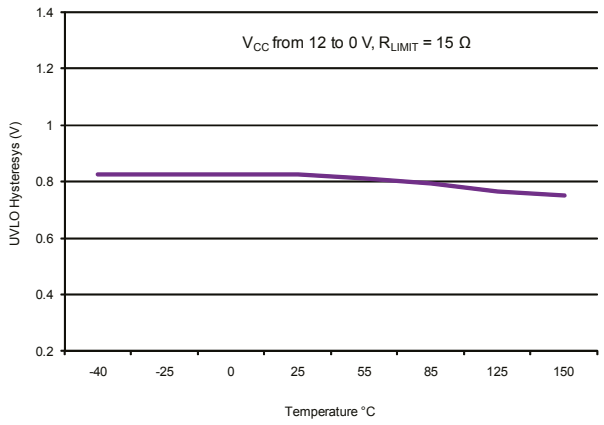


Figure 10. Off-state voltage vs. temperature

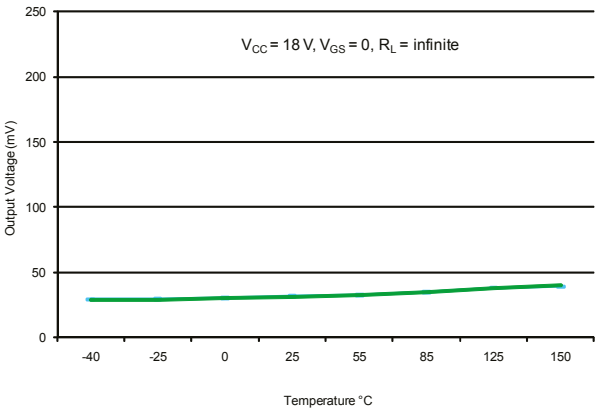


Figure 11. Bias current (device operational)

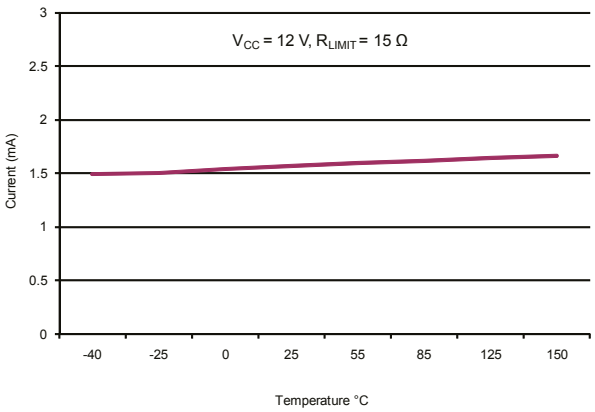


Figure 12. ON resistance vs. temperature

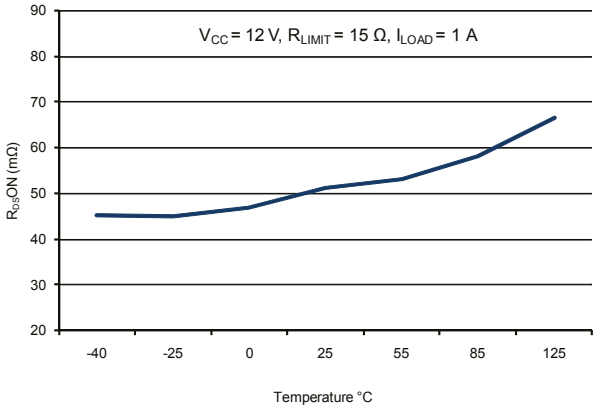


Figure 13. Current limit vs. R_{Limit}

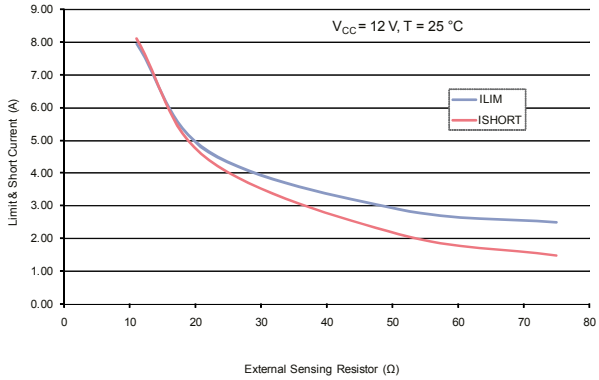


Figure 14. Thermal latch delay vs. power

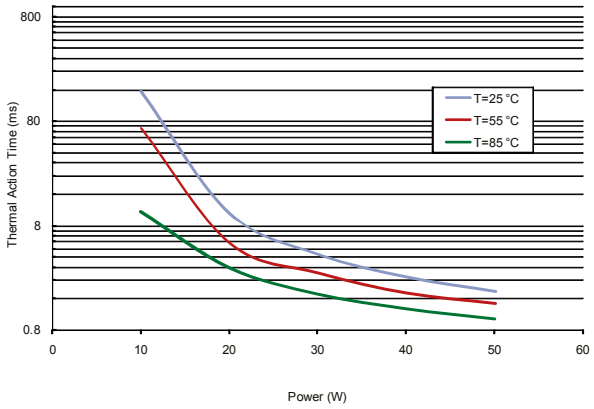
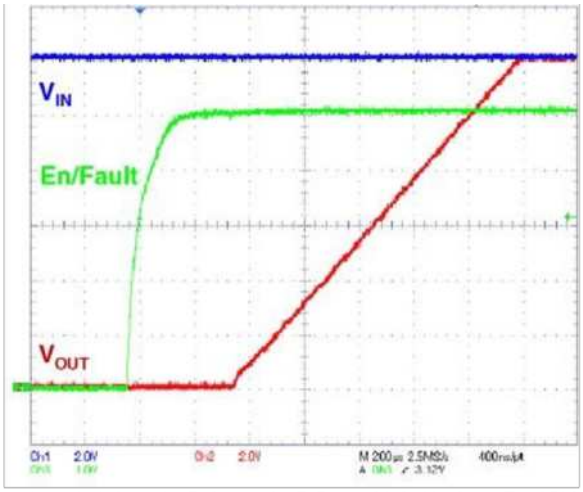
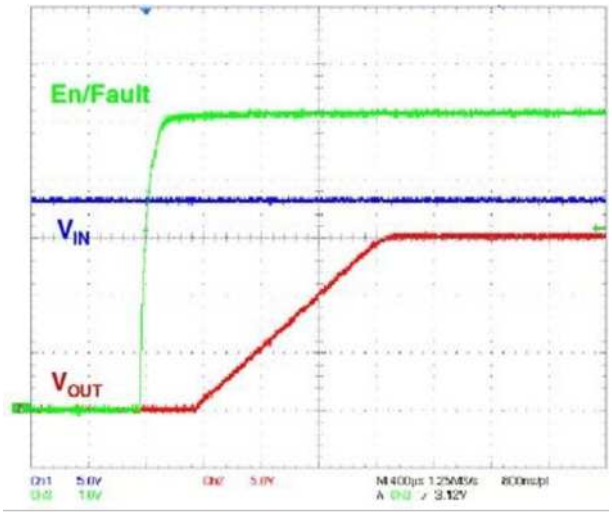


Figure 15. V_{OUT} ramp-up vs. enable



V_{CC}=12 V, C_{IN}=10 µF, C_{OUT}=10 µF, R_{LIMIT}=22 Ω, No $C_{dv/dt}$, T = 25°C

Figure 16. V_{OUT} clamping



V_{CC}=18 V, C_{IN}=10 µF, R_{LIMIT}=22 Ω, No $C_{dv/dt}$, T = 25°C

Figure 17. Line transient

V_{CC} = from 12 to 18 V, R_{LIMIT} = 22 Ω, I_{OUT} = 500 mA, T_{RISE} = 100 µs

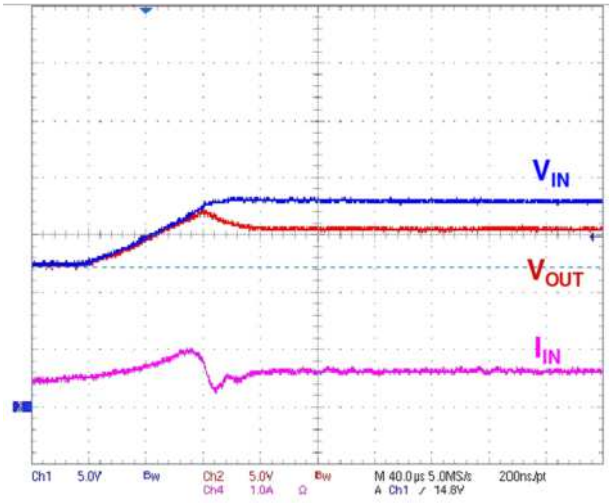


Figure 18. Startup into output short-circuit

V_{CC} = 12 V, R_{LIMIT} = 22 Ω , V_{OUT} = Connected to GND

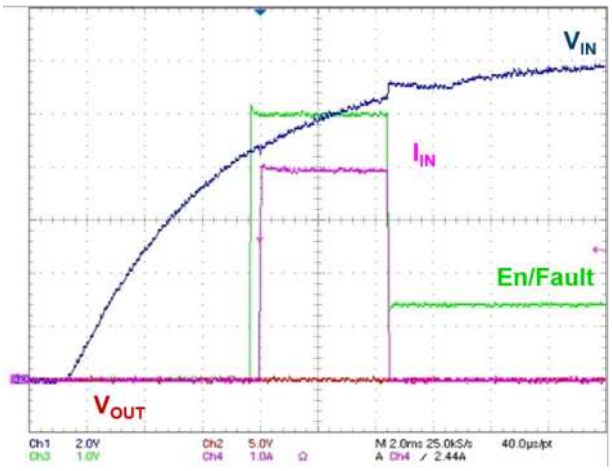


Figure 19. **Thermal latch from 2 A load to short-circuit**

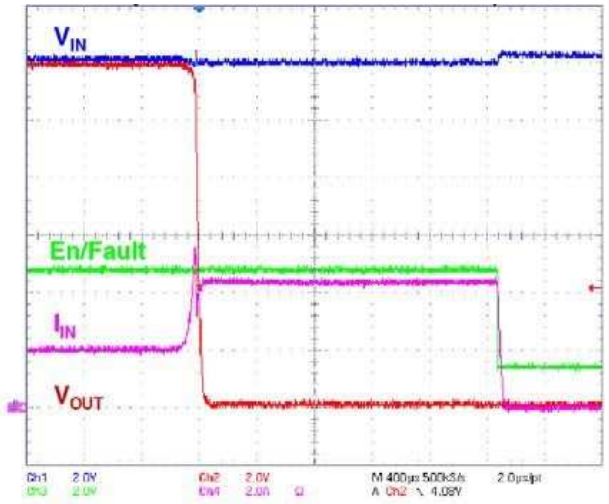
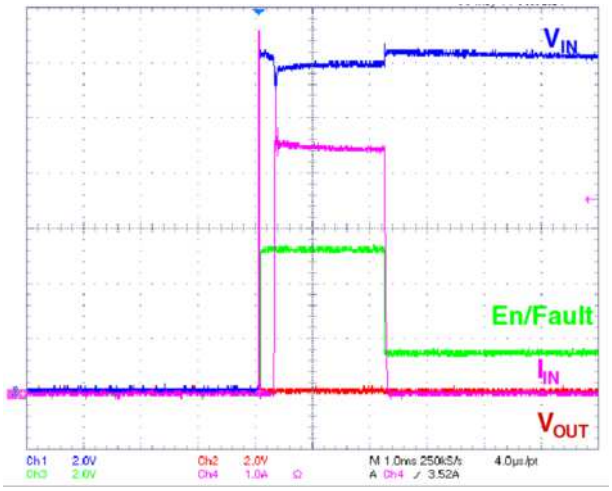


Figure 20. **Startup into output short-circuit (fast rise)**



VCC = 12 V, RLIMIT = 22 Ω, VOUT = Connected to GND

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 DFN10L (3x3 mm) package information

Figure 21. DFN10L (3x3 mm) package outline

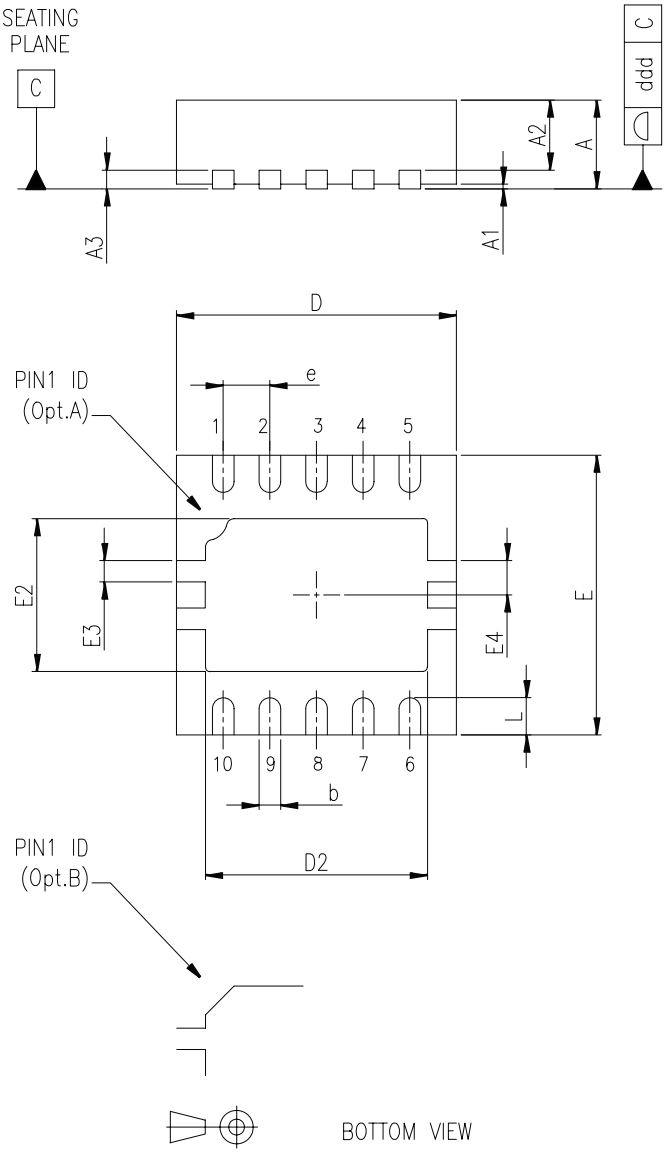
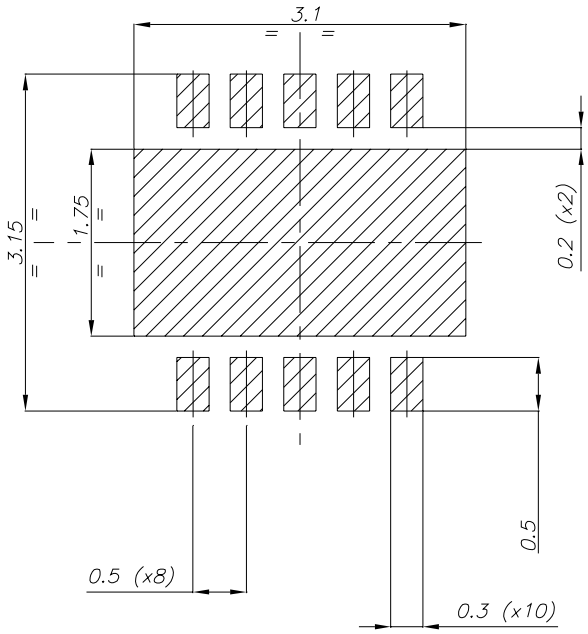


Table 6. **DFN10L (3x3 mm) mechanical data**

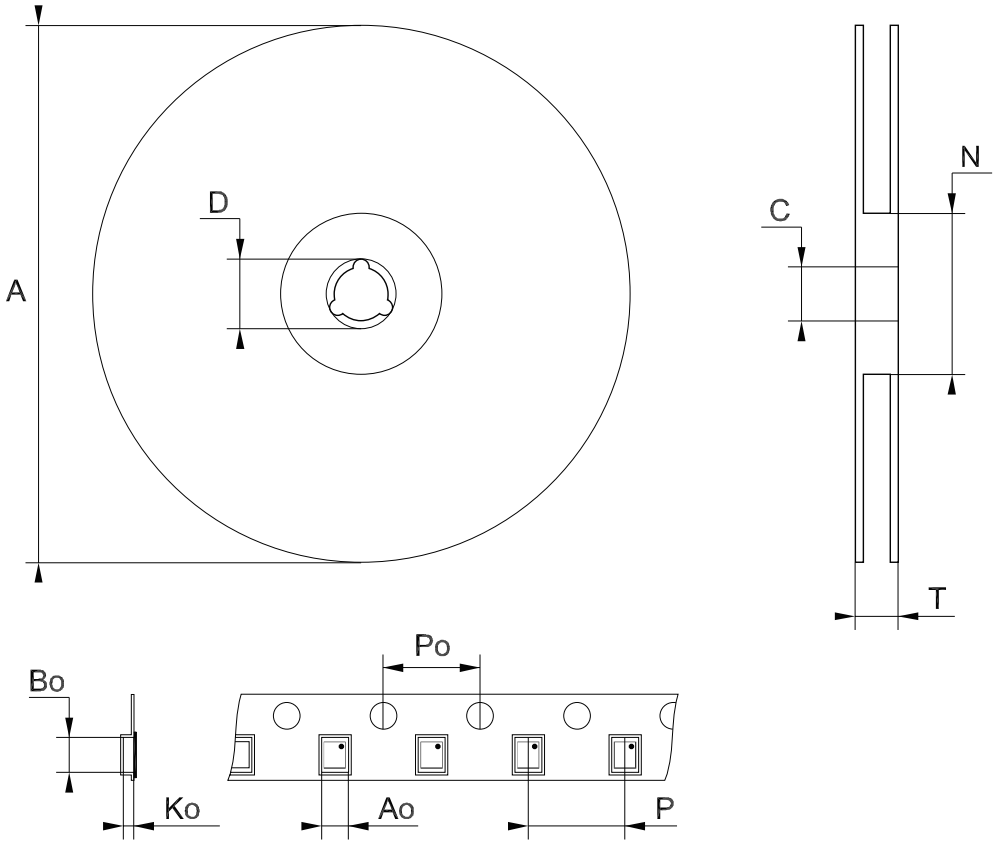
Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A2	0.55	0.65	0.80
A3		0.20	
b	0.18	0.25	0.30
D	2.85	3.00	3.15
D2	2.20		2.70
E	2.85	3.00	3.15
E2	1.40		1.75
E3	0.230		
E4	0.365		
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

Figure 22. **DFN10L (3x3 mm) recommended footprint**



7.2 DFN10L (3x3 mm) packing information

Figure 23. **DFN10L (3x3) tape and reel outline**



Note: Drawing not in scale

Table 7. **DFN10L (3x3) tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			18.4
Ao		3.3	
Bo		3.3	
Ko		1.1	
Po		4	
P		8	

8 Ordering information

Table 8. **Order codes**

Order code	Package	Packaging
STEF12PUR	DFN10 (3x3 mm)	Tape and reel

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
15-Jul-2011	1	Initial release.
08-Aug-2011	2	Modified definition for T_{op} in Table 3: Absolute maximum ratings.
14-Dec-2011	3	Removed $V_{dv/dt}$ and $I_{dv/dt}$ rows from dv/dt circuit Table 6 on page 6.
06-Mar-2012	4	Updated: package mechanical data Table 7 on page 17, Figure 21 on page 16 and Figure 24 on page 19.
14-Jan-2013	5	Updated: package mechanical data Table 7 on page 17 and Figure 21 on page 16.
03-Aug-2015	6	Updated Equation 2, Equation 3 and Section 7: Package information. Minor text changes.
07-Feb-2020	7	Updated Figure 17 and Figure 18.
27-Jun-2022	8	Added Features on the cover page.

Contents

1 **Device block diagram** 2
2 **Pin configuration** 3
3 **Maximum ratings** 4
4 **Electrical characteristics** 5
5 **Typical application** 6
5.1 Operating modes 6
5.1.1 Turn-on 6
5.1.2 Normal operating condition 6
5.1.3 Output voltage clamp 6
5.1.4 Current limiting 7
5.1.5 Thermal shutdown 7
5.2 R limit calculation 7
5.3 $C_{dv/dt}$ calculation 7
5.4 Enable/Fault pin 8
6 **Typical characteristics** 9
7 **Package information** 13
7.1 DFN10L (3x3 mm) package information 13
7.2 DFN10L (3x3 mm) packing information 15
8 **Ordering information** 16
Revision history 17

List of tables

Table 1. Pin description . . . 3
Table 2. Absolute maximum ratings . . . 4
Table 3. Thermal data . . . 4
Table 4. ESD performance . . . 4
Table 5. Electrical characteristics V_{CC} = 12 V, V_{EN} = 3.3 V, C_I = 10 µF, C_O = 47 µF, T_J = 25 °C (unless otherwise specified). 5
Table 6. DFN10L (3x3 mm) mechanical data . . . 14
Table 7. DFN10L (3x3) tape and reel mechanical data . . . 15
Table 8. Order codes . . . 16
Table 9. Document revision history . . . 17

List of figures

Figure 1. Block diagram . . . 2
Figure 2. Pin connection (top view) . . . 3
Figure 3. Application circuit . . . 6
Figure 4. Typical HDD application circuit . . . 6
Figure 5. Delay time and V_{OUT} ramp-up time . . . 7
Figure 6. Enable/Fault pin status . . . 8
Figure 7. Clamping voltage vs. temperature . . . 9
Figure 8. UVLO voltage vs. temperature . . . 9
Figure 9. UVLO hysteresis vs. temperature . . . 9
Figure 10. Off-state voltage vs. temperature . . . 9
Figure 11. Bias current (device operational) . . . 10
Figure 12. ON resistance vs. temperature . . . 10
Figure 13. Current limit vs. R_{Limit} . . . 10
Figure 14. Thermal latch delay vs. power . . . 10
Figure 15. V_{OUT} ramp-up vs. enable . . . 11
Figure 16. V_{OUT} clamping . . . 11
Figure 17. Line transient . . . 11
Figure 18. Startup into output short-circuit . . . 11
Figure 19. Thermal latch from 2 A load to short-circuit . . . 12
Figure 20. Startup into output short-circuit (fast rise) . . . 12
Figure 21. DFN10L (3x3 mm) package outline . . . 13
Figure 22. DFN10L (3x3 mm) recommended footprint . . . 14
Figure 23. DFN10L (3x3) tape and reel outline . . . 15

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved