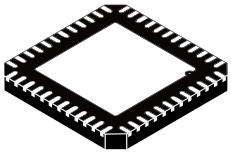
L6206Q

DMOS dual full bridge driver

Datasheet - production data



VFQFPN48
(7 x 7 mm)

Features

- Operating supply voltage from 8 to 52 V
- 5.6 A output peak current $R_{DS(on)}$ 0.3 Ω typ. value at T_j = 25 °C
- Operating frequency up to 100 kHz
- Programmable high side overcurrent detection and protection
- Diagnostic output
- Paralleled operation
- Cross conduction protection
- Thermal shutdown
- Undervoltage lockout
- Integrated fast free wheeling diodes

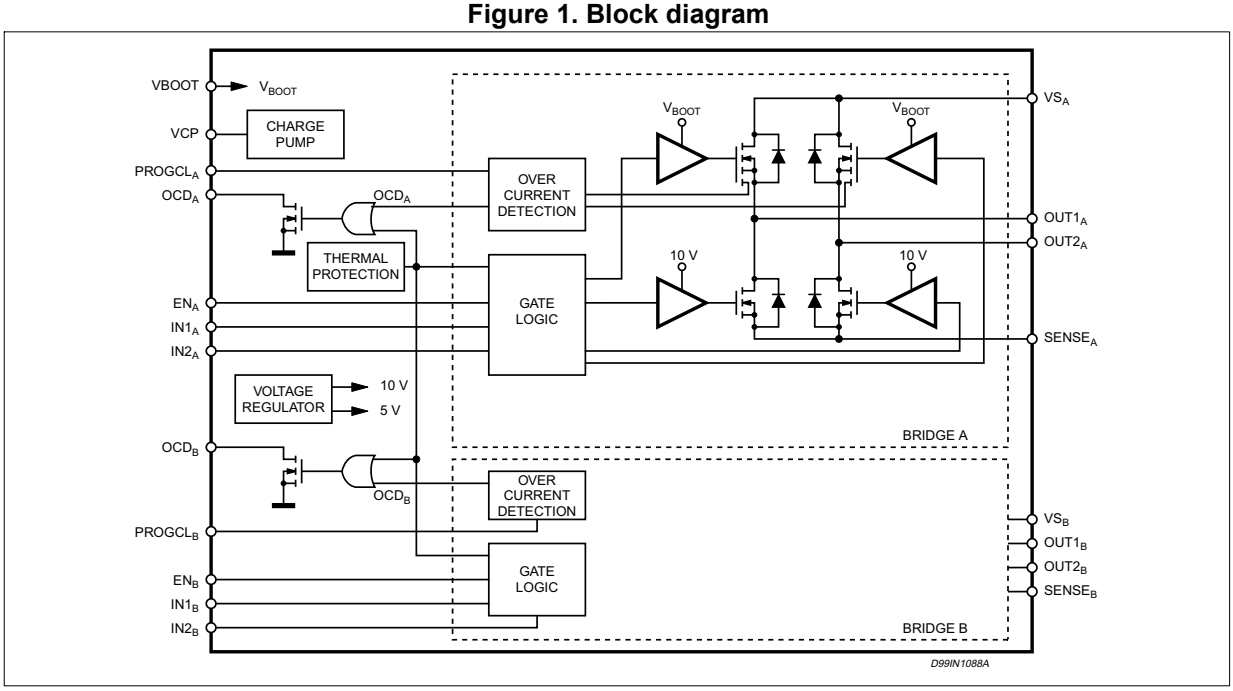
Application

- Bipolar stepper motor
- Dual or quad DC motor

Description

The L6206Q device is a DMOS dual full bridge driver designed for motor control applications, developed using BCDmultipower technology, which combines isolated DMOS power transistors with CMOS and bipolar circuits on the same chip. Available in a VFQFPN48 7 x 7 package, the L6206Q device features thermal shutdown and a non-dissipative overcurrent detection on the high side Power MOSFETs plus a diagnostic output that can be easily used to implement the overcurrent protection.

Figure 1. Block diagram



This is information on a product in full production. www.st.com

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1 Electrical data

1.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_S	Supply voltage	$V_{SA} = V_{SB} = V_S$	60	V
V_{OD}	Differential voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S$ = 60 V; $V_{SENSEA} = V_{SENSEB}$ = GND	60	V
V_{OCDA}, V_{OCDB}	OCD pins voltage range	-	-0.3 to +10	V
$V_{PROGCLA}$, $V_{PROGCLB}$	PROGCL pins voltage range	-	-0.3 to +7	V
V_{BOOT}	Bootstrap peak voltage	$V_{SA} = V_{SB} = V_S$	V_S + 10	V
V_{IN},V_{EN}	Input and enable voltage range	-	-0.3 to +7	V
V_{SENSEA}, V_{SENSEB}	Voltage range at pins $SENSE_A$ and $SENSE_B$	-	-1 to +4	V
$I_{S(peak)}$	Pulsed supply current (for each VS pin), internally limited by the overcurrent protection	$V_{SA} = V_{SB} = V_S$; t_{PULSE} < 1 ms	7.1	A
I_S	RMS supply current (for each VS pin)	$V_{SA} = V_{SB} = V_S$	2.5	A
T_{stg}, T_{OP}	Storage and operating temperature range	-	-40 to 150	°C

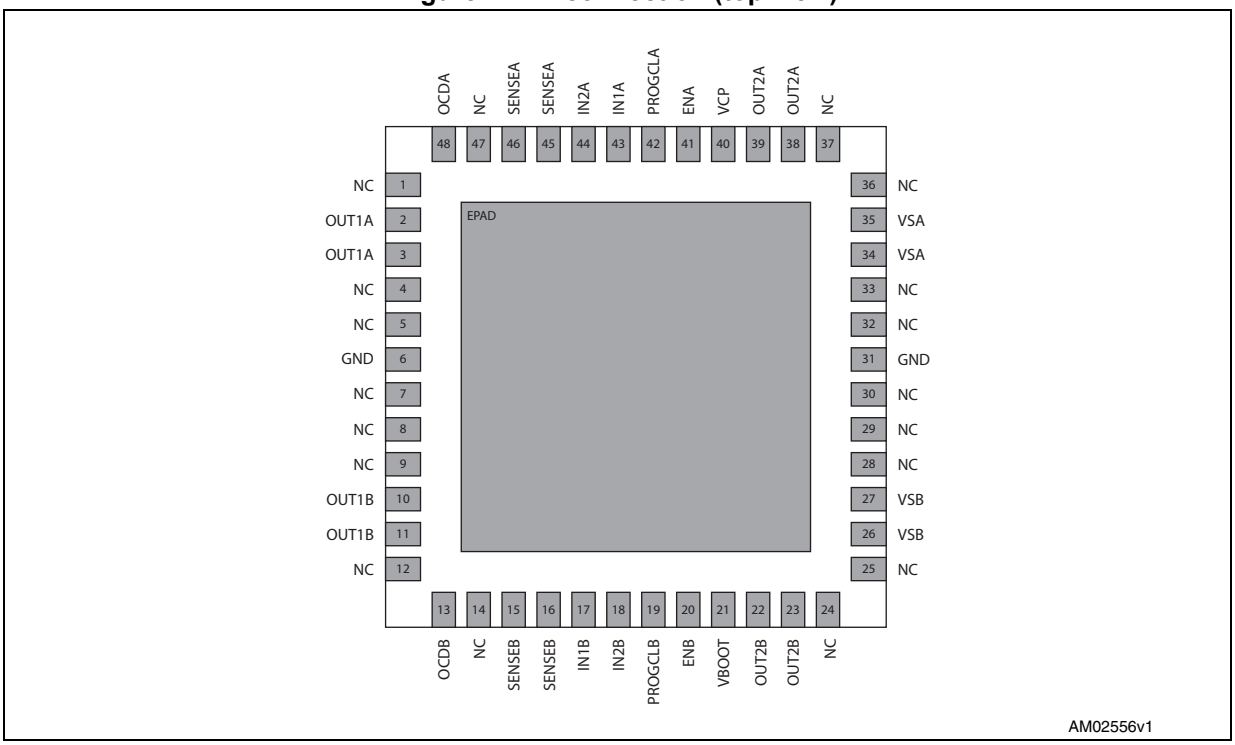
1.2 Recommended operating conditions

Table 2. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Max.	Unit
V_S	Supply voltage	$V_{SA} = V_{SB} = V_S$	8	52	V
V_{OD}	Differential voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S$; $V_{SENSEA} = V_{SENSEB}$		52	V
V_{SENSEA}, V_{SENSEB}	Voltage range at pins $SENSE_A$ and $SENSE_B$	Pulsed $t_W < t_{rr}$	-6	6	V
		DC	-1	1	V
I_{OUT}	RMS output current	-		2.5	A
T_j	Operating junction temperature	-	-25	+125	°C
f_{sw}	Switching frequency	-		100	kHz

2 Pin connection

Figure 2. Pin connection (top view)



1. The exposed PAD must be connected to GND pin.

Table 3. Pin description

Pin	Name	Type	Function
43	IN1A	Logic input	Bridge A logic input 1.
44	IN2A	Logic input	Bridge A logic input 2.
45, 46	SENSEA	Power supply	Bridge A source pin. This pin must be connected to power ground directly or through a sensing power resistor.
48	OCDA	Open-drain output	Bridge A overcurrent detection and thermal protection pin. An internal open-drain transistor pulls to GND when overcurrent on bridge A is detected or in case of thermal protection.
2, 3	OUT1A	Power output	Bridge A output 1.
6, 31	GND	GND	Signal ground terminals. These pins are also used for heat dissipation toward the PCB.
10, 11	OUT1B	Power output	Bridge B output 1.
13	OCDB	Open-drain output	Bridge B overcurrent detection and thermal protection pin. An internal open-drain transistor pulls to GND when overcurrent on bridge B is detected or in case of thermal protection.
15, 16	SENSEB	Power supply	Bridge B source pin. This pin must be connected to power ground directly or through a sensing power resistor.
17	IN1B	Logic input	Bridge B input 1

Table 3. Pin description (continued)

Pin	Name	Type	Function
18	IN2B	Logic input	Bridge B input 2
19	PROGCLB	R pin	Bridge B overcurrent level programming. A resistor connected between this pin and ground sets the programmable current limiting value for bridge B. By connecting this pin to ground the maximum current is set. This pin cannot be left unconnected.
20	ENB	Logic input	Bridge B enable. LOW logic level switches OFF all Power MOSFETs of bridge B. If not used, it must be connected to +5 V.
21	VBOOT	Supply voltage	Bootstrap voltage needed for driving the upper Power MOSFETs of both bridge A and bridge B.
22, 23	OUT2B	Power output	Bridge B output 2.
26, 27	VSB	Power supply	Bridge B power supply voltage. It must be connected to the supply voltage together with pin VSA.
34, 35	VSA	Power supply	Bridge A power supply voltage. It must be connected to the supply voltage together with pin VSB.
38, 39	OUT2A	Power output	Bridge A output 2.
40	VCP	Output	Charge pump oscillator output.
41	ENA	Logic input	Bridge A enable. LOW logic level switches OFF all Power MOSFETs of bridge A. If not used, it must be connected to +5 V.
42	PROGCLA	R pin	Bridge A overcurrent level programming. A resistor connected between this pin and ground sets the programmable current limiting value for bridge A. By connecting this pin to ground, the maximum current is set. This pin cannot be left unconnected.

3 Electrical characteristics

V_S = 48 V, T_A = 25 °C, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{Sth(ON)}$	Turn-on threshold	-	6.6	7	7.4	V
$V_{Sth(OFF)}$	Turn-off threshold	-	5.6	6	6.4	V
I_S	Quiescent supply current	All bridges OFF; T_j = -25 °C to 125 °C(1)	-	5	10	mA
$T_{j(OFF)}$	Thermal shutdown temperature	-	-	165	-	°C
Output DMOS transistors						
$R_{DS(ON)}$	High-side switch ON resistance	T_j = 25 °C	-	0.34	0.4	Ω
		T_j = 125 °C(1)	-	0.53	0.59	
	Low-side switch ON resistance	T_j = 25 °C	-	0.28	0.34	
		T_j = 125 °C(1)	-	0.47	0.53	
I_{DSS}	Leakage current	EN = low; OUT = V_S	-	-	2	mA
		EN = low; OUT = GND	-0.15	-	-	mA
Source drain diodes						
V_{SD}	Forward ON voltage	I_{SD} = 2.5 A, EN = LOW	-	1.15	1.3	V
t_{rr}	Reverse recovery time	I_f = 2.5 A	-	300	-	ns
t_{fr}	Forward recovery time	-	-	200	-	ns
Logic input						
V_{IL}	Low level logic input voltage	-	-0.3	-	0.8	V
V_{IH}	High level logic input voltage	-	2	-	7	V
I_{IL}	Low level logic input current	GND logic input voltage	-10	-	-	µA
I_{IH}	High level logic input current	7 V logic input voltage	-	-	10	µA
$V_{th(ON)}$	Turn-on input threshold	-	-	1.8	2	V
$V_{th(OFF)}$	Turn-off input threshold	-	0.8	1.3	-	V
$V_{th(HYS)}$	Input threshold hysteresis	-	0.25	0.5	-	V
Switching characteristics						
$t_{D(on)EN}$	Enable pin to out, turn ON delay time(2)	I_{LOAD} = 2.5 A, resistive load	100	250	400	ns
$t_{D(on)IN}$	Input pin to out, turn ON delay time	I_{LOAD} = 2.5 A, resistive load (deadtime included)	-	1.6	-	µs
t_{RISE}	Output rise time(2)	I_{LOAD} = 2.5 A, resistive load	40	-	250	ns
$t_{D(off)EN}$	Enable pin to out, turn OFF delay time(2)	I_{LOAD} = 2.5 A, resistive load	300	550	800	ns

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{D(off)IN}$	Input pin to out, turn OFF delay time	I_{LOAD} = 2.5 A, resistive load	-	600	-	ns
t_{FALL}	Output fall time(2)	I_{LOAD} = 2.5 A, resistive load	40	-	250	ns
t_{DT}	Deadtime protection	-	0.5	1	-	µs
f_{CP}	Charge pump frequency	-25 °C < T_j < 125 °C	-	0.6	1	MHz
Overcurrent detection						
$I_{s\ over}$	Input supply overcurrent detection threshold	-25 °C < T_j < 125 °C; R_{CL} = 39 kΩ -25 °C < T_j < 125 °C; R_{CL} = 5 kΩ -25 °C < T_j < 125 °C; R_{CL} = GND	-	0.57 4.42 5.6	-	A A A
R_{OPDR}	Open-drain ON resistance	I = 4 mA	-	40	60	Ω
$t_{OCD(ON)}$	OCD turn-on delay time(3)	I = 4 mA; C_{EN} < 100 pF	-	200	-	ns
$t_{OCD(OFF)}$	OCD turn-off delay time(3)	I = 4 mA; C_{EN} < 100 pF	-	100	-	ns

1. Tested at 25 °C in a restricted range and guaranteed by characterization.
2. See *Figure 3*.
3. See *Figure 4*.

Figure 3. Switching characteristic definition

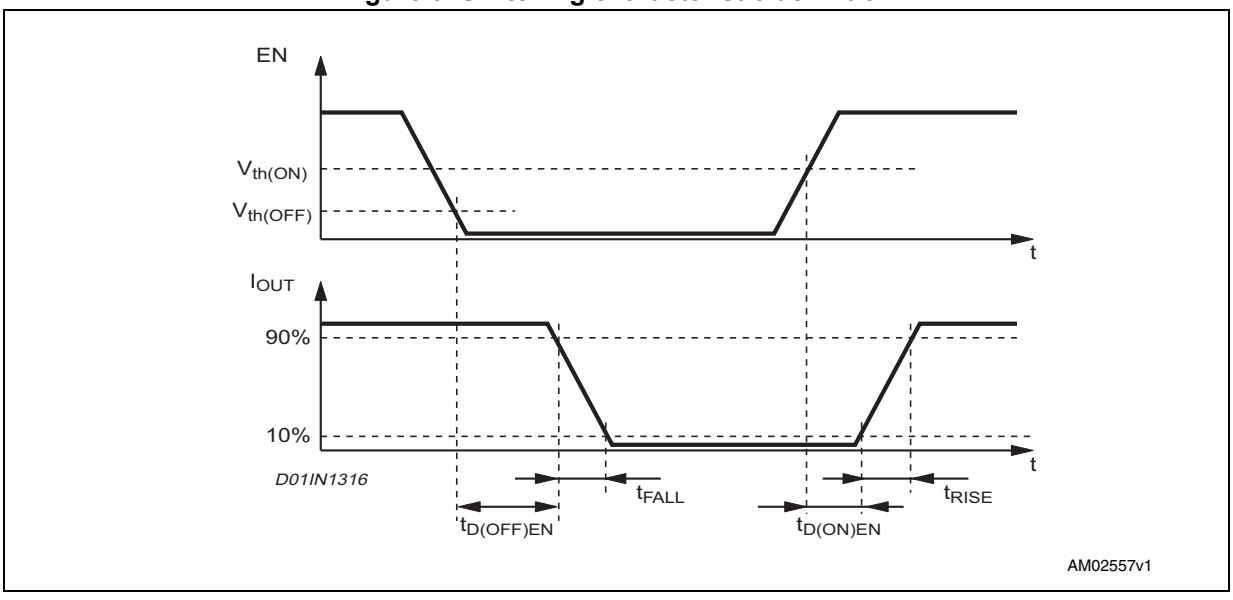
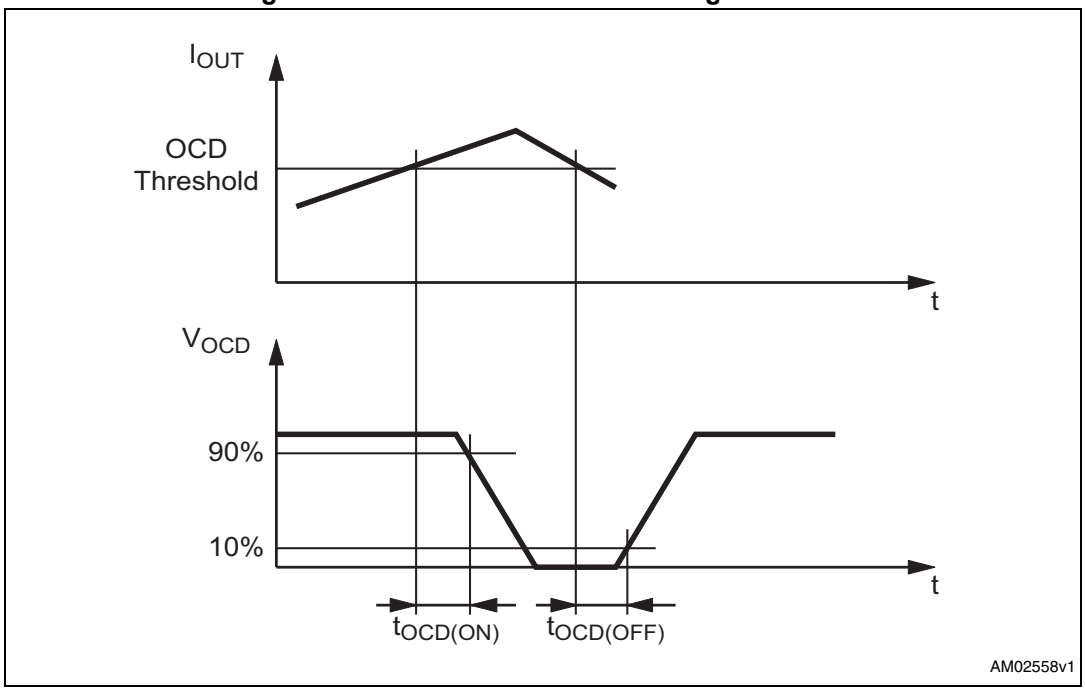


Figure 4. Overcurrent detection timing definition



4 Circuit description

4.1 Power stages and charge pump

The L6206Q device integrates two independent Power MOS full bridges. Each power MOS has an $R_{DS(ON)}$ = 0.3 Ω (typical value at 25 °C) with intrinsic fast freewheeling diode. Cross conduction protection is implemented by using a deadtime (t_{DT} = 1 µs typical value) set by an internal timing circuit between the turn-off and turn-on of two Power MOSFETs in one leg of a bridge.

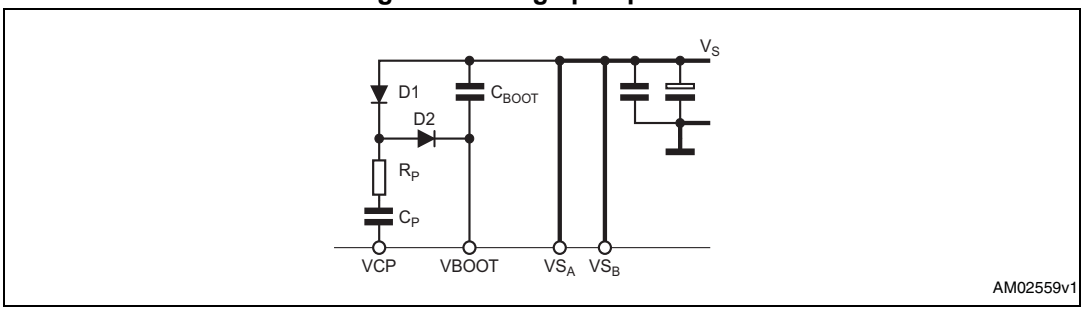
Pins VS_A and VS_B must be connected together to the supply voltage (V_S).

Using an N-channel Power MOSFET for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The bootstrapped supply (V_{BOOT}) is obtained through an internal oscillator and few external components to realize a charge pump circuit, as shown in *Figure 5*. The oscillator output (pin VCP) is a square wave at 600 kHz (typically) with 10 V amplitude. Recommended values/part numbers for the charge pump circuit are shown in *Table 5*.

Table 5. Charge pump external component values

Component	Value
C_{BOOT}	220 nF
C_P	10 nF
R_P	100 Ω
D1	1N4148
D2	1N4148

Figure 5. Charge pump circuit



4.2 Logic inputs

Pins $IN1_A$, $IN2_A$, $IN1_B$, $IN2_B$, EN_A, and EN_B are TTL/CMOS and µC compatible logic inputs. The internal structure is shown in *Figure 6*. The typical values for turn-on and turn-off thresholds are respectively $V_{th(ON)}$ = 1.8 V and $V_{th(OFF)}$ = 1.3 V.

Pins EN_A and EN_B are commonly used to implement overcurrent and thermal protection by connecting them respectively to the outputs OCD_A and OCD_B, which are open-drain outputs. If this type of connection is chosen, particular care needs to be taken in driving these pins. Two configurations are shown in *Figure 7* and *Figure 8*. If driven by an open-drain (collector) structure, a pull-up resistor R_{EN} and a capacitor C_{EN} are connected as

shown in *Figure 7*. If the driver is a standard push-pull structure the resistor R_{EN} and the capacitor C_{EN} are connected as shown in *Figure 8*. The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 kΩ. Recommended values for R_{EN} and C_{EN} are respectively 100 kΩ and 5.6 nF. More information on selecting the values can be found in *Section 4.3: Non-dissipative overcurrent detection and protection*.

Figure 6. Logic inputs internal structure

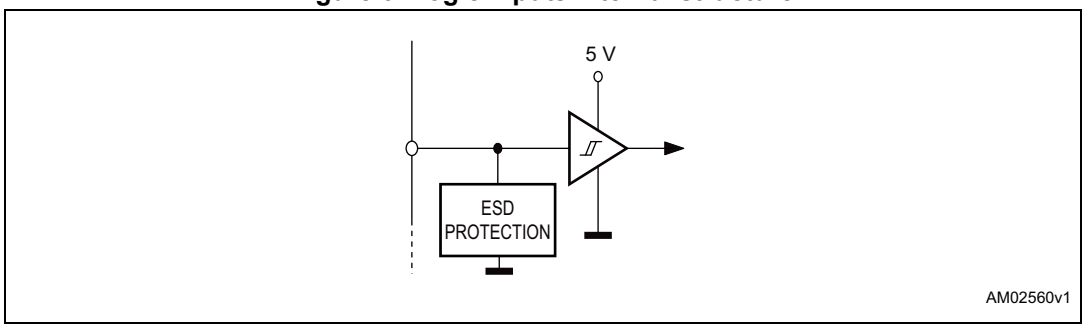


Figure 7. EN_A and EN_B pins open collector driving

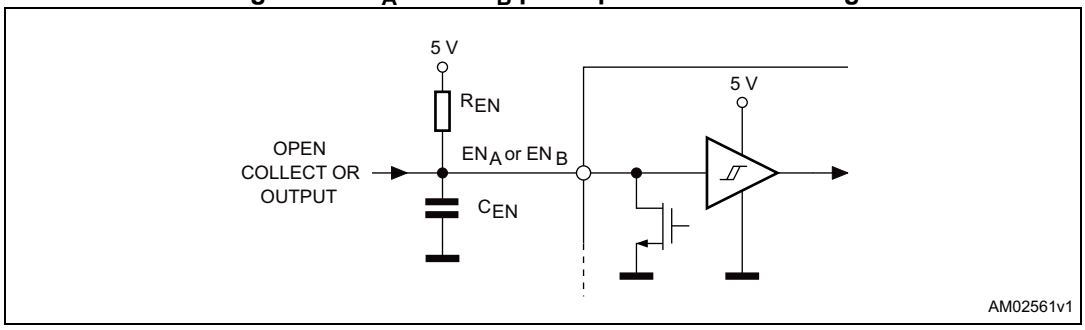


Figure 8. EN_A and EN_B pins push-pull driving

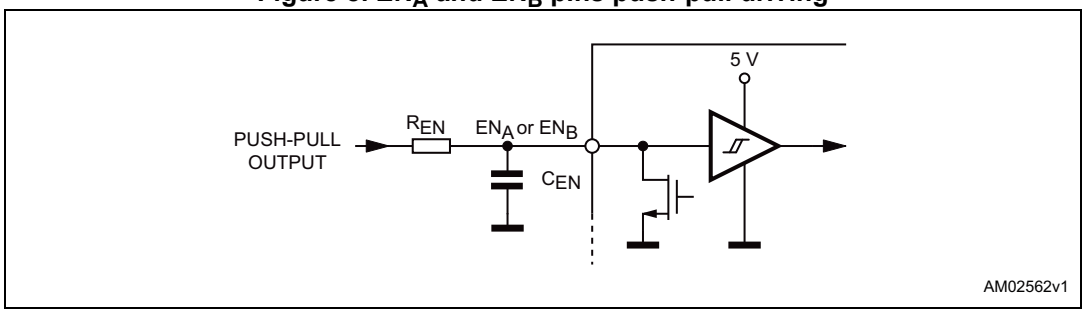


Table 6. Truth table

Inputs			Outputs	
EN	**IN1**	**IN2**	**OUT1**	**OUT2**
L	X(1)	X(1)	High Z(2)	High Z(2)
H	L	L	GND	GND
H	H	L	V_S	GND
H	L	H	GND	V_S
H	H	H	V_S	V_S

1. X = Do not care.
2. High Z = high impedance output.

4.3 Non-dissipative overcurrent detection and protection

The L6206Q device integrates an overcurrent detection circuit (OCD). With this internal overcurrent detection, the external current sense resistor normally used and its associated power dissipation are eliminated. *Figure 9* shows a simplified schematic of the overcurrent detection circuit for bridge A. Bridge B is provided with an analogous circuit.

To implement the overcurrent detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high side Power MOSFET. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current I_{REF}. When the output current reaches the detection threshold I_{sover}, the OCD comparator signals a fault condition. When a fault condition is detected, an internal open-drain MOSFET with a pull-down capability of 4 mA connected to the OCD pin is turned on. *Figure 10* shows the OCD operation.

This signal can be used to regulate the output current simply by connecting the OCD pin to the EN pin and adding an external R-C, as shown in *Figure 9*. The off-time before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs.

I_{REF} and, therefore, the output current detection threshold, are selectable by the R_{CL} value, following *Equation 1* and *Equation 2*:

Equation 1

I_{sover} = 5.6 A ± 30% at -25 °C < T_j < 125 °C if R_{CL} = 0 Ω (PROGCL connected to GND)

Equation 2

$$I_{sover} = \frac{22100}{R_{CL}} \pm 10\% \text{ at } -25\ °C < T_j < 125\ °C \text{ if } 5\ k\Omega < R_{CL} < 40\ k\Omega$$

Figure 11 shows the output current protection threshold versus R_{CL} value in the range 5 kΩ to 40 kΩ.

The disable time ($t_{DISABLE}$), before recovering normal operation, can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected either by C_{EN} or R_{EN} values and its magnitude is reported in *Figure 12*. The delay time (t_{DELAY}), before turning off the bridge when an overcurrent has been detected, depends only on the C_{EN} value. Its magnitude is reported in *Figure 13*.

C_{EN} is also used for providing immunity to pin EN against fast transient noises. Therefore the value of C_{EN} should be chosen as big as possible according to the maximum tolerable delay time and the R_{EN} value should be chosen according to the desired disable time.

The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 kΩ. Recommended values for R_{EN} and C_{EN} are respectively 100 kΩ and 5.6 nF which allow a 200 µs disable time to be obtained.

Figure 9. Overcurrent protection simplified schematic

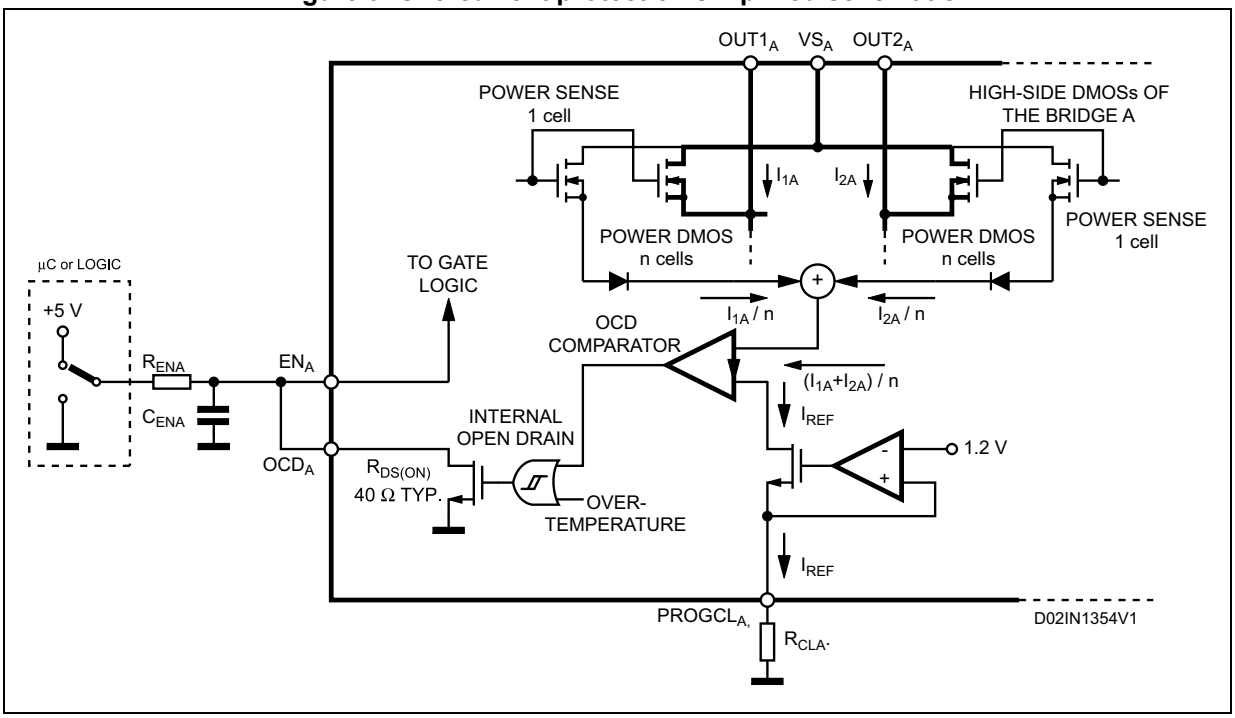


Figure 10. Overcurrent protection waveforms

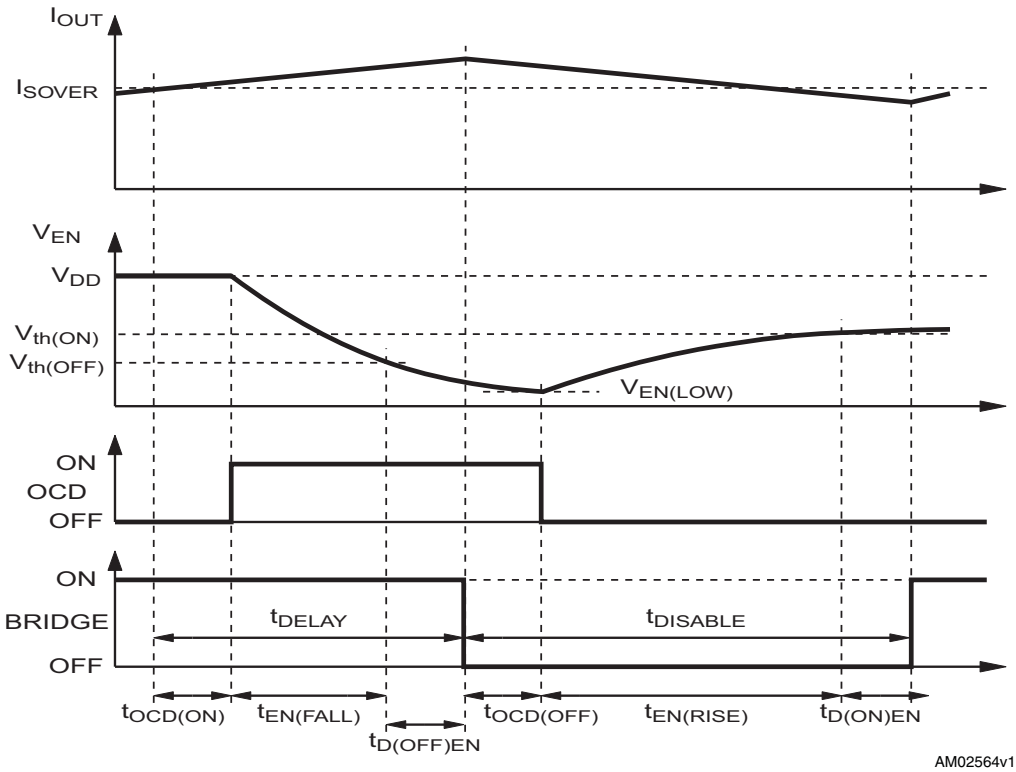


Figure 11. Output current protection threshold versus R_{CL} value

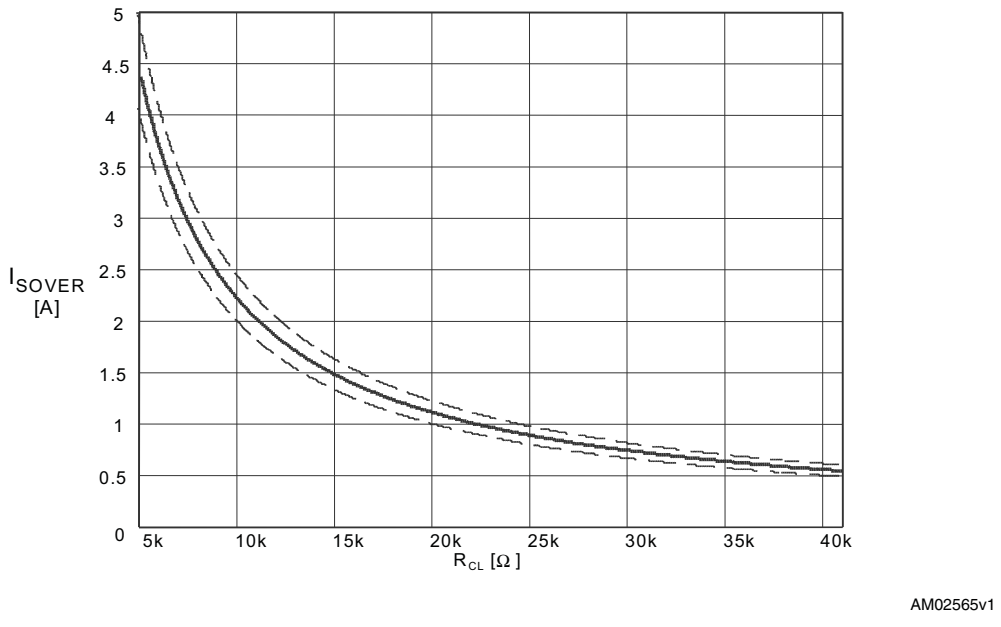


Figure 12. $t_{DISABLE}$ versus C_{EN} and R_{EN} (V_{DD} = 5 V)

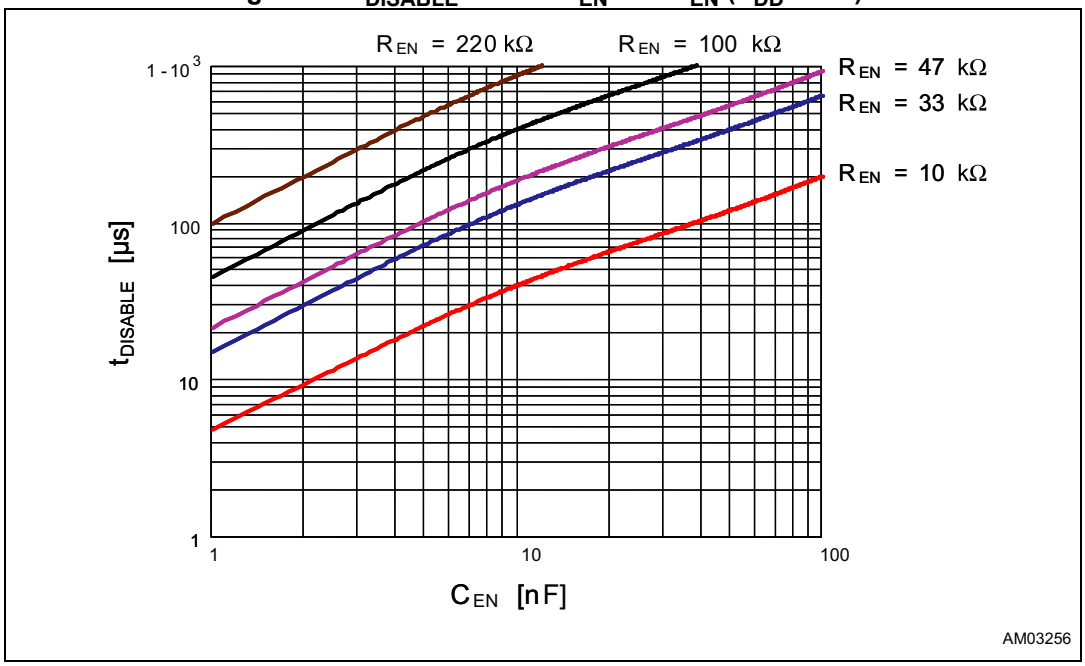
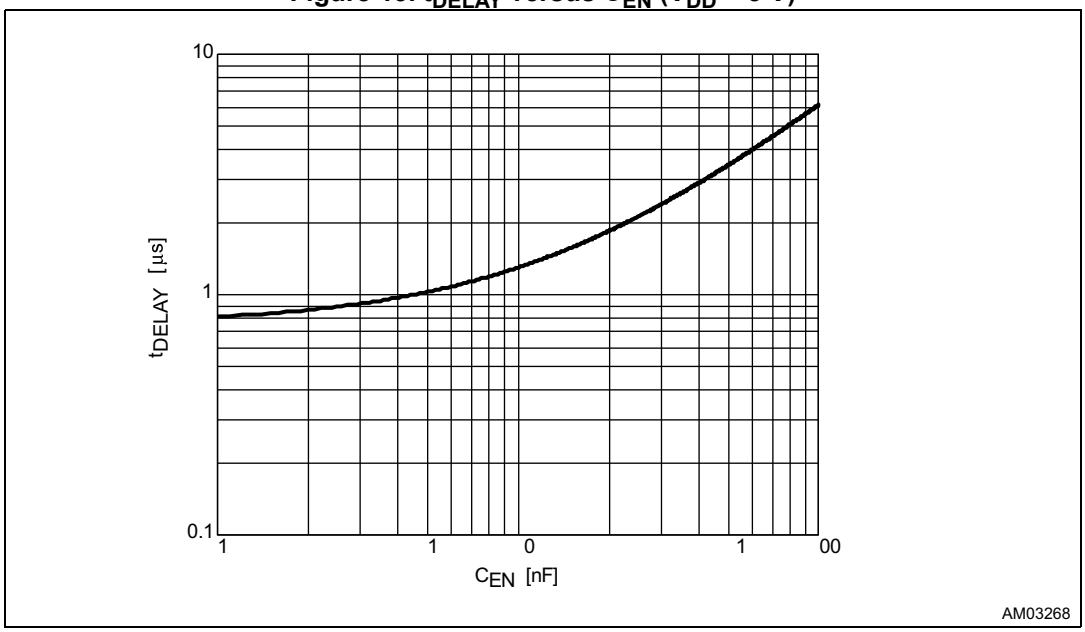


Figure 13. t_{DELAY} versus C_{EN} (V_{DD} = 5 V)



4.4 Thermal protection

In addition to overcurrent detection, the L6206Q device integrates a thermal protection for preventing device destruction in the case of junction overtemperature. It works by sensing the die temperature by means of a sensitive element integrated in the die. The device switches off when the junction temperature reaches 165 °C (typ. value) with 15 °C hysteresis (typ. value).

5 Application information

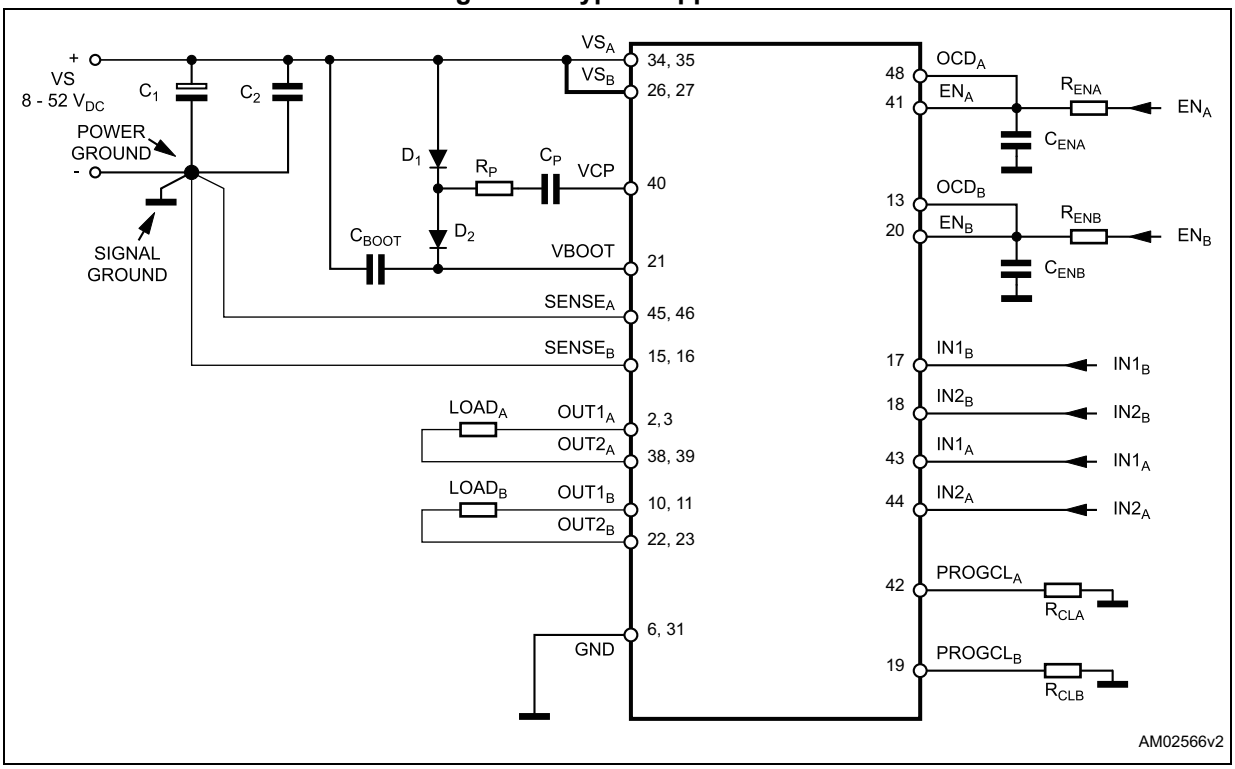
A typical application using the L6206Q device is shown in *Figure 14*. Typical component values for the application are shown in *Table 7*. A high quality ceramic capacitor in the range of 100 to 200 nF should be placed between the power pins (VS_A and VS_B) and ground near the L6206Q to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitors connected from the EN_A/OCD_A and EN_B/OCD_B nodes to ground set the shutdown time for bridge A and bridge B respectively when an overcurrent is detected (see *Section 4.3: Non-dissipative overcurrent detection and protection*). The two current sources ($SENSE_A$ and $SENSE_B$) should be connected to power ground with a trace length as short as possible in the layout. To increase noise immunity, unused logic pins are best connected to 5 V (high logic level) or GND (low logic level) (see *Table 3.*).

It is recommended to keep power ground and signal ground separated on the PCB.

Table 7. Component values for typical application

Component	Value
C_1	100 µF
C_2	100 nF
C_{BOOT}	220 nF
C_P	10 nF
C_{ENA}	5.6 nF
C_{ENB}	5.6 nF
D_1	1N4148
D_2	1N4148
R_{CLA}	5 kΩ
R_{CLB}	5 kΩ
R_{ENA}	100 kΩ
R_{ENB}	100 kΩ
R_P	100 Ω

Figure 14. Typical application



Note: To reduce the IC thermal resistance, and therefore improve the dissipation path, the NC pins can be connected to GND.

6 Paralleled operation

The outputs of the L6206Q device can be paralleled to increase the output current capability or reduce the power dissipation in the device at a given current level. It must be noted, however, that the internal wire bond connections from the die to the power or sense pins of the package must carry current in both of the associated half bridges.

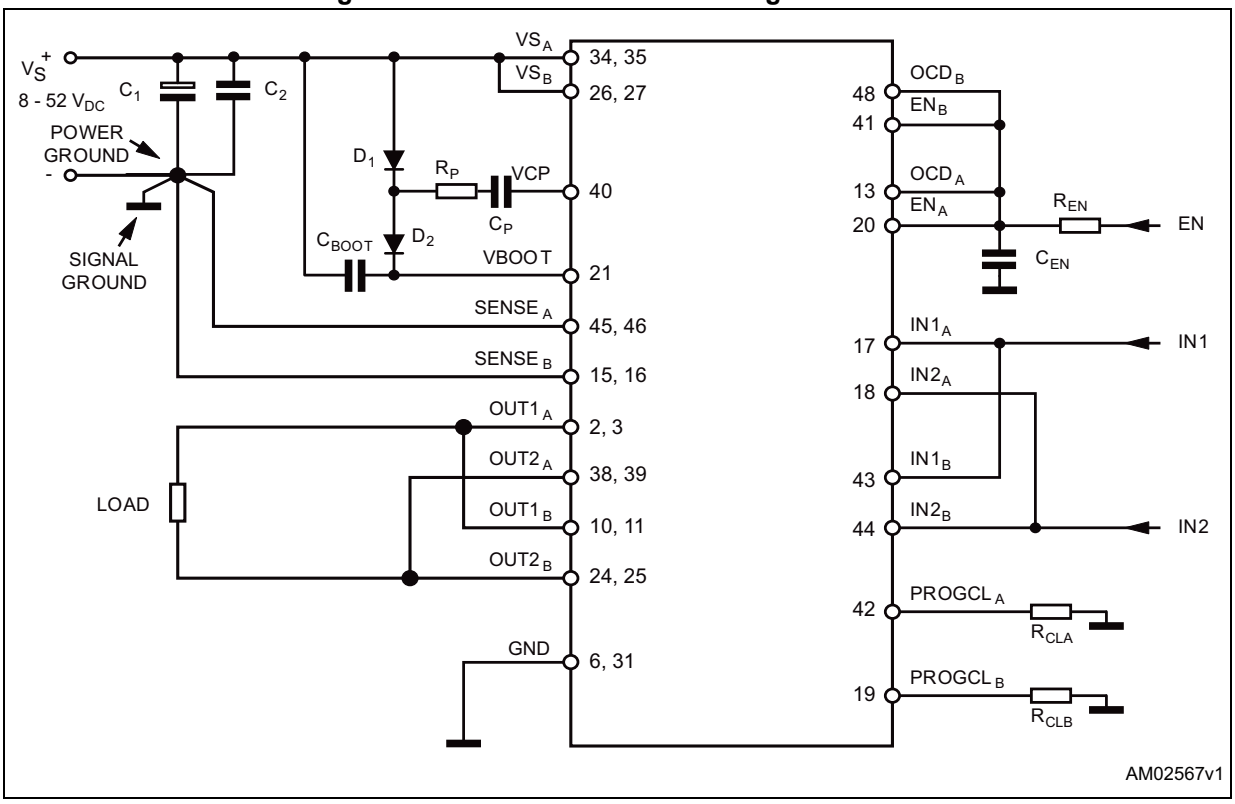
When the two halves of one full bridge (for example $OUT1_A$ and $OUT2_A$) are connected in parallel, the peak current rating is not increased as the total current must still flow through one bond wire on the power supply or sense pin. In addition, the overcurrent detection senses the sum of the current in the upper devices of each bridge (A or B) so connecting the two halves of one bridge in parallel does not increase the overcurrent detection threshold.

For most applications the recommended configuration is half bridge 1 of bridge A paralleled with the half bridge 1 of bridge B, and the same for the half bridges 2, as shown in *Figure 15*. The current in the two devices connected in parallel share well as the $R_{DS(ON)}$ of the devices on the same die is well matched. When connected in this configuration the overcurrent detection circuit, which senses the current in each bridge (A and B), senses the current in the upper devices connected in parallel independently and the sense circuit with the lowest threshold trips first. With the enable pins connected in parallel, the first detection of an overcurrent in either upper DMOS device turns off both bridges. Assuming that the two DMOS devices share the current equally, the resulting overcurrent detection threshold is twice the minimum threshold set by the resistors R_{CLA} or R_{CLB} in *Figure 15*. It is recommended to use $R_{CLA} = R_{CLB}$.

In this configuration the resulting bridge has the following characteristics.

- Equivalent device: full bridge
- $R_{DS(ON)}$ 0.15 Ω typ. value at T_j = 25 °C
- 5 A max. RMS load current
- 11.2 A max. OCD threshold

Figure 15. Parallel connection for higher current



To operate the device in parallel and maintain a lower overcurrent threshold, half bridge 1 and the half bridge 2 of bridge A can be connected in parallel and the same is done for bridge B, as shown in *Figure 16*. In this configuration, the peak current for each half bridge is still limited by the bond wires for the supply and sense pins so the dissipation in the device is reduced, but the peak current rating is not increased.

When connected in this configuration the overcurrent detection circuit, senses the sum of the current in upper devices connected in parallel. With the enable pins connected in parallel, an overcurrent turns off both bridges.

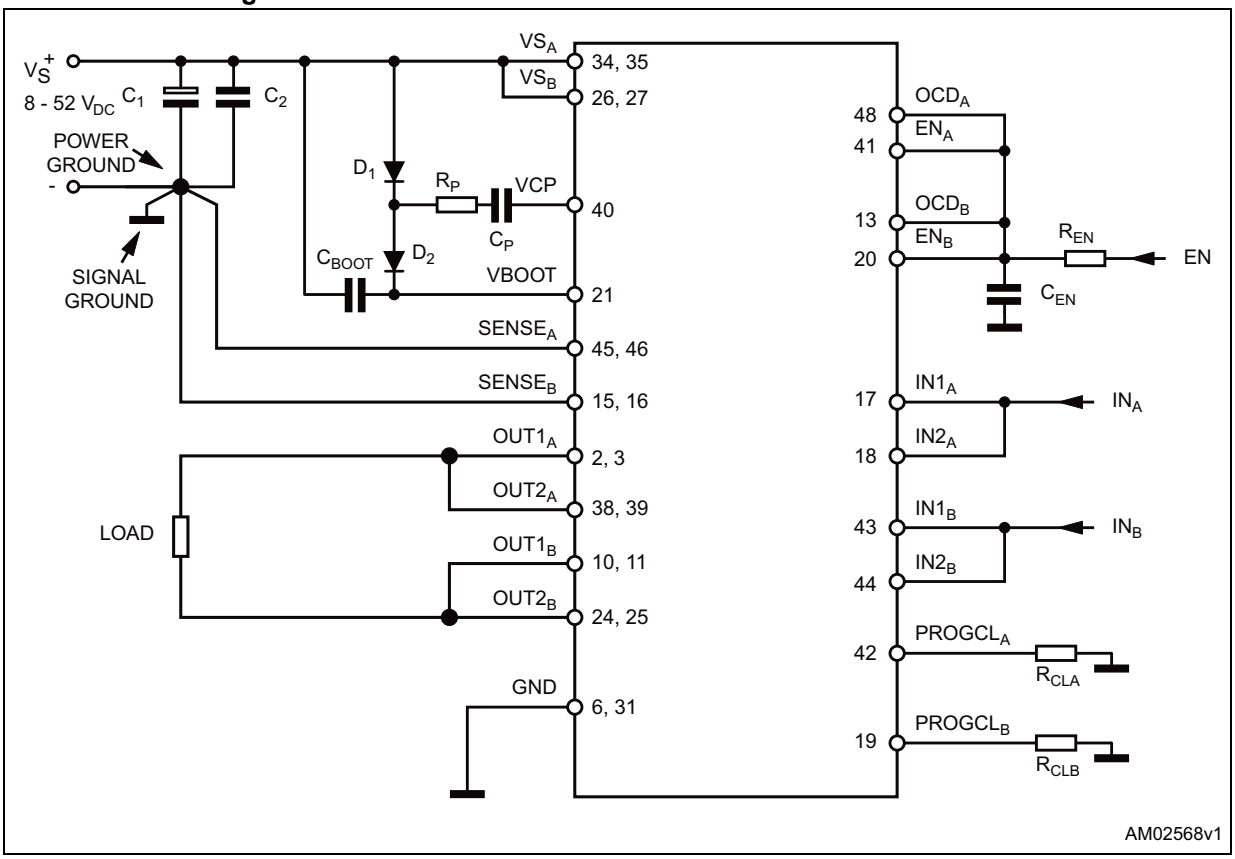
Since the circuit senses the total current in the upper devices, the overcurrent threshold is equal to the threshold set by the resistor R_{CLA} or R_{CLB} in *Figure 16*. R_{CLA} sets the threshold when outputs OUT1A and OUT2A are high and resistor R_{CLB} sets the threshold when outputs $OUT1_B$ and $OUT2_B$ are high.

It is recommended to use $R_{CLA} = R_{CLB}$.

In this configuration, the resulting bridge has the following characteristics.

- Equivalent device: full bridge
- $R_{DS(ON)}$ 0.15 Ω typ. value at T_j = 25 °C
- 2.5 A max. RMS load current
- 5.6 A max. OCD threshold

Figure 16. Parallel connection with lower overcurrent threshold

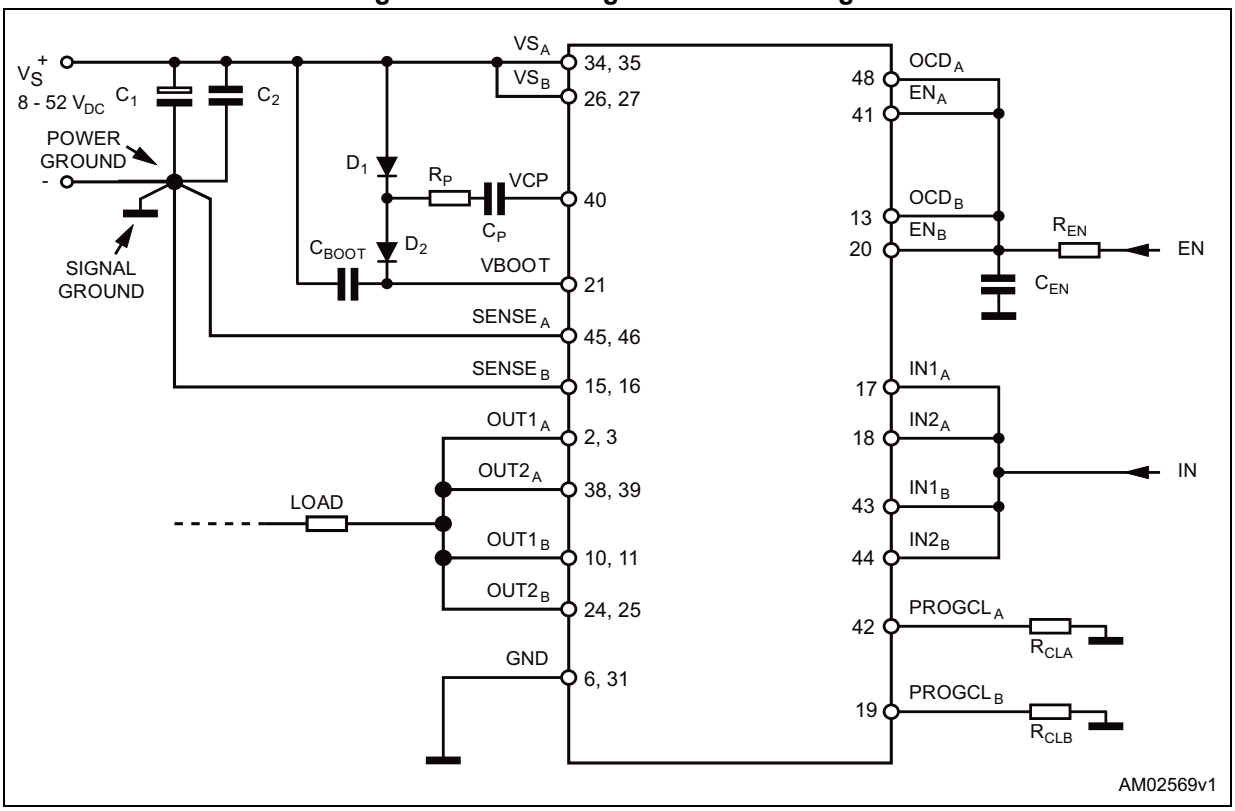


It is also possible to parallel the four half bridges to obtain a simple half bridge as shown in *Figure 17*. In this configuration the overcurrent threshold is equal to twice the minimum threshold set by the resistors R_{CLA} or R_{CLB} in *Figure 17*. It is recommended to use $R_{CLA} = R_{CLB}$.

The resulting half bridge has the following characteristics.

- Equivalent device: half bridge
- $R_{DS(ON)}$ 0.075 Ω typ. value at T_j = 25 °C
- 5 A max. RMS load current
- 11.2 A max. OCD threshold

Figure 17. Paralleling the four half bridges



7 Output current capability and IC power dissipation

Figure 18 and *Figure 19* show the approximate relation between the output current and the IC power dissipation using PWM current control driving two loads, for two different driving types:

- One full bridge ON at a time (*Figure 18*) in which only one load at a time is energized.
- Two full bridges ON at the same time (*Figure 19*) in which two loads at the same time are energized.

For a given output current and driving type the power dissipated by the IC can be easily evaluated, in order to establish which package should be used and how large the onboard copper dissipating area must be in order to guarantee a safe operating junction temperature (125 °C maximum).

Figure 18. IC power dissipation vs. output current with one full bridge on at a time

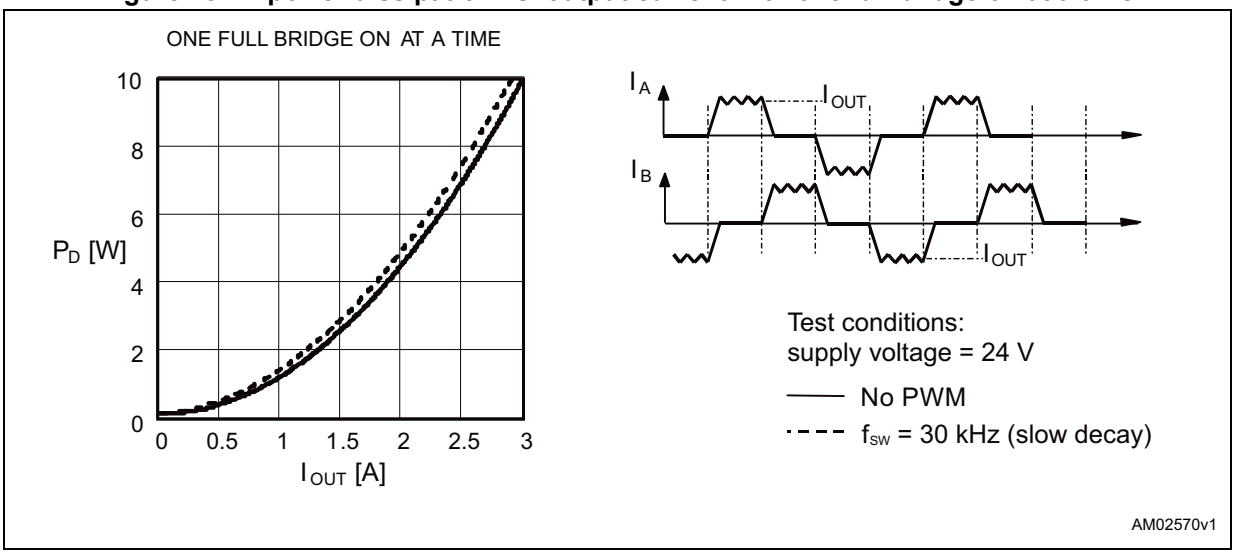
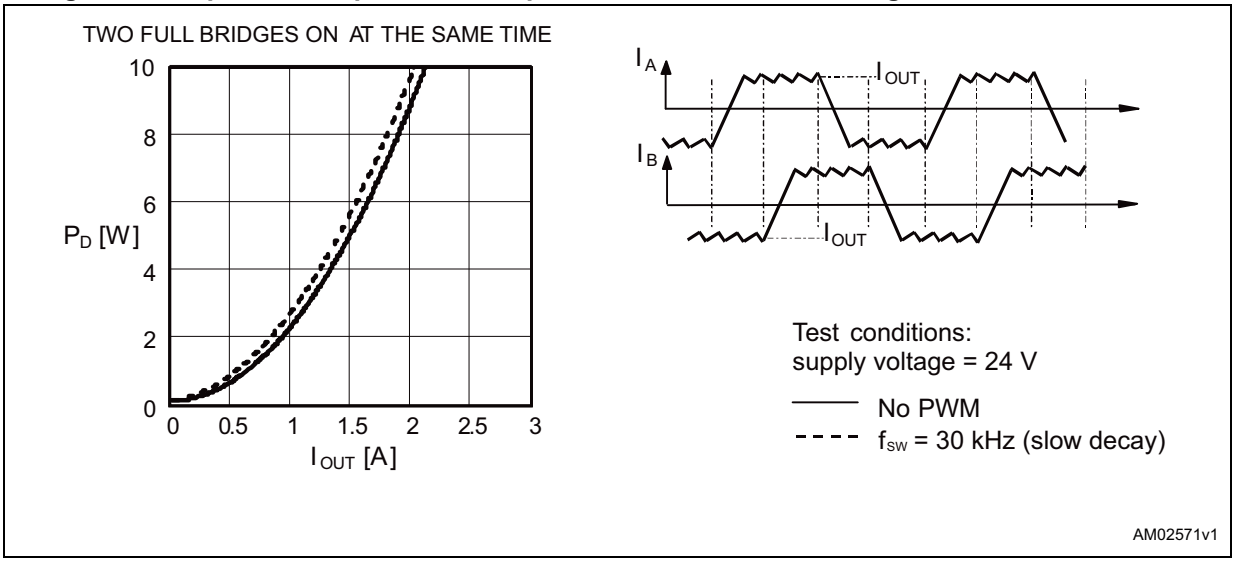


Figure 19. IC power dissipation vs. output current with two full bridges ON at the same time



8 Thermal management

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Therefore, it must be taken into account very carefully. Besides the available space on the PCB, the right package should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness.

Table 8. Thermal data

Symbol	Parameter	Package	Typ.	Unit
R_{thJA}	Thermal resistance junction-ambient	VFQFPN48(1)	17	°C/W

1. VFQFPN48 mounted on EVAL6208Q rev. 1.1 board (see EVAL6208Q databrief): four-layer FR4 PCB with a dissipating copper surface of about 45 cm^2 on each layer and 25 via holes below the IC.

9 Electrical characteristics curves

Figure 20. Typical quiescent current vs. supply voltage

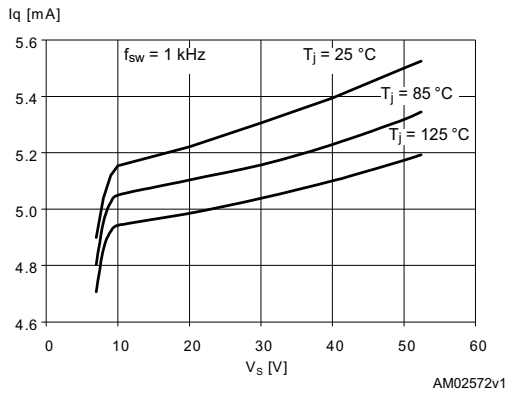


Figure 21. Typical high-side $R_{DS(on)}$ vs. supply voltage

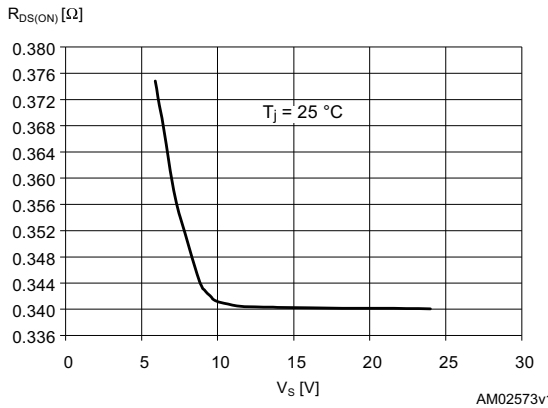


Figure 22. Normalized typical quiescent current vs. switching frequency

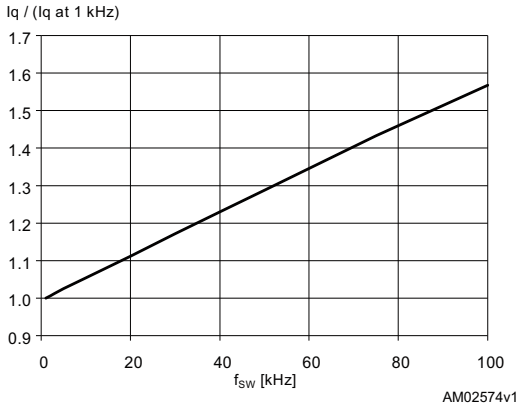


Figure 23. Normalized $R_{DS(on)}$ vs. junction temperature (typical value)

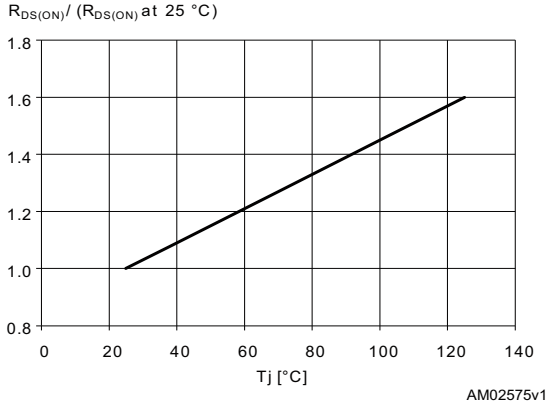


Figure 24. Typical low-side $R_{DS(on)}$ vs. supply voltage

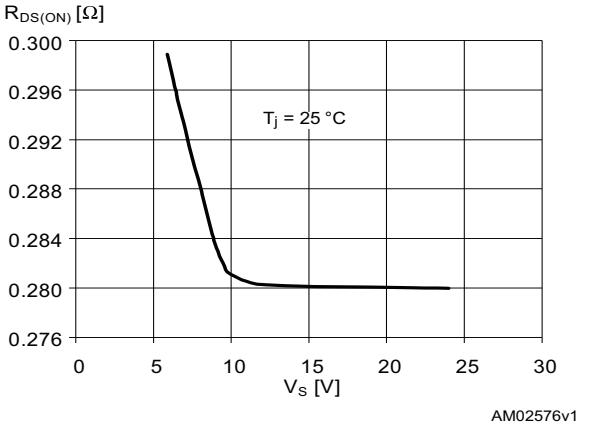
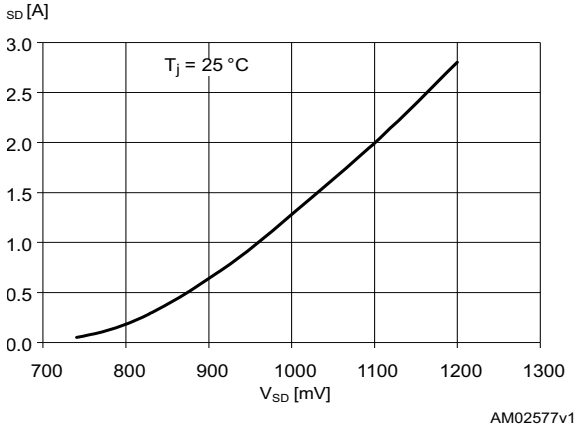


Figure 25. Typical drain-source diode forward ON characteristic



10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 VFQFPN48 (7 x 7 x 1.0 mm) package information

Figure 26. VFQFPN48 (7 x 7 x 1.0 mm) package outline

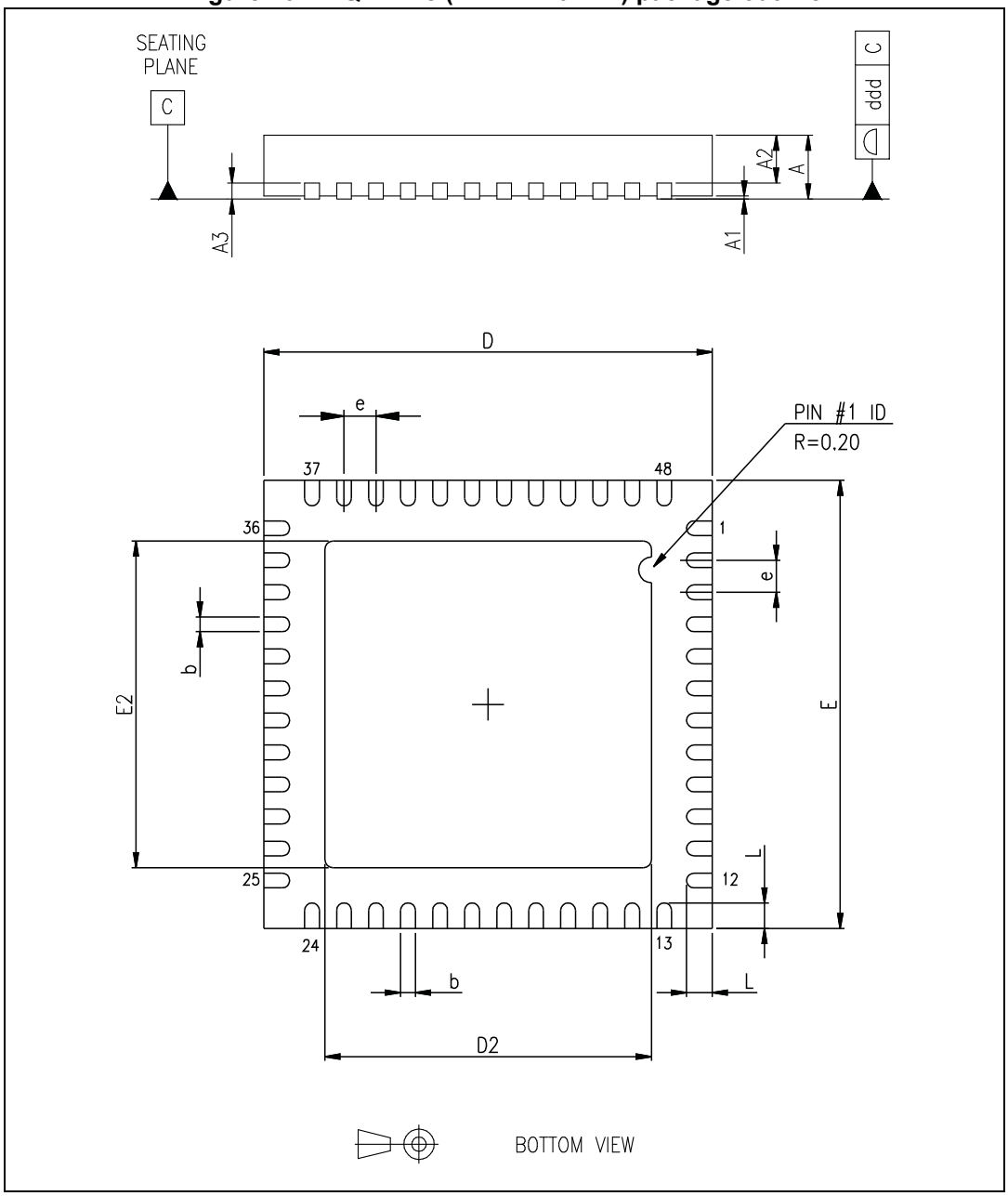


Table 9. VFQFPN48 (7 x 7 x 1.0 mm) package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	-	0.02	0.05
A2	-	0.65	1.00
A3	-	0.25	-
b	0.18	0.23	0.30
D	6.85	7.00	7.15
D2	4.95	5.10	5.25
E	6.85	7.00	7.15
E2	4.95	5.10	5.25
e	0.45	0.50	0.55
L	0.30	0.40	0.50
ddd	-	0.08	-

11 Order codes

Table 10. Ordering information

Order codes	Package	Packaging
L6206Q	VFQFPN48 7 x 7 x 1.0 mm	Tray
L6206QTR		Tape and reel

12 Revision history

Table 11. Document revision history

Date	Revision	Changes
15-Nov-2011	1	First release
10-Jun-2013	2	Unified package name to “VFQFPN48” in the whole document. Corrected headings in *Table 1* and *Table 2* (replaced “Parameter” by “Test condition”). Updated *Table 4* (Added subscripts to “I_f” and “R_{OPDR}”). Added titles to *Equation 1* and *Equation 2* and cross-references in *Section 4.3: Non-dissipative overcurrent detection and protection*. Corrected unit in *Table 7* (row C_1). Updated *Figure 13* (added subscripts to “t_{DELAY}” and “C_{EN}”). Added *Table 8: Thermal data* in *Section 8: Thermal management*. Updated *Section 10: Package information* (modified titles, reversed order of *Figure 26* and *Table 9*). Minor corrections throughout document.
01-Aug-2013	3	Updated *Figure 1 on page 1*. Corrected note *1.* below *Table 8 on page 22*.
10-Mar-2017	4	Updated *Table 7 on page 15* (removed C_{REF} row). Updated *Figure 9 on page 12* and *Figure 14 on page 16* (replaced by new figures). Minor modifications throughout document.

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