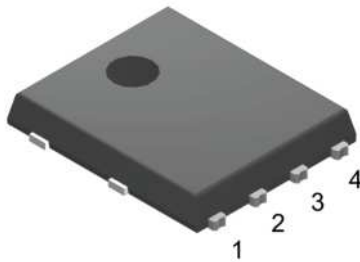
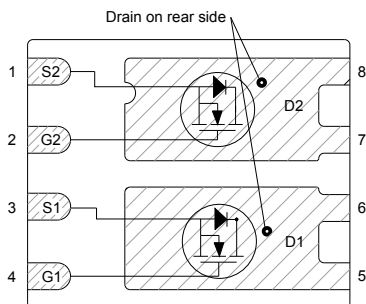


Automotive-grade dual N-channel 60 V, 22.5 mΩ typ., 7.8 A STripFET F3 Power MOSFET in a PowerFLAT 5x6 double island package



PowerFLAT 5x6
double island



NG14G22D1D2RSS13S21



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STL8DN6LF3	60 V	30 mΩ	7.8 A

- AEC-Q101 qualified 
- Logic level V_{GS(th)}
- 175 °C maximum junction temperature
- 100% avalanche rated
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STripFET F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

Product status link

[STL8DN6LF3](#)

Product summary

Order code	STL8DN6LF3
Marking	8DN6LF3
Package	PowerFLAT 5x6 double island
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 20	V
V_{DS}	Drain-source voltage	60	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	20	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	20	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	7.8	A
	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	5.5	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	31.2	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	65	W
$P_{TOT}^{(2)}$	Total power dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.3	W
I_{AV}	Non-repetitive avalanche current	7.8	A
$E_{AS}^{(4)}$	Single pulse avalanche energy	190	mJ
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Current is limited by bonding, with $R_{thJC} = 2.3\text{ }^\circ\text{C/W}$; the chip is able to carry 30 A at $25\text{ }^\circ\text{C}$.
2. When mounted on an 1 inch² 2 Oz. Cu board, $t < 10\text{ s}$.
3. Pulse width is limited by safe operating area.
4. Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AS}$, $V_{DD} = 25\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.3	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	

1. When mounted on an 1 inch² 2 Oz. Cu board, $t < 10\text{ s}$.

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	60			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 60\text{ V}$			1	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 4\text{ A}$		22.5	30	m Ω
		$V_{GS} = 5\text{ V}$, $I_D = 4\text{ A}$		30	44	m Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	668	-	pF
C_{oss}	Output capacitance		-	144	-	pF
C_{rss}	Reverse transfer capacitance		-	14	-	pF
Q_g	Total gate charge	$V_{DD} = 30\text{ V}$, $I_D = 7.8\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	13	-	nC
Q_{gs}	Gate-source charge		-	2.4	-	nC
Q_{gd}	Gate-drain charge		-	3	-	nC
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	4	-	Ω

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$, $I_D = 4\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	9	-	ns
t_r	Rise time		-	7.7	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	32.5	-	ns
t_f	Fall time		-	5	-	ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7.8	A
I_{SDM}	Source-drain current (pulsed)		-		31.2	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 7.8\text{ A}$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 7.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 48\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	30		ns
Q_{rr}	Reverse recovery charge		-	35		nC
I_{RRM}	Reverse recovery current		-	2.35		A

1. Pulse width is limited by safe operating area.

2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

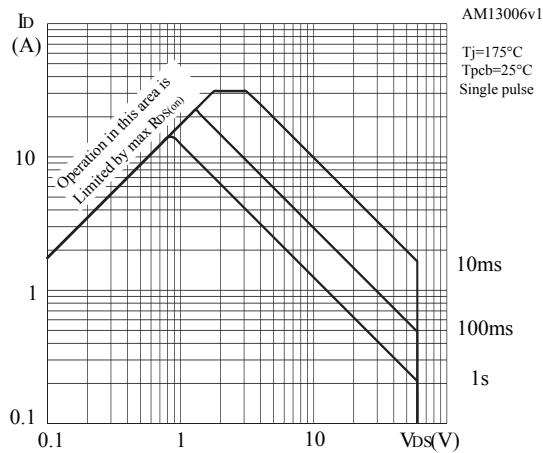
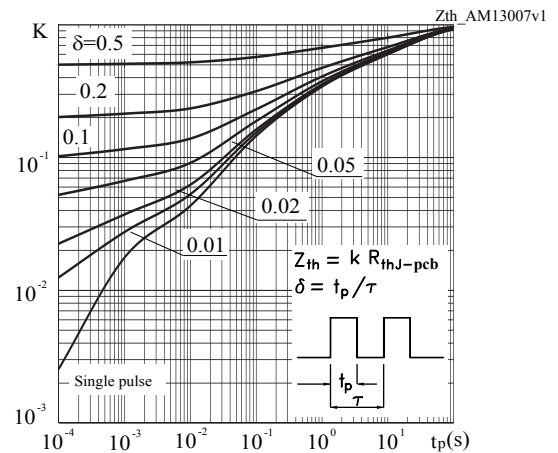
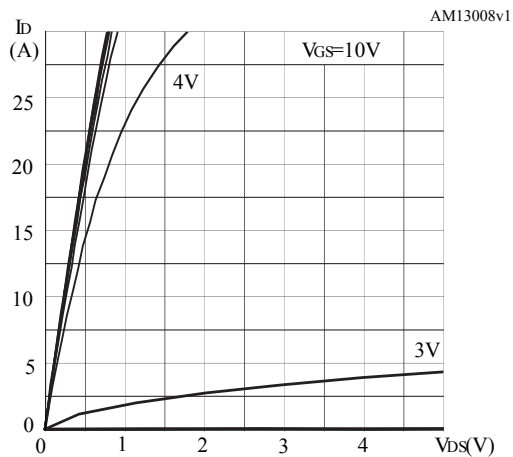
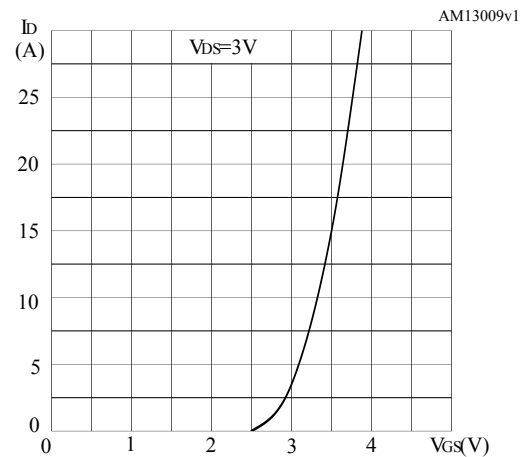
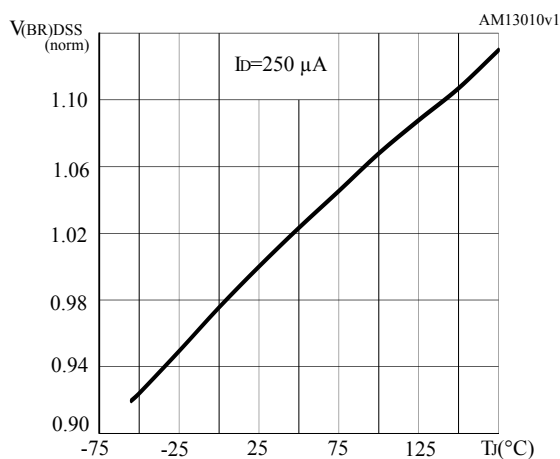
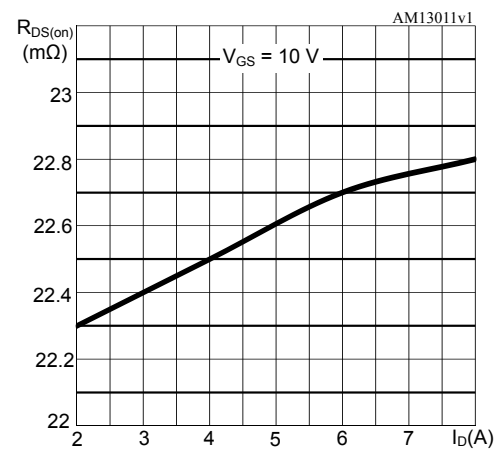
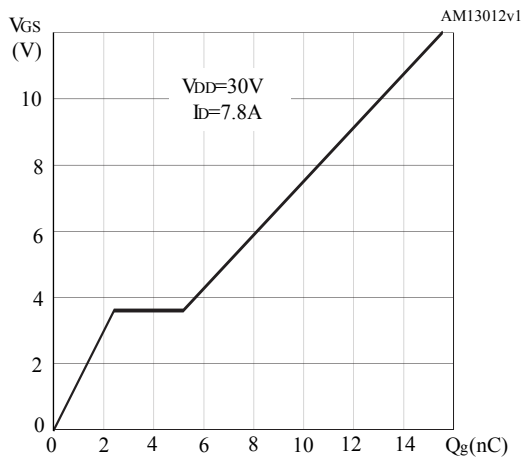
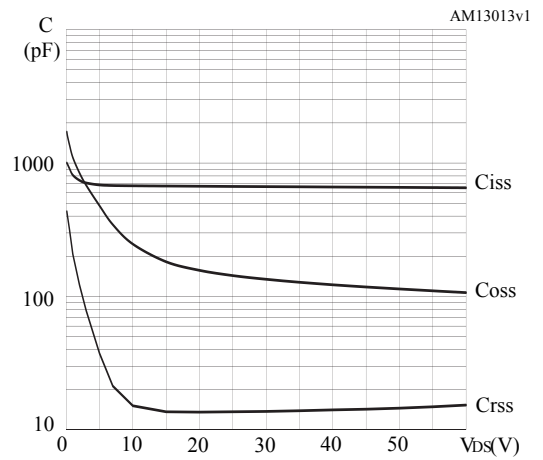
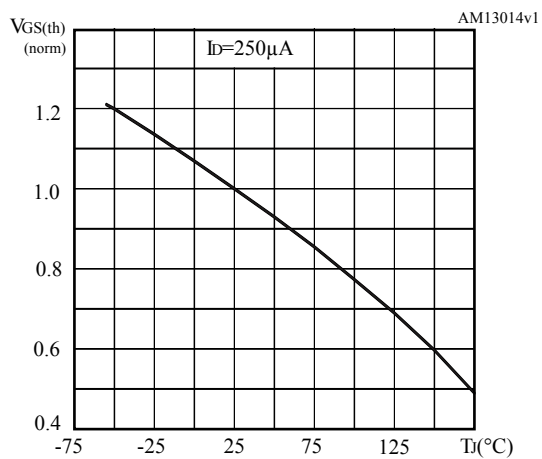
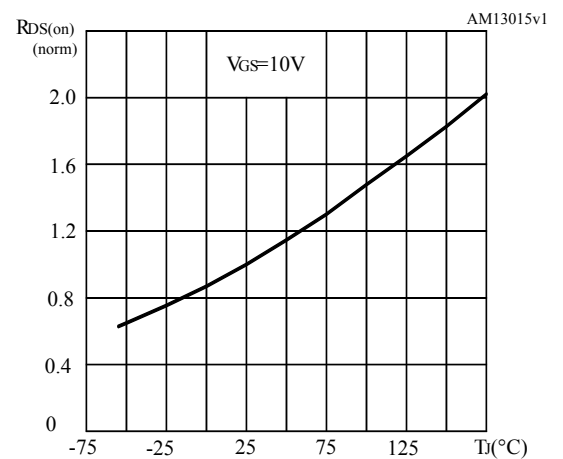
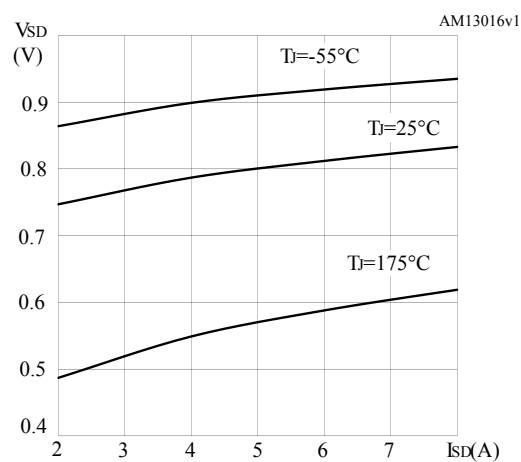
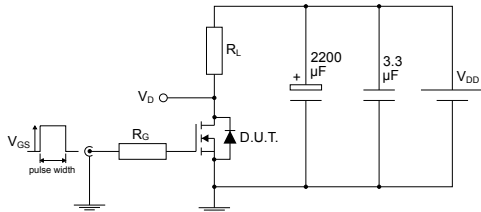
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Normalized $V_{(\text{BR})\text{DSS}}$ vs. temperature

Figure 6. Static drain-source on-resistance


Figure 7. Gate charge vs. gate-source voltage

Figure 8. Capacitance variations

Figure 9. Normalized gate threshold voltage vs. temperature

Figure 10. Normalized on-resistance vs. temperature

Figure 11. Source-drain diode forward characteristics


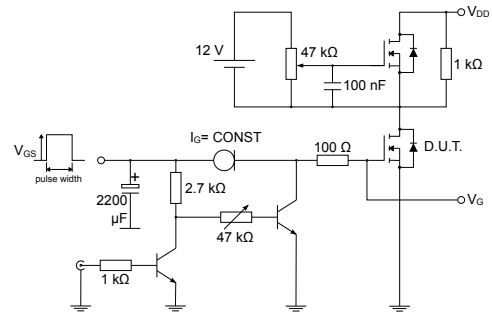
3 Test circuits

Figure 12. Test circuit for resistive load switching times



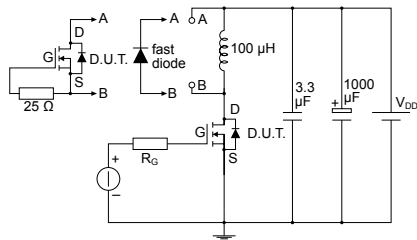
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Figure 13. Test circuit for gate charge behavior



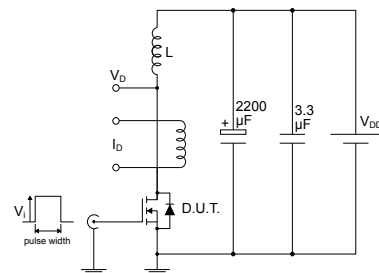
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Figure 14. Test circuit for inductive load switching and diode recovery times



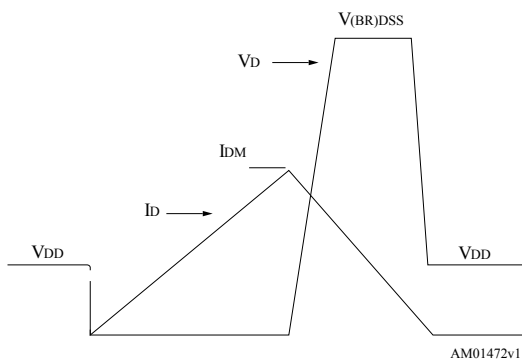
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Figure 15. Unclamped inductive load test circuit



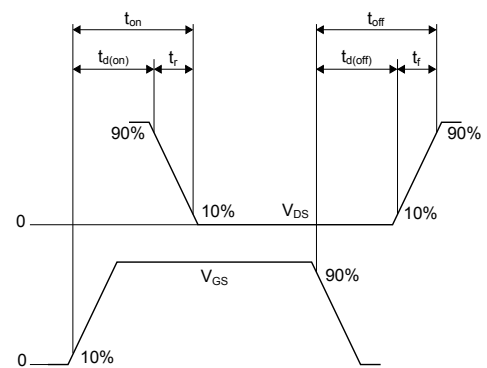
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Figure 16. Unclamped inductive waveform



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Figure 17. Switching time waveform



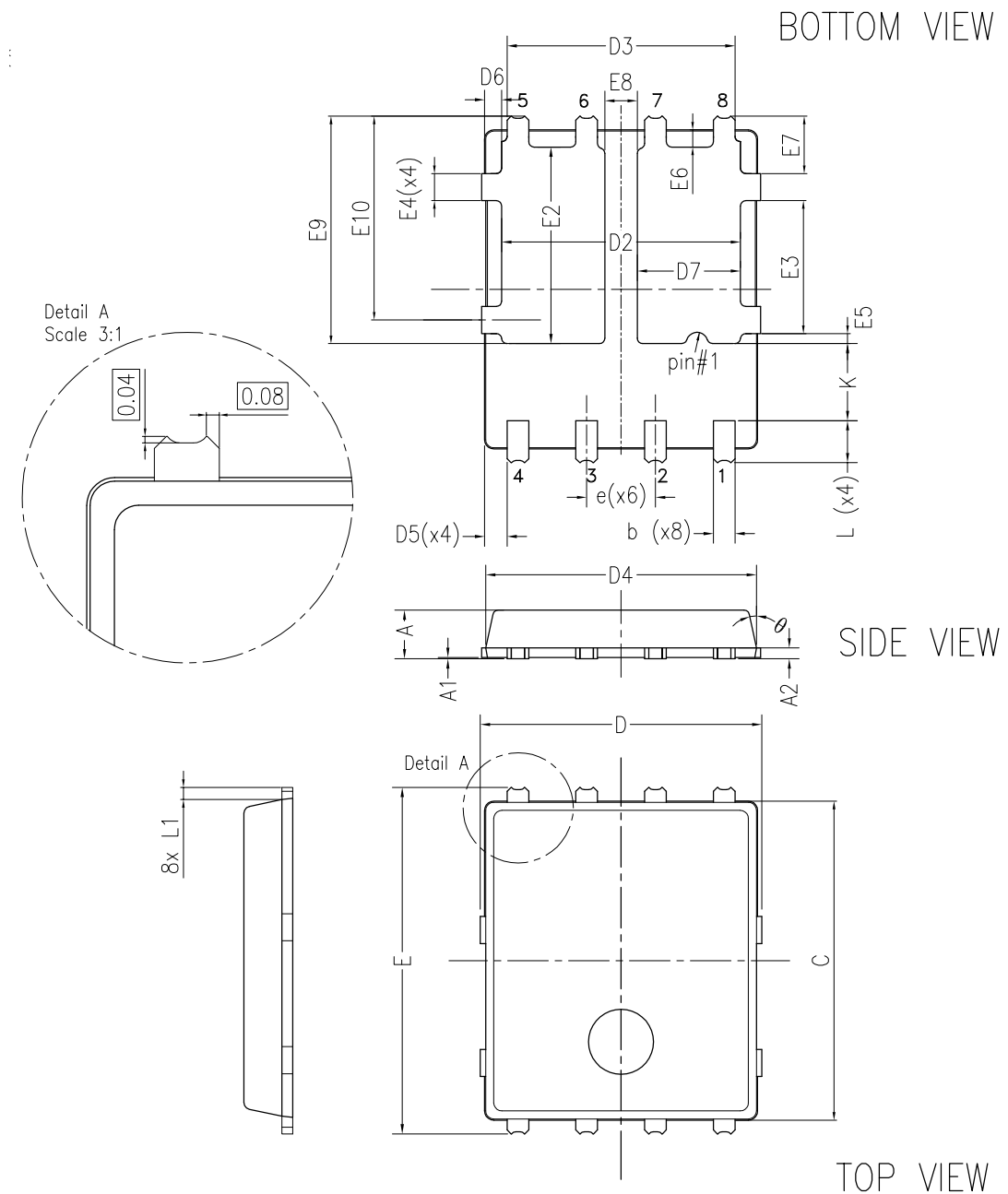
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 double island WF type R package information

Figure 18. PowerFLAT 5x6 double island WF type R package outline

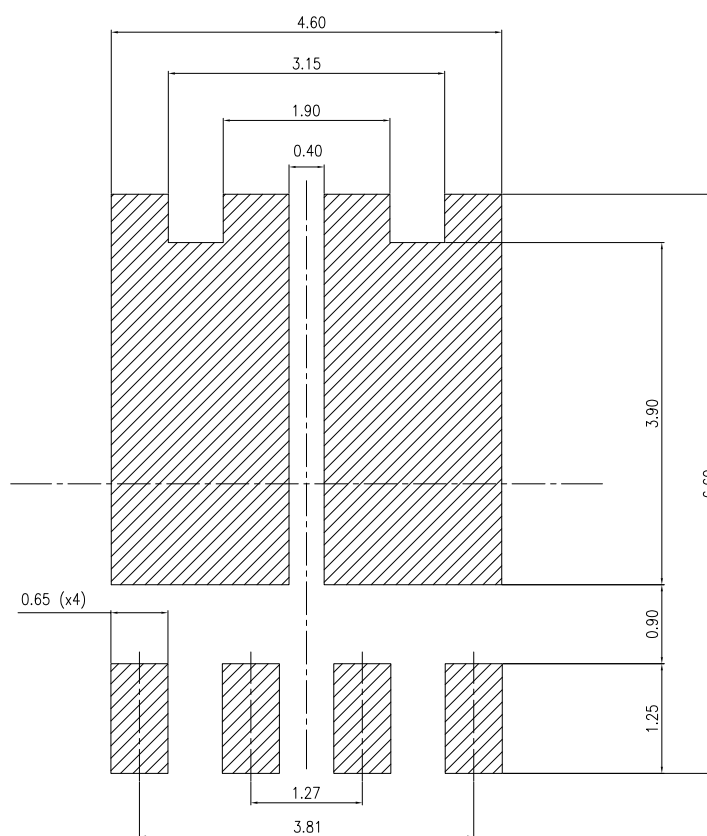


8256945_typeR-WF_R18

Table 7. PowerFLAT 5x6 double island WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
D7	1.68		1.98
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E8	0.55		0.75
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
θ	0°		12°

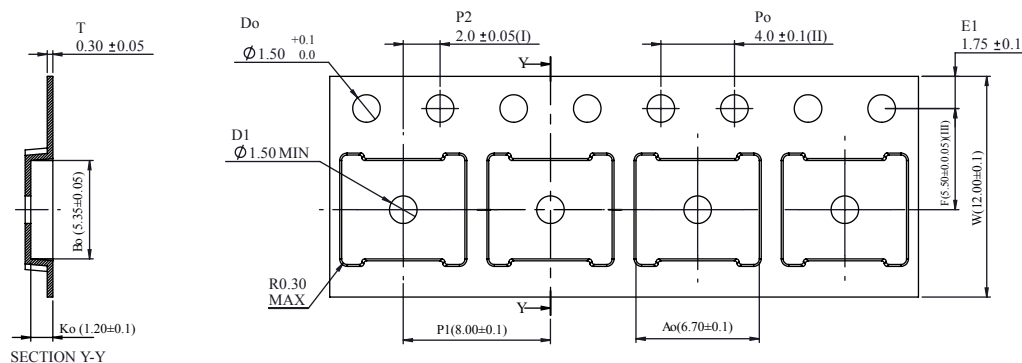
Figure 19. PowerFLAT 5x6 double island recommended footprint (dimensions are in mm)



8256945_DI_FP_smp_R18

4.2 PowerFLAT 5x6 WF packing information

Figure 20. PowerFLAT 5x6 WF tape (dimensions are in mm)



- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
- (III) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk quantity 3000 pcs

8234350_TapeWF_rev_C

Figure 21. PowerFLAT 5x6 package orientation in carrier tape

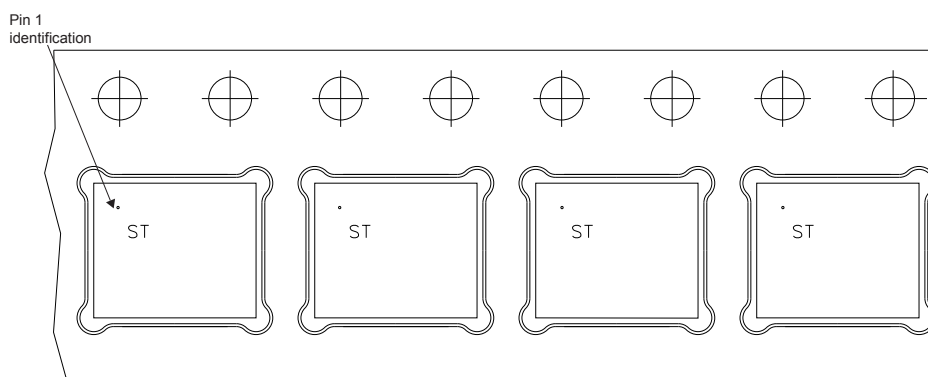
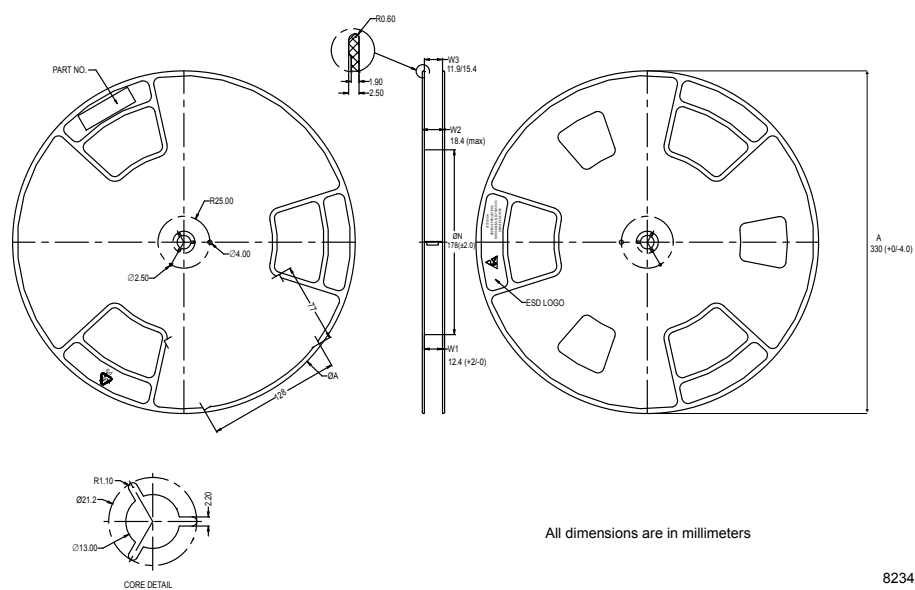


Figure 22. PowerFLAT 5x6 reel (dimensions are in mm)



Revision history

Table 8. Document revision history

Date	Revision	Changes
11-Oct-2011	1	First release.
19-Jun-2012	2	Added <i>Section 2.1: Electrical characteristics (curves)</i> . Updated <i>Section 4: Package mechanical data</i> and title on the cover page.
26-Jun-2012	3	Document status promoted from preliminary to production data.
24-Oct-2013	4	- Updated title and features in cover page - Modified: VGS(th) value in <i>Table 4</i> - Updated: <i>Section 4: Package mechanical data</i> and <i>Section 5: Packaging mechanical data</i> - Minor text changes
20-Feb-2014	5	- Added: <i>Features</i> in cover page - Added: <i>note 1</i> in <i>Table 1</i> - Added: <i>Table 20</i> and <i>Table 9</i> - Added: <i>Figure 23</i> - Minor text changes
11-May-2017	6	Updated title and description on cover page. Updated <i>Figure 6: "Normalized V(BR)DSS vs. temperature"</i> and <i>Figure 11: "Normalized on-resistance vs. temperature"</i>. Updated <i>Section 4: "Package information"</i> Minor text changes
04-Mar-2020	7	Updated Section 4 Package information. Minor text changes.

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3	Test circuits	7
4	Package information	8
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4.2	PowerFLAT 5x6 WF packing information	11
	Revision history	13

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