VNQ6004SA-E

Quad-channel high-side driver with 16-bit SPI interface

Datasheet - production data

PSSO36

Features

Channel	V_{CC}	$R_{ON(typ)}$	$I_{LIMH(min)}$
0–1	28 V	30 mΩ	25 A
2–3	28 V	10 mΩ	55 A

- General
  - 16-bit ST-SPI for full and diagnostic
  - Programmable Bulb/LED mode for ch. 0–1
  - Integrated PWM and phase shift generation unit
  - 160 Hz internal PWM fallback frequency
  - Advanced limp home functionalities for robust fail-safe system
  - Very low standby current
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/EC
- Diagnostic functionalities
  - Multiplex proportional load current sense
  - Synchronous diagnostic of over load and short to GND, output shorted to V_{CC}, ON-state and OFF-state open-load
  - Programmable case over temperature warning
- Protection
  - Load current limitation
  - Self limiting of fast thermal transients
  - Power limitation and over temperature shutdown (latching-off or auto restart)
  - Undervoltage shutdown
  - Overvoltage clamp
  - Reverse battery protected through power outputs self turn-on (no external components)
  - Load dump protected
  - Protection against loss of ground

Description

The VNQ6004SA-E is a device made using STMicroelectronics® VIPower® technology. It is intended for driving resistive or inductive loads directly connected to ground. The device is protected against voltage transient on V_{CC} pin.

Programming, control and diagnostics are implemented via the SPI bus.

An analog current feedback for each channel is connected to the CURRENT-SENSE pin via a multiplexer. A CS_SYNC pin delivers a synchronous signal for sampling the current sense while the corresponding output is on.

The device detects open-load for both on and OFF-state conditions.

Real time diagnostic is available through the SPI bus (open-load, output short to V_{CC}, over temperature, communication error, power limitation).

Output current limitation protects the device in an over load condition. The device can limit the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown can be configured as latched off or with automatic restart.

The device enters a limp home mode in case of loss of digital supply (V_{DD}), reset of digital memory or CSN monitoring time-out event. In this mode states of channel 0, 1, 2 or 3 are respectively controlled by four dedicated pins IN0, IN1, IN2 and IN3. Channel 0,1 can be programmed in BULB/LED mode.

This is information on a product in full production. www.st.com

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1 Block diagram and pin description

Figure 1. SPI configurable functionalities

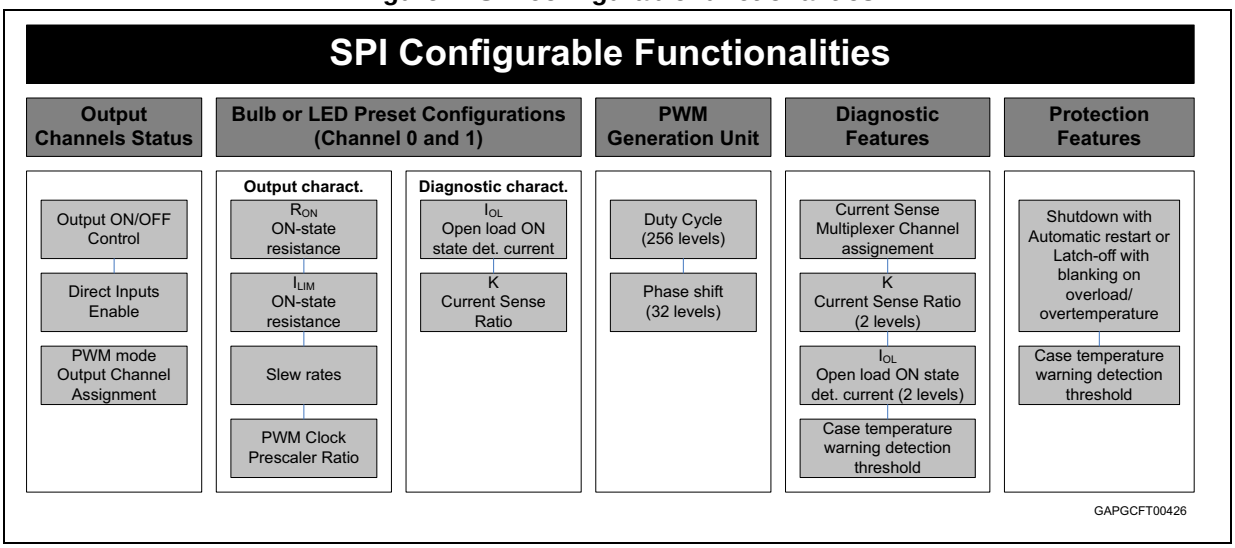


Figure 2. SPI diagnostic reporting

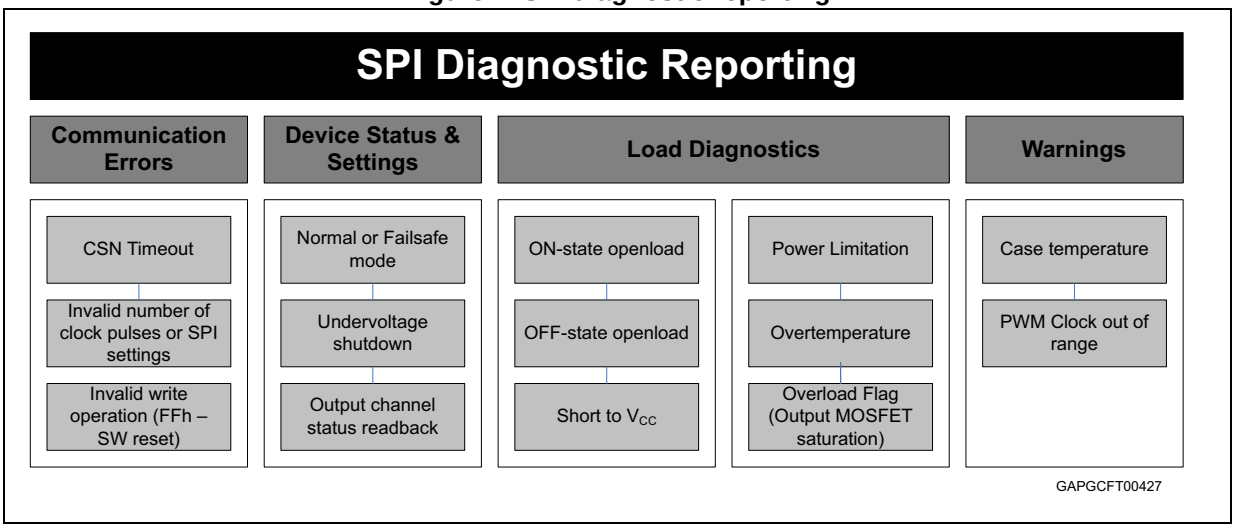
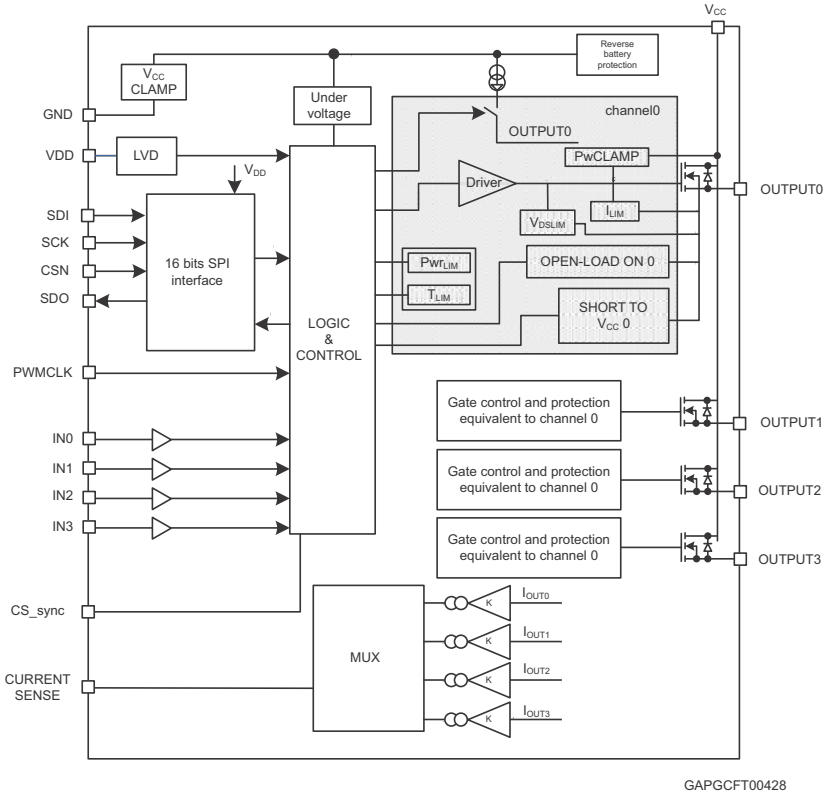
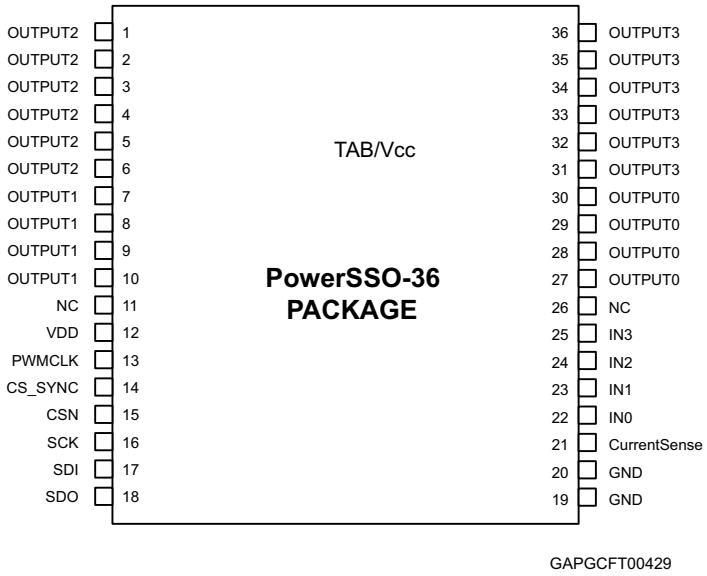


Figure 3. Block diagram



Note:
VNQ6004SA-E block diagram illustrates only a major internal device functionality and it is not intended to mimic any details of hardware design.

Figure 4. Connection diagram (top view—not in scale)



Note:
Pins 31,32,33,34,35 and 36 (OUTPUT3) must be connected together.
Pins 27,28,29 and 30 (OUTPUT0) must be connected together.
Pins 7,8,9 and 10 (OUTPUT1) must be connected together.
Pins 1,2,3,4,5 and 6 (OUTPUT2) must be connected together.

Table 1. Pin functionality description

Pin number	Name	Function
—	V_{CC}	Battery connection. This is the backside TAB and is the direct connection to drain Power MOSFET switches.
19, 20	GND	Ground connection. This pin serves as the ground connection for the logic part of the device.
27, 28, 29, 30	OUTPUT0	Power OUTPUT 0. It is the direct connection to the source Power MOSFET switch No. 0.
7, 8, 9, 10	OUTPUT1	Power OUTPUT 1. It is the direct connection to the source Power MOSFET switch No. 1.
1, 2, 3, 4, 5, 6	OUTPUT2	Power OUTPUT 2. It is the direct connection to the source Power MOSFET switch No. 2.
31, 32, 33, 34, 35, 36	OUTPUT3	Power OUTPUT 3. It is the direct connection to the source Power MOSFET switch No. 3.
15	CSN	Chip select not (active low). It is the selection pin of the device. It is a CMOS compatible input. It is also used as CSN monitoring pin. It must be toggled within a CSN monitoring timeout period to keep the device from switching to limp home operation.
16	SCK	Serial clock. It is a CMOS compatible input.
17	SDI	Serial data input. Transfers data to be written serially into the device on SCK rising edge.
18	SDO	Serial data output. Transfers data serially out of the device on SCK falling edge.
13	PWMCLK	PWM external clock. The frequency of the internal PWM signal is 1/512 x PWMCLK frequency for channels operating in BULB mode and 1/256 x PWMCLK frequency for channels operating in LED mode. Device defaults to internally generated fixed PWM frequencies if PWMCLK frequency decreases below the minimum specified value.
14	CS_SYNC	Current sense synchronization pin. The pin is high when the output, whose currents is reflected on current sense pin, is on.
22	IN0	Direct Input pin for channel 0. Controls the OUTPUT 0 state in limp home mode, is ORed to SPI control register in normal operating mode when corresponding bit is set in DIENCR (Direct Input ENable) control register.
23	IN1	Direct Input pin for channel 1. Controls the OUTPUT 1 state in limp home mode, is ORed to SPI control register in normal operating mode when corresponding bit is set in DIENCR (Direct Input ENable) control register.
24	IN2	Direct Input pin for channel 2. Controls the OUTPUT 2 state in limp home mode, is ORed to SPI control register in normal operating mode when corresponding bit is set in DIENCR (Direct Input ENable) control register.

Table 1. Pin functionality description (continued)

Pin number	Name	Function
25	IN3	Direct Input pin for channel 3. Controls the OUTPUT 3 state in limp home mode, is ORed to SPI control register in normal operating mode when corresponding bit is set in DIENCR (Direct Input ENable) control register.
12	V_{DD}	External 5V supply. Powers the digital control and SPI interface.
21	Current sense	Analog current sense generator proportional to output current. Current sense ratio can be programmed for each channel. The pin can output the current sense of OUTPUT 0, 1, 2 or 3. The value of resistance that is connected between the CURRENT SENSE pin and device ground determines the reading level for the microcontroller.
26	NC	Not connected

2 Functional description

2.1 Operating modes

The device can operate in 7 different modes:

- Reset mode
  Reset mode is entered after startup, and if the digital voltage V_{DD} falls below V_{DDR}. In this condition, the outputs are controlled by the direct inputs INX. The SPI is inactive, all SPI registers are cleared.
- Fail Safe mode
  After reset, after wake-up from Standby or Sleep mode 1 or 2 and in case of several error conditions, the device operates in Fail Safe mode. In this condition, the outputs are controlled by the direct inputs INX regardless of SPI commands. Diagnosis is available through SPI bus.
- Normal mode
  If the device is in Fail Safe mode, Normal mode can be entered using a special SPI sequence. In Normal mode, outputs can be driven by SPI commands or a combination of SPI command and direct inputs INX. Diagnosis is available through SPI bus and CurrentSense pin.
- Standby mode
  If the device is in Normal mode or Fail Safe mode, Standby mode can be entered using a special SPI sequence. In Standby mode the consumption of the digital part is nearly 0. The outputs are controlled by the direct inputs INX regardless of SPI commands.
- Sleep mode 1
  If the device is in Reset mode and the direct inputs INX are all 0, the device enters Sleep mode 1. In Sleep mode 1, the output stages are off, the current consumption of the digital part is nearly 0 and the current consumption on V_{CC} is below I_{Soff}.
- Sleep mode 2
  If the device is in Standby mode and the direct inputs INX are all 0, the device enters Sleep mode 2. In Sleep mode 2, the output stages are off, the current consumption of the digital part is nearly 0 and the current consumption on V_{CC} is below I_{Soff}.
- Battery undervoltage mode
  If the battery voltage V_{CC} is below the undervoltage threshold, the device enters Battery undervoltage mode. In this condition, the output stages are off regardless of SPI commands.

The Reset mode, the Fail Safe mode and the Sleep mode 1 are combined into the Limp home mode. In this mode the chip is able to operate without the connection to the SPI. All transitions between the states in limp home mode are driven by V_{DD} and INX. The outputs are controlled by the direct inputs INX.

For an overview over the operating modes and the triggering conditions please refer to *Table 2*.

Table 2. Operating modes

Operating mode	Entering conditions	Leaving conditions	Characteristics
Reset	– Startup – Any mode: $V_{DD} < V_{DDR}$ – Sleep 1: INX low to high	– All INX low: sleep 1 – $V_{DD} > V_{DDR}$: fail safe	– Outputs: according to INX – SPI: inactive – Registers: cleared – Diagnostics: not available
Fail Safe	– Reset or sleep 1: $V_{DD} > V_{DDR}$ – Standby or sleep 2: CSN low for $t > t_{stdby_out}$ – Normal: EN = 0 or CSN time out or SW reset	– $V_{DD} < V_{DDR}$: reset – SPI sequence 1. UNLOCK = 1 2. STBY = 0 and EN = 1: normal – SPI sequence 1. UNLOCK = 1 2. STBY = 1 and EN = 0: fail safe	– Outputs: according to INX – SPI: active – Registers: read/writeable, cleared if entered after HW or SW reset – Diagnostics: SPI possible CurrentSense not possible
Normal	– Fail Safe: SPI sequence 1. UNLOCK = 1 2. STBY = 0 and EN = 1	– $V_{DD} < V_{DDR}$: reset – SPI sequence 1. UNLOCK = 1 2. STBY = 1 and EN = 0: standby – EN = 0 or CSN time out or SW reset: fail safe	– Outputs: according to SPI register settings and INX – SPI: active – Registers: read/writeable – Diagnostics: SPI and CurrentSense possible – Regular toggling of CSN necessary
Standby	– Normal: SPI sequence 1. UNLOCK = 1 2. STBY = 1 and EN = 0 – Fail Safe: SPI sequence 1. UNLOCK = 1 2. STBY = 1 and EN = 0 – Sleep 2: INX low to high	– $V_{DD} < V_{DDR}$: reset – CSN low for $t > t_{stdby_out}$: fail safe – All INX low: sleep 2	– Outputs: according to INX – SPI: inactive – Registers: frozen – Diagnostics: not available – Low supply current from V_{DD}
Sleep 1	Reset: all INX = 0	– $V_{DD} > V_{DDR}$: fail safe – INX low to high: reset	– Outputs: OFF – SPI: inactive – Registers: cleared – Diagnostics: not available – Low supply current from V_{DD} and V_{CC}

Table 2. Operating modes (continued)

Operating mode	Entering conditions	Leaving conditions	Characteristics
Sleep 2	Standby: all INX = 0	– $V_{DD} < V_{DDR}$: reset – CSN low for $t > t_{stdby_out}$: fail safe – INX low to high: standby	– Outputs: OFF – SPI: inactive – Registers: frozen – Diagnostics: not available – Low supply current from V_{DD} and V_{CC}
Battery undervoltage	Any mode: $V_{CC} < V_{USD}$	$V_{CC} > V_{USD}$: back to last mode	– Outputs: OFF – SPI: active – Register: read/writeable – Diagnostics: SPI possible, CurrentSense not possible

2.1.1 Reset mode

The device enters Reset mode under three conditions:

- Automatically during startup
- If it is in any other mode and if V_{DD} falls below V_{DDR}
- If it is in Sleep mode 1 and if one input INX is set to 1

In Reset mode, the output stages are according to the inputs INX. The SPI is inactive and all SPI registers are cleared. The reset bit inside the Global Status Byte is set to 0. The diagnostics is not available, but the protection are fully functional. In case of over temperature or power limitation, the outputs work in Autorestart.

Reset mode can be left with 2 conditions:

- If V_{DD} rises above V_{DDR}, the device enters Fail Safe mode
- If all inputs INX are 0, the device enters Sleep mode 1.

2.1.2 Fail Safe mode

The device enters Fail Safe mode under five conditions:

- If it is in Reset mode or in Sleep mode 1 and V_{DD} rises above V_{DDR}
- If it is in Standby mode or in Sleep mode 2 and CSN is low for $t > t_{stdby_out}$
- If it is in Normal mode and bit EN is cleared
- If it is in Normal mode and CSN is not toggled within t_{WHCH} (CSN timeout)
- If it is in Normal mode and the SPI sends a SW reset (Command byte = FFh).

In Fail Safe mode, the output stages are according to the inputs INX. The SPI is active. The reset bit is 0 if the last state was Reset mode or the last command was a SW reset and it is set to 1 after the first SPI access. The SPI diagnostics is available, the CurrentSense pin is not available. The protection are fully functional. In case of over temperature or power limitation, the outputs work in Autorestart.

The device exits Fail Safe mode under two conditions:

- If the SPI sends the goto Normal mode sequence, the device enters Normal mode:
  - In a first communication set bit UNLOCK = 1
    In the consecutive communication set bit STBY = 0 and bit EN = 1
  - This mechanism avoids entering the Normal mode unintentionally.
- If the SPI sends the goto standby mode sequence, the device enters Standby mode:
  - In a first communication set bit UNLOCK = 1
    In the consecutive communication set bit STBY = 1 and bit EN = 0
  - This mechanism avoids entering the Standby mode unintentionally.
- If V_{DD} falls below V_{DDR}, the device enters Reset mode.

2.1.3 Normal mode

The device enters Normal mode if it is in Fail Safe mode and the SPI sends the goto Normal mode sequence:

- In a first communication set bit UNLOCK = 1
  In the consecutive communication set bit STBY = 0 and bit EN = 1
- This mechanism avoids entering the Normal mode unintentionally.

In Normal mode, the output stages are controlled by the SPI and the INX settings. The SPI is active. CSN must be toggled regularly within t_{WHCH} to keep the device in Normal mode. The SPI diagnostics and the CurrentSense pin are both available. The protection are fully functional. The outputs can be set to Autorestart or Latch. In Autorestart the outputs are switched on again automatically after an over temperature or power limitation event, while in Latch the relevant status register has to be cleared to switch them on again.

Normal mode can be left with 5 conditions:

- If V_{DD} falls below V_{DDR}, the device enters Reset mode.
- If the SPI sends the goto standby sequence, the devices enters Standby mode:
  - In a first communication set UNLOCK = 1
    In the consecutive communication set STBY = 1 and EN = 0
  - This mechanism avoids entering the Standby mode unintentionally.
- If the SPI clears the EN bit (EN = 0), the devices enters Fail Safe mode
- CSN time out: If CSN is not toggled within the minimum CSN monitoring timeout period t_{WHCH}, the device enters Fail Safe mode.
- If the SPI sends a SW reset command (Command byte = FFh), all registers are cleared and the device enters Fail Safe mode.

2.1.4 Standby mode

The device enters Standby mode under three conditions:

- If it is in Fail Safe mode and the SPI sends the goto standby sequence:
  - In a first communication set UNLOCK = 1
    In the consecutive communication set STBY = 1 and EN = 0
  - This mechanism avoids entering the Standby mode unintentionally.
- If it is in Normal mode and the SPI sends the goto standby sequence:
  - In a first communication set UNLOCK = 1
    In the consecutive communication set STBY = 1 and EN = 0
  - This mechanism avoids entering the Standby mode unintentionally.
- If it is in Sleep mode 2 and one input INX is set to one.

The output stages are according to INX settings, the current from V_{DD} is nearly 0.The SPI is inactive and all registers are frozen to the last state. The diagnostics is not available.

Standby mode can be left with three conditions:

- If V_{DD} falls below V_{DDR}, the device enters Reset mode.
- If CSN is low for $t > t_{stdby_out}$, the device wakes up. As EN has been set to 0, the device enters Fail Safe mode and recovers full functionality with command of the outputs and diagnostics.
- If all direct inputs INX are 0, the device enters Sleep Mode 2 resulting in minimal supply current from V_{CC} and V_{DD}.

2.1.5 Sleep mode 1

The device enters Sleep mode 1, if it is in Reset mode and if all inputs INX are 0.

All outputs are off, the current from V_{DD} is nearly 0, and the current from V_{CC} is reduced to I_{Soff}. The SPI is inactive and all registers are cleared. The diagnostics is not available.

Sleep mode 1 can be left with two conditions:

- If V_{DD} rises above V_{DDR}, the device enters Fail Safe mode.
- If one of the inputs INX is set to 1, the device enters Reset mode.

2.1.6 Sleep mode 2

The device enters Sleep mode 2, if it is in Standby mode and if all inputs INX are 0.

All outputs are off, the current from V_{DD} is nearly 0, and the current from V_{CC} is reduced to I_{Soff}. The SPI is inactive and all registers are frozen to the last state. The diagnostics is not available.

Sleep mode 2 can be left with three conditions:

- If V_{DD} falls below V_{DDR}, the device enters Reset mode.
- If CSN is low for $t > t_{stdby_out}$, the device enters Fail Safe mode.
- If one of the inputs INX is set to 1, the device enters Standby mode.

2.1.7 Battery undervoltage mode

If the battery supply voltage V_{CC} falls below the undervoltage shutdown threshold V_{USD} while VDD remains above the reset threshold V_{DDR}, the device enters Battery undervoltage mode independent from the operation mode. In Battery undervoltage mode, the outputs are turned off. The SPI is active and the SPI register contents are retained. The SPI diagnostics is available, the CurrentSense pin is not available. The bit VCCUV in the general status register GENSTR is set. If V_{CC} rises above the threshold V_{USD} + $V_{USDhyst}$, the device returns to the last mode and VCCUV is cleared.

Figure 5. Battery undervoltage shutdown diagram

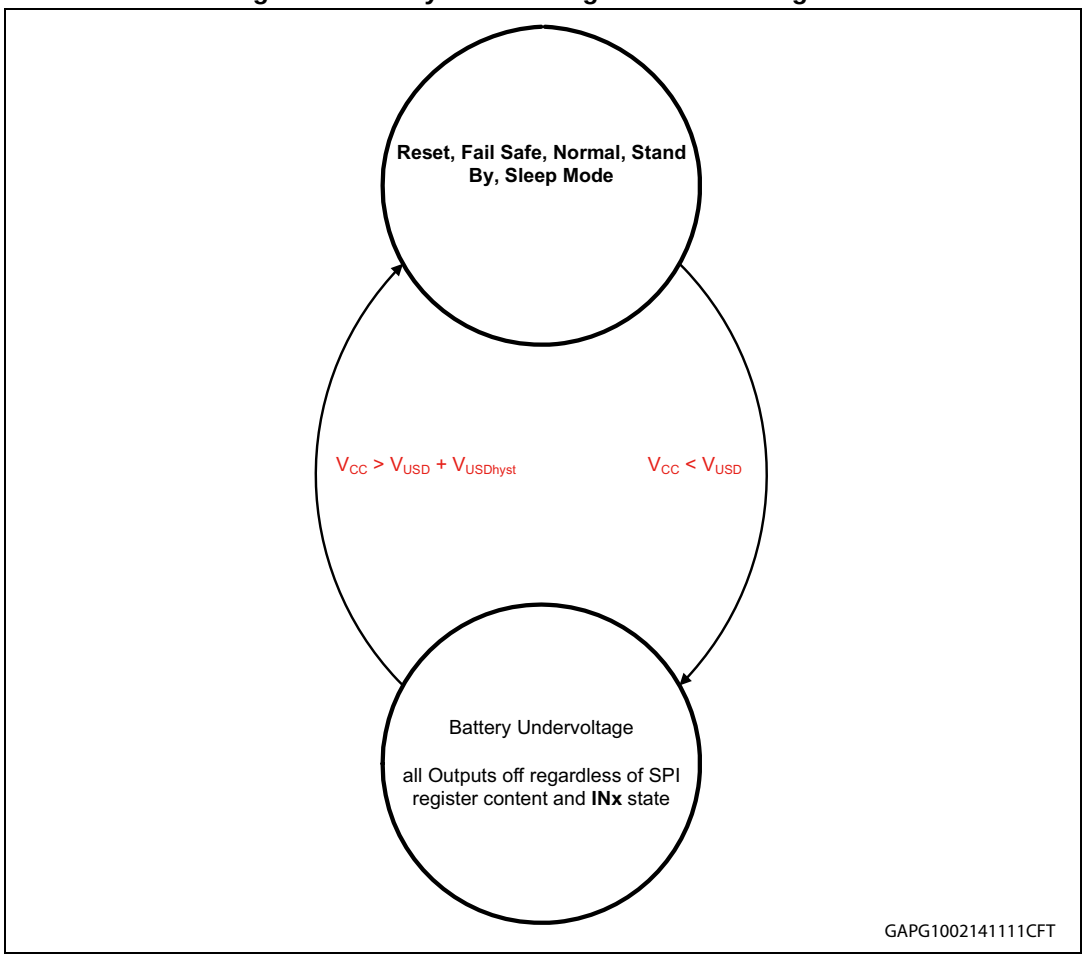
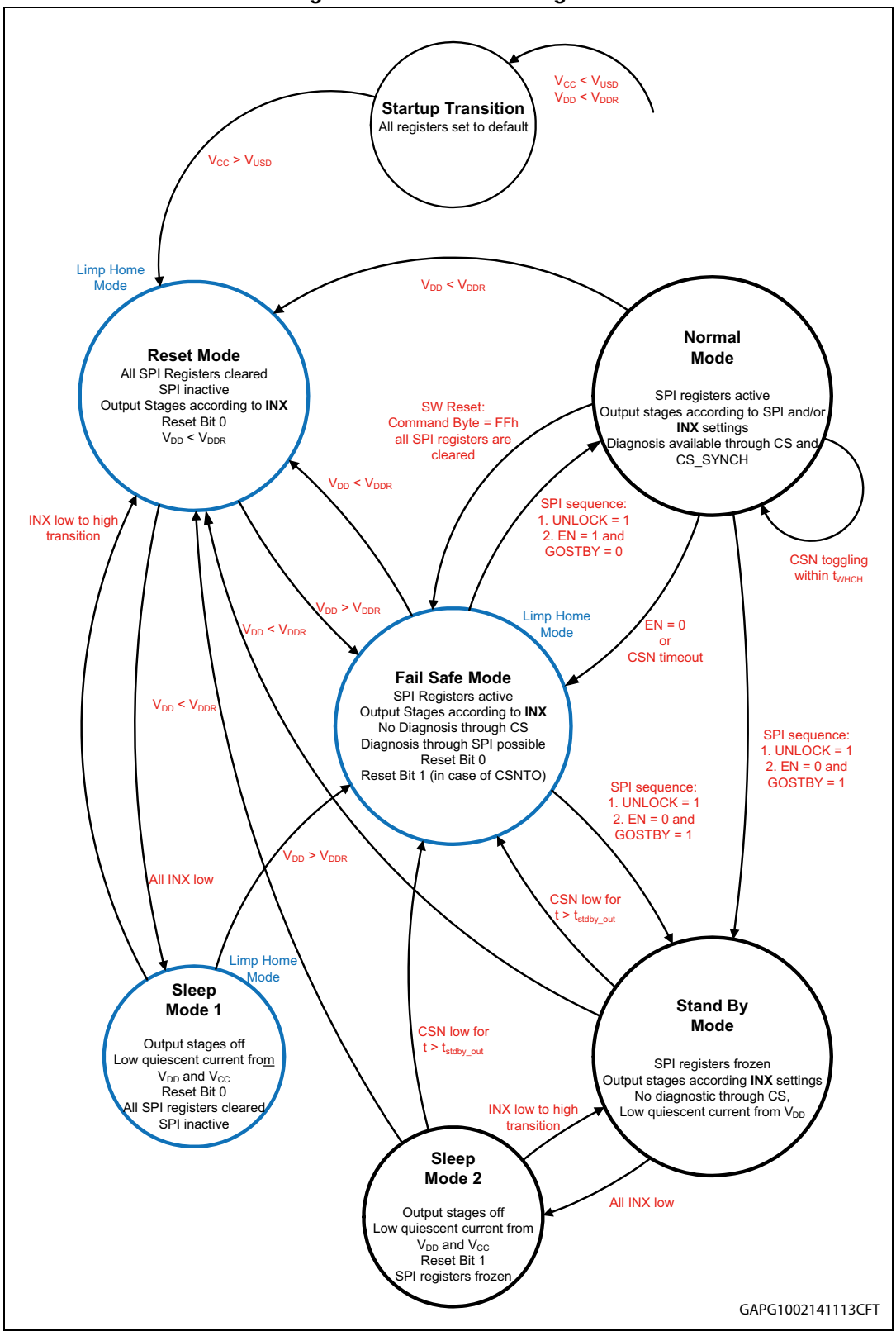


Figure 6. Device state diagram



2.2 Programmable functions

2.2.1 Outputs configuration

The status of the output drivers is configured via the SPI output control register (SOCR), the direct input enable control register (DIENCR), the PWM mode control register (PWMCR) and the channel control register (CCR). The DIENCR selects if the outputs OUTPUTX are controlled also by the direct inputs INX or only by the SOCR. The PWMCR selects if the outputs operates in PWM mode. Please refer to *Table 3* for details.

Table 3. Output control truth table

DIENCRX	INX	SOCRX	PWMCRX	OUTPUTX
0	X	0	0	OFF
0	X	0	1	OFF
0	X	1	0	ON
0	X	1	1	PWM
1	L	0	0	OFF
1	L	0	1	OFF
1	L	1	0	ON
1	L	1	1	PWM
1	H	X	0	ON
1	H	X	1	PWM

The output channels 0 and 1 can be configured to operate in BULB or LED mode using the channel control register (CCR). If the relevant bit in CCR is 0, the output is configured in BULB mode, if it is set to 1, the output is configured in LED mode. This configuration has an influence on the base frequency for PWM operation (see below in this chapter), on the open-load thresholds (see *Chapter 2.2.4*) and on the current sense ratio (see *Chapter 2.2.6*).

PWM operation

If the PWMCRX bit is set, the relevant output OUTPUTX operates in PWM mode. The duty cycle and the phase of the PWM signal are configured via the DUTYCXCR and the PHASEXCR registers, respectively.

The signal on the PWMCLK is divided internally by 512 or 256 depending on the output operating mode (BULB mode or LED mode) to generate the base frequency for the output.

The duty cycle of the output signal is configured for each OUTPUTX with the DUTYCXCR register using 8 bits (MSB first). DUTYCXCR = 00h means that the duty cycle is 0, and consequently the output is OFF, while DUTYCXCR = FFh results in a maximum duty cycle of 255/256 = 99.6 %. To switch the output permanently ON, it is necessary to select PWMCRX = 0 (see *Table 3*).

The phase shift of the output signal is configured for each OUTPUTX with the PHASEXCR register using 5 bits (MSB first, bit2–bit0 are ignored). PHASEXCR = 00h means a phase shift of 0, while PHASEXCR = F8h results in a maximum phase shift of 31/32 = 96.9 %. The phase shift is relative to the base frequency of the selected channel. Thus, the exact point in

time when the channel switches on depends also on the operating mode (BULB or LED mode) of the selected channel.

Below, an example with a 30% duty cycle and a 16% phase is given:

1. 30% duty cycle results in a DUTYCXCR register content equal to 76 = 4Ch (30 % x 256 = 76).
2. 16% phase results in a PHASECXR register content equal to 5 (16 % x 32 = 5), equivalent to a content of 40 = 28 h for a 8 bit register.

Table 4. Example of DUTYCXCR register

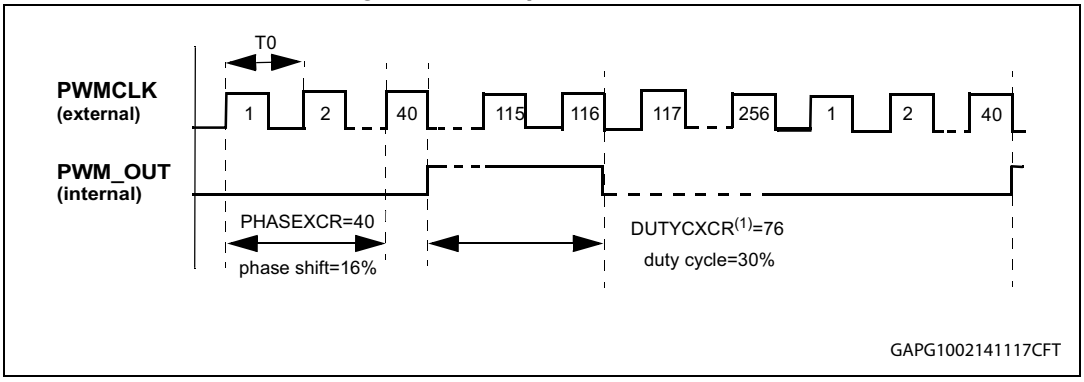
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	1	0	0	1	1	0	0

Table 5. Example of PHASEXCR register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	1	0	1	X	X	X

Figure 7 shows the resulting waveforms.

Figure 7. Example of PWM mode



Note: 1 If the frequency on PWMCLK is too low ($f < f_{pwm}$), the device falls back to an internally generated PWM frequency of about 160 Hz in BULB mode and 320 Hz in LED mode. In this case the PWMLOW bit in the General Status Register (GENSTR) and the global error flag are set.

2 The application should ensure that the duty cycle is not chosen too low. For very low duty cycle there are two restrictions: Due to the slew-rate control of the outputs, the outputs do not switch on and off immediately. Therefore, for low duty cycles, the output pulses are no longer rectangular but change to triangular form, resulting in a non-linear duty cycle - power relationship. Moreover, if the output is switched off while the voltage drop on the PowerMOS V_{DS} is still above V_{DSmax}, this causes a false over load detection (see also Section 2.2.3).

2.2.2 Case over temperature

If the case temperature rises above the case thermal detection pre-warning threshold T_{CSD}, the bit T_{FRAME} in the Global Status Byte is set. T_{FRAME} is cleared automatically when the case temperature drops below the case temperature reset threshold T_{CR}. The typical value

of T_{CSD} can be set using the bits CTDTH1 and CTDTH0 inside the CTLR register (see *Section 3.3.1*).

2.2.3 Protections

Junction over temperature

If the junction temperature of one channel rises above the shutdown temperature T_{TSD}, an over temperature event (OT) is detected. The channel is switched OFF and the corresponding bit in the over temperature status register OTFLTR (address 30h) is set. Consequently, the thermal shutdown bit (bit 4) in the Global Status Byte and the Global Error Flag are set.

Each output channel can be either set in Autorestart or Latched OFF operation in case of junction over temperature event by setting the corresponding ASDTCR register bit (address 08h).

In Autorestart operation, the output is switched off as described and switches on again automatically when the junction temperature falls below the reset temperature T_R. The status bit is latched during OFF-state of the channel in order to allow asynchronous diagnostic and it is automatically cleared when the junction temperature falls below the thermal reset temperature of OT detection T_{RS}.

In Latched OFF operation, the output remains switched OFF until the junction temperature falls below T_{RS} and a read and clear command is sent.

Power limitation

If the difference between junction temperature and case temperature ($\Delta T = T_j - T_c$) rises above the power limitation threshold ΔT_{PLIM}, a power limitation event is detected. The corresponding bit in the power limitation status register PWLMFLTR (address 33h) is set and the channel is switched OFF. Consequently, the power limitation bit (bit 4) in the Global Status Byte and the Global Error Flag are set.

Each output channel can be either set in Autorestart or Latched OFF operation in case of power limitation event by setting the corresponding ASDTCR register bit (address 08h).

In Autorestart operation, the output is switched off as described and switches on again automatically when ΔT falls below the reset threshold $\Delta T_{PLIMreset}$. The status bit is latched during OFF-state of the channel in order to allow asynchronous diagnostic and it is automatically cleared in ON-state when the power limitation event is removed.

In Latched OFF operation, the output remains switched OFF until ΔT falls below the reset threshold $\Delta T_{PLIMreset}$ and a read and clear command is sent.

Each time a channel is switched on via the corresponding bit in SOCR, a blanking time $t_{blanking}$ is initialized which masks a power limitation event and its relevant diagnostic in the PWLMFLTR register. The blanking time does not account for an over temperature event, i.e. the outputs are switched OFF and the relevant bits in OTFLTR are set even during the blanking time, or for an over load event.

The blanking filter is only active, if the channel is turned on through SOCR. There are, however, additional conditions which cause the output to switch from OFF to steady ON-state or to PWM output which do not activate the blanking filter. Refer to *Table 6* for more details.

Table 6. Activation of blanking filter in case of power limitation

Action	Output state	Blanking filter
SOCR = 0 to 1	Switches from off to steady state or PWM according to PWMCR	Active
SOCR = 0 DIEN = 1 INX = 0 to 1	Switches from off to steady state or PWM according to PWMCR	Not active
SOCR = 1, DIEN = 0 PWMCR = 1 DUTYCRX = 00h to nonzero value	Switches from off to PWM	Not active
SOCR = 1, DIEN = 0 PWMCR = 1 to 0 DUTYCRX = 00h	Switches from off to steady state	Not active

Over load

During low duty cycle PWM operation on a shorted load, ON-time may be too short to allow power limitation or over temperature detection. Current sense output is 0. This would make detection of this over load condition impossible. To overcome this, always when an output channel is turned OFF, the voltage drop on the PowerMOS (V_{DS}) is measured. If V_{DS} exceeds the threshold V_{DSmax}, an over load condition is detected. The corresponding bit in the over load status register OVLFLTR (address 34H) is set. Consequently, the over load bit (bit 4) in the Global Status Byte and the Global Error Flag are set.

The OVLFLTR is a warning and the channel can be switched on again even if the OVLFLTRX bit is set. The OVLFLTRX bit remains unchanged until a read and clear command on OVLFLTR is sent by the SPI or until the output is turned off the next time, when V_{DS} is evaluated again.

If the output channel is switched ON for a very short time, V_{DS} might be greater than V_{DSmax} even if the output is not in over load state so that a false warning is issued. Please refer to *Table 37* for more details.

2.2.4 Open-load ON-state detection

If the current through the output during the ON-state falls below the open-load ON-state detection thresholds, an open-load condition is detected for the relevant channel. The corresponding bit in the open-load ON-state status register (OLFLTR) is set. At the same time, the open-load at ON-state bit (bit 2) in the Global Status Byte and the Global Error Flag are set.

Two different open-load ON-state detection thresholds (see *Table 7*) can be set for each channel by writing into OLONCR register (address 06H). For channel related information, bit0 corresponds to channel0, bit1 to channel1, bit2 to channel2, bit3 to channel3.

Table 7. Nominal open-load thresholds

Channel	OLONCRX	I_{OLnom} BULB mode	I_{OLnom} LED mode
0, 1	0	75 mA	19 mA
	1	470 mA	160 mA
2, 3	0	180 mA	—
	1	1250 mA	—

2.2.5 Open-load OFF-state detection

If the output voltage V_{OUT} in OFF-state of the output is greater than the open-load detection threshold voltage V_{OL}, an open-load OFF-state / Stuck to V_{CC} event is detected (see *Figure 8*). The corresponding bit in the Open-load OFF-state / Stuck to VCC status register STKFLTR (Address 32h) is set. Consequently, the OLOFF bit (bit 1) in the Global Status Register and the Global Error Flag are set. To avoid false detection, the diagnosis starts after turn-off of a channel with an additional delay t_{DOLOFF}.

To distinguish between an open-load OFF-state event and a short to VCC condition, an internal pull-up current generator can be enabled for each channel by setting the corresponding bit in the open-load OFF-state control register (OLOFFCR, address 07h), see *Table 8*.

The activated pull-up current generators are active in Normal Mode, in Fail Safe Mode and in Standby Mode. In Sleep Mode 2, the current generators are switched off. The register contents, however, are saved also in Sleep Mode 2, consequently the current generators are reactivated after a return to Standby or a wakeup to Fail Safe Mode. A hardware reset ($V_{DD} < V_{DDR}$) or a software reset (Command byte = FFh) clears all register contents and hence the current generators are switched off.

Figure 8. Open-load OFF-state detection

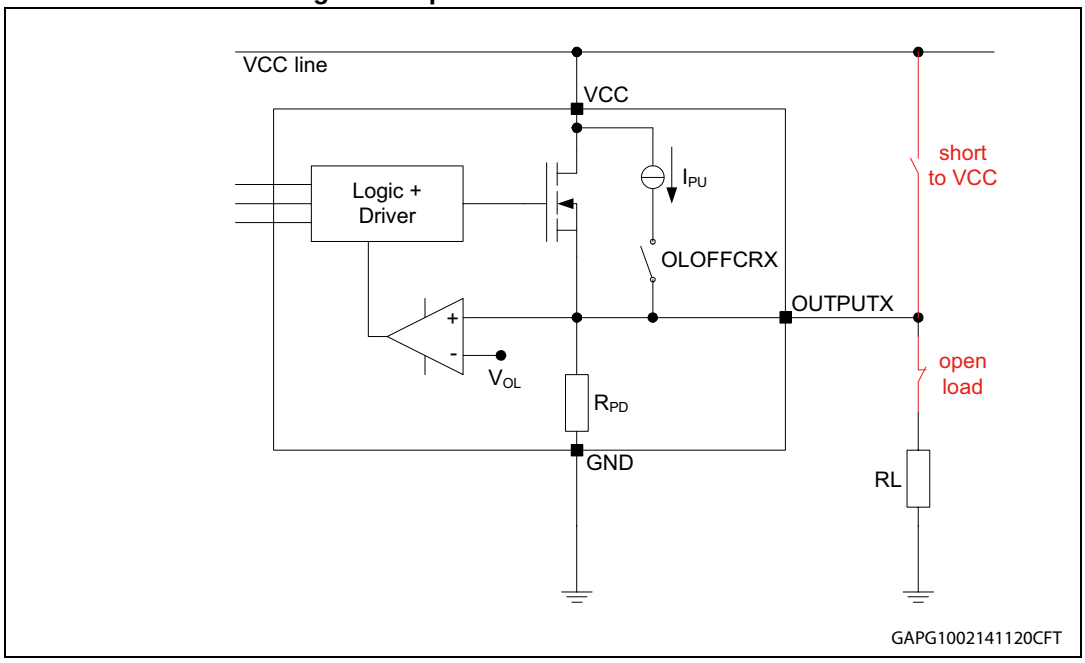


Table 8. STKFLTR state

	With internal pull-up generator	Without internal pull-up generator
Case 1: load connected	“0” / no fault	“0” / no fault
Case 2: no load	“1” / fault	“0” / no fault
Case 3: output shorted to V_{CC}	“1” / fault	“1” / fault

2.2.6 Current sense

Each channel integrates an analog current sense function which can be connected to the current sense pin by setting the CURSEN bit (bit 3) in the CTLR register (address 00H) and by setting the corresponding channel in the CSMUXCR register (address 03H).

The ratio between output current and sense current can be also selected by writing into the CSRATCR register (address 04H).

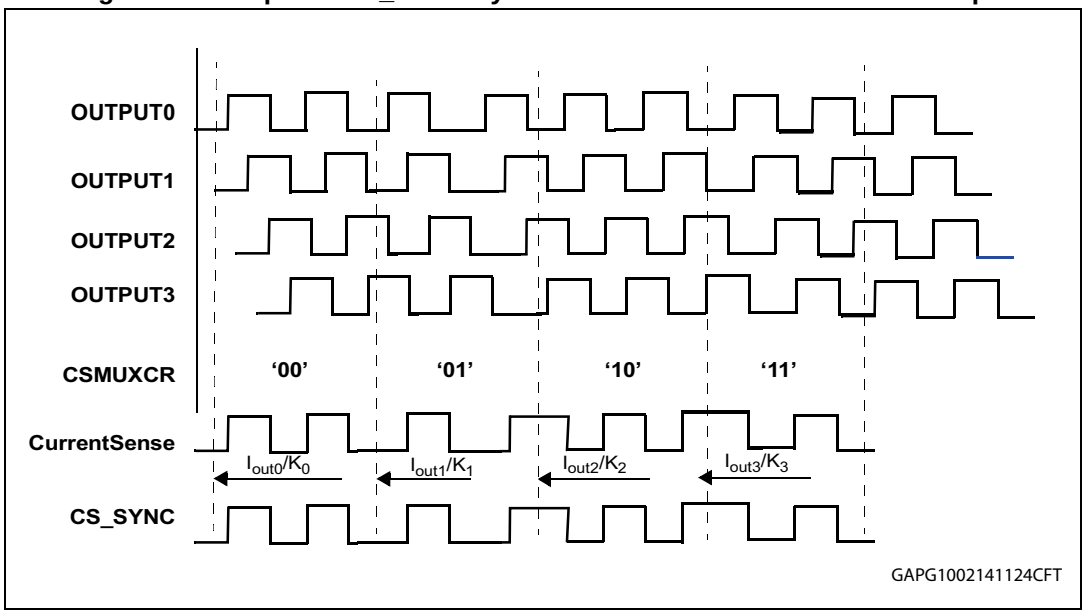
The current sense ratio is as shown in *Table 9*.

Table 9. Current sense ratio

Channel	CSRATCRX	Current sense ratio K (typical) BULB mode	Current sense ratio K (typical) LED mode
0, 1	0	2080	700
	1	5360	1900
2, 3	0	5800	—
	1	15250	—

The output CS_SYNC provides a synchronization signal for the current sense pin. It is “1” if the corresponding output is ON, and “0” if the output is OFF. If no output is selected (CURSEN = 0), CS_SYNC is in high impedance state. Please refer also to *Figure 9*.

Figure 9. Example of CS_SYNC synchronization and the current sense pin



2.3 Test mode (reserved)

The Digital core and most of the advanced functionalities integrated in the VNQ6004SA-E are tested by setting the device in a special Test Mode. In this state, the CSN monitoring timeout control is disabled and the functionality of the other SPI pins (SDI and SDO) might be different from the standardized communication protocol, whilst other pins might be configured as diagnostic I/O's.

Test Mode is intended only for the ST serial production testing flow.

Accessing Test Mode in the application might lead the device to operate in uncontrolled conditions.

Entering Test Mode is prevented by operating the device within its Absolute Maximum Ratings.

3 SPI functional description

3.1 SPI communication

The SPI communication is based on a standard ST-SPI 16-bit interface, using CSN, SDI, SDO and SCK signal lines.

Input data are shifted into SDI, MSB first while Output data are shifted out on SDO, MSB first.

3.1.1 Signal description

During all operations, V_{DD} must be held stable and within the specified valid range: V_{DD} min. to V_{DD} max.

Table 10. SPI signal description

Name	Function
Serial clock SCK	This input signal provides the timing of the serial interface. Data present at Serial Data Input (SDI) are latched on the rising edge of Serial Clock (SCK). Data on Serial Data Output (SDO) change after the falling edge of Serial Clock (SCK).
Serial data input SDI	This input signal is used to transfer data serially into the device. It receives data to be written. Values are sampled on the rising edge of Serial Clock (SCK).
Serial data output SDO	This output signal is used to transfer data serially out of the device. Data are shifted out on the falling edge of Serial Clock (SCK).
Chip select CSN	When this input signal is High, the device is deselected and Serial Data Output (SDO) is high impedance. Driving this input Low enables the communication. The communication must start on a Low level of Serial Clock (SCK). Data are accepted only if exactly 16 bits have been shifted in. This signal is used as CSN monitoring input and must be toggled within CSN monitoring timeout period to stay in Normal mode. Otherwise the device enters Fail Safe mode. SPI registers contents are unchanged.

3.1.2 Connecting to the SPI bus

A schematic view of the architecture between the bus and devices can be seen in *Figure 10*.

All input data bytes are shifted into the device, MSB first. The Serial Data Input (SDI) is sampled on the first rising edge of the Serial Clock (SCK) after Chip Select (CSN) goes low.

All output data bytes are shifted out of the device on the falling edge of SCK, MSB first on the first falling edge of the Chip Select (CSN).

3.1.3 SPI mode

Supported SPI mode during a communication phase can be seen in *Figure 11*.

This device can be driven by a micro controller with its SPI peripheral running in the following mode:

- CPOL=0, CPHA=0

Figure 10. Bus master and two devices in a normal configuration

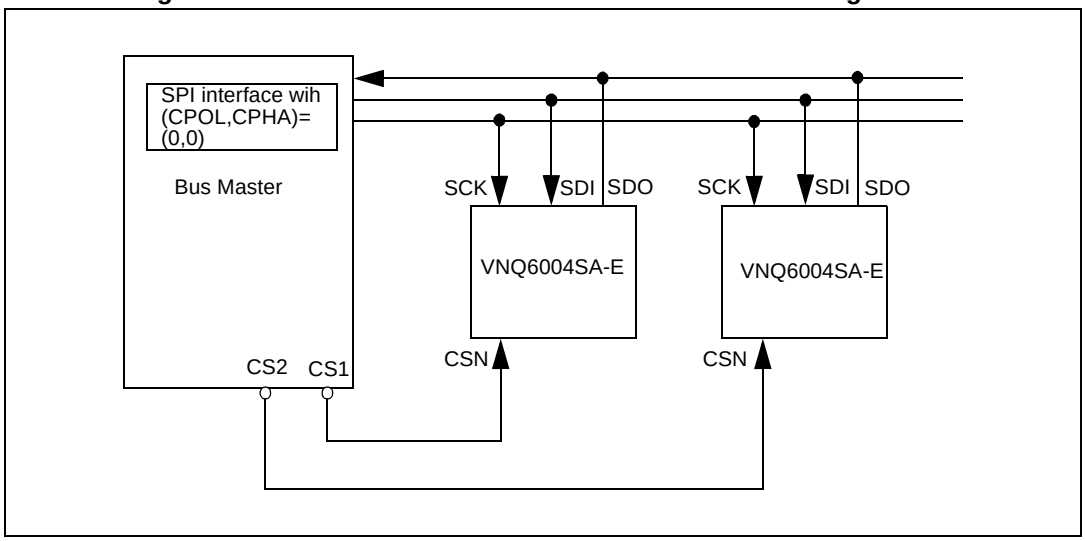
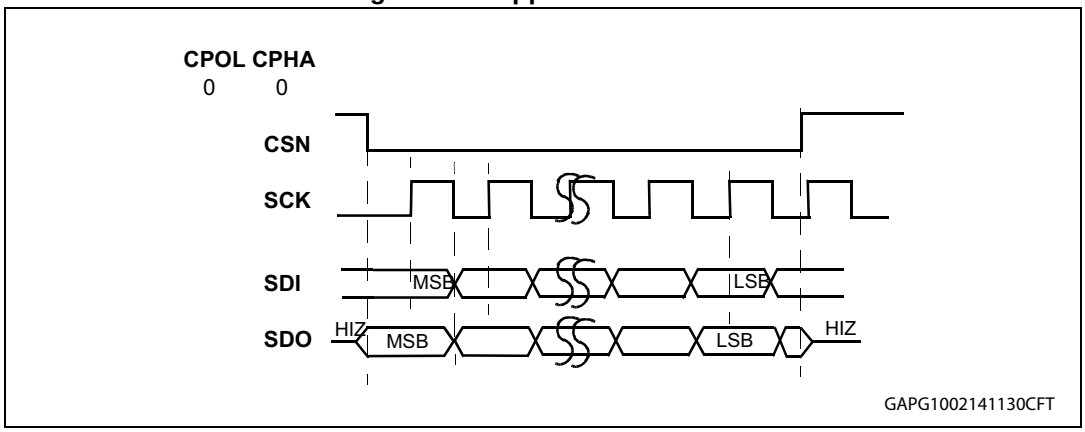


Figure 11. Supported SPI mode



3.2 SPI protocol

3.2.1 SDI, SDO format

SDI format during each communication frame starts with a command byte. It begins with two bits of operating code (OC0, OC1) which specify the type of operation (read, write, read and clear status, read device information) and is followed by a 6 bit address (A0:A5). The command byte is followed by an input data byte (D0:D7).

Table 11. Command byte

MSB							LSB
OC1	OC0	A5	A4	A3	A2	A1	A0

Table 12. Input data byte

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

SDO format during each communication frame starts with a specific byte called Global Status Byte (see *Section 3.2.2: Global status byte description* for more details of bit0-bit7). This byte is followed by an output data byte (D0:D7).

Table 13. Global status byte

MSB							LSB
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

Table 14. Output data byte

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

3.2.2 Global status byte description

The data shifted out on SDO during each communication starts with a specific byte called Global Status Byte. This one is used to inform the microcontroller about global faults which can be happened on the channel part (like thermal shutdown, OLON,...) or on the SPI interface (like CSN monitoring timeout event, communication error,...). This specific register has the following format.

Table 15. Global status byte

Bit	Name	Reset	Content
7 (MSB)	Global error flag	1	Active high: this bit is set in case of any fault on any channel or CSNTO, a communication error, a chip reset, a V_{CC} undervoltage or a too low PWM clock frequency. This bit is also accessible while CSN is held low and SCK is stable (high or low). This operation does not set the communication error bit.
6	Communication error	0	Active high: this bit is set at the end of the communication in case of wrong number of clock cycles during a communication frame or invalid bus condition (SPI mode not equal to CPOL = 0, CPHA = 0). A clock monitor counts the number of clock pulses during a communication frame (while CSN is low). If the number of pulses does not correspond with the frame width indicated in the 'SPI-frame_ID' (address 3Eh), the frame is ignored and the communication error bit is set.The communication error bit can be read in the frame which follows the erroneous one and is automatically cleared once a frame with valid number of clock pulses is transferred.

Table 15. Global status byte

Bit	Name	Reset	Content
5	Not (ChipReset or ComError)	0	Active low: this bit is low in case of chip reset (hardware reset due to a loss of V_{DD} supply or software reset) or a communication error (wrong number of clock pulses during a communication frame). The bit is reset when the next valid communication frame is transferred.
4	Thermal shutdown (OT) or Power limitation (PWLM) or Over load (OVL)	0	Active high: this bit is set in case of thermal shutdown or power limitation or in case of high V_{DS} (OVL) at turn-off detected on any channel. The bit reflects the corresponding faulty channel bits in OTFLTR, PWLMFLTR and OVLFLTR registers.
3	T_{Frame}	0	Active high: this bit is set if the case temperature is greater than T_{CSD} and can be used as a temperature prewarning.The bit is cleared automatically when the case temperature drops below the case temperature reset threshold (T_{CR}).
2	Open-load at ON-state (OLON)	0	Active high: this bit is set in case of open-load ON-state detected on any channel. This bit reflects the corresponding faulty channel bit in the OLFLTR register
1	Open-load at OFF-state or output shorted to V_{CC} (OLOFF)	0	Active high: this bit is set in case of open-load OFF-state or output shorted to V_{CC} condition detected on any channel. This bit reflects the corresponding faulty channel bit in the STKFLTR register.
0 (LSB)	FailSafe	1	Active high: This bit is set in case of failsafe mode.

Note: The FFh or 00h combinations for the Global Status Byte are not possible due to the active low of chip reset bit (bit 5) and the exclusive combination between bit 5 and 6. Consequently a FFh or 00h combination for the Global Status Byte must be detected by the microcontroller as a failure (SDO stuck to GND or to V_{DD} or loss of SCK).

3.2.3 Operating code definition

The SPI interface features four different addressing modes which are listed in *Table 16*.

Table 16. Operating codes

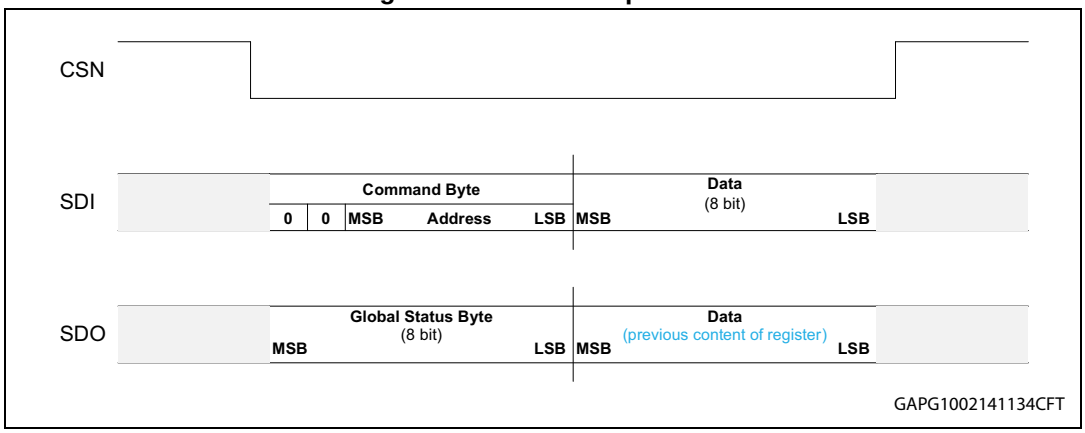
OC1	OC0	Meaning
0	0	Write operation
0	1	Read operation
1	0	Read and clear status operation
1	1	Read device information

Write mode

The write mode of the device allows to write the content of the input data byte into the addressed register (see list of registers in *Table 17*). Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

During the same sequence outgoing data are shifted out MSB first on the falling edge of the CSN pin and subsequent bits on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status Byte and the second to the previous content of the addressed register.

Figure 12. SPI write operation



Read mode

The read mode of the device allows to read and to check the state of any register.

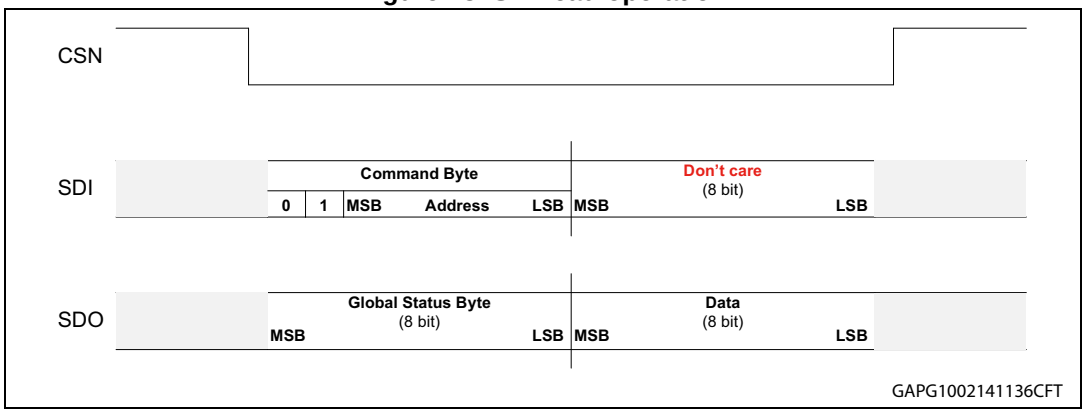
Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status Byte and the second to the content of the addressed register.

In case of a read mode on an unused address, the ‘global status/error’ byte on the SDO pin is following by 00H byte.

In order to avoid inconsistency between the Global status byte and the status register, the status register contents are frozen during SPI communication.

Figure 13. SPI read operation



Read and clear status command

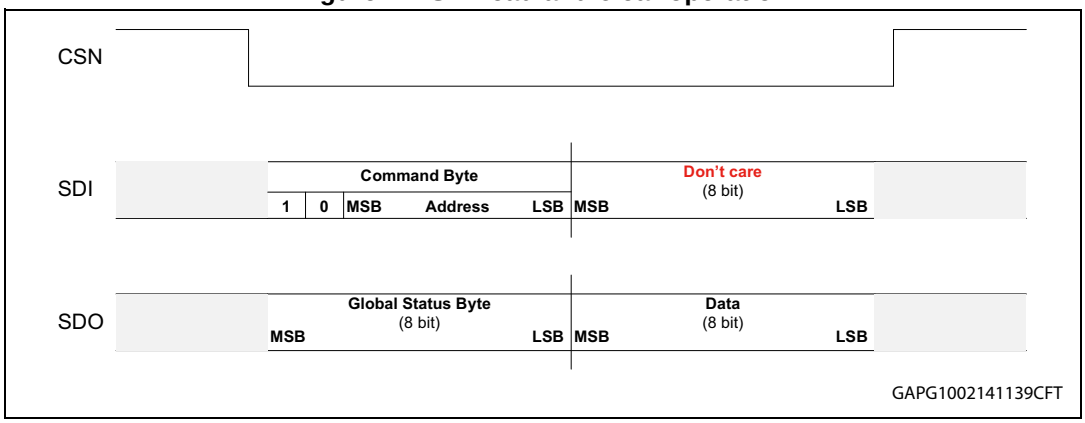
The read and clear status operation is used to clear the content of the addressed status register (see *Table 17*). A read and clear status operation with address 3Fh clears all status registers simultaneously and reads back the Configuration register (GLOBCTR).

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which register content is read then erased while the data byte is ‘don’t care’.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte and the second to the content of the addressed register.

In order to avoid inconsistency between the Global status byte and the status register, the status register contents are frozen during SPI communication.

Figure 14. SPI read and clear operation



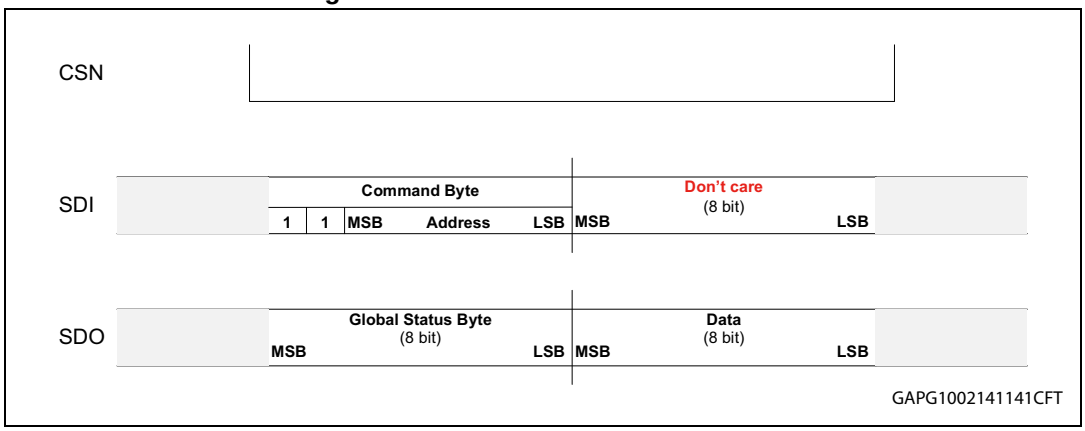
Read device information

Specific informations can be read but not modified during this mode. Accessible data can be seen in *Table 18*.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which information is read while the data byte is ‘don’t care’.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte and the second to the content of the addressed register.

Figure 15. SPI read device information



3.3 Address mapping

Table 17. RAM memory map

Address	Name	Access	Content
Control registers			
00h	CTRL	Read/write	Device enable, standby, current sense
01h	SOCR	Read/write	SPI Output Control Register
02h	DIENCR	Read/write	Direct Input Enable Control Register
03h	CSMUXCR	Read/write	Current Sense Multiplexer Control Register
04h	CSRATCR	Read/write	Current Sense Ratio Control Register
05h	PWMCR	Read/write	PWM Mode Control Register
06h	OLONCR	Read/write	Open-load ON-state Control Register
07h	OLOFFCR	Read/write	Open-load OFF-state Control Register
08h	ASDTCR	Read/write	Automatic Shutdown Control Register
09h	CCR	Read/write	Channel Control Register
0Ah-0Fh			not used
10h	DUTYC0CR	Read/write	Duty Cycle Control Register 0
11h	DUTYC1CR	Read/write	Duty Cycle Control Register 2
12h	DUTYC2CR	Read/write	Duty Cycle Control Register 2
13h	DUTYC3CR	Read/write	Duty Cycle Control Register 3
14h-17h			not used
18h	PHASE0CR	Read/write	Phase Control Register 0
19h	PHASE1CR	Read/write	Phase Control Register 1
1Ah	PHASE2CR	Read/write	Phase Control Register 2
1Bh	PHASE3CR	Read/write	Phase Control Register 3

Table 17. RAM memory map

Address	Name	Access	Content
1Ch-2Dh			not used
Status registers			
2Eh	CHDRVR	Read only	Channel Read Back Status Register
2Fh	GENSTR	Read only	General Status Register
30h	OTFLTR	Read/clear	Over Temperature Status Register
31h	OLFLTR	Read/clear	Open-load ON-state Status Register
32h	STKFLTR	Read/clear	Open-load OFF-state/Stuck to Vcc Status Register
33h	PWLMFLTR	Read/clear	Power Limitation Status Register
34h	OVLFLTR	Read/clear	Over load Status Register
35h-3Dh			not used
Other registers			
3Eh	TEST	Read/write	Test Register (reserved)
3Fh	GLOBCTR	Read/write	Configuration Register

Note: 1 Any command (write, read or read and clear status) executed on a "not used" RAM register, i.e. a not assigned address, does not have any effect:
There is no change in the Global Status byte (no communication error, no error flag).
The data written to this address (2nd byte of SDI is ignored.
The data read from this address (2nd byte of SDO) contains 00, independent of what has been written previously to this address.

2 A write command on don't care bits of an assigned RAM register address does not have any effect:
There is no change on the Global Status byte.
The data written to the "don't care bits" is ignored.
The content of the "don't care bits" remains at "0" independent of the data written to these bits.

Table 18. ROM memory map

Address	Name	Access	Content
00h	ID Header	Read only	82h
01h	Version	Read only	02h
02h	Product Code 1	Read only	1ah
03h	Product Code 2	Read only	00h
3Eh	SPI-Frame ID	Read only	01h

3.3.1 Address 00h - Control Register (CTLR)

Table 19. Control register

<table>
<tr><th>Bit</th><th>Name</th><th>Access</th><th>Reset</th><th>Content</th></tr>
<tr><td>7</td><td></td><td></td><td>0</td><td>Reserved (not used): read as 0 and write to 0</td></tr>
<tr><td>6</td><td></td><td></td><td>0</td><td>Reserved (not used): read as 0 and write to 0</td></tr>
<tr><td>5</td><td>STBY</td><td>R/W</td><td>0</td><td>Enter Standby mode
1: Enter Standby mode
It is necessary to do 2 write accesses to enter standby:
1. Write UNLOCK = 1
2. Write STBY = 1 and EN = 0</td></tr>
<tr><td>4</td><td>UNLOCK</td><td>R/W</td><td>0</td><td>Unlock bit, has to be set before STBY or EN can be set to 1</td></tr>
<tr><td>3</td><td>CURSEN</td><td>R/W</td><td>0</td><td>Current sense enable
1: Current sense reading enabled
0: Current sense reading disabled</td></tr>
<tr><td>2</td><td>CTDTH1</td><td>R/W</td><td>0</td><td rowspan="2">Case thermal detection threshold
These bits allow to configure the case thermal detection of the device. Three temperature thresholds are available by programming these two bits.

<table><tr><th>CTDTH1</th><th>CTDTH0</th><th>Detection temperature</th></tr><tr><td>0</td><td>0</td><td>120 °C</td></tr><tr><td>0</td><td>1</td><td>130 °C</td></tr><tr><td>1</td><td>X</td><td>140 °C</td></tr></table></td></tr>
<tr><td>1</td><td>CTDTH0</td><td>R/W</td><td>0</td></tr>
<tr><td>0</td><td>EN</td><td>R/W</td><td>0</td><td>Enter Normal mode
1: Normal mode
0: Fail Safe mode
It is necessary to do 2 write accesses to enter Normal mode:
1. Write UNLOCK = 1
2. Write EN = 1</td></tr>
</table>

3.3.2 Address 01h - SPI Output Control Register (SOCR)

Table 20. SPI output control register

<table>
<tr><th>Bit</th><th>Name</th><th>Access</th><th>Reset</th><th>Content</th></tr>
<tr><td>7</td><td></td><td></td><td>0</td><td rowspan="4">Reserved (they have to be written to "0" and are read "0")</td></tr>
<tr><td>6</td><td></td><td></td><td>0</td></tr>
<tr><td>5</td><td></td><td></td><td>0</td></tr>
<tr><td>4</td><td></td><td></td><td>0</td></tr>
</table>

Table 20. SPI output control register

Bit	Name	Access	Reset	Content
3	SOCR3	R/W	0	The SOCR register controls the output drivers. The four bits correspond to the four output channels. 1: the corresponding output is enabled 0: the corresponding output is disabled
2	SOCR2	R/W	0	
1	SOCR1	R/W	0	
0	SOCR0	R/W	0	

3.3.3 Address 02h - Direct Input Enable Control Register (DIENCR)

Table 21. Direct enable control register

Bit	Name	Access	Reset	Content
7			0	Reserved (they have to be written to "0" and are read "0")
6			0	
5			0	
4			0	
3	DIENCR3	R/W	0	The DIENCR enables the control of the corresponding output channel by the direct input. 1: parallel input INX controls OUTPUTX 0: function disabled
2	DIENCR2	R/W	0	
1	DIENCR1	R/W	0	
0	DIENCR0	R/W	0	

3.3.4 Address 03h - Current Sense Multiplexer Control Register (CSMUXCR)

Table 22. Current sense multiplexer control register

Bit	Name	Access	Reset	Content
7			0	Reserved (they have to be written to "0" and are read "0")
6			0	
5			0	
4			0	
3			0	
2			0	

Table 22. Current sense multiplexer control register (continued)

<table>
<tr><th>Bit</th><th>Name</th><th>Access</th><th>Reset</th><th>Content</th></tr>
<tr><td>1</td><td>CSMUXCR1</td><td>R/W</td><td>0</td><td rowspan="2">The CSMUXCR selects which output channel is connected to the current sense pin.

<table><tr><th>CSMUXCR1</th><th>CSMUXCR0</th><th>Selected channel</th></tr><tr><td>0</td><td>0</td><td>OUTPUT0</td></tr><tr><td>0</td><td>1</td><td>OUTPUT1</td></tr><tr><td>1</td><td>0</td><td>OUTPUT2</td></tr><tr><td>1</td><td>1</td><td>OUTPUT3</td></tr></table></td></tr>
<tr><td>0</td><td>CSMUXCR0</td><td>R/W</td><td>0</td></tr>
</table>

3.3.5 Address 04h - Current Sense Ratio Control Register (CSRATCR)

Table 23. Current sense ratio control register

Bit	Name	Access	Reset	Content
7			0	Reserved (they have to be written to "0" and are read "0")
6			0	
5			0	
4			0	
3	CSRATCR3	R/W	0	The CSRATCR adjusts the current sense ratio for the the corresponding output channel. 1: select high current sense ratio for OUTPUTX 0: select low current sense ratio for OUTPUTX For details see *Table 9*.
2	CSRATCR2	R/W	0	
1	CSRATCR1	R/W	0	
0	CSRATCR0	R/W	0	

3.3.6 Address 05h - PWM Mode Control Register (PWMCR)

Table 24. PWM mode control register

Bit	Name	Access	Reset	Content
7			0	Reserved (they have to be written to "0" and are read "0")
6			0	
5			0	
4			0	
3	PWMCR3	R/W	0	The PWMCR selects the PWM mode for each corresponding output channel. 1: PWM mode enabled for OUTPUTX 0: PWM mode disabled
2	PWMCR2	R/W	0	
1	PWMCR1	R/W	0	
0	PWMCR0	R/W	0	

3.3.7 Address 06h - Open-load ON-State Control Register (OLONCR)

Table 25. Open-load ON-state control register

Bit	Name	Access	Reset	Content
7			0	Reserved (they have to be written to "0" and are read "0")
6			0	
5			0	
4			0	
3	OLONCR3	R/W	0	The OLONCR selects the open-load threshold for each corresponding output channel. 1: High threshold selected for OUTPUTX 0: Low threshold selected for OUTPUTX For details see *Table 7*.
2	OLONCR2	R/W	0	
1	OLONCR1	R/W	0	
0	OLONCR0	R/W	0	

3.3.8 Address 07h - Open-load OFF-State Control Register (OLOFFCR)

Table 26. Open-load OFF-state control register

Bit	Name	Access	Reset	Content
7			0	Reserved (they have to be written to “0” and are read “0”)
6			0	
5			0	
4			0	
3	OLOFFCR3	R/W	0	The OLOFFCR enables an internal pull-up current generator to distinguish between the open-load OFF-state fault from the output shorted to V_{CC} fault. 1: Pull-up current generator enabled for OUTPUTX 0: Pull-up current generator disabled for OUTPUTX See *Table 8* for details.
2	OLOFFCR2	R/W	0	
1	OLOFFCR1	R/W	0	
0	OLOFFCR0	R/W	0	

3.3.9 Address 08h - Automatic Shutdown Control Register (ASDTCR)

Table 27. Automatic shutdown control register

Bit	Name	Access	Reset	Content
7			0	Reserved (they have to be written to “0” and are read “0”)
6			0	
5			0	
4			0	

Table 27. Automatic shutdown control register

Bit	Name	Access	Reset	Content
3	ASDTCR3	R/W	0	The ASDTCR selects the autorestart mode after over temperature or power limitation for the corresponding output. 1: Autorestart mode enabled for OUTPUTX 0: Latched OFF-state enabled for OUTPUTX In latched OFF-state the fault has to be cleared to re-enable the output channel after an over temperature or power limitation event.
2	ASDTCR2	R/W	0	
1	ASDTCR1	R/W	0	
0	ASDTCR0	R/W	0	

3.3.10 Address 09h - Channel Control Register (CCR)

Table 28. Channel control register

Bit	Name	Access	Reset	Content
7			0	Reserved (they have to be written to "0" and are read "0")
6			0	
5			0	
4			0	
3			0	
2			0	
1	CCR1	R/W	0	The CCR selects the BULB or LED mode for the corresponding output. 1: LED mode selected for OUTPUTX 0: BULB mode selected for OUTPUTX
0	CCR0	R/W	0	

3.3.11 Address 10h - 13h - Duty Cycle Control Register (DUTYXCR)

There are four Duty Cycle Control Registers, one for each output channel:

- Address 10h - Duty Cycle Control Register for channel 0 (DUTY0CR)
- Address 11h - Duty Cycle Control Register for channel 1 (DUTY1CR)
- Address 12h - Duty Cycle Control Register for channel 2 (DUTY2CR)
- Address 13h - Duty Cycle Control Register for channel 3 (DUTY3CR)

Table 29. DUTYCXCR - duty cycle control register

Bit	Name	Access	Reset	Content						
7	DUTYXCR7	R/W	0	0	0	0	...	...	1	1
6	DUTYXCR6	R/W	0	0	0	0	...	...	1	1
5	DUTYXCR5	R/W	0	0	0	0	...	...	1	1
4	DUTYXCR4	R/W	0	0	0	0	...	...	1	1
3	DUTYXCR3	R/W	0	0	0	0	...	...	1	1
2	DUTYXCR2	R/W	0	0	0	0	...	...	1	1
1	DUTYXCR1	R/W	0	0	0	1	...	...	1	1

Table 29. DUTYCXCR - duty cycle control register (continued)

Bit	Name	Access	Reset	Content						
0	DUTYXCR0	R/W	0	0	1	0	...	...	0	1
Resulting Duty Cycle				$\frac{0}{256}$	$\frac{1}{256}$	$\frac{2}{256}$	...	...	$\frac{254}{256}$	$\frac{255}{256}$

3.3.12 Address 18h - 1Ah - Phase Control Register (PHASEXCR)

There are four Phase Control Registers, one for each output channel:

- Address 18h - Phase Control Register of Channel 0 (PHASE0CR)
- Address 19h - Phase Control Register of Channel 1 (PHASE1CR)
- Address 1Ah - Phase Control Register of Channel 2 (PHASE2CR)
- Address 1Bh - Phase Control Register of Channel 3 (PHASE3CR)

Table 30. PHASECXCR - duty cycle control register

Bit	Name	Access	Reset	Content						
7	PHASEXCR4	R/W	0	0	0	0	...	...	1	1
6	PHASEXCR3	R/W	0	0	0	0	...	...	1	1
5	PHASEXCR2	R/W	0	0	0	0	...	...	1	1
4	PHASEXCR1	R/W	0	0	0	1	...	...	1	1
3	PHASEXCR0	R/W	0	0	1	0	...	...	0	1
2			0	Reserved (not used): read as 0 and write to 0						
1			0	Reserved (not used): read as 0 and write to 0						
0			0	Reserved (not used): read as 0 and write to 0						
Resulting Phase				$\frac{0}{32}$	$\frac{1}{32}$	$\frac{2}{32}$	...	...	$\frac{30}{32}$	$\frac{31}{32}$

3.3.13 Address 2Eh - Channel Read Back Status Register (CHDRVR)

Table 31. Channel read back status register

Bit	Name	Access	Reset	Content
7			0	Reserved
6			0	
5			0	
4			0	
3	CHRBSR3	R	0	The CHDRVR allows to read back the actual state of each channel. 1: channel OUTPUTX is on 0: channel OUTPUTX is off
2	CHRBSR2	R	0	
1	CHRBSR1	R	0	
0	CHRBSR0	R	0	

3.3.14 Address 2Fh - General Status Register (GENSTR)

Table 32. General status register

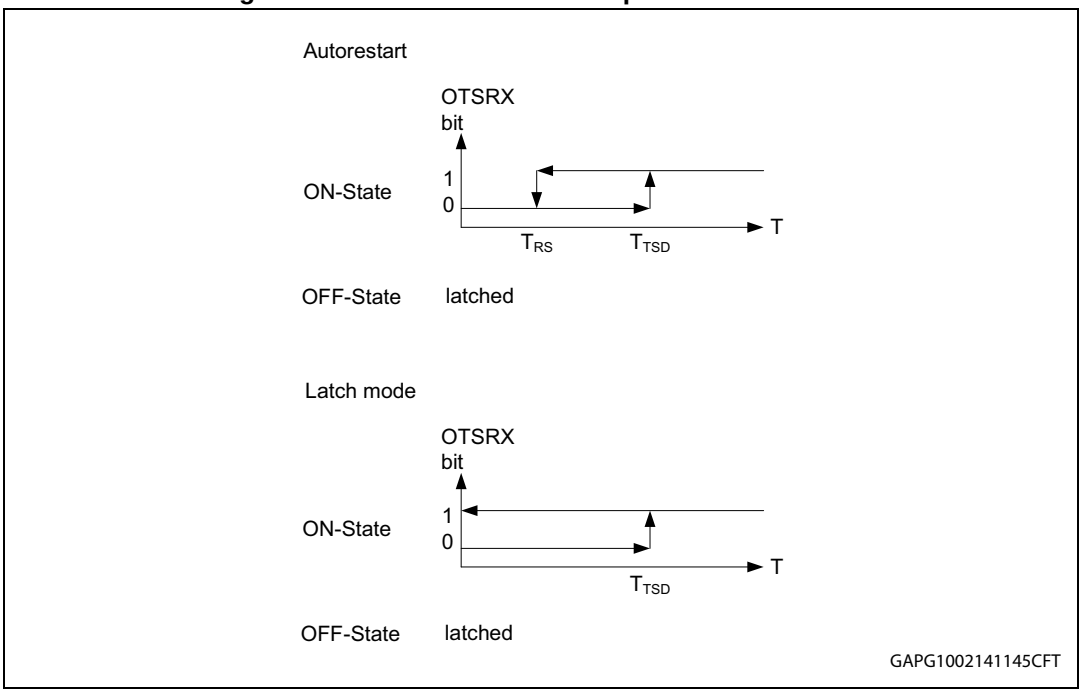
Bit	Name	Access	Reset	Content
7			0	Reserved
6			0	
5			0	
4			0	
3			0	
2	PWMLOW	R	0	This bit is set if the input PWM clock frequency is below 11.0 kHz (typ.) and reset if this frequency is above 16.0 kHz (typ.). If the PWMLOW bit is set, the PWM frequency is generated by an internal PWM clock signal at 160 Hz for channels programmed in BULB mode and 320 Hz for channels programmed in LED mode. The PWMLOW bit sets the global error flag.
1	CSNTO	R	0	The CSNTO bit is toggled at each half period of the CSN Timeout period and it is reset at the CSN rising edge.
0	VCCUV	R	0	V_{CC} undervoltage detection, is set when $V_{CC} < V_{USD}$ and it is automatically cleared as soon as $V_{CC} > V_{USD} + V_{USDhyst}$. This bit sets the Global Error Flag.

3.3.15 Address 30h - Over Temperature Status Register (OTFLTR)

Table 33. Over temperature status register

Bit	Name	Access	Reset	Content
7			0	Reserved
6			0	
5			0	
4			0	
3	OTSR3	R/C	0	The OTSR reflects the thermal state of the corresponding channel OUTPUTX. According to Autorestart or to Latch the bit is kept or removed as shown in *Figure 16*. In Autorestart the bit is latched during OFF-state of the channel in order to allow asynchronous diagnostic and it is automatically cleared when the OT condition is removed. In Latch the bit is latched until a read and clear command is sent. 1: thermal shutdown occured for OUTPUTX 0: no fault detected
2	OTSR2	R/C	0	
1	OTSR1	R/C	0	
0	OTSR0	R/C	0	

Figure 16. Behaviour of overtemperature status bits



3.3.16 Address 31h - Open-Load ON-State Status Register (OLFLTR)

Table 34. Open-load ON-state status register

Bit	Name	Access	Reset	Content
7			0	Reserved
6			0	
5			0	
4			0	
3	OLONSR3	R/C	0	The OLONSRX is set if an open-load event in ON-state has occured on the corresponding channel OUTPUTX. The bit is continuously refreshed in ON-state and latched in OFF-state. In order to clear the bit in OFF-state it is necessary to send a read and clear command. 1: open-load in ON-state occured for OUTPUTX 0: no fault detected
2	OLONSR2	R/C	0	
1	OLONSR1	R/C	0	
0	OLONSR0	R/C	0	

3.3.17 Address 32h - Open-Load OFF-State / Stuck to V_{CC} Status Register (STKFLTR)

Table 35. Open-load OFF-state / stuck to V_{CC} status register

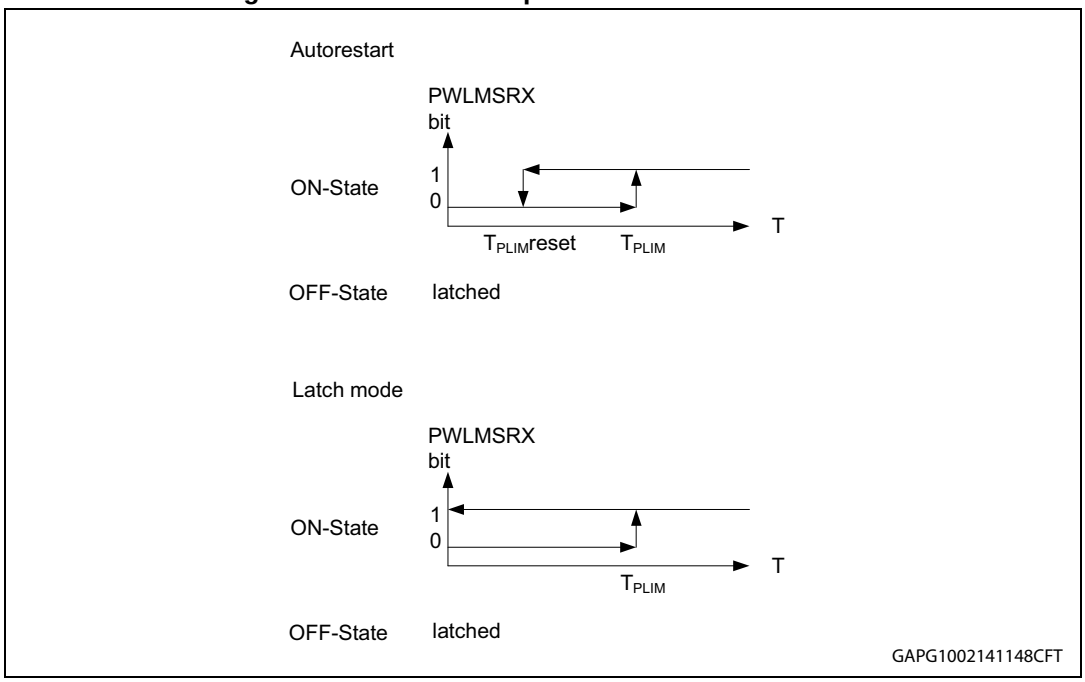
Bit	Name	Access	Reset	Content
7			0	Reserved
6			0	
5			0	
4			0	
3	STKSR3	R/C	0	The STKSRX bit is set in OFF-state after the T_{DOLOFF} is elapsed if $V_{OUT} > V_{OL}$. It gives an information about open-load or a stuck to V_{CC} which depends on the configuration of the OLOFFCR register (for details refer to the the functional description). The bit is continuously refreshed in OFF-state and it is latched during ON-state. In order to clear the bit in ON-state it is necessary to send a read and clear command. 1: open-load in OFF-state or stuck to V_{CC} condition occured for OUTPUTX 0: no fault detected
2	STKSR2	R/C	0	
1	STKSR1	R/C	0	
0	STKSR0	R/C	0	

3.3.18 Address 33h - Power Limitation Status Register (PWLMFLTR)

Table 36. Power limitation status register

Bit	Name	Access	Reset	Content
7			0	Reserved
6			0	
5			0	
4			0	
3	PWLMSR3	R/C	0	The PWLMSRX is set if a power limitation event has occured on the corresponding channel OUTPUTX. According to Autorestart or to Latch the bit is kept or removed as shown in *Figure 17*. In Autorestart the bit is latched during OFF-state of the channel in order to allow asynchronous diagnostic and it is automatically cleared when the PWLM condition is removed. In Latch the bit is latched until a read and clear command is sent. 1: power limitation event occured for OUTPUTX 0: no fault detected
2	PWLMSR2	R/C	0	
1	PWLMSR1	R/C	0	
0	PWLMSR0	R/C	0	

Figure 17. Behaviour of power limitation status bits



3.3.19 Address 34h - Over Load Status Register (OVLFLTR)

Table 37. Over load status register

Bit	Name	Access	Reset	Content
7			0	Reserved
6			0	
5			0	
4			0	
3	OVLSR3	R/C	0	The OVLSRX bit is set if at turn OFF of the channel OUTPUTX, the output voltage V_{OUT} is lower than V_{OVL}. The bit is latched until the next turn OFF. In order to clear the bit it is necessary to send a read and clear command. 1: over load event occured for OUTPUTX 0: no fault detected Note: As the status register is not updated while CSN is low, it is possible that the update of the OVLSR is delayed until the next turn-off if the PowerMOS is turned off during an SPI-frame.
2	OVLSR2	R/C	0	
1	OVLSR1	R/C	0	
0	OVLSR0	R/C	0	

3.3.20 Minimum duty cycle vs frequency

In order to avoid a false over load detection by the device a minimum duty cycle, DC, is requested for the correct operation. The minimum DC depends on the frequency as shown in *Figure 18* and *Figure 19*.

Figure 18. Min duty cycle vs frequency - BULB_MODE

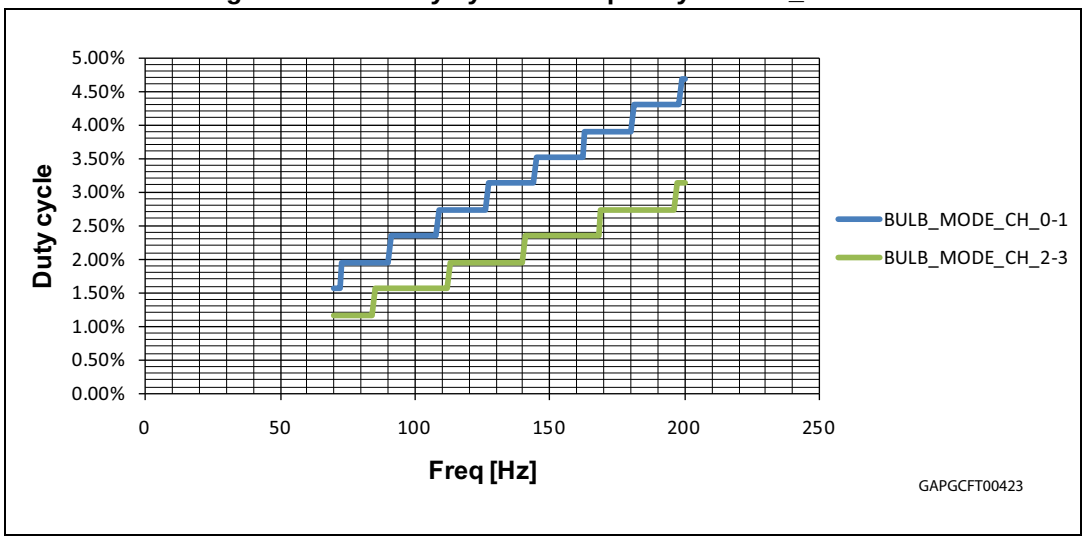
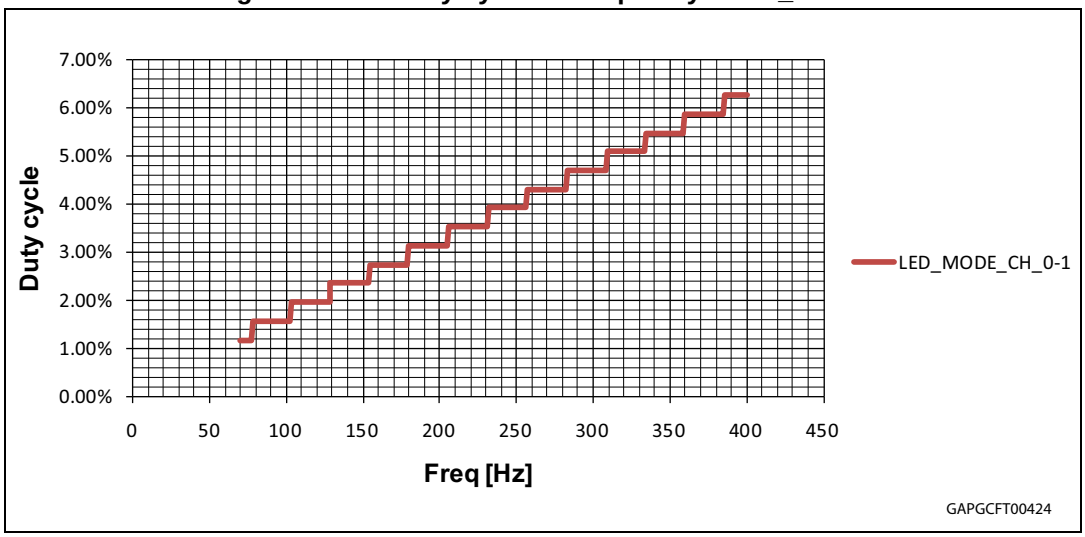


Figure 19. Min duty cycle vs frequency - LED_MODE



3.3.21 Address 3Eh - Test Register (TEST)

Table 38. Test register

Bit	Name	Access	Reset	Content
7			0	Reserved
6			0	
5			0	
4			0	
3			0	
2			0	
1			0	
0			0	

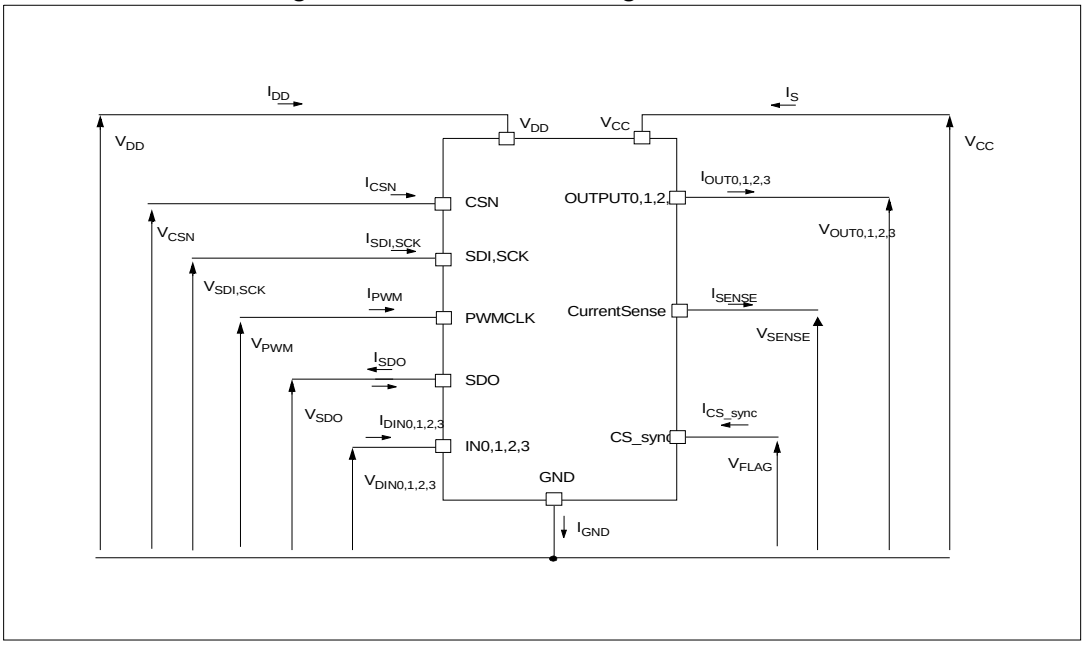
3.3.22 Address 3Fh - Configuration Register (GLOBCTR)

Table 39. Configuration register

Bit	Name	Access	Reset	Content
7			0	Reserved (they have to be written to "0" and are read "0")
6			0	
5			0	
4			0	
3	TFRAMEMASK	R/W	0	Masks the contribution of the TFRAME status bit in the Global Status Byte to the global error flag 1: TFRAME bit is masked 0: TFRAME bit not masked
2	OLONMASK	R/W	0	Masks the contribution of the OLON status bit in the Global Status byte to the global error flag. 1: OLON bit is masked 0: OLON bit not masked
1	OLOFFMASK	R/W	0	Masks the contribution of the OLOFF status bit in the Global Status byte to the global error flag. 1: OLOFF bit is masked 0: OLOFF bit not masked
0				Reserved (has to be written to "0" and is read "0")

4 Electrical specifications

Figure 20. Current and voltage conventions



4.1 Absolute maximum ratings

Stressing the device above the rating listed in the*Table 40: Absolute maximum ratings* may cause permanent damage to the device . These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 40. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	40	V
$-V_{CC}$	Reverse DC supply voltage	-40	V
$I_{OUT\ 0,1,2,3}$	Maximum DC output current	Internally limited	A
$-I_{OUT\ 0,1}$	Reverse DC output current	12	A
$-I_{OUT\ 2,3}$		27	A
I_{SENSE}	DC current sense input current	+10/-1	mA
$I_{SDI,CSN,SCK}$	DC SPI pin current	+10/-1	mA
V_{PWM}	DC PWMCLK pin voltage	11	V
V_{DD}	DC SPI supply voltage	7	V
$-V_{DD}$	Reverse DC SPI supply voltage	–0.3	V

Table 40. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
$I_{DIN\ 0,1}$	DC direct input current	+1/–1	mA
$I_{DIN\ 2,3}$		+10/–1	mA
V_{CS_sync}	DC CS_sync pin voltage	V_{DD} + 0.3	V
$-V_{CS_sync}$	Reverse DC CS_sync pin voltage	–0.3	V
V_{ESD}	Electrostatic discharge (R = 1.5 kΩ; C = 100 pF)	4000	V
	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	–40 to 150	°C
T_{STG}	Storage temperature	–55 to 150	°C
I_{LAT}	Latch up current	+/-20	mA

4.2 Thermal data

Table 41. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.6	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	See *Figure 29*	°C/W

4.3 Electrical characteristics

4.5 V < V_{DD} < 5.5 V, –40 °C < T_j < 150 °C, unless otherwise specified.

4.3.1 SPI

Table 42. DC characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD} pin						
V_{DDR}	Supply voltage reset			3.0	3.5	V
V_{DDSD}	Supply voltage shutdown		1.75	2.5		V
I_{DD}	Supply current ON-state	V_{DD} = 5 V		0.6	1	mA
I_{DDstd}	Supply current in standby state	V_{DD} = 5 V, T_j = 125 °C, INx = 0 V		5	20	µA
SDI, SCK, PWMCLK pins						
I_{IL}	Low level Input current	$V_{SDI,SCK,PWMCLK}$ = 0.3 V_{DD}	1			µA
I_{IH}	High level Input current	$V_{SDI,SCK,PWMCLK}$ = 0.7 V_{DD}			10	µA
V_{IL}	Input low voltage				0.3V_{DD}	V
V_{IH}	Input high voltage		0.7V_{DD}			V
V_{SDI_CL}	SDI pin clamp voltage	I_{IN} = 1 mA	5.5		7.5	V
		I_{IN} = –1 mA		–0.7		V
V_{SCK_CL}	SCK pin clamp voltage	I_{IN} = 1 mA	5.5		7.5	V
		I_{IN} = –1 mA		–0.7		V
SDO pin (–40 °C < T_j < 85 °C)						
V_{OL}	Output low voltage	I_{SDO} = 5 mA, CSN low, no fault condition			0.2V_{DD}	V
V_{OH}	Output high voltage	I_{SDO} = -5 mA, CSN low, fault condition	0.8V_{DD}			V
I_{LO}	Output leakage current	V_{SDO} = 0 V or V_{DD}, CSN high	–5		5	µA
CSN pin						
I_{IL_CSN}	Low level Input current	V_{CSN} = 0.3 V_{DD}	–10			µA
I_{IH_CSN}	High level Input current	V_{CSN} = 0.7 V_{DD}			-1	µA
V_{IL_CSN}	Output low voltage				0.3V_{DD}	V
V_{IH_CSN}	Output high voltage		0.7V_{DD}			V
V_{CSN_CL}	CSN pin clamp voltage	I_{IN} = 1 mA	5.5		7.5	V
		I_{IN} = –1 mA		–0.7		V

Table 43. AC characteristics (SDI, SCK, CSN, SDO, PWMCLK pins)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
C_{OUT}	Output capacitance (SDO)	V_{OUT} = 0 V to 5 V	—	—	10	pF
C_{IN}	Input capacitance (SDI)	V_{IN} = 0 V to 5 V	—	—	10	pF
	Input capacitance (other pins)	V_{IN} = 0 V to 5 V	—	—	10	pF

Table 44. Dynamic characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f_C	Clock frequency	Duty cycle = 50 %	0		4	MHz
f_{pwm}	PWM clock frequency	See (1)	20		200	kHz
t_{WHCH}	CSN monitoring timeout		30		70	ms
t_{SLCH}	CSN low setup time		120			ns
t_{SHCH}	CSN high setup time		1200			ns
t_{DVCH}	Data in setup time		20			ns
t_{CHDX}	Data in hold time		30			ns
t_{CH}	Clock high time		115			ns
t_{CL}	Clock low time		115			ns
t_{CLQV}	Clock low to output valid	C_{OUT} = 1 nF		150		ns
t_{QLQH}	Output rise time	C_{OUT} = 1 nF		110		ns
t_{QHQL}	Output fall time	C_{OUT} = 1 nF		110		ns
t_{WU}	Rising edge of V_{DD} to first allowed communication		3		23	µs
t_{stdby_out}	Minimum time during which CSN must be toggled low to go out of STDBY mode		20	55	100	µs
$t_{blanking}$	Blanking time of the power limitation protection		7.5		18	ms

1. Output PWM frequency is 1/512 * f_{pwm} in BULB mode and 1/256 * f_{pwm} in LED mode. If f_{pwm} is below minimum frequency, device falls back to an internal 83 kHz (typical) oscillator (160 Hz output PWM frequency in BULB mode and 320 Hz in LED mode)

Table 45. CS_sync pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CS_syncl}	Output low level Voltage	I_{CS_sync} = 1 mA, all channels OFF		—	$0.2V_{DD}$	V
V_{CS_synch}	Output high level voltage	I_{CS_sync} = –1 mA OUT0 ON, CSMUXCR=”01”	$0.8V_{DD}$	—		V

8 V < V_{CC} < 24 V; –40 °C < T_j < 150 °C, unless otherwise specified.

Table 46. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5	13	28	V
V_{USD}	Undervoltage shutdown			4	5	V
$V_{USDhyst}$	Under voltage shutdown hysteresis			0.25		V
V_{clamp}	V_{CC} clamp voltage	I_{CC} = 20 mA; $I_{OUT0,1,2,3}$ = 0 A	41	46	52	V
V_{clamp2}	Reverse V_{CC} clamp voltage	I_{CC} = -20 mA; $I_{OUT0,1,2,3}$ = 0 A	-52	-46	-41	V
I_S	Supply current	OFF-state; V_{CC} = 13 V; T_j = 25 °C; V_{DD} = 0 V		3	5	µA
		OFF-state; V_{CC} = 13 V; T_j = 25 °C; V_{DD} = 5 V standby mode; Direct input low		5	10	µA
		ON-state (all channels ON); V_{CC} = 13 V; V_{DD} = 5 V; I_{OUT} = 0 A		8.5	14	mA
$I_{L(off)}$	OFF-state output current	V_{DD} = 0 V; V_{CC} = 13 V; T_j = 25 °C	0		3	µA
		V_{DD} = 0 V; V_{CC} = 13 V; T_j = 125 °C	0		5	µA

Table 47. Logic inputs ($IN_{0,1,2,3}$ pins)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL0,1,2,3}$	Input low level voltage				0.8	V
$I_{IL0,1,2,3}$	Low level input current	V_{DIN} = 0.9 V	1			µA
$V_{IH0,1,2,3}$	Input high level voltage		2			V
$I_{IH0,1,2,3}$	High level input current	V_{DIN} = 2.1 V			10	µA
$V_{I(hyst)0,1,2,3}$	Input hysteresis voltage		0.2			V
$V_{ICL2,3}$	Input clamp voltage	I_{IN} = 1 mA	5.5		7.5	V
		I_{IN} = –1 mA		–0.7		V
$I_{ILIN0,1}$	Allowed input current for normal operation				1	mA
$V_{ICL0,1}$	Input clamp voltage	I_{IN} = 15 mA	11		15	V
		I_{IN} = –1 mA		–0.7		V

Table 48. Protection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔT_{PLIM}(1)	Junction-case temperature difference triggering power limitation protection	V_{CC} = 13 V		60		°C
ΔT_{PLIM}reset	Junction-case temperature difference resetting power limitation protection	V_{CC} = 13 V		35		°C
T_{TSD}	Shutdown temperature	V_{CC} = 13 V	150	175	200	°C
T_R	Reset temperature	V_{CC} = 13 V, latched off mode disabled	T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of OTFLTR fault detection	V_{CC} = 13 V, latched off mode disabled	135			°C
T_{HYST}	Thermal hysteresis ($T_{TSD} - T_R$)	V_{CC} = 13 V, latched off mode disabled		10		°C
T_{CSD}	Case thermal detection pre-warning	V_{CC} = 13 V (see *Table 19*)	T_{CSD} nom – 10	T_{CSD} nom	T_{CSD} nom +10	°C
T_{CR}	Case thermal detection reset	V_{CC} = 13 V		T_{CSD} nom-10		°C
V_{OVL}	Over load detection output voltage threshold (set bit OVLSRX in OVLFLTR register)			V_{CC} – 1.5		V

1. $Z_{thj\text{-}case}xP = \Delta T_{PLIM}$, $Z_{th\text{-}case}$ is the thermal impedance, P is the Power.

Table 49. Open-load detection (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load OFF-state voltage detection threshold	V_{IN} = 0 V		V_{CC} – 1.5		V
I_{PU}	Pull-up current generator for open-load at OFF-state detection	Pull-up current generator active, V_{out} = V_{CC} - 1.5 V	-1.3	-0.8	-0.3	mA
t_{DOLOFF}	Delay time after turn off to allow open-load OFF-state detection			1		ms

4.3.2 BULB mode

Table 50. BULB - power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{ON_ch0,1}$	ON-state resistance	I_{OUT} = 3 A; T_j = 25 °C	—	30		mΩ
		I_{OUT} = 3 A; T_j = 150 °C	—		60	mΩ
		I_{OUT} = 3 A; V_{CC} = 5 V; T_j = 25 °C	—		45	mΩ
$R_{ON\ REV_ch0,1}$	R_{DSON} in reverse battery condition	V_{CC} = -13 V; I_{OUT} = -3 A; T_j = 25 °C	—	30		mΩ
$R_{ON_ch2,3}$	ON-state resistance	I_{OUT} = 6 A; T_j = 25 °C	—	10		mΩ
		I_{OUT} = 6 A; T_j = 150 °C	—		20	mΩ
		I_{OUT} = 6 A; V_{CC} = 5 V; T_j = 25 °C	—		15	mΩ
$R_{ON\ REV_ch2,3}$	R_{DSON} in reverse battery condition	V_{CC} = -13 V; I_{OUT} = -6 A; T_j = 25 °C	—	10		mΩ

Table 51. BULB - switching (V_{CC} = 13 V channel 0,1,2,3)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{don}	Turn-on delay time $Ch_{0,1}$	from 50% CSN to 10% V_{OUT}(1) R_L = 4.3 Ω	—	90	—	µs
	Turn-on delay time $Ch_{2,3}$	from 50% CSN to 10% V_{OUT}(1) R_L = 2.2 Ω	—	45	—	µs
t_{doff}	Turn-off delay time $Ch_{0,1}$	from 50% CSN to 90% V_{OUT}(1) R_L = 4.3 Ω	—	90	—	µs
	Turn-off delay time $Ch_{2,3}$	from 50% CSN to 90% V_{OUT}(1) R_L = 2.2 Ω	—	70	—	µs
t_{skew}	Turn-off turn-on time $Ch_{0,1}$	from 50% CSN to 50% V_{OUT} R_L = 4.3 Ω	—	10	—	µs
	Turn-off turn-on time $Ch_{2,3}$	from 50% CSN to 50% V_{OUT} R_L = 2.2 Ω	—	25	—	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope $Ch_{0,1}$	from V_{OUT} = 1.3 V to 10.4 V(1) R_L = 4.3 Ω	—	0.3	—	V/µs
	Turn-on voltage slope $Ch_{2,3}$	from V_{OUT} = 1.3 V to 10.4 V(1) R_L=2.2Ω	—	0.4	—	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope $Ch_{0,1}$	from V_{OUT} = 11.7 V to 1.3 V(1) R_L = 4.3 Ω	—	0.2	—	V/µs
	Turn-off voltage slope $Ch_{2,3}$	from V_{OUT} = 11.7 V to 1.3 V(1) R_L = 2.2 Ω	—	0.2	—	V/µs
W_{ON}	Switching losses energy at turn-on $Ch_{0,1}$	R_L = 4.3 Ω	—	0.28	—	mJ
	Switching losses energy at turn-on $Ch_{2,3}$	R_L = 2.2 Ω	—	0.56	—	mJ

Table 51. BULB - switching (V_{CC} = 13 V channel 0,1,2,3) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
W_{OFF}	Switching losses energy at turn-off $Ch_{0,1}$	R_L = 4.3 Ω	—	0.33	—	mJ
	Switching losses energy at turn-off $Ch_{2,3}$	R_L = 2.2 Ω	—	0.63	—	mJ

1. See *Figure 22: Switching characteristics*.

Table 52. BULB - open-load detection (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Open-load ON-state detection threshold	V_{IN} = 5 V	30 % I_{OL} nom	I_{OL}(1) nom	170 % I_{OL} nom	mA

1. See *Table 7: Nominal open-load thresholds*.

Table 53. BULB - protection and diagnosis

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{limH_ch0,1}$	Short circuit current	V_{CC} = 13 V, V_{DD} = 0 V, $V_{IN0,1}$ = 5 V	25	35	55	A
		5 V < V_{CC} < 18 V			55	A
$I_{limL_ch0,1}$	Short circuit current during thermal cycling	V_{CC} = 13 V, V_{DD} = 0 V, $V_{IN0,1}$ = 5 V, $T_R < T_j < T_{TSD}$		11.5		A
$I_{limH_ch2,3}$	Short circuit current	V_{CC} = 13 V, V_{DD} = 0 V, $V_{IN2,3}$ = 5 V	55	80	120	A
		5 V < V_{CC} < 18 V			120	A
$I_{limL_ch2,3}$	Short circuit current during thermal cycling	V_{CC} = 13 V, V_{DD} = 0 V, $V_{IN2,3}$ = 5 V, $T_R < T_j < T_{TSD}$		26.5		A
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; $V_{IN0,1}$ = 0 V; L = 6 mH; 25 °C < T_J < 150 °C	V_{CC}–40	V_{CC}–44	V_{CC}–48	V
V_{ON}	Output voltage drop limitation	$Ch_{0,1}$ I_{OUT} = 0.15 A $Ch_{2,3}$ I_{OUT} = 0.5 A T_j = –40 °C to +150 °C		25		mV

Table 54. BULB - current sense (8 V < V_{CC} < 18 V, channel 0,1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.075 A; V_{SENSE} = 0.5 V; Logic [0] on bit bx in CSRATCR T_j = –40 °C T_j = 25 °C to 150 °C	 810 1090	 2180	 3470 3280	
dK_0/K_0	Current sense ratio drift	I_{OUT} = 0.075 A; V_{SENSE} = 0.5 V; Logic [0] on bit bx in CSRATCR T_j = –40 °C to +150 °C	–30		30	%

Table 54. BULB - current sense (8 V < V_{CC} < 18 V, channel 0,1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.6 A; V_{SENSE} = 0.5 V; Logic [0] on bit bx in CSRATCR T_j = –40 °C T_j = 25 °C to 150 °C	 1540 1550	 2080	 2630 2610	
dK_1/K_1	Current sense ratio drift	I_{OUT} = 0.6 A; V_{SENSE} = 0.5 V; Logic [0] on bit bx in CSRATCR T_j = –40 °C to +150 °C	–15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 3 A; V_{SENSE} = 4 V; Logic [1] on bit bx in CSRATCR T_j = –40 °C T_j = 25 °C to 150 °C	 4500 4710	 5360	 6230 6020	
dK_2/K_2	Current sense ratio drift	I_{OUT} = 3 A; V_{SENSE} = 4 V; Logic [1] on bit bx in CSRATCR T_j = –40 °C to +150 °C	–10		+10	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 4 V; Logic [1] on bit bx in CSRATCR T_j = –40 °C T_j = 25 °C to 150 °C	 4800 4940	 5340	 5880 5750	
dK_3/K_3	Current sense ratio drift	I_{OUT} = 6 A; V_{SENSE} = 4 V; Logic [1] on bit bx in CSRATCR T_j = –40 °C to +150 °C	–6		+6	%
I_{SENSE0}	Analog sense current	I_{OUT} = 0 A; V_{SENSE} = 0 V; Channel at OFF-state; T_j = –40 °C to +150 °C	0		1	µA
		Channel at ON-state; T_j = –40 °C to +150 °C	0		2	µA
$t_{DSENSE1H}$	Delay response time from rising edge of CS pin (turn-on of the channel)	V_{SENSE} < 4 V, R_{SENSE} = 2 KΩ I_{SENSE} = 90% of $I_{SENSE\ max}$ (see *Figure 21*)		70	250	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS pin (turn-off of the channel)	V_{SENSE} < 4 V, R_{SENSE} = 2 KΩ I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 21*)		5	20	µs

Table 55. BULB - current sense (8 V < V_{CC} < 18 V, channel 2,3)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.2 A; V_{SENSE} = 0.5 V; Logic [0] on bit bx in CSRATCR T_j = –40 °C T_j = 25 °C to 150 °C	 2020 2300	 5620	 8650 8650	
dK_0/K_0	Current sense ratio drift	I_{OUT} = 0.2 A; V_{SENSE} = 0.5 V; Logic [0] on bit bx in CSRATCR T_j = –40 °C to +150 °C	–30		+30	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1.2 A; V_{SENSE} = 0.5 V; Logic [0] on bit bx in CSRATCR T_j = –40 °C T_j = 25 °C to 150 °C	 3870 4000	 5800	 7500 7500	
dK_1/K_1	Current sense ratio drift	I_{OUT} = 1.2 A; V_{SENSE} = 0.5 V; Logic [0] on bit bx in CSRATCR T_j = –40 °C to +150 °C	–15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 4 V; Logic [1] on bit bx in CSRATCR T_j = –40 °C T_j = 25 °C to 150 °C	 12140 12810	 15250	 18610 17700	
dK_2/K_2	Current sense ratio drift	I_{OUT} = 6 A; V_{SENSE} = 4 V; Logic [1] on bit bx in CSRATCR T_j = –40 °C to +150 °C	–10		+10	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 12 A; V_{SENSE} = 4 V; Logic [1] on bit bx in CSRATCR T_j = –40 °C T_j = 25 °C to 150 °C	 13290 13660	 15100	 16920 16540	
dK_3/K_3	Current sense ratio drift	I_{OUT} = 12 A; V_{SENSE} = 4 V; Logic [1] on bit bx in CSRATCR T_j = –40 °C to 150 °C	–6		+6	%
I_{SENSE0}	Analog sense current	I_{OUT} = 0 A; V_{SENSE} = 0 V; Channel at OFF-state; T_j = –40 °C to +150 °C	0		1	µA
		Channel at ON-state; T_j = –40 °C to +150 °C	0		2	µA
$t_{DSENSE1H}$	Delay response time from rising edge of CS pin (turn-on of the channel)	V_{SENSE} < 4 V, R_{SENSE} = 2 KΩ I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 21*)		70	250	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS pin (turn-off of the channel)	V_{SENSE} < 4 V, R_{SENSE} = 2 KΩ I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 21*)		5	20	µs

4.3.3 LED mode (Channel 0, 1)

8 V < V_{CC} < 24 V; –40 °C < T_j < 150 °C, unless otherwise specified.

Table 56. LED - power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON} $Ch_{0,1}$	ON-state resistance	I_{OUT} = 1.3 A; T_j = 25 °C	—	90		mΩ
		I_{OUT} = 1.3 A; T_j = 150 °C	—		180	mΩ
		I_{OUT} = 1.3 A; V_{CC} = 5 V; T_j = 25 °C	—		135	mΩ

Table 57. LED - switching (V_{CC} = 13 V channel 0,1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{don}	Turn-on delay time	from 50 % CSN to 10 % V_{OUT}(1) R_L = 13 Ω	—	60	—	µs
t_{doff}	Turn-off delay time	from 50 % CSN to 90 % V_{OUT}(1) R_L = 13 Ω	—	40	—	µs
t_{skew}	Turn-off, turn-on time	from 50 % CSN to 50 % V_{OUT} R_L = 13 Ω	—	20	—	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	from V_{OUT} = 11.3 V to 10.4 V(1) R_L = 13 Ω	—	0.46	—	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	from V_{OUT} = 11.7 V to 1.3 V(1) R_L = 13 Ω	—	0.55	—	V/µs
W_{ON}	Switching losses energy at turn-on	R_L = 13 Ω	—	0.07	—	mJ
W_{OFF}	Switching losses energy at turn-off	R_L = 13 Ω	—	0.05	—	mJ

1. see *Figure 22: Switching characteristics*

Table 58. LED - open-load detection (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Open-load ON-state detection threshold	V_{IN} = 5 V	30 % I_{OL} nom	I_{OL}(1) nom	170 % I_{OL} nom	mA

1. See *Table 7: Nominal open-load thresholds*

Table 59. LED - protection and diagnosis

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{limH_ch0,1}$	Short circuit current	V_{CC} = 13 V, V_{DD} =0 V, $V_{IN0,1}$ = 5 V	7	12	18	A
		5 V < V_{CC} < 18 V			18	A

Table 59. LED - protection and diagnosis (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{limL_ch0,1}$	Short circuit current during thermal cycling	V_{CC} = 13 V, V_{DD} = 0 V, $V_{IN0,1}$ = 5 V, $T_R < T_j < T_{TSD}$		4		A
V_{ON}	Output voltage drop limitation	$Ch_{0,1}$ I_{OUT} = 0.05 A T_j = –40 °C to +150 °C		25		mV

Table 60. LED - current sense (8 V < V_{CC} < 18 V, channel 0,1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.025 A; V_{SENSE} = 0.5 V; Logic [0] on bit bx in CSRATCR T_j = –40 °C T_j = 25 °C to 150 °C	 290 340	 680	 1030 1030	
dK_0/K_0	Current sense ratio drift	I_{OUT} = 0.025 A; V_{SENSE} = 0.5 V; Logic [0] on bit bx in CSRATCR T_j = –40 °C to +150 °C	–30		30	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.2 A; V_{SENSE} = 0.5 V; Logic [0] on bit bx in CSRATCR T_j = –40 °C T_j = 25 °C to 150 °C	 500 510	 700	 900 890	
dK_1/K_1	Current sense ratio drift	I_{OUT}=0.2A; V_{SENSE}=0.5V; Logic [0] on bit bx in CSRATCR T_j = –40 °C to +150 °C	–15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 1 A V_{SENSE} = 4 V; Logic [1] on bit bx in CSRATCR T_j = –40 °C T_j = 25 °C to 150 °C	 1640 1680	 1900	 2180 2100	
dK_2/K_2	Current sense ratio drift	I_{OUT} = 1 A; V_{SENSE} = 4 V; Logic [1] on bit bx in CSRATCR T_j = –40 °C to +150 °C	–10		+10	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 2 A; V_{SENSE} = 4 V; Logic [1] on bit bx in CSRATCR T_j = –40 °C T_j = 25 °C to 150 °C	 1730 1760	 1890	 2070 2010	
dK_3/K_3	Current sense ratio drift	I_{OUT} = 2 A; V_{SENSE} = 4 V; Logic [1] on bit bx in CSRATCR T_j = –40 °C to +150 °C	–6		+6	%
I_{SENSE0}	Analog sense current	I_{OUT} = 0 A; V_{SENSE} = 0 V; Channel at OFF-state; T_j = –40 °C to +150 °C	0		1	µA
		Channel at ON-state; T_j = –40 °C to +150 °C	0		2	µA

Table 60. LED - current sense (8 V < V_{CC} < 18 V, channel 0,1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE1H}$	Delay response time from rising edge of CS pin (turn-on of the channel)	V_{SENSE} < 4 V, R_{SENSE} = 2 KΩ I_{SENSE} = 90 % of $I_{SENSE\ max}$ (see *Figure 21*)		50	180	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS pin (turn-off of the channel)	V_{SENSE} < 4 V, R_{SENSE} = 2 KΩ I_{SENSE} = 10 % of $I_{SENSE\ max}$ (see *Figure 21*)		5	20	µs

Figure 21. Current sense delay characteristics

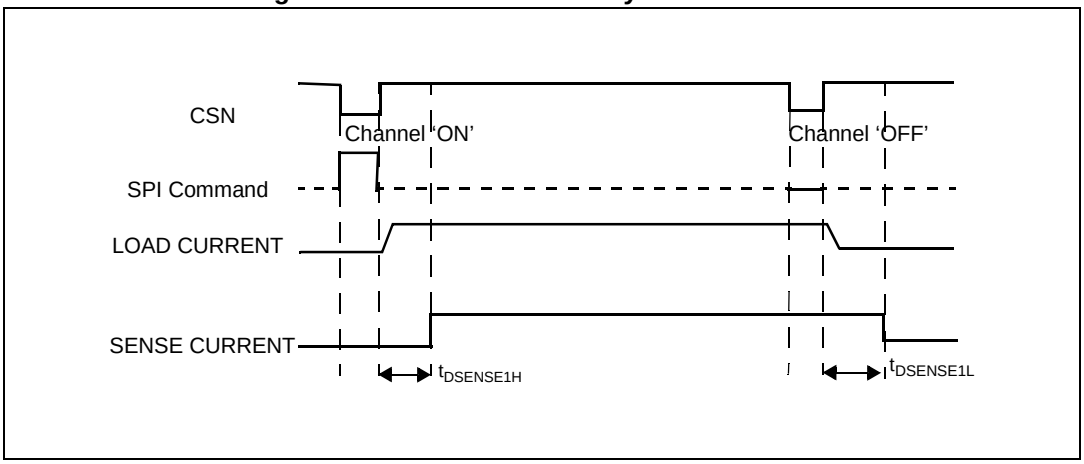


Figure 22. Switching characteristics

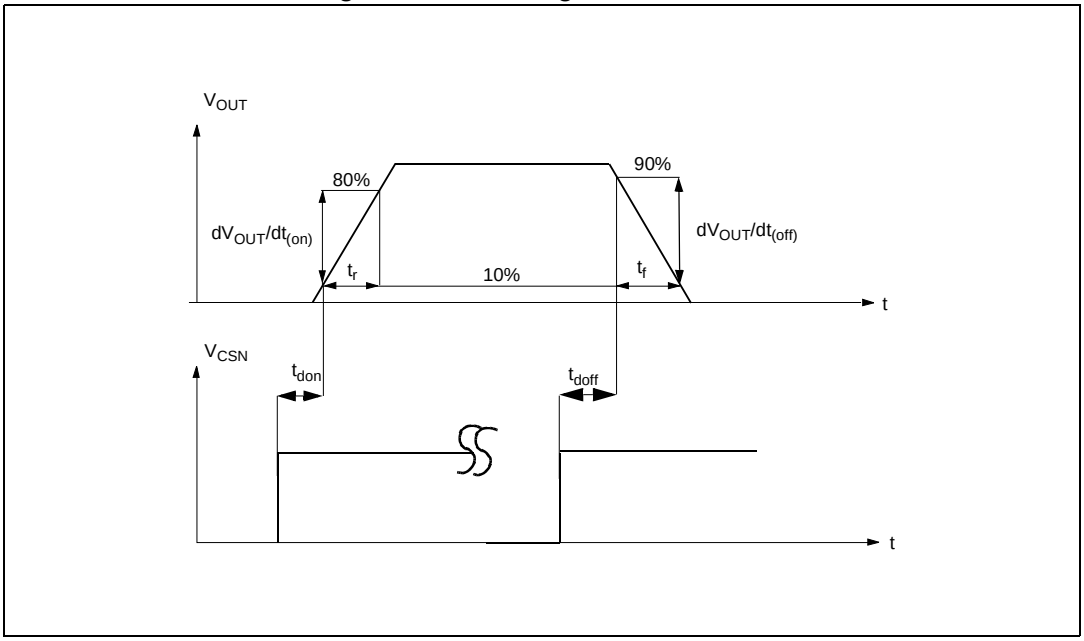


Table 61. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test Pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b(2)	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to V_{CC} = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 62. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) test pulse	Test level results(1) (2)	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b (3)	C	C

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. The above test levels are withstood with at least one output connected to its nominal resistive load.
3. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 63. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the

Figure 23. Application schematic (simplified)

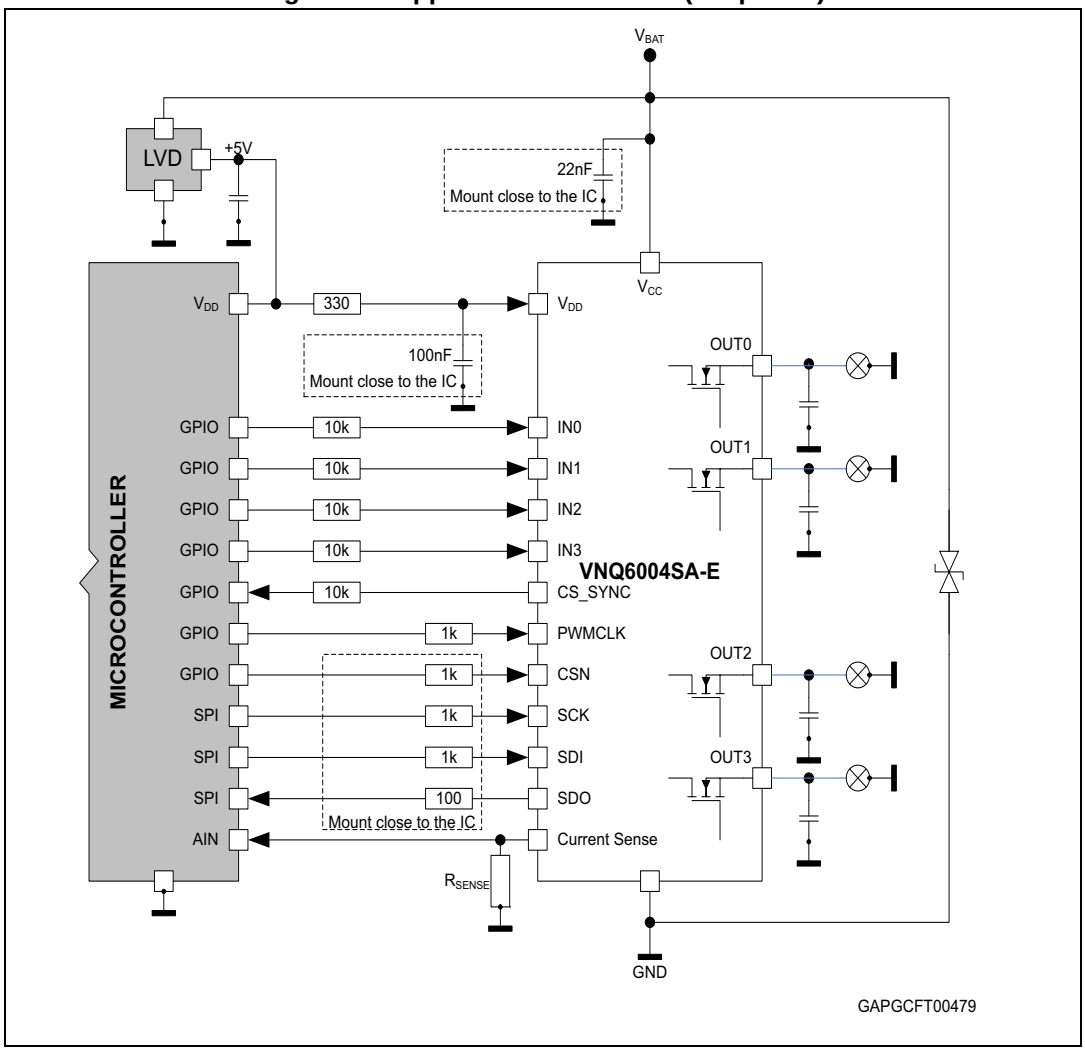
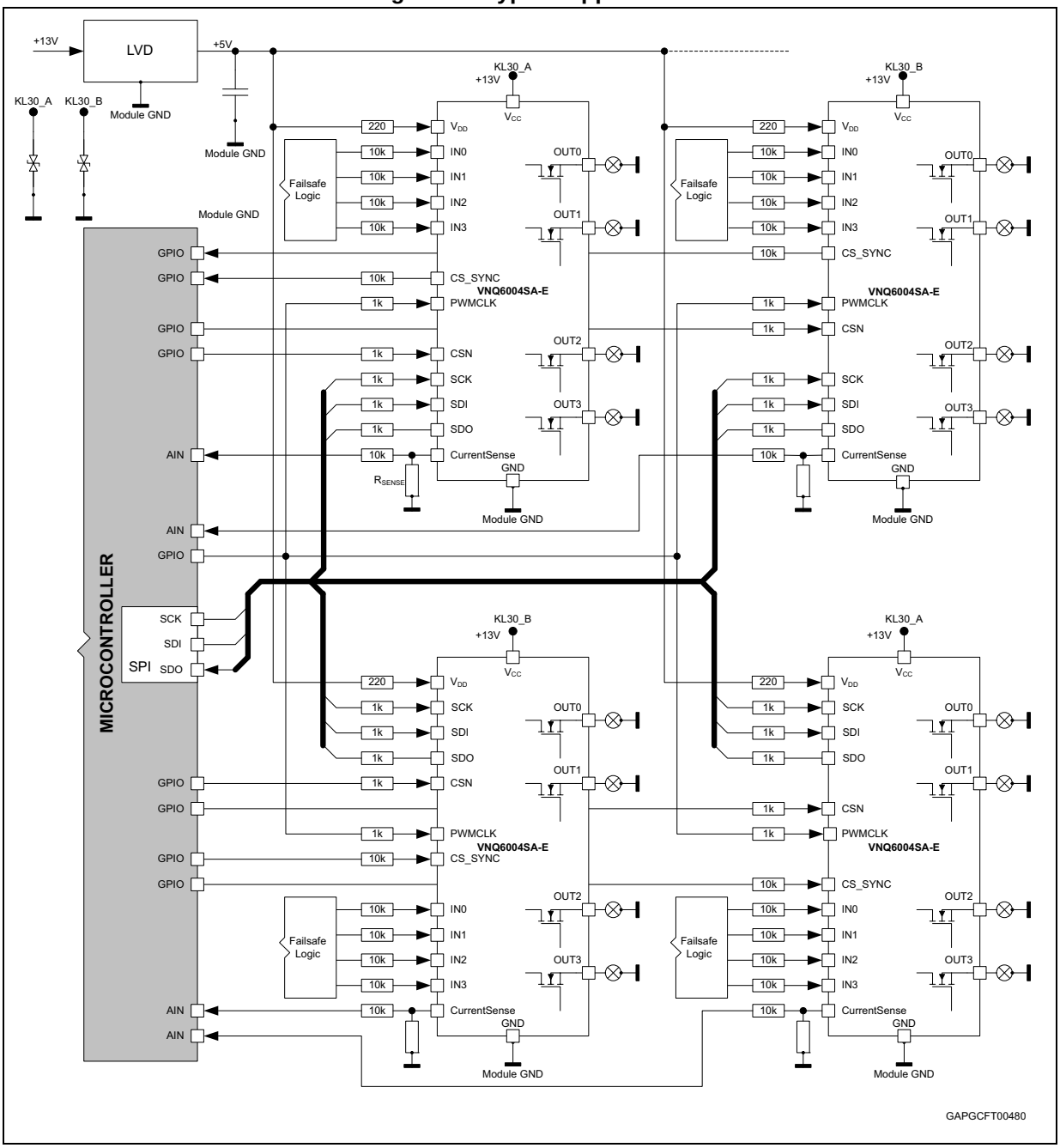
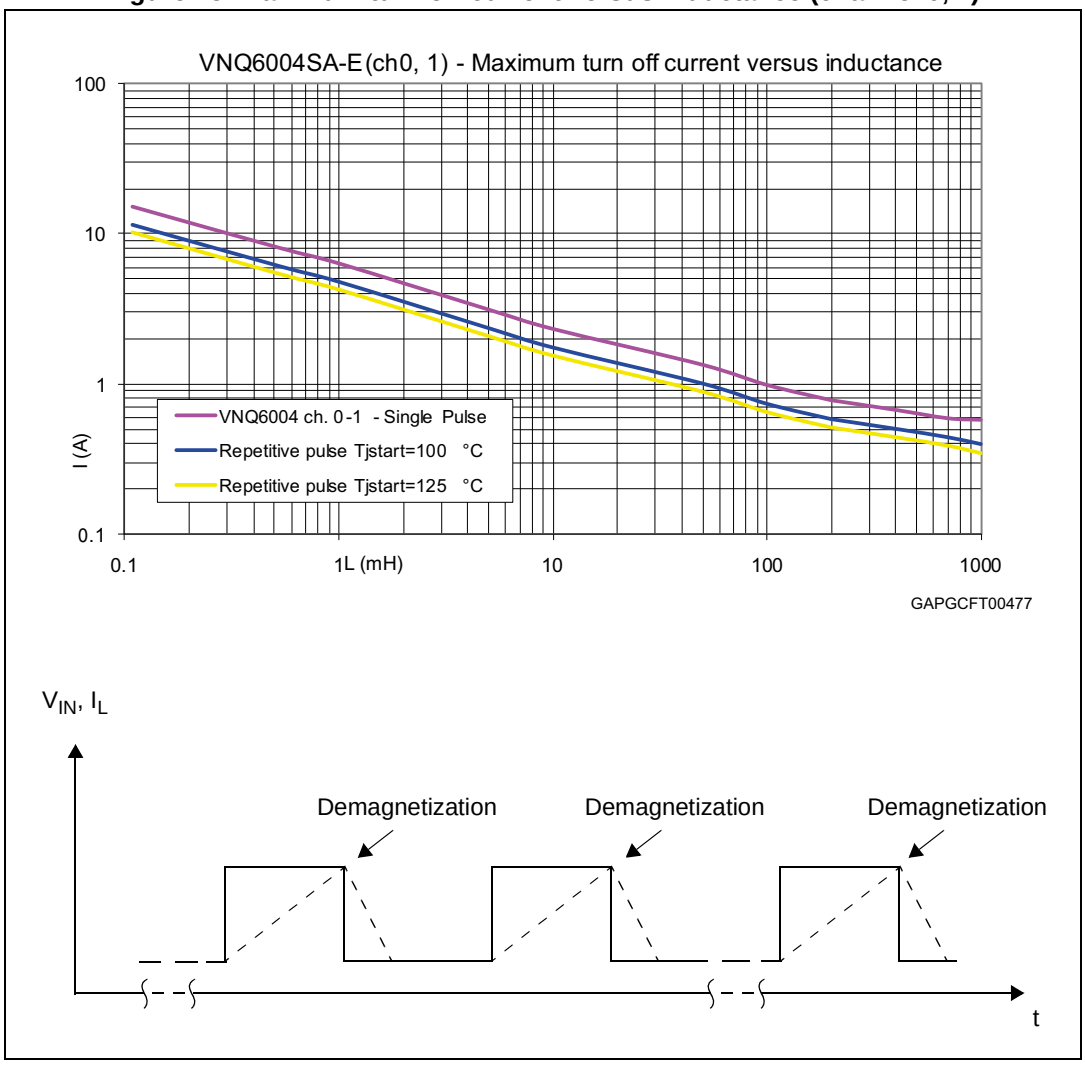


Figure 24. Typical application



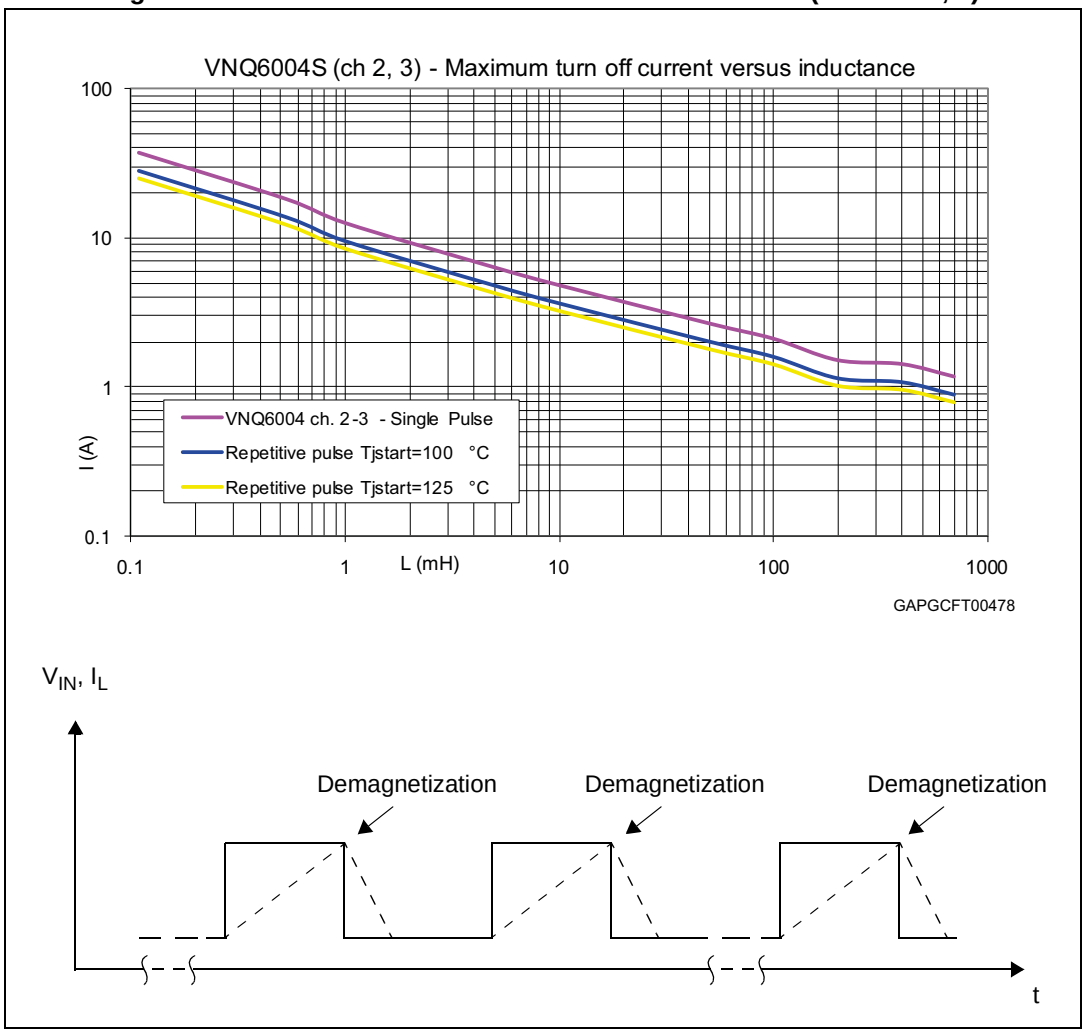
4.4 Maximum demagnetization energy (V_{CC} = 13.5 V)

Figure 25. Maximum turn off current versus inductance (channel 0, 1)



1. Values are generated with R_L = 0 Ω.
In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

Figure 26. Maximum turn off current versus inductance (channel 2, 3)

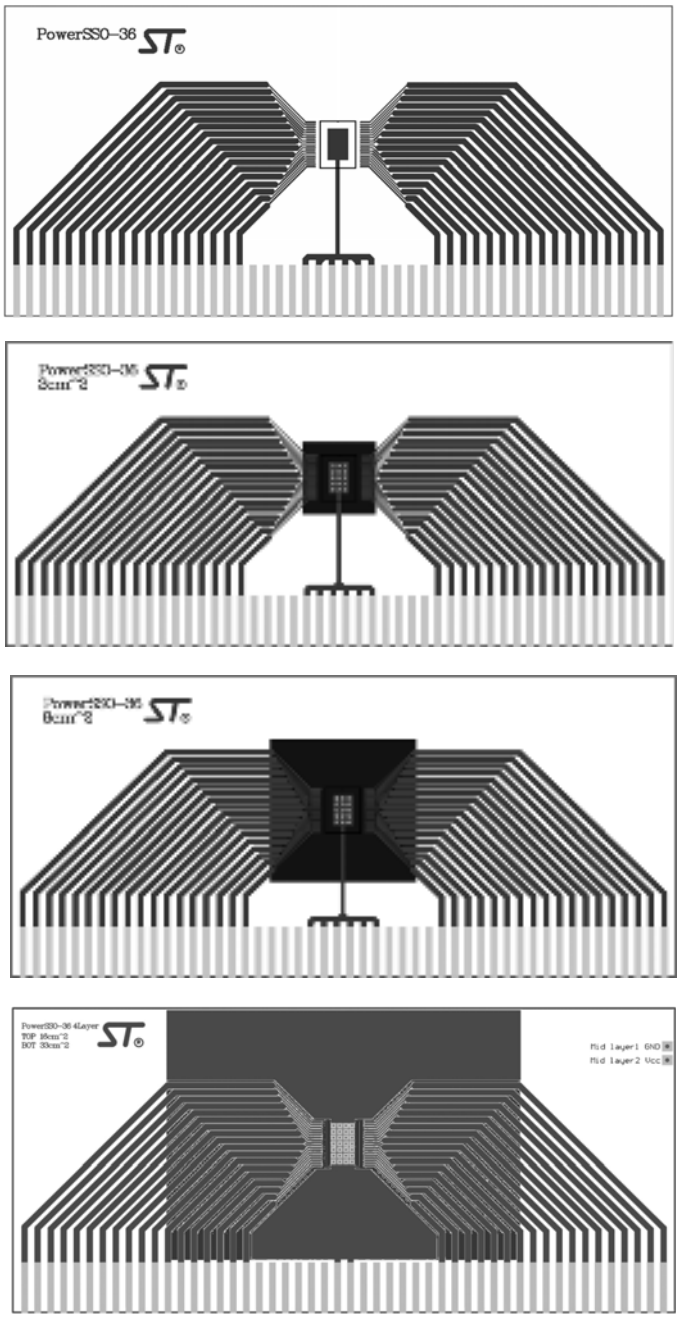


1. Values are generated with R_L = 0 Ω.
In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

5 Package and PCB thermal data

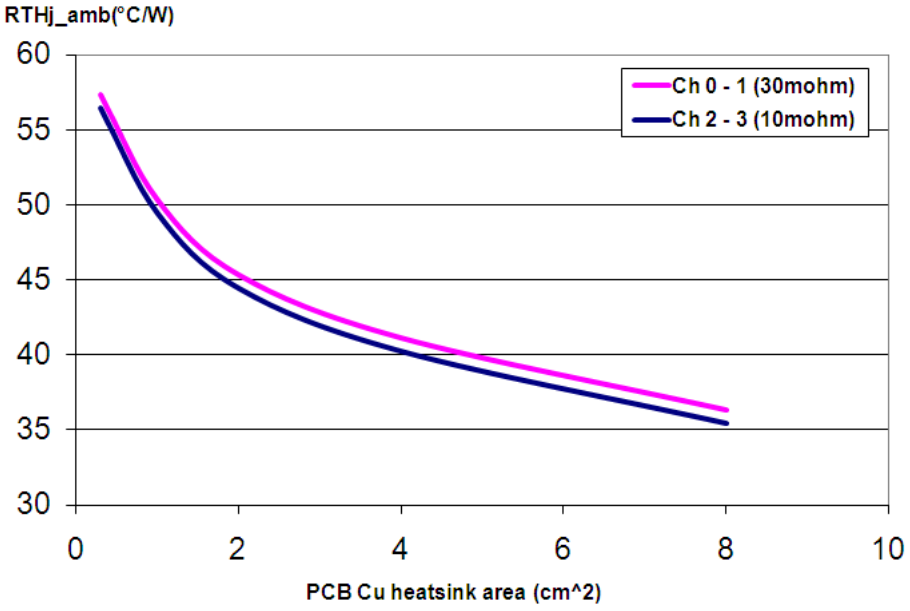
5.1 PowerSSO-36 thermal data

Figure 27. PowerSSO-36 PC board



Note:
Board finish thickness 1.6 mm +/- 10%; Board double layer and four layers; Board dimension 129x60; Board Material FR4; Cu thickness 0.070 mm (outer layers); Cu thickness 0.035 mm (inner layers); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm; Footprint dimension 4.1 mm x 6.5 mm

Figure 28. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel ON)



R_{THj_amb} on 4Layer PCB:
Ch 0-1 (30 mW) ® 22.3 °C/W
Ch 2-3 (10 mW) ® 21.4 °C/W

Figure 29. PowerSSO-36 Thermal impedance junction ambient single pulse (one channel ON)

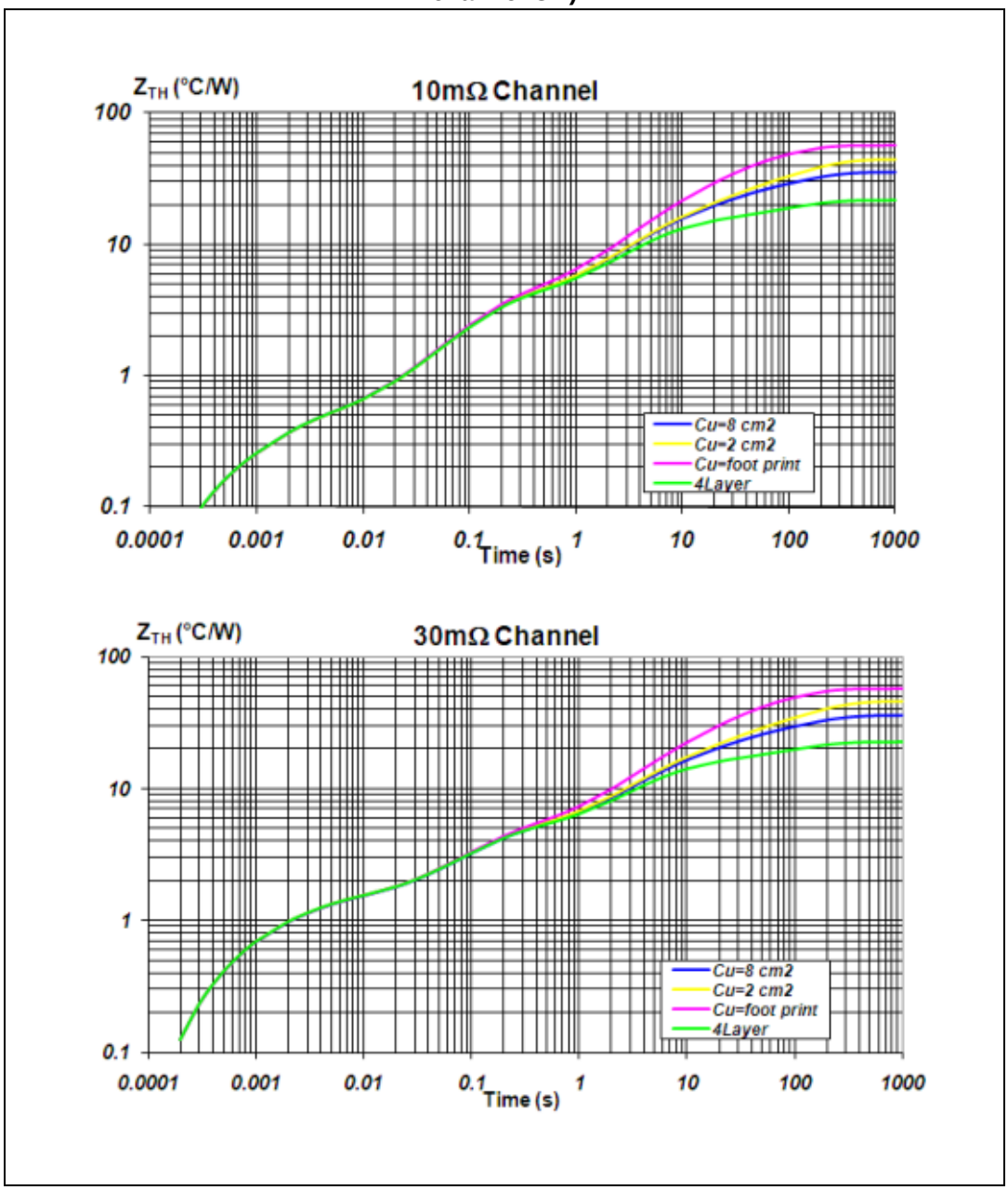
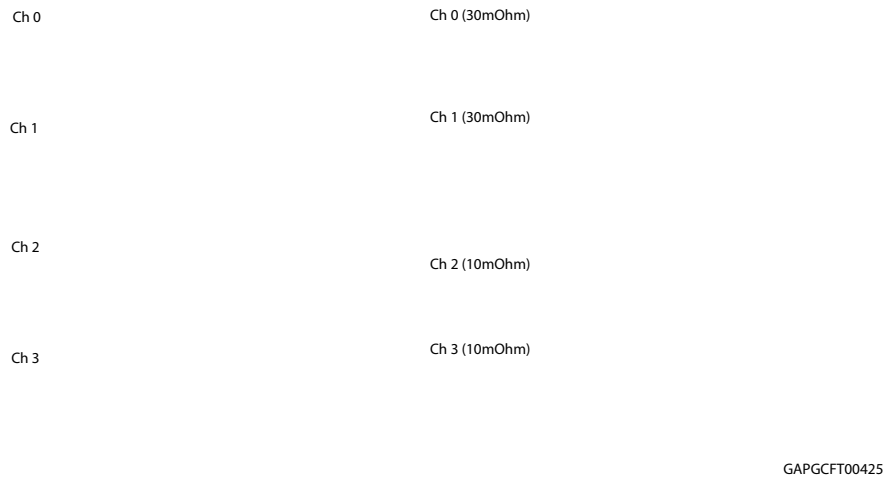


Figure 30. Thermal fitting model of a double channel HSD in PowerSSO-36



Note:
The fitting model is a semplified thermal tool and is valid for transient evolutions where

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 64. Thermal parameter

Area/island (cm^2)	Footprint	2	8	4L
R1 = R7 (°C/W)	0.5			
R2 = R8 (°C/W)	0.8			
R3 (°C/W)	3			
R4 (°C/W)	8			
R5 (°C/W)	18	10	10	3
R6 (°C/W)	27	23	14	7
R9 = R11 (°C/W)	0.1			
R10 = R12 (°C/W)	0.3			
C1 = C7 (W.s/°C)	0.001			
C2 = C8 (W.s/°C)	0.003			
C3 (W.s/°C)	0.04			
C4 (W.s/°C)	0.5			
C5 (W.s/°C)	1	2	2	4
C6 (W.s/°C)	3	6	9	15
C9 = C11 (W.s/°C)	0.0025			
C10 = C12 (W.s/°C)	0.005			

6 Package information

6.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

6.2 PowerSSO-36 mechanical data

Figure 31. PowerSSO-36 package dimensions

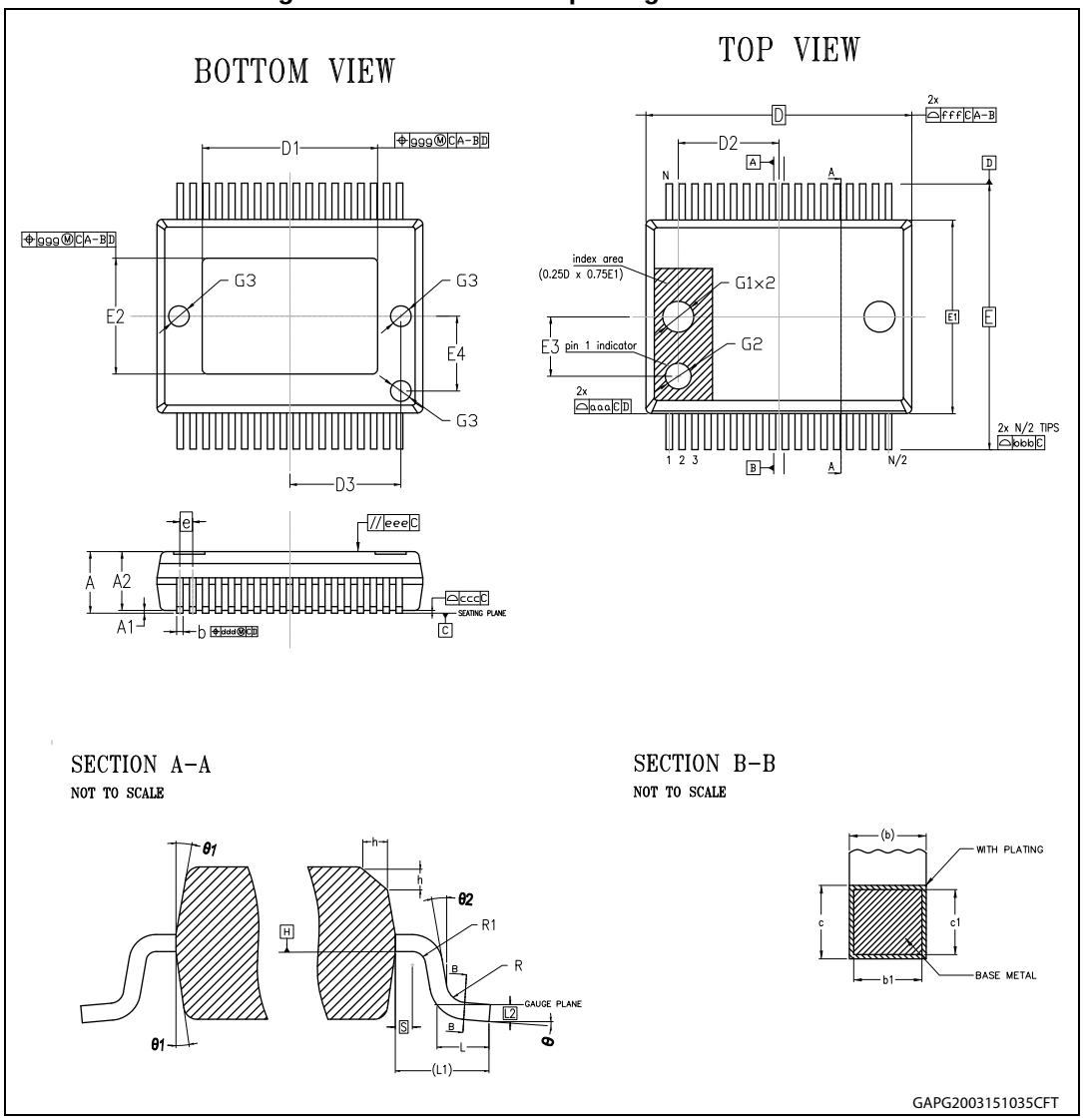


Table 65. PowerSSO-36 mechanical data

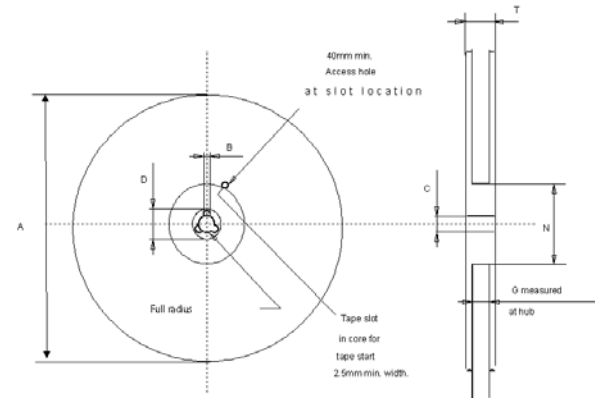
Symbol	millimeters		
	Min	Typ	Max
Θ	0º	—	8º
Θ1	5º	—	10º
Θ2	0º	—	—
A	2.15	—	2.45
A1	0.00	—	0.10
A2	2.15	—	2.35
b	0.18	—	0.32
b1	0.13	0.25	0.30
c	0.23	—	0.32
c1	0.20	0.20	0.30
D	10.30 BSC		
D1	6.90	—	7.50
D2	—	3.65	—
D3	—	4.30	—
e	0.50 BSC		
E	10.30 BSC		
E1	7.50 BSC		
E2	4.30	—	5.20
E3	—	2.30	—
E4	—	2.90	—
G1	—	1.20	—
G2	—	1.00	—
G3	—	0.80	—
h	0.30	—	0.40
L	0.55	0.70	0.85
L1	1.40		
L2	0.25 BSC		
N	36		
R	0.30	—	—
R1	0.20	—	—
S	0.25	—	—
Tolerance of form and position			
aaa	0.20		

Table 65. PowerSSO-36 mechanical data (continued)

Symbol	millimeters		
	Min	Typ	Max
bbb		0.20	
ccc		0.10	
ddd		0.20	
eee		0.10	
ffff		0.20	
ggg		0.15	

6.3 Packing information

Figure 32. PowerSSO-36 tape and reel shipment (suffix “TR”)



REEL DIMENSIONS

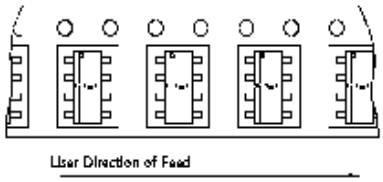
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	100
T (max)	30.4

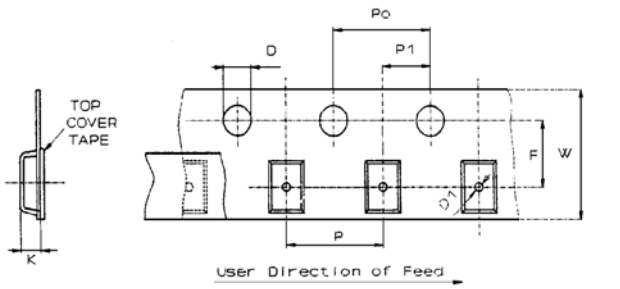
TAPE DIMENSIONS

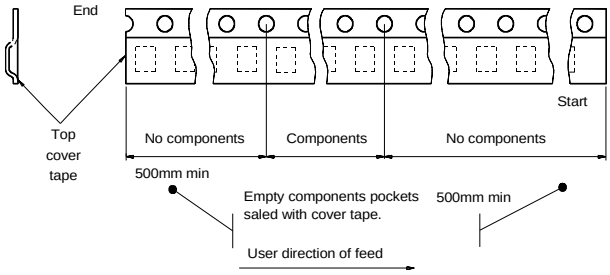
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







7 Order codes

Table 66. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	—	VNQ6004SATR-E

8 Revision history

Table 67. Document revision history

Date	Revision	Changes
04-Oct-2011	1	Initial release
05-Oct-2012	2	Changed document status from preliminary data to datasheet. *Table 44: Dynamic characteristics*: – t_{SLCH}, t_{SHCH}, t_{DVCH}, t_{CHDX}, t_{CH}, t_{CL}: updated test conditions. Updated *Figure 25: Maximum turn off current versus inductance (channel 0, 1)* and *Figure 31: PowerSSO-36 package dimensions*
18-Sep-2013	3	Updated Disclaimer
14-Feb-2014	4	*Table 40: Absolute maximum ratings*: – $V_{SDI,CSN,SCK}$, $-V_{SDI,CSN,SCK}$: removed rows *Table 42: DC characteristics*: – V_{SDI_CL}, V_{SCK_CL}, V_{CSN_CL}: added rows
23-Mar-2015	5	*Table 44: Dynamic characteristics*: – t_{SHCH}: updated value Updated *Chapter 6: Package information* Removed *Figure: PowerSSO-36 tube shipment (no suffix)* Updated *Table 66: Device summary*

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