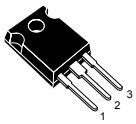
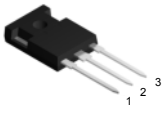
STW88N65M5, STWA88N65M5

Datasheet

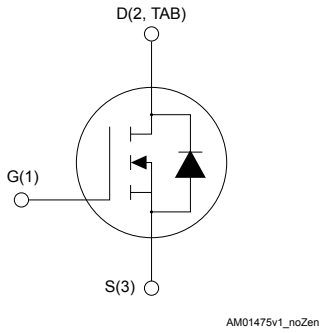
N-channel 650 V, 24 mΩ typ., 84 A MDmesh M5 PowerMOSFETs in TO-247 and TO-247 long leads packages



TO-247



TO-247 long leads



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D
STW88N65M5	650 V	29 mΩ	84 A
STWA88N65M5			

- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

Applications

- High efficiency switching applications:
  - Servers
  - PV inverters
  - Telecom infrastructure
  - Multi kW battery chargers

Description

These devices are N-channel Power MOSFETs based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Product status links
STW88N65M5
STWA88N65M5

Product summary	
Order code	**STW88N65M5**
Marking	88N65M5
Package	TO-247
Packing	Tube
Order code	**STWA88N65M5**
Marking	88N65M5
Package	TO-247 long leads
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	84	A
	Drain current (continuous) at T_C = 100 °C	50.5	
I_{DM}(1)	Drain current (pulsed)	336	A
P_{TOT}	Total power dissipation at T_C = 25 °C	450	W
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	15	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	2000	mJ
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 84 A, di/dt ≤ 400 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.28	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	50	°C/W

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 42 A		24	29	mΩ

1. *Specified by design, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	8825	-	pF
C_{oss}	Output capacitance		-	223	-	pF
C_{rss}	Reverse transfer capacitance		-	11	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	778	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	202	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	1.79	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 42 A	-	204	-	nC
Q_{gs}	Gate-source charge	V_{GS} = 0 to 10 V	-	51	-	nC
Q_{gd}	Gate-drain charge	(see Figure 15. Test circuit for gate charge behavior)	-	84	-	nC

1. *$C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*
2. *$C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 56 A,	-	141	-	ns
$t_{r(v)}$	Voltage rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	16	-	ns
$t_{f(i)}$	Current fall time	(see Figure 16. Test circuit for inductive load switching and diode recovery times	-	29	-	ns
$t_{c(off)}$	Crossing time	and Figure 19. Switching time waveform)	-	56	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		84	A
I_{SDM}(1)	Source-drain current (pulsed)		-		336	A
V_{SD}(2)	Forward on voltage	I_{SD} = 84 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 84 A, di/dt = 100 A/µs,	-	544		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	14		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	50		A
t_{rr}	Reverse recovery time	I_{SD} = 84 A, di/dt = 100 A/µs,	-	660		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_J = 150 °C	-	20		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	60		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

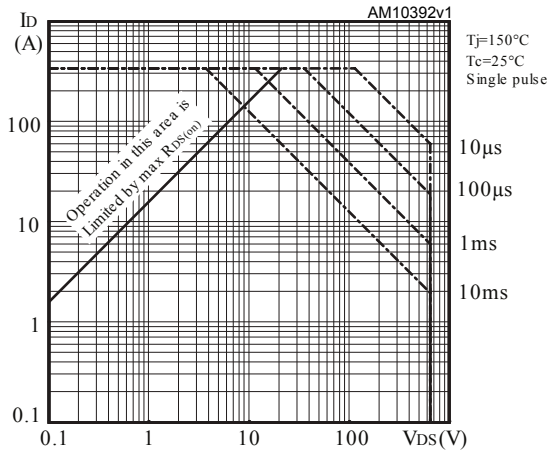


Figure 2. Normalized transient thermal impedance

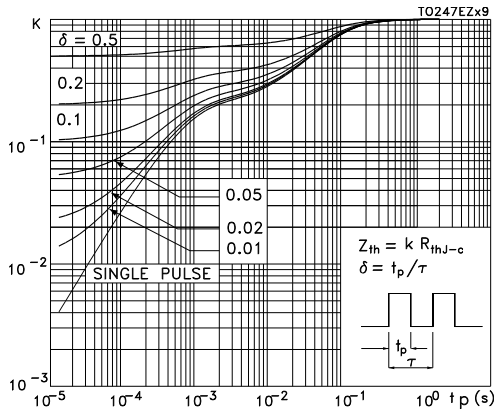


Figure 3. Typical output characteristics

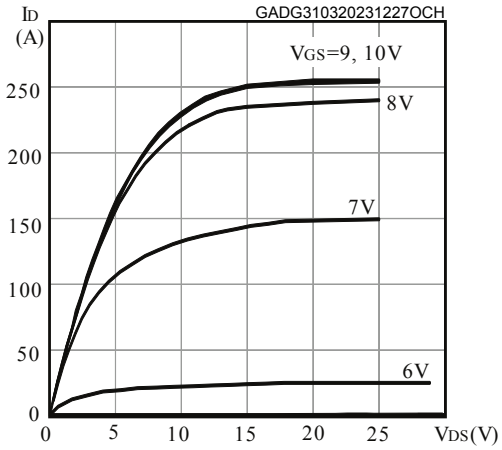


Figure 4. Typical transfer characteristics

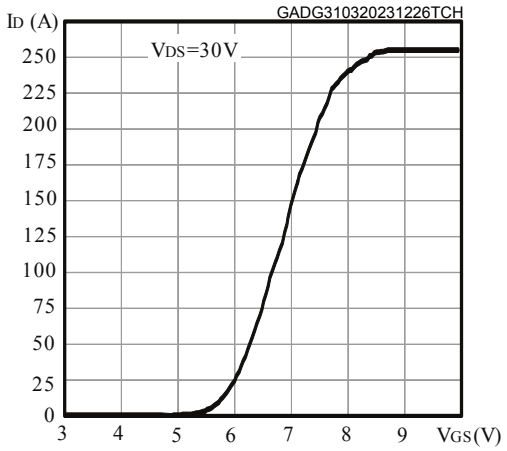


Figure 5. Normalized breakdown voltage vs temperature

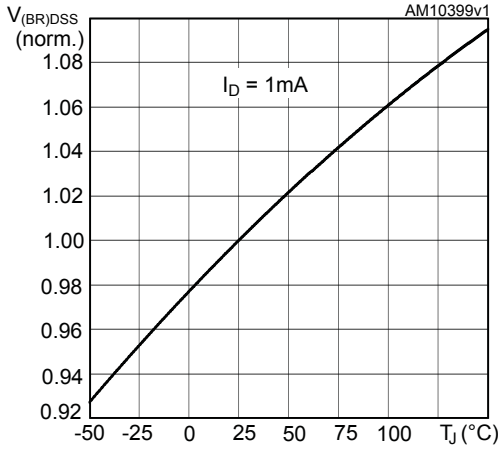


Figure 6. Typical drain-source on-resistance

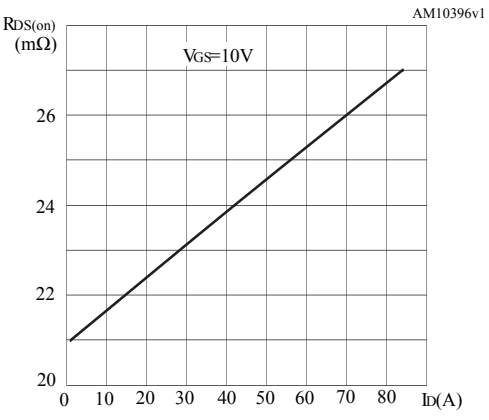


Figure 7. Typical reverse diode forward characteristics

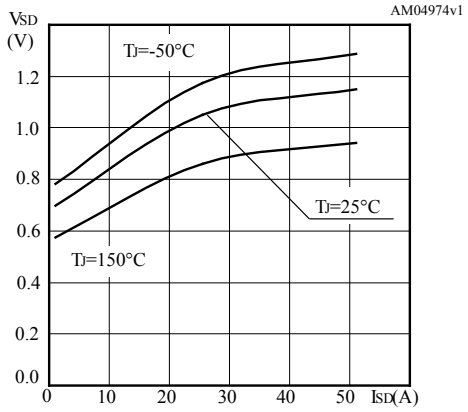


Figure 8. Typical gate charge characteristics

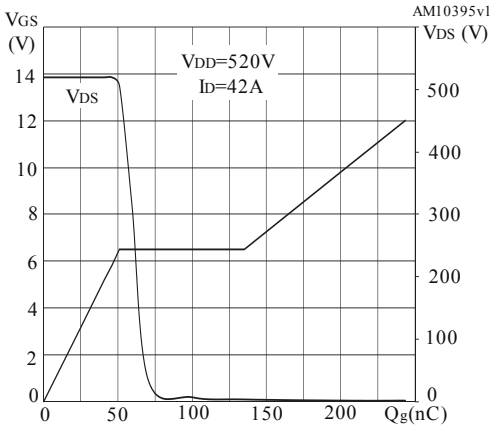


Figure 9. Typical capacitance characteristics

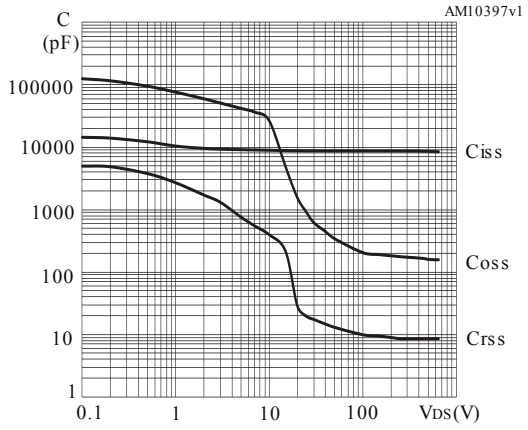


Figure 10. Normalized gate threshold vs temperature

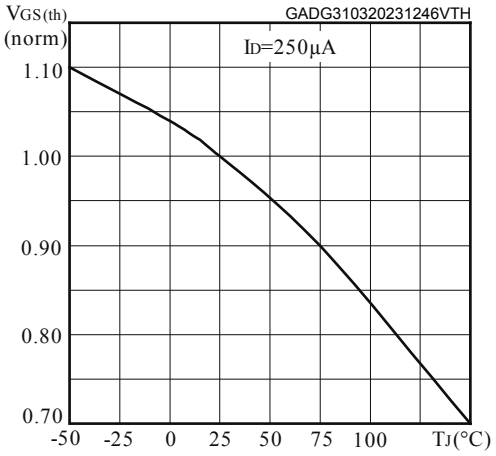


Figure 11. Normalized on-resistance vs temperature

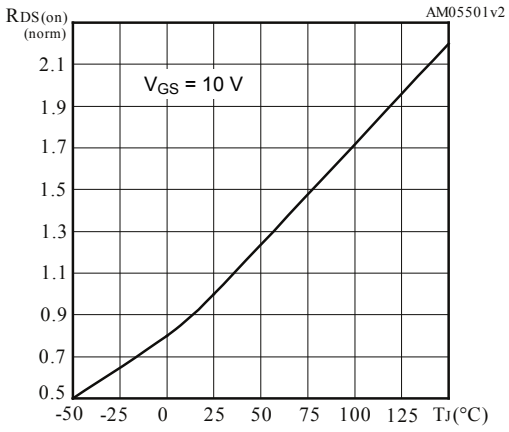


Figure 12. Typical output capacitance stored energy

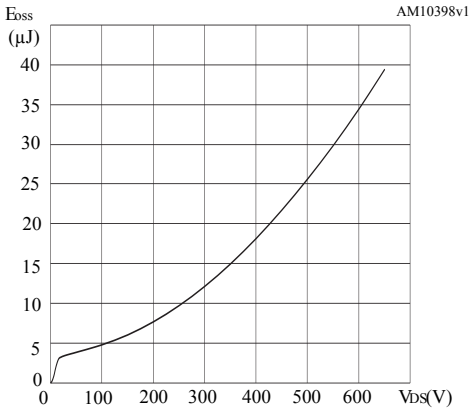
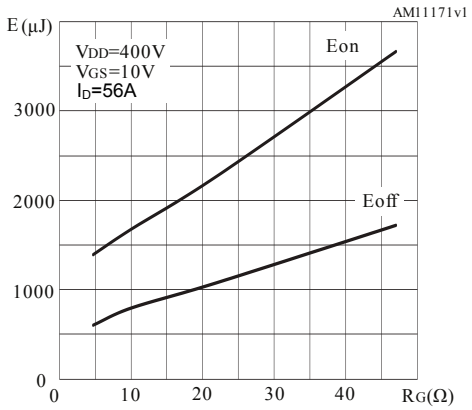


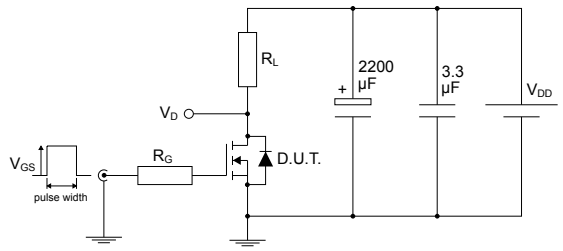
Figure 13. Typical switching energy vs gate resistance



Note: E_{on} including reverse recovery of a SiC diode.

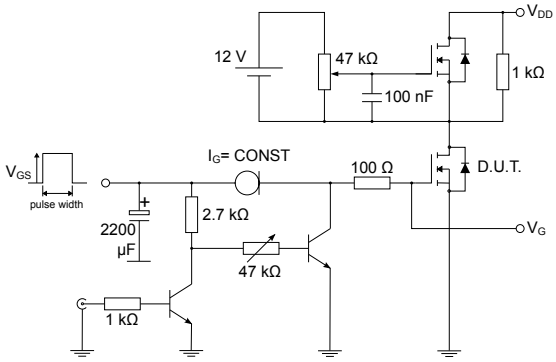
3 Test circuits

Figure 14. Test circuit for resistive load switching times



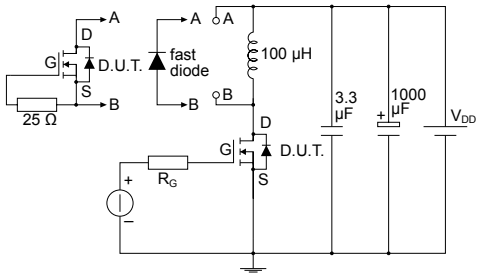
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Figure 15. Test circuit for gate charge behavior



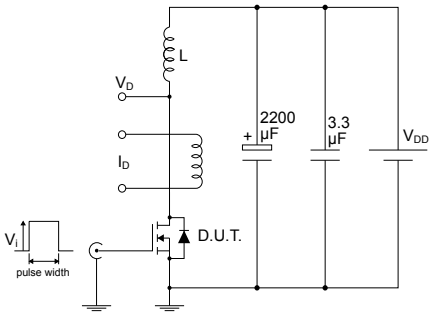
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Figure 16. Test circuit for inductive load switching and diode recovery times



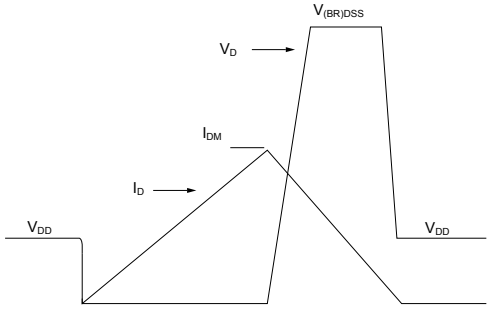
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Figure 17. Unclamped inductive load test circuit



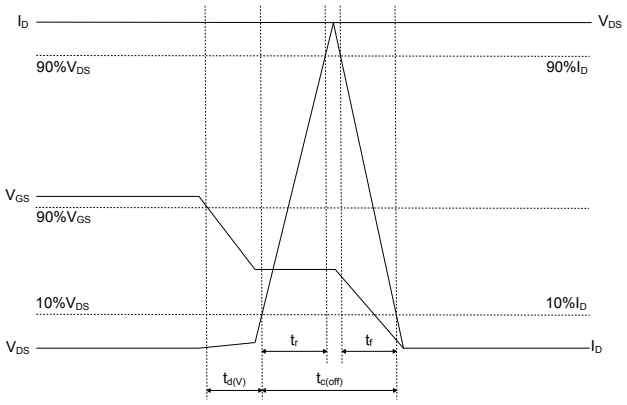
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Figure 18. Unclamped inductive waveform



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Figure 19. Switching time waveform



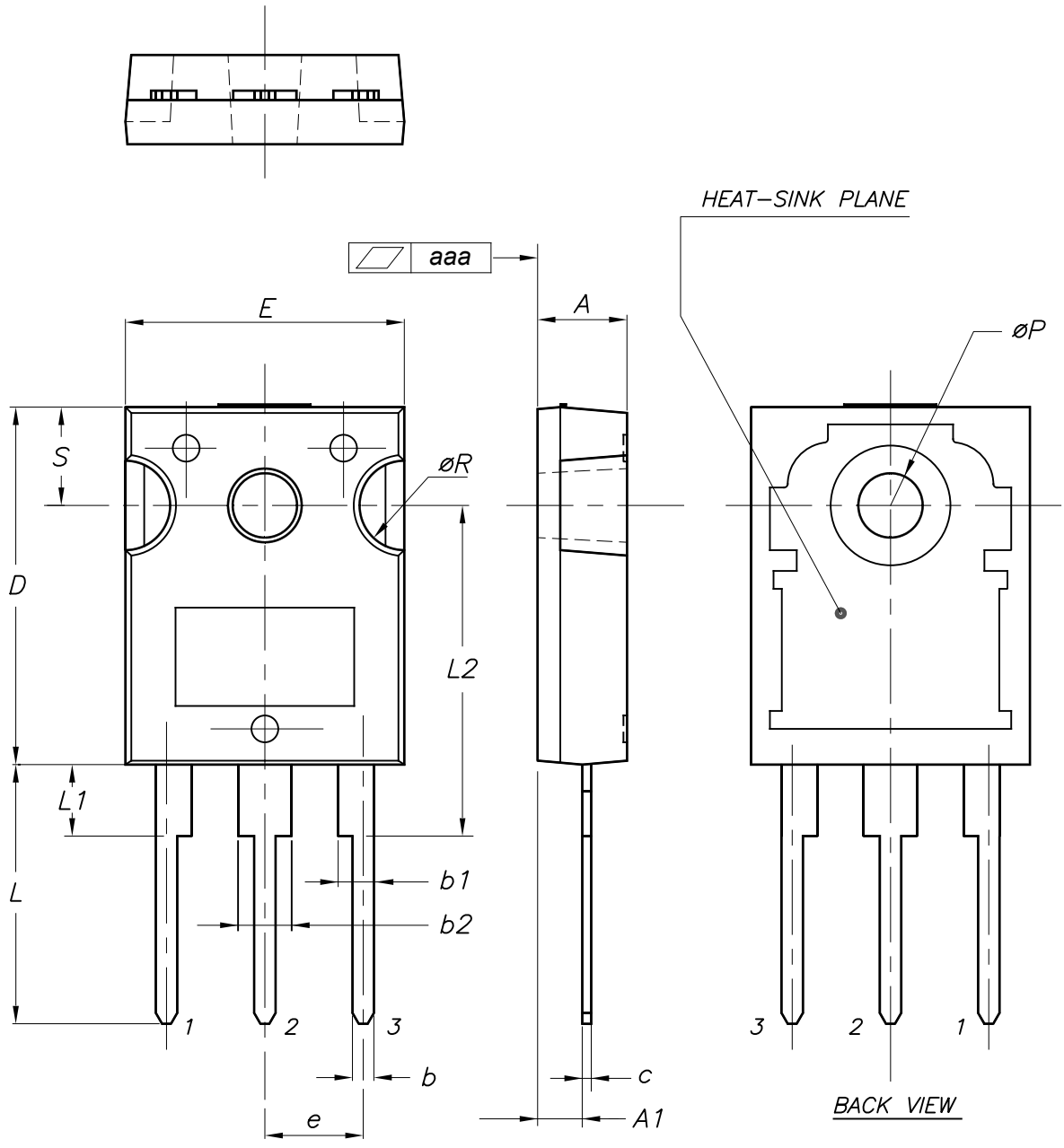
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 20. TO-247 package outline



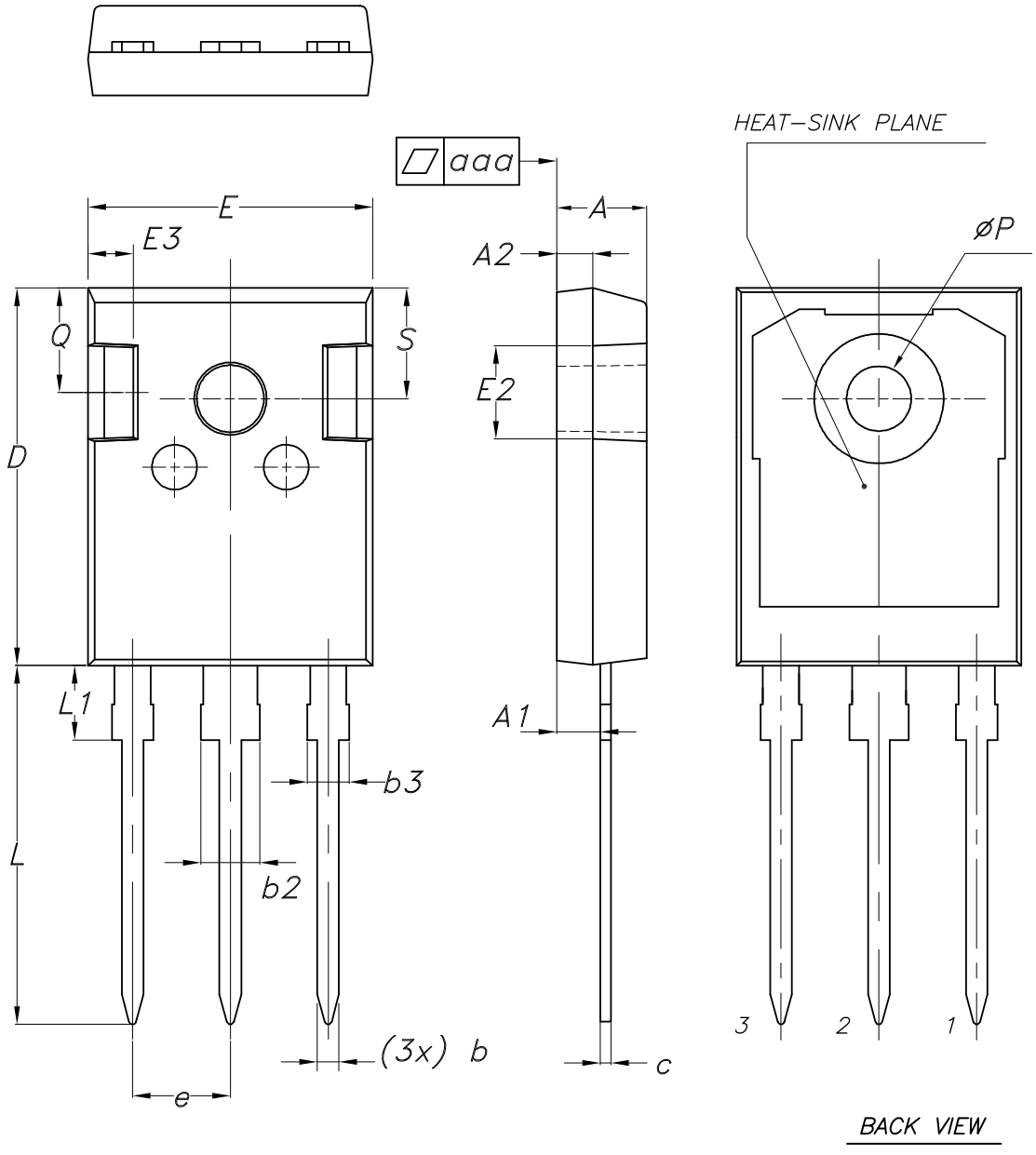
0075325_10

Table 7. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10

4.2 TO-247 long leads package information

Figure 21. **TO-247 long leads package outline**



8463846_4

Table 8. **TO-247 long leads package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25
aaa		0.04	0.10

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
23-Nov-2011	1	First release.
09-Dec-2011	2	Document status promoted from preliminary data to datasheet.
12-Jun-2012	3	Updated title on the cover page.
30-Nov-2012	4	Added new part number: STWA88N65M5 Updated: *Section 4: Package mechanical data*
16-Jul-2014	5	– Updated: *Figure 4* and *5* – Minor text changes
12-Apr-2023	6	Modified title and Features Updated Section 4 Package information Minor text changes

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