STM32F373xx

ARM®Cortex®-M4 32b MCU+FPU, up to 256KB Flash+32KB SRAM, timers, 4 ADCs (16-bit Sig. Delta / 12-bit SAR), 3 DACs, 2 comp., 2.0-3.6 V

Datasheet - production data

Features

- Core: ARM® 32-bit Cortex®-M4 CPU (72 MHz max), single-cycle multiplication and HW division, DSP instruction with FPU (floating-point unit) and MPU (memory protection unit)
- 1.25 DMIPS/MHz (Dhrystone 2.1)
- Memories
  - 64 to 256 Kbytes of Flash memory
  - 32 Kbytes of SRAM with HW parity check
- CRC calculation unit
- Reset and power management
  - Voltage range: 2.0 to 3.6 V
  - Power-on/Power down reset (POR/PDR)
  - Programmable voltage detector (PVD)
  - Low power modes: Sleep, Stop, Standby
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x16 PLL option
  - Internal 40 kHz oscillator
- Up to 84 fast I/Os
  - All mappable on external interrupt vectors
  - Up to 45 I/Os with 5 V tolerant capability
- 12-channel DMA controller
- One 12-bit, 1.0 µs ADC (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Separate analog supply from 2.4 up to 3.6
- Three 16-bit Sigma Delta ADC
  - Separate analog supply from 2.2 to 3.6 V, up to 21 single/ 11 diff channels
- Three 12-bit DAC channels
- Two fast rail-to-rail analog comparators with programmable input and output
- Up to 24 capacitive sensing channels

LQFP48 (7 × 7 mm)
LQFP64 (10 × 10 mm)
LQFP100 (14 × 14 mm)

UFBGA100 (7 x 7 mm)

- 17 timers
  - Two 32-bit timers and three 16-bit timers with up to 4 IC/OC/PWM or pulse counters
  - Two 16-bit timers with up to 2 IC/OC/PWM or pulse counters
  - Four 16-bit timers with up to 1 IC/OC/PWM or pulse counter
  - Independent and system watchdog timers
  - SysTick timer: 24-bit down counter
  - Three 16-bit basic timers to drive the DAC
- Calendar RTC with Alarm and periodic wakeup from Stop/Standby
- Communication interfaces
  - CAN interface (2.0B Active)
  - Two I^2Cs supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from STOP
  - Three USARTs supporting synchronous mode, modem control, ISO/IEC 7816, LIN, IrDA, auto baud rate, wakeup feature
  - Three SPIs (18 Mbit/s) with 4 to 16 programmable bit frames, muxed I2S
  - HDMI-CEC bus interface
  - USB 2.0 full speed interface
- Serial wire devices, JTAG, Cortex®-M4 ETM
- 96-bit unique ID

Table 1. Device summary

Reference	Part numbers
STM32F373xx	STM32F373C8, STM32F373R8, STM32F373V8, STM32F373CB, STM32F373RB, STM32F373VB, STM32F373CC, STM32F373RC, STM32F373VC

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Contents

1 Introduction 9

2 Description 10

3 Functional overview 13

3.1 ARM® Cortex®-M4 core with embedded Flash and SRAM 13

3.2 Memory protection unit 13

3.3 Embedded Flash memory 14

3.4 Cyclic redundancy check (CRC) calculation unit 14

3.5 Embedded SRAM 14

3.6 Boot modes 14

3.7 Power management 15

3.7.1 Power supply schemes 15

3.7.2 Power supply supervisor 15

3.7.3 Voltage regulator 15

3.7.4 Low-power modes 16

3.8 Clocks and startup 16

3.9 General-purpose input/outputs (GPIOs) 16

3.10 Direct memory access (DMA) 17

3.11 Interrupts and events 17

3.11.1 Nested vectored interrupt controller (NVIC) 17

3.11.2 Extended interrupt/event controller (EXTI) 17

3.12 12-bit analog-to-digital converter (ADC) 18

3.12.1 Temperature sensor 18

3.12.2 Internal voltage reference (V_{REFINT}) 18

3.12.3 V_{BAT} battery voltage monitoring 18

3.13 16-bit sigma delta analog-to-digital converters (SDADC) 19

3.14 Digital-to-analog converter (DAC) 19

3.15 Fast comparators (COMP) 20

3.16 Touch sensing controller (TSC) 20

3.17 Timers and watchdogs 22

3.17.1 General-purpose timers (TIM2 to TIM5, TIM12 to TIM17, TIM19) 23

3.17.2 Basic timers (TIM6, TIM7, TIM18) 23
3.17.3 Independent watchdog (IWDG) 24
3.17.4 System window watchdog (WWDG) 24
3.17.5 SysTick timer 24
3.18 Real-time clock (RTC) and backup registers 24
3.19 Inter-integrated circuit interface (I^2C) 25
3.20 Universal synchronous/asynchronous receiver transmitter (USART) . . . 26
3.21 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I^2S) . 27
3.22 High-definition multimedia interface (HDMI) - consumer electronics control (CEC) 27
3.23 Controller area network (CAN) 27
3.24 Universal serial bus (USB) 28
3.25 Serial wire JTAG debug port (SWJ-DP) 28
3.26 Embedded trace macrocell™ 28

4 Pinouts and pin description 29

5 Memory mapping 48

6 Electrical characteristics 52
6.1 Parameter conditions 52
6.1.1 Minimum and maximum values 52
6.1.2 Typical values 52
6.1.3 Typical curves 52
6.1.4 Loading capacitor 52
6.1.5 Pin input voltage 52
6.1.6 Power supply scheme 53
6.1.7 Current consumption measurement 54
6.2 Absolute maximum ratings 55
6.3 Operating conditions 57
6.3.1 General operating conditions 57
6.3.2 Operating conditions at power-up / power-down 58
6.3.3 Embedded reset and power control block characteristics 59
6.3.4 Embedded reference voltage 60
6.3.5 Supply current characteristics 61
6.3.6 Wakeup time from low-power mode 71

6.3.7 External clock source characteristics 72
6.3.8 Internal clock source characteristics 77
6.3.9 PLL characteristics 78
6.3.10 Memory characteristics 79
6.3.11 EMC characteristics 80
6.3.12 Electrical sensitivity characteristics 81
6.3.13 I/O current injection characteristics 82
6.3.14 I/O port characteristics 84
6.3.15 NRST characteristics 89
6.3.16 Communications interfaces 91
6.3.17 12-bit ADC characteristics 98
6.3.18 DAC electrical specifications 101
6.3.19 Comparator characteristics 103
6.3.20 Temperature sensor characteristics 105
6.3.21 V_{BAT} monitoring characteristics 105
6.3.22 Timer characteristics 105
6.3.23 USB characteristics 107
6.3.24 CAN (controller area network) interface 108
6.3.25 SDADC characteristics 108

7 Package information 115
7.1 UFBGA100 package information 115
7.2 LQFP100 package information 118
7.3 LQFP64 package information 121
7.4 LQFP48 package information 124
7.5 Thermal characteristics 127
7.5.1 Reference document 127
7.5.2 Selecting the product temperature range 128

8 Part numbering 130

9 Revision history 131

List of tables

Table 1. Device summary . . . 1
Table 2. Device overview . . . 11
Table 3. Capacitive sensing GPIOs available on STM32F373xx devices . . . 20
Table 4. No. of capacitive sensing channels available on STM32F373xx devices . . . 21
Table 5. Timer feature comparison . . . 22
Table 6. Comparison of I^2C analog and digital filters . . . 25
Table 7. STM32F373xx I^2C implementation . . . 25
Table 8. STM32F373xx USART implementation . . . 26
Table 9. STM32F373xx SPI/I2S implementation . . . 27
Table 10. Legend/abbreviations used in the pinout table . . . 33
Table 11. STM32F373xx pin definitions . . . 33
Table 12. Alternate functions for port PA . . . 41
Table 13. Alternate functions for port PB . . . 43
Table 14. Alternate functions for port PC . . . 44
Table 15. Alternate functions for port PD . . . 45
Table 16. Alternate functions for port PE . . . 46
Table 17. Alternate functions for port PF . . . 47
Table 18. STM32F373xx peripheral register boundary addresses . . . 49
Table 19. Voltage characteristics . . . 55
Table 20. Current characteristics . . . 56
Table 21. Thermal characteristics . . . 56
Table 22. General operating conditions . . . 57
Table 23. Operating conditions at power-up / power-down . . . 58
Table 24. Embedded reset and power control block characteristics . . . 59
Table 25. Programmable voltage detector characteristics . . . 59
Table 26. Embedded internal reference voltage calibration values . . . 60
Table 27. Embedded internal reference voltage . . . 60
Table 28. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V . . . 61
Table 29. Typical and maximum current consumption from V_{DDA} supply . . . 63
Table 30. Typical and maximum V_{DD} consumption in Stop and Standby modes . . . 63
Table 31. Typical and maximum V_{DDA} consumption in Stop and Standby modes . . . 64
Table 32. Typical and maximum current consumption from V_{BAT} supply . . . 64
Table 33. Typical current consumption in Run mode, code with data processing running from Flash 66
Table 34. Typical current consumption in Sleep mode, code running from Flash or RAM . . . 67
Table 35. Switching output I/O current consumption . . . 69
Table 36. Peripheral current consumption . . . 70
Table 37. Low-power mode wakeup timings . . . 72
Table 38. High-speed external user clock characteristics . . . 72
Table 39. Low-speed external user clock characteristics . . . 73
Table 40. HSE oscillator characteristics . . . 74
Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) . . . 76
Table 42. HSI oscillator characteristics . . . 77
Table 43. LSI oscillator characteristics . . . 78
Table 44. PLL characteristics . . . 78
Table 45. Flash memory characteristics . . . 79
Table 46. Flash memory endurance and data retention . . . 79
Table 47. EMS characteristics . . . 80
Table 48. EMI characteristics . . . 81

Table 49. ESD absolute maximum ratings . . . 81
Table 50. Electrical sensitivities . . . 82
Table 51. I/O current injection susceptibility . . . 83
Table 52. I/O static characteristics . . . 84
Table 53. Output voltage characteristics . . . 87
Table 54. I/O AC characteristics . . . 88
Table 55. NRST pin characteristics . . . 89
Table 56. I2C characteristics . . . 91
Table 57. I^2C analog filter characteristics . . . 92
Table 58. SPI characteristics . . . 93
Table 59. I^2S characteristics . . . 96
Table 60. ADC characteristics . . . 98
Table 61. R_{SRC} max for f_{ADC} = 14 MHz . . . 99
Table 62. ADC accuracy . . . 99
Table 63. DAC characteristics . . . 101
Table 64. Comparator characteristics . . . 103
Table 65. Temperature sensor calibration values . . . 105
Table 66. TS characteristics . . . 105
Table 67. V_{BAT} monitoring characteristics . . . 105
Table 68. TIMx characteristics . . . 106
Table 69. IWDG min/max timeout period at 40 kHz (LSI) . . . 106
Table 70. WWDG min-max timeout value @72 MHz (PCLK) . . . 106
Table 71. USB startup time . . . 107
Table 72. USB DC electrical characteristics . . . 107
Table 73. USB: Full-speed electrical characteristics . . . 108
Table 74. SDADC characteristics . . . 108
Table 75. VREFSD+ pin characteristics . . . 114
Table 76. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data . . . 115
Table 77. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA) . . . 116
Table 78. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data . . . 119
Table 79. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data . . . 122
Table 80. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data . . . 125
Table 81. Package thermal characteristics . . . 127
Table 82. Ordering information scheme . . . 130
Table 83. Document revision history . . . 131

List of figures

Figure 1. Block diagram . . . 12
Figure 2. STM32F373xx LQFP48 pinout . . . 29
Figure 3. STM32F373xx LQFP64 pinout . . . 30
Figure 4. STM32F373xx LQFP100 pinout . . . 31
Figure 5. STM32F373xx BGA100 ballout . . . 32
Figure 6. STM32F373xx memory map . . . 48
Figure 7. Pin loading conditions . . . 52
Figure 8. Pin input voltage . . . 52
Figure 9. Power supply scheme . . . 53
Figure 10. Current consumption measurement scheme . . . 54
Figure 11. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0]='00') . . . 65
Figure 12. High-speed external clock source AC timing diagram . . . 73
Figure 13. Low-speed external clock source AC timing diagram . . . 74
Figure 14. Typical application with an 8 MHz crystal . . . 75
Figure 15. Typical application with a 32.768 kHz crystal . . . 77
Figure 16. HSI oscillator accuracy characterization results . . . 78
Figure 17. TC and TTa I/O input characteristics - CMOS port . . . 85
Figure 18. TC and TTa I/O input characteristics - TTL port . . . 85
Figure 19. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port . . . 86
Figure 20. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port . . . 86
Figure 21. I/O AC characteristics definition . . . 89
Figure 22. Recommended NRST pin protection . . . 90
Figure 23. I^2C bus AC waveforms and measurement circuit . . . 92
Figure 24. SPI timing diagram - slave mode and CPHA = 0 . . . 94
Figure 25. SPI timing diagram - slave mode and CPHA = 1(1) . . . 94
Figure 26. SPI timing diagram - master mode(1) . . . 95
Figure 27. I^2S slave timing diagram (Philips protocol)(1) . . . 97
Figure 28. I^2S master timing diagram (Philips protocol)(1) . . . 97
Figure 29. ADC accuracy characteristics . . . 100
Figure 30. Typical connection diagram using the ADC . . . 100
Figure 31. 12-bit buffered /non-buffered DAC . . . 102
Figure 32. Maximum V_{REFINT} scaler startup time from power down . . . 104
Figure 33. USB timings: definition of data signal rise and fall time . . . 108
Figure 34. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline . . . 115
Figure 35. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint . . . 116
Figure 36. UFBGA100 marking example (package top view) . . . 117
Figure 37. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline . . . 118
Figure 38. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint . . . 120
Figure 39. LQFP100 marking example (package top view) . . . 120
Figure 40. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline . . . 121
Figure 41. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint . . . 123
Figure 42. LQFP64 marking example (package top view) . . . 123
Figure 43. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline . . . 124
Figure 44. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package

recommended footprint 126
Figure 45. LQFP48 marking example (package top view) 126
Figure 46. LQFP64 P_D max vs. T_A 129

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F373xx microcontrollers.

This STM32F373xx datasheet should be read in conjunction with the RM0313 reference manual. The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Cortex®-M4 with FPU core, please refer to:

- Cortex®-M4 with FPU Technical Reference Manual, available from www.arm.com.
- STM32F3xxx and STM32F4xxx Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

2 Description

The STM32F373xx family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an Embedded Trace Macrocell™ (ETM). The family incorporates high-speed embedded memories (up to 256 Kbyte of Flash memory, up to 32 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32F373xx devices offer one fast 12-bit ADC (1 Msps), three 16-bit Sigma delta ADCs, two comparators, two DACs (DAC1 with 2 channels and DAC2 with 1 channel), a low-power RTC, 9 general-purpose 16-bit timers, two general-purpose 32-bit timers, three basic timers.

They also feature standard and advanced communication interfaces: two I2Cs, three SPIs, all with muxed I2Ss, three USARTs, CAN and USB.

The STM32F373xx family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

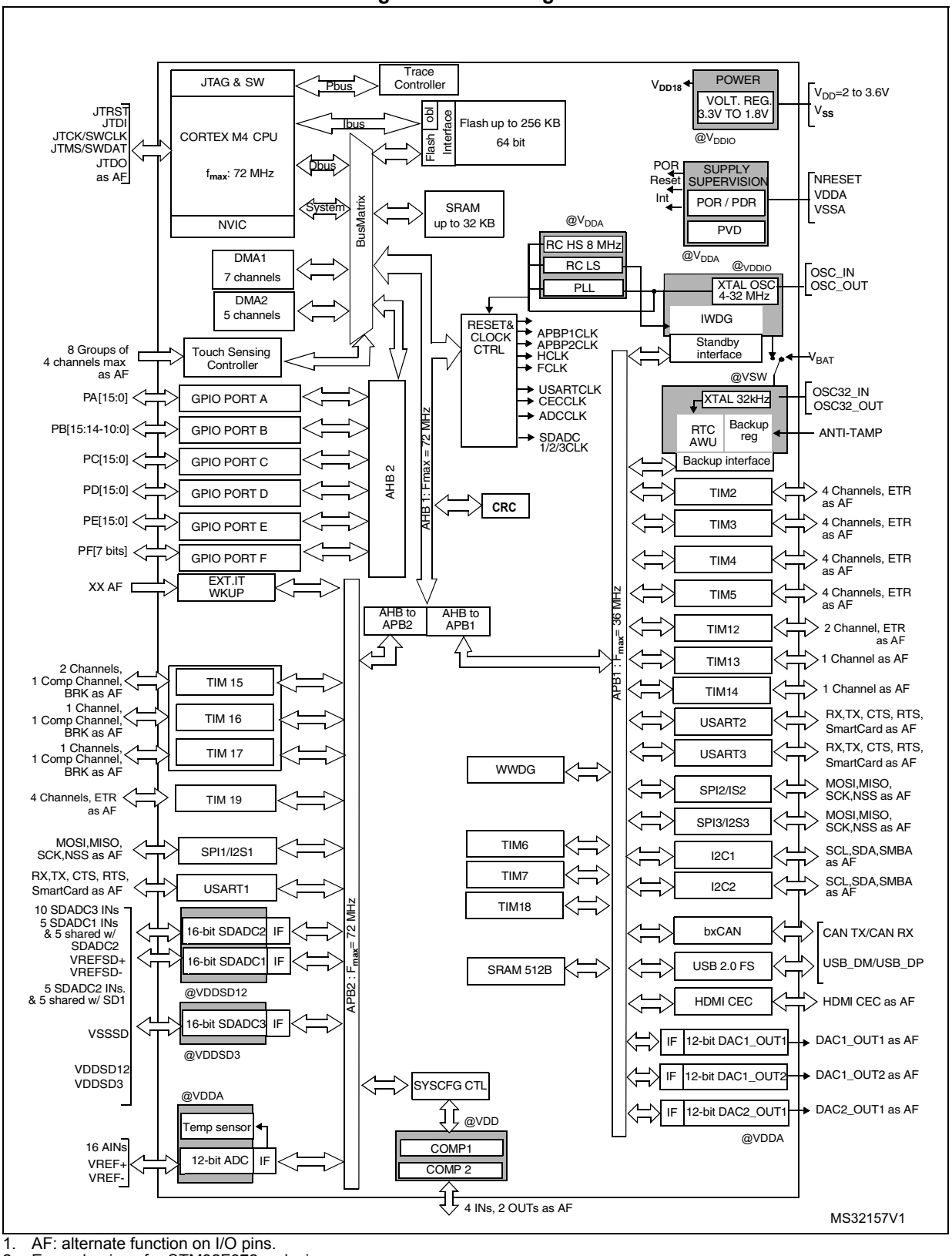
The STM32F373xx family offers devices in five packages ranging from 48 pins to 100 pins. The set of included peripherals changes with the device chosen.

Table 2. Device overview

Peripheral		STM32F 373Cx			STM32F 373Rx			STM32F 373Vx		
Flash (Kbytes)		64	128	256	64	128	256	64	128	256
SRAM (Kbytes)		16	24	32	16	24	32	16	24	32
Timers	General purpose	9 (16-bit) 2 (32 bit)								
	Basic	3 (16-bit)								
Comm. interfaces	SPI/I2S	3								
	I^2C	2								
	USART	3								
	CAN	1								
	USB	1								
GPIOs	Normal I/Os (TC, TTa)	36			52			84		
	5 volts Tolerant I/Os (FT, Ftf)	20			28			45		
12-bit ADCs		1								
16-bit ADCs Sigma- Delta		3								
12-bit DACs outputs		3								
Analog comparator		2								
Capacitive sensing channels		14			17			24		
Max. CPU frequency		72 MHz								
Main operating voltage		2.0 to 3.6 V								
16-bit SDADC operating voltage		2.2 to 3.6 V								
Operating temperature		Ambient operating temperature: -40 to 85 °C / -40 to 105 °C Junction temperature: - -40 to 125 °C								
Packages		LQFP48			LQFP64			LQFP100, UFBGA100(1)		

1. UFBGA100 package available on 256-KB versions only.

Figure 1. Block diagram



1. AF: alternate function on I/O pins.
2. Example given for STM32F372xx device.

3 Functional overview

3.1 ARM® Cortex®-M4 core with embedded Flash and SRAM

The ARM Cortex-M4 processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F373xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F373xx family.

3.2 Memory protection unit

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

The Cortex-M4 processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

- Outstanding processing performance combined with fast interrupt handling
- Enhanced system debug with extensive breakpoint and trace capabilities
- Efficient processor core, system and memories
- Ultralow power consumption with integrated sleep modes
- Platform security robustness with optional integrated memory protection unit (MPU).

With its embedded ARM core, the STM32F373xx devices are compatible with all ARM development tools and software.

3.3 Embedded Flash memory

All STM32F373xx devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.4 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.5 Embedded SRAM

All STM32F373xx devices feature up to 32 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PD5/PD6) or USB (PA11/PA12) through DFU (device firmware upgrade).

3.7 Power management

3.7.1 Power supply schemes

- V_{DD}: external power supply for I/Os and the internal regulator. It is provided externally through V_{DD} pins, and can be 2.0 to 3.6 V.
- V_{DDA} = 2.0 to 3.6 V:
  - external analog power supplies for Reset blocks, RCs and PLL
  - supply voltage for 12-bit ADC, DACs and comparators (minimum voltage to be applied to V_{DDA} is 2.4 V when the 12-bit ADC and DAC are used).
- V_{DDSD12} and V_{DDSD3} = 2.2 to 3.6 V: supply voltages for SDADC1/2 and SDADCD3 sigma delta ADCs. Independent from V_{DD}/V_{DDA}.
- V_{BAT}= 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers when V_{DD} is not present.

3.7.2 Power supply supervisor

- The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit. The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.7.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR), and power-down.

- The MR mode is used in the nominal regulation mode (Run)
- The LPR mode is used in Stop mode.
- The power-down mode is used in Standby mode: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The voltage regulator is always enabled after reset. It is disabled in Standby mode.

3.7.4 Low-power modes

The STM32F373xx supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USARTs, the I2Cs, the CEC, the USB wakeup, the COMPx and the RTC alarm.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.8 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

3.9 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Do not reconfigure GPIO pins which are not present on 48 and 64 pin packages to the analog mode. Additional current consumption in the range of tens of µA per pin can be observed if V_{DDA} is higher than V_{DDIO}.

3.10 Direct memory access (DMA)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The two DMAs can be used with the main peripherals: SPIs, I2Cs, USARTs, DACs, ADC, SDADCs, general-purpose timers.

3.11 Interrupts and events

3.11.1 Nested vectored interrupt controller (NVIC)

The STM32F373xx devices embed a nested vectored interrupt controller (NVIC) able to handle up to 60 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.11.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 29 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 84 GPIOs can be connected to the 16 external interrupt lines.

3.12 12-bit analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter is based on a successive approximation register (SAR) architecture. It has up to 16 external channels (AIN15:0) and 3 internal channels (temperature sensor, voltage reference, V_{BAT} voltage measurement) performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers (TIMx) can be internally connected to the ADC start and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.12.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode. See *Table 65: Temperature sensor calibration values on page 105*.

3.12.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

3.12.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.13 16-bit sigma delta analog-to-digital converters (SDADC)

Three 16-bit sigma-delta analog-to-digital converters are embedded in the STM32F373xx. They have up to two separate supply voltages allowing the analog function voltage range to be independent from the STM32F373xx power supply. They share up to 21 input pins which may be configured in any combination of single-ended (up to 21) or differential inputs (up to 11).

The conversion speed is up to 16.6 ksps for each SDADC when converting multiple channels and up to 50 ksps per SDADC if single channel conversion is used. There are two conversion modes: single conversion mode or continuous mode, capable of automatically scanning any number of channels. The data can be automatically stored in a system RAM buffer, reducing the software overhead.

A timer triggering system can be used in order to control the start of conversion of the three SDADCs and/or the 12-bit fast ADC. This timing control is very flexible, capable of triggering simultaneous conversions or inserting a programmable delay between the ADCs.

Up to two external reference pins (VREFSD+, VREFSD-) and an internal 1.2/1.8 V reference can be used in conjunction with a programmable gain (x0.5 to x32) in order to fine-tune the input voltage range of the SDADC. VREFSD - pin is used as negative signal reference in case of single-ended input mode.

3.14 Digital-to-analog converter (DAC)

The devices feature two 12-bit buffered DACs with three output channels that can be used to convert three digital signals into three analog voltage signal outputs. The internal structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital Interface supports the following features:

- Two DAC converters with three output channels:
  - DAC1 with two output channels
  - DAC2 with one output channel.
- 8-bit or 10-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation (DAC1 only)
- Triangular wave generation (DAC1 only)
- Dual DAC channel independent or simultaneous conversions (DAC1 only)
- DMA capability for each channel
- External triggers for conversion

3.15 Fast comparators (COMP)

The STM32F373xx embeds 2 comparators with rail-to-rail inputs and high-speed output. The reference voltage can be internal or external (delivered by an I/O).

The threshold can be one of the following:

- DACs channel outputs
- External I/O
- Internal reference voltage (V_{REFINT}) or submultiple (1/4 V_{REFINT}, 1/2 V_{REFINT} and 3/4 V_{REFINT})

The comparators can be combined into a window comparator.

Both comparators can wake up the device from Stop mode and generate interrupts and breaks for the timers.

3.16 Touch sensing controller (TSC)

The devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect the presence of a finger near an electrode which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Up to 24 touch sensing electrodes can be controlled by the TSC. The touch sensing I/Os are organized in 8 acquisition groups, with up to 4 I/Os in each group.

Table 3. Capacitive sensing GPIOs available on STM32F373xx devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB14
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB15
	TSC_G2_IO3	PA6		TSC_G6_IO3	PD8
	TSC_G2_IO4	PA7		TSC_G6_IO4	PD9

Table 3. Capacitive sensing GPIOs available on STM32F373xx devices (continued)

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
3	TSC_G3_IO1	PC4	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PC5		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB0		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB1		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

Table 4. No. of capacitive sensing channels available on STM32F373xx devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F373Cx	STM32F373Rx	STM32F373Vx
G1	3	3	3
G2	2	3	3
G3	1	3	3
G4	3	3	3
G5	3	3	3
G6	2	2	3
G7	0	0	3
G8	0	0	3
Number of capacitive sensing channels	14	17	24

3.17 Timers and watchdogs

The STM32F373xx includes two 32-bit and nine 16-bit general-purpose timers, three basic timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
General-purpose	TIM2 TIM5	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM3, TIM4, TIM19	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	0
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	0
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7, TIM18	16-bit	Up	Any integer between 1 and 65536	Yes	0	0

3.17.1 General-purpose timers (TIM2 to TIM5, TIM12 to TIM17, TIM19)

There are eleven synchronizable general-purpose timers embedded in the STM32F373xx (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, 4, 5 and 19

  These five timers are full-featured general-purpose timers:

  – TIM2 and TIM5 have 32-bit auto-reload up/downcounters and 32-bit prescalers

  – TIM3, 4, and 19 have 16-bit auto-reload up/downcounters and 16-bit prescalers

  These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM12, 13, 14, 15, 16, 17

  These six timers general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM12 has 2 channels

  – TIM13 and TIM14 have 1 channel

  – TIM15 has 2 channels and 1 complementary channel

  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.17.2 Basic timers (TIM6, TIM7, TIM18)

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

3.17.3 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.17.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB1 clock (PCLK1) derived from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.17.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.18 Real-time clock (RTC) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either from V_{DD} supply when present or through the V_{BAT} pin. The backup registers are thirty two 32-bit registers used to store 128 bytes of user application data.

They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28th, 29th (leap year), 30th and 31st day of the month.
- 2 programmable alarms with wake up from Stop and Standby mode capability.
- Periodic wakeup unit with programmable resolution and period.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- 3 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.19 Inter-integrated circuit interface (I^2C)

Two I^2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes with 20 mA output drive. They support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I^2C analog and digital filters

-	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I^2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeout verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the application to wake up the MCU from Stop mode on address match.

The I^2C interfaces can be served by the DMA controller

Refer to *Table 7* for the differences between I2C1 and I2C2.

Table 7. STM32F373xx I^2C implementation

I^2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X

Table 7. STM32F373xx I²C implementation (continued)

I²C features(1)	I2C1	I2C2
SMBus	X	X
Wakeup from STOP	X	X

1. X = supported.

3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F373xx embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

All USARTs interfaces are able to communicate at speeds of up to 9 Mbit/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode, Smartcard mode (ISO/IEC 7816 compliant), autobaudrate feature and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

Refer to *Table 8* for the features of USART1, USART2 and USART3.

Table 8. STM32F373xx USART implementation

USART modes/features(1)	USART1	USART2	USART3
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode	X	X	X
Smartcard mode	X	X	X
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	X
LIN mode	X	X	X
Dual clock domain and wakeup from Stop mode	X	X	X
Receiver timeout interrupt	X	X	X
Modbus communication	X	X	X
Auto baud rate detection	X	X	X
Driver Enable	X	X	X

1. X = supported.

3.21 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I^2S)

Three SPIs are able to communicate at up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

Three standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All I2S interfaces can operate in half-duplex mode only.

Refer to *Table 9* for the features between SPI1, SPI2 and SPI3.

Table 9. STM32F373xx SPI/I2S implementation

SPI features[1]	SPI1	SPI2	SPI3
Hardware CRC calculation	X	X	X
Rx/Tx FIFO	X	X	X
NSS pulse mode	X	X	X
I2S mode	X	X	X
TI mode	X	X	X
I2S full-duplex mode	-	-	-

1. X = supported.

3.22 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.23 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.24 Universal serial bus (USB)

The STM32F373xx embeds an USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

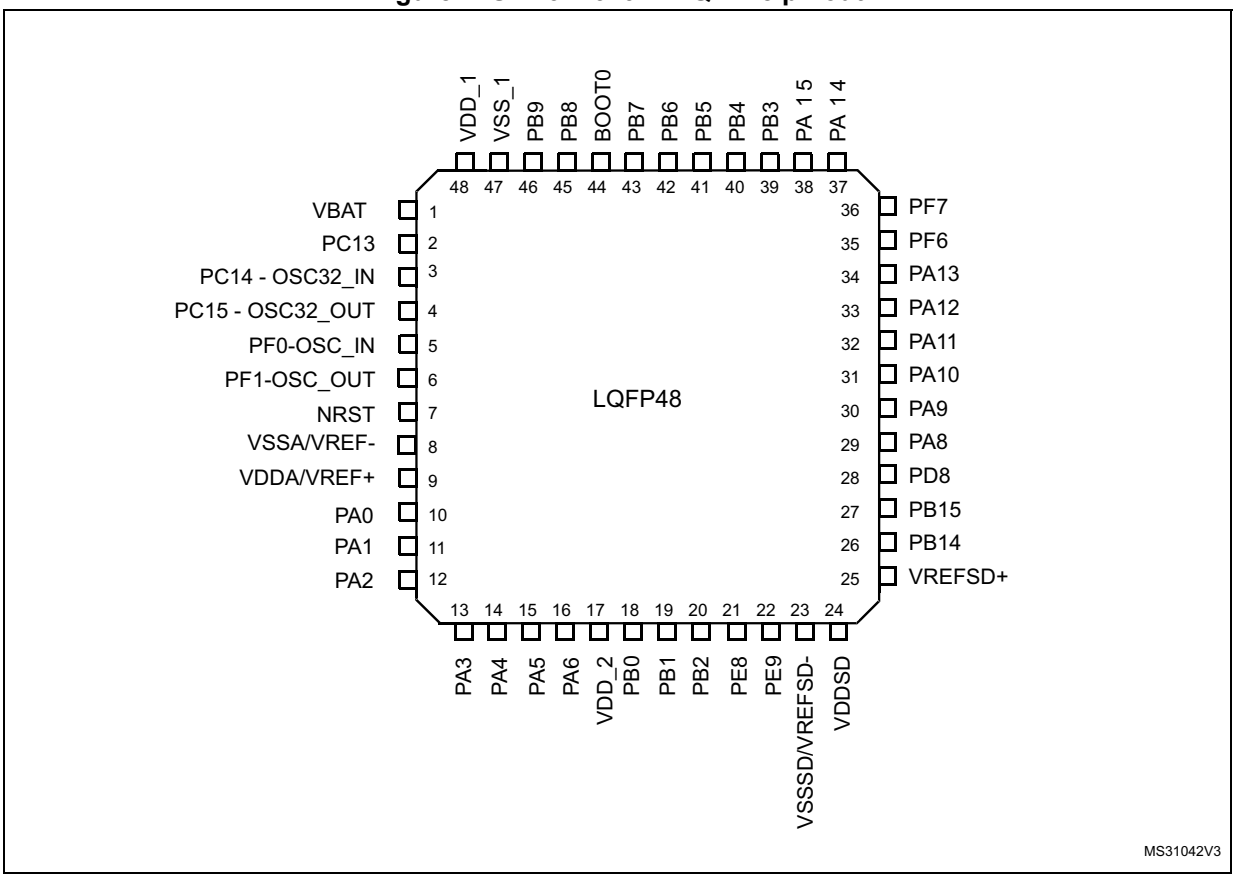
The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.26 Embedded trace macrocell™

The ARM embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F373xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

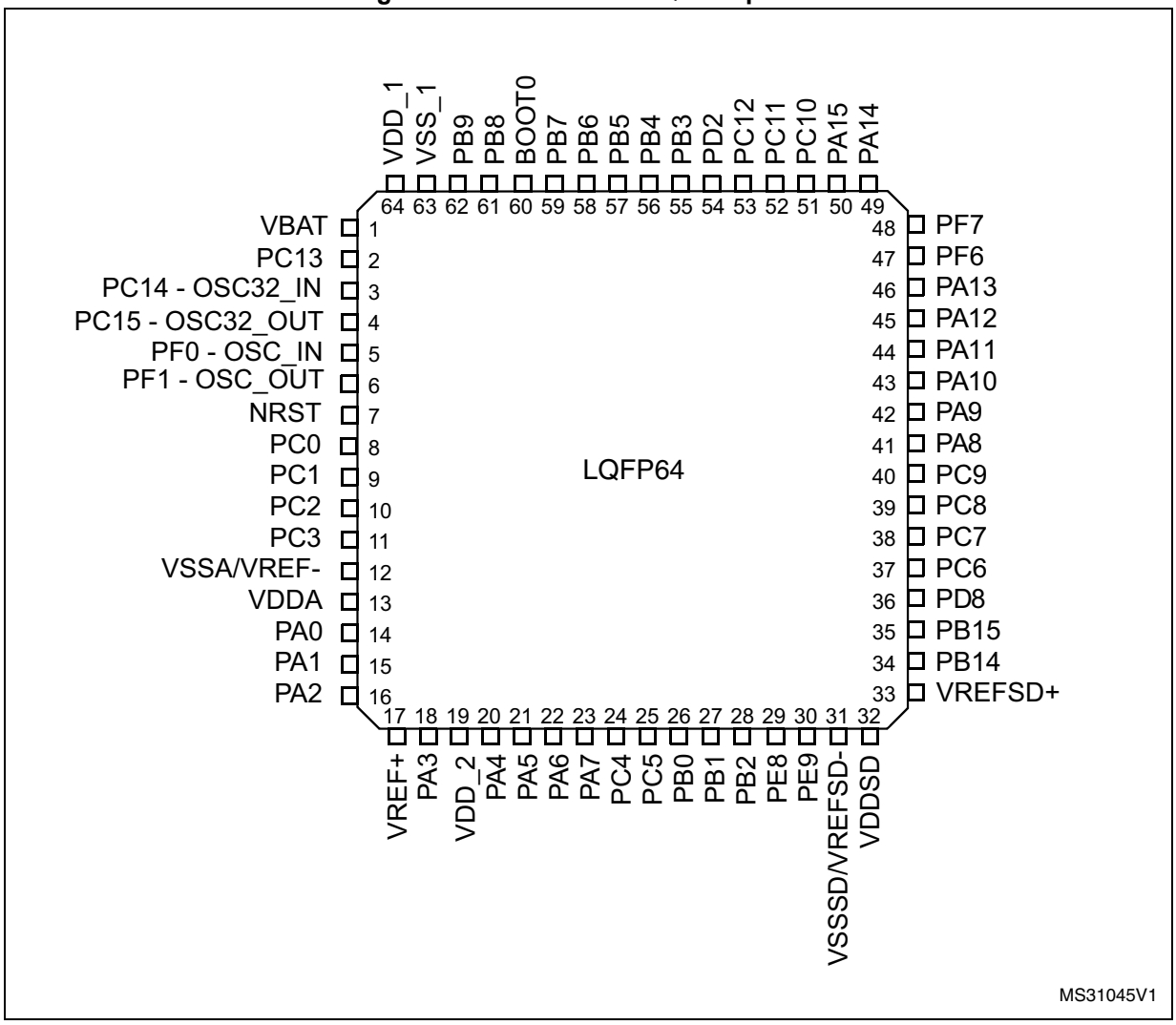
4 Pinouts and pin description

Figure 2. STM32F373xx LQFP48 pinout



1. The above figure shows the package top view.

Figure 3. STM32F373xx LQFP64 pinout



1. The above figure shows the package top view.

Figure 4. STM32F373xx LQFP100 pinout

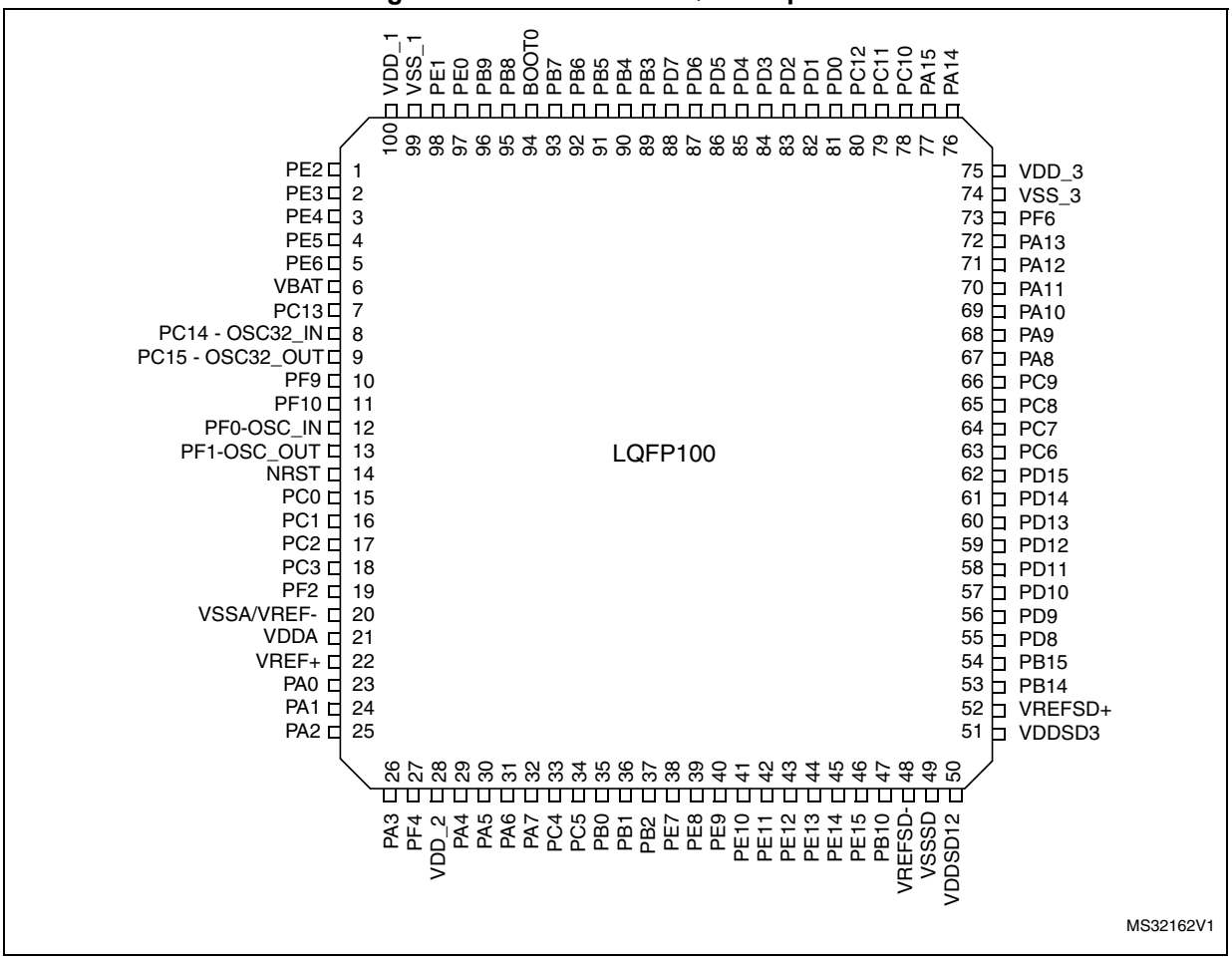
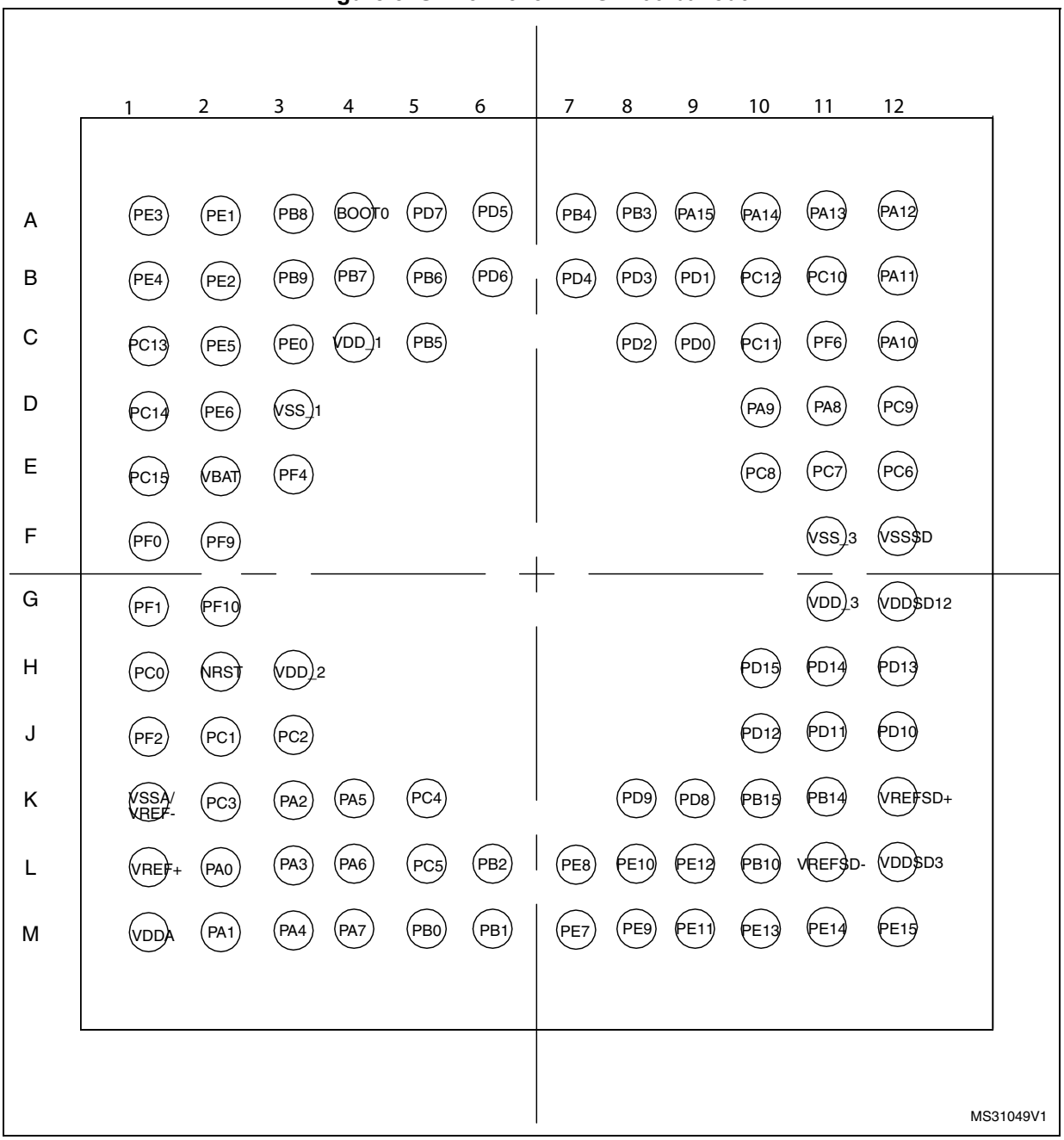


Figure 5. STM32F373xx BGA100 ballout



1. The above figure shows the package top view.

Table 10. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 11. STM32F373xx pin definitions

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
1	B2	-	-	PE2	I/O	FT	(2)	TSC_G7_IO1, TRACECLK	-
2	A1	-	-	PE3	I/O	FT	(2)	TSC_G7_IO2, TRACED0	-
3	B1	-	-	PE4	I/O	FT	(2)	TSC_G7_IO3, TRACED1	-
4	C2	-	-	PE5	I/O	FT	(2)	TSC_G7_IO4, TRACED2	-
5	D2	-	-	PE6	I/O	FT	(2)	TRACED3	WKUP3, RTC_TAMPER3
6	E2	1	1	VBAT	S	-	-	Backup power supply	
7	C1	2	2	PC13(1)	I/O	TC	-	-	WKUP2, ALARM_OUT, CALIB_OUT, TIMESTAMP, RTC_TAMPER1

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
8	D1	3	3	PC14 - OSC32_IN(1)	I/O	TC	-	-	OSC32_IN
9	E1	4	4	PC15 - OSC32_OUT(1)	I/O	TC	-	-	OSC32_OUT
10	F2	-	-	PF9	I/O	FT	(2)	TIM14_CH1	-
11	G2	-	-	PF10	I/O	FT	(2)	-	-
12	F1	5	5	PF0 - OSC_IN	I/O	FTf	-	I2C2_SDA	OSC_IN
13	G1	6	6	PF1 - OSC_OUT	I/O	FTf	-	I2C2_SCL	OSC_OUT
14	H2	7	7	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
15	H1	8	-	PC0	I/O	TTa	(2)	TIM5_CH1_ETR	ADC_IN10
16	J2	9	-	PC1	I/O	TTa	(2)	TIM5_CH2	ADCIN11
17	J3	10	-	PC2	I/O	TTa	(2)	SPI2_MISO/I2S2_MCK, TIM5_CH3	ADC_IN12
18	K2	11	-	PC3	I/O	TTa	(2)	SPI2_MOSI/I2S2_SD, TIM5_CH4	ADC_IN13
19	J1	-	-	PF2	I/O	FT	(2)	I2C2_SMBA	-
20	K1	12	8	VSSA/VREF-	S	-	-	Analog ground	
-	-	-	9	VDDA/VREF+	S	-	(2)	Analog power supply / Reference voltage for ADC, COMP, DAC	
21	M1	13	-	VDDA	S	-	(2)	Analog power supply	
22	L1	17	-	VREF+	S	-	(2)	Reference voltage for ADC, COMP, DAC	
23	L2	14	10	PA0	I/O	TTa	-	USART2_CTS, TIM2_CH1_ETR, TIM5_CH1_ETR, TIM19_CH1, TSC_G1_IO1, COMP1_OUT	RTC_ TAMPER2, WKUP1, ADC_IN0, COMP1_INM
24	M2	15	11	PA1	I/O	TTa	-	SPI3_SCK/I2S3_CK, USART2_RTS, TIM2_CH2, TIM15_CH1N, TIM5_CH2, TIM19_CH2, TSC_G1_IO2, RTC_REFIN	ADC_IN1, COMP1_INP

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
25	K3	16	12	PA2	I/O	TTa	-	COMP2_OUT, SPI3_MISO/I2S3_MCK, USART2_TX, TIM2_CH3, TIM15_CH1, TIM5_CH3, TIM19_CH3, TSC_G1_IO3	ADC_IN2, COMP2_INM
26	L3	18	13	PA3	I/O	TTa	-	SPI3_MOSI/I2S3_SD, USART2_RX, TIM2_CH4, TIM15_CH2, TIM5_CH4, TIM19_CH4, TSC_G1_IO4	ADC_IN3, COMP2_INP
27	E3	-	-	PF4	I/O	FT	(2)	-	
28	H3	19	17	VDD_2	S	-	-	Digital power supply	
29	M3	20	14	PA4	I/O	TTa	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, TIM3_CH2, TIM12_CH1, TSC_G2_IO1,	ADC_IN4, DAC1_OUT1
30	K4	21	15	PA5	I/O	TTa	-	SPI1_SCK/I2S1_CK, CEC, TIM2_CH1_ETR, TIM14_CH1, TIM12_CH2, TSC_G2_IO2	ADC_IN5, DAC1_OUT2
31	L4	22	16	PA6	I/O	TTa	-	SPI1_MISO/I2S1_MCK, COMP1_OUT, TIM3_CH1, TIM13_CH1, TIM16_CH1, TSC_G2_IO3	ADC_IN6, DAC2_OUT1,
32	M4	23	-	PA7	I/O	TTa	(2)	TSC_G2_IO4, TIM14_CH1, SPI1_MOSI/I2S1_SD, TIM17_CH1, TIM3_CH2, COMP2_OUT	ADC_IN7
33	K5	24	-	PC4	I/O	TTa	(2)	TIM13_CH1, TSC_G3_IO1, USART1_TX	ADC_IN14
34	L5	25	-	PC5	I/O	TTa	(2)	TSC_G3_IO2, USART1_RX	ADC_IN15
35	M5	26	18	PB0	I/O	TTa	-	SPI1_MOSI/I2S1_SD, TIM3_CH3, TSC_G3_IO3, TIM3_CH2	ADC_IN8, SDADC1_AIN6P
36	M6	27	19	PB1	I/O	TTa	-	TIM3_CH4, TSC_G3_IO4	ADC_IN9, SDADC1_AIN5P, SDADC1_AIN6M
37	L6	28	20	PB2	I/O	TC	(3)	-	SDADC1_AIN4P, SDADC2_AIN6P

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
38	M7	-	-	PE7	I/O	TC	(3) (2)	-	SDADC1_AIN3P, SDADC1_AIN4M, SDADC2_AIN5P, SDADC2_AIN6M
39	L7	29	21	PE8	I/O	TC	(3)	-	SDADC1_AIN8P, SDADC2_AIN8P
40	M8	30	22	PE9	I/O	TC	(3)	-	SDADC1_AIN7P, SDADC1_AIN8M, SDADC2_AIN7P, SDADC2_AIN8M
41	L8	-	-	PE10	I/O	TC	(3) (2)	-	SDADC1_AIN2P
42	M9	-	-	PE11	I/O	TC	(3) (2)	-	SDADC1_AIN1P, SDADC1_AIN2M, SDADC2_AIN4P
43	L9	-	-	PE12	I/O	TC	(3) (2)	-	SDADC1_AIN0P, SDADC2_AIN3P, SDADC2_AIN4M
44	M10	-	-	PE13	I/O	TC	(3) (2)	-	SDADC1_AIN0M , SDADC2_AIN2P
45	M11	-	-	PE14	I/O	TC	(3) (2)	-	SDADC2_AIN1P, SDADC2_AIN2M
46	M12	-	-	PE15	I/O	TC	(3) (2)	USART3_RX	SDADC2_AIN0P
47	L10	-	-	PB10	I/O	TC	(3) (2)	SPI2_SCK/I2S2_CK, USART3_TX, CEC, TSC_SYNC, TIM2_CH3	SDADC2_AIN0M
48	L11	-	-	VREFSD-	S	-	(2)	External reference voltage for SDADC1, SDADC2, SDADC3 (negative input), negative SDADC analog input in SDADC single ended mode	
49	F12	-	-	VSSSD	S	-	(2)	SDADC1, SDADC2, SDADC3 ground	
-	-	31	23	VSSSD/ VREFSD-	S	-	-	SDADC1, SDADC2, SDADC3 ground / External reference voltage for SDADC1, SDADC2, SDADC3 (negative input), negative SDADC analog input in SDADC single ended mode	
50	G12	-	-	VDDSD12	S	-	(2)	SDADC1 and SDADC2 power supply	
-	-	32	24	VDDSD	S	-	-	SDADC1, SDADC2, SDADC3 power supply	

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
51	L12	-	-	VDDSD3	S	-	(2)	SDADC3 power supply	
52	K12	33	25	VREFSD+	S	-	-	External reference voltage for SDADC1, SDADC2, SDADC3 (positive input)	
53	K11	34	26	PB14	I/O	TC	(4)	SPI2_MISO/I2S2_MCK, USART3_RTS, TIM15_CH1, TIM12_CH1, TSC_G6_IO1	SDADC3_AIN8P
54	K10	35	27	PB15	I/O	TC	(4)	SPI2_MOSI/I2S2_SD, TIM15_CH1N, TIM15_CH2, TIM12_CH2, TSC_G6_IO2, RTC_REFIN	SDADC3_AIN7P, SDADC3_AIN8M
55	K9	36	28	PD8	I/O	TC	(4)	SPI2_SCK/I2S2_CK, USART3_TX, TSC_G6_IO3	SDADC3_AIN6P
56	K8	-	-	PD9	I/O	TC	(4) (2)	USART3_RX, TSC_G6_IO4	SDADC3_AIN5P, SDADC3_AIN6M
57	J12	-	-	PD10	I/O	TC	(4) (2)	USART3_CK	SDADC3_AIN4P
58	J11	-	-	PD11	I/O	TC	(4) (2)	USART3_CTS	SDADC3_AIN3P, SDADC3_AIN4M
59	J10	-	-	PD12	I/O	TC	(4) (2)	USART3_RTS, TIM4_CH1, TSC_G8_IO1	SDADC3_AIN2P
60	H12	-	-	PD13	I/O	TC	(4) (2)	TIM4_CH2, TSC_G8_IO2	SDADC3_AIN1P, SDADC3_AIN2M
61	H11	-	-	PD14	I/O	TC	(4) (2)	TIM4_CH3, TSC_G8_IO3	SDADC3_AIN0P
62	H10	-	-	PD15	I/O	TC	(4) (2)	TIM4_CH4, TSC_G8_IO4	SDADC3_AIN0M
63	E12	37	-	PC6	I/O	FT	(2)	TIM3_CH1, SPI1_NSS/I2S1_WS	-
64	E11	38	-	PC7	I/O	FT	(2)	TIM3_CH2, SPI1_SCK/I2S1_CK,	-
65	E10	39	-	PC8	I/O	FT	(2)	SPI1_MISO/I2S1_MCK, TIM3_CH3	-
66	D12	40	-	PC9	I/O	FT	(2)	SPI1_MOSI/I2S1_SD, TIM3_CH4	-

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
67	D11	41	29	PA8	I/O	FT	-	SPI2_SCK/I2S2_CK, I2C2_SMBA, USART1_CK, TIM4_ETR, TIM5_CH1_ETR, MCO	-
68	D10	42	30	PA9	I/O	FTf	-	SPI2_MISO/I2S2_MCK, I2C2_SCL, USART1_TX, TIM2_CH3, TIM15_BKIN, TIM13_CH1, TSC_G4_IO1	-
69	C12	43	31	PA10	I/O	FTf	-	SPI2_MOSI/I2S2_SD, I2C2_SDA, USART1_RX, TIM2_CH4, TIM17_BKIN, TIM14_CH1, TSC_G4_IO2	-
70	B12	44	32	PA11	I/O	FT	-	SPI2_NSS/I2S2_WS, SPI1_NSS/I2S1_WS, USART1_CTS, CAN_RX, TIM4_CH1, USB_DM, TIM5_CH2, COMP1_OUT	-
71	A12	45	33	PA12	I/O	FT	-	SPI1_SCK/I2S1_CK, USART1_RTS, CAN_TX, USB_DP, TIM16_CH1, TIM4_CH2, TIM5_CH3, COMP2_OUT	-
72	A11	46	34	PA13	I/O	FT	-	SPI1_MISO/I2S1_MCK, USART3_CTS, IR_OUT, TIM16_CH1N, TIM4_CH3, TIM5_CH4, TSC_G4_IO3, SWDIO-JTMS	-
73	C11	47	35	PF6	I/O	FTf	-	SPI1_MOSI/I2S1_SD, USART3_RTS, TIM4_CH4, I2C2_SCL	-
74	F11	-	-	VSS_3	S	-	(2)	Ground	
75	G11	-	-	VDD_3	S	-	(2)	Digital power supply	
-	-	48	36	PF7	I/O	FTf	-	I2C2_SDA, USART2_CK	-
76	A10	49	37	PA14	I/O	FTf	-	I2C1_SDA, TIM12_CH1, TSC_G4_IO4, SWCLK-JTCK	-

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
77	A9	50	38	PA15	I/O	FTf	-	SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, I2C1_SCL, TIM2_CH1_ETR, TIM12_CH2, TSC_SYNC, JTDI	-
78	B11	51	-	PC10	I/O	FT	(2)	SPI3_SCK/I2S3_CK, USART3_TX, TIM19_CH1	-
79	C10	52	-	PC11	I/O	FT	(2)	SPI3_MISO/I2S3_MCK, USART3_RX, TIM19_CH2	-
80	B10	53	-	PC12	I/O	FT	(2)	SPI3_MOSI/I2S3_SD, USART3_CK, TIM19_CH3	-
81	C9	-	-	PD0	I/O	FT	(2)	CAN_RX, TIM19_CH4	-
82	B9	-	-	PD1	I/O	FT	(2)	CAN_TX, TIM19_ETR	-
83	C8	54	-	PD2	I/O	FT	(2)	TIM3_ETR	-
84	B8	-	-	PD3	I/O	FT	(2)	SPI2_MISO/I2S2_MCK, USART2_CTS	-
85	B7	-	-	PD4	I/O	FT	(2)	SPI2_MOSI/I2S2_SD, USART2_RTS	-
86	A6	-	-	PD5	I/O	FT	(2)	USART2_TX	-
87	B6	-	-	PD6	I/O	FT	(2)	SPI2_NSS/I2S2_WS, USART2_RX	-
88	A5	-	-	PD7	I/O	FT	(2)	SPI2_SCK/I2S2_CK, USART2_CK	-
89	A8	55	39	PB3	I/O	FT	-	SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART2_TX, TIM2_CH2, TIM3_ETR, TIM4_ETR, TIM13_CH1, TSC_G5_IO1, JTDO-TRACESWO	-
90	A7	56	40	PB4	I/O	FT	-	SPI1_MISO/I2S1_MCK, SPI3_MISO/I2S3_MCK, USART2_RX, TIM16_CH1, TIM3_CH1, TIM17_BKIN, TIM15_CH1N, TSC_G5_IO2, NJTRST	-

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48					Alternate function	Additional functions
91	C5	57	41	PB5	I/O	FT	-	SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, I2C1_SMBAI, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM17_CH1, TIM19_ETR	-
92	B5	58	42	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TIM3_CH3, TIM4_CH1, TIM19_CH1, TIM15_CH1, TSC_G5_IO3	-
93	B4	59	43	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N, TIM3_CH4, TIM4_CH2, TIM19_CH2, TIM15_CH2, TSC_G5_IO4	-
94	A4	60	44	BOOT0	I	B	-	Boot memory selection	
95	A3	61	45	PB8	I/O	FTf	-	SPI2_SCK/I2S2_CK, I2C1_SCL, USART3_TX, CAN_RX, CEC, TIM16_CH1, TIM4_CH3, TIM19_CH3, COMP1_OUT, TSC_SYNC	-
96	B3	62	46	PB9	I/O	FTf	-	SPI2_NSS/I2S2_WS, I2C1_SDA, USART3_RX, CAN_TX, IR_OUT, TIM17_CH1, TIM4_CH4, TIM19_CH4, COMP2_OUT	-
97	C3	-	-	PE0	I/O	FT	(2)	USART1_TX, TIM4_ETR	-
98	A2	-	-	PE1	I/O	FT	(2)	USART1_RX	-
99	D3	63	47	VSS_1	S	-	-	Ground	
100	C4	64	48	VDD_1	S	-	-	Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED)
   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0313 reference manual.
2. When using the small packages (48 and 64 pin packages), the GPIO pins which are not present on these packages, must not be configured in analog mode.
3. these pins are powered by VDDSD12.
4. these pins are powered by VDDSD3.

Table 12. Alternate functions for port PA

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA0	-	TIM2_ CH1_ ETR	TIM5_ CH1_ ETR	TSC_ G1_IO1	-	-	-	USART2_CTS	COMP1 _OUT	-	-	TIM19 _CH1	-	EVENT OUT
PA1	RTC_ REFIN	TIM2_ CH2	TIM5_ CH2	TSC_ G1_IO2	-	-	SPI3_SCK/ I2S3_CK	USART2_RTS	-	TIM15_ CH1N	-	TIM19 _CH2	-	EVENT OUT
PA2	-	TIM2_ CH3	TIM5_ CH3	TSC_ G1_IO3	-	-	SPI3_MISO/ I2S3_MCK	USART2_TX	COMP2 _OUT	TIM15_ CH1	-	TIM19 _CH3	-	EVENT OUT
PA3	-	TIM2_ CH4	TIM5_ CH4	TSC_ G1_IO4	-	-	SPI3_MOSI /I2S3_SD	USART2_RX	-	TIM15_ CH2	-	TIM19 _CH4	-	EVENT OUT
PA4	-	-	TIM3_ CH2	TSC_ G2_IO1	-	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	USART2_CK	-	-	TIM12 _CH1	-	-	EVENT OUT
PA5	-	TIM2_ CH1_ ETR	-	TSC_ G2_IO2	-	SPI1_SCK/ I2S1_CK	-	CEC	-	TIM14_ CH1	TIM12 _CH2	-	-	EVENT OUT
PA6	-	TIM16_ CH1	TIM3_ CH1	TSC_ G2_IO3	-	SPI1_MISO /I2S1_MCK	-	-	COMP1 _OUT	TIM13_ CH1	-	-	-	EVENT OUT
PA7	-	TIM17_ CH1	TIM3_ CH2	TSC_ G2_IO4	-	SPI1_MOSI /I2S1_SD	-	-	COMP2 _OUT	TIM14_ CH1	-	-	-	EVENT OUT
PA8	MCO	-	TIM5_ CH1_ ETR	-	I2C2_ SMBA	SPI2_SCK/ I2S2_CK	-	USART1_CK	-	-	TIM4_ ETR	-	-	EVENT OUT
PA9	-	-	TIM13 _CH1	TSC_ G4_IO1	I2C2_ SCL	SPI2_MISO /I2S2_MCK	-	USART1_TX	-	TIM15_ BKIN	TIM2_ CH3	-	-	EVENT OUT
PA10	-	TIM17_ BKIN	-	TSC_ G4_IO2	I2C2_ SDA	SPI2_MOSI /I2S2_SD	-	USART1_RX	-	TIM14_ CH1	TIM2_ CH4	-	-	EVENT OUT
PA11	-	-	TIM5_ CH2	-	-	SPI2_NSS/ I2S2_WS	SPI1_NSS/ I2S1_WS	USART1_CTS	COMP1 _OUT	CAN_ RX	TIM4_ CH1	-	-	EVENT OUT
PA12	-	TIM16_ CH1	TIM5_ CH3	-	-	-	SPI1_SCK/ I2S1_CK	USART1_RTS	COMP2 _OUT	CAN_TX	TIM4_ CH2	-	-	EVENT OUT

Table 12. Alternate functions for port PA (continued)

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA13	SWDIO -JTMS	TIM16_ CH1N	TIM5_ CH4	TSC_ G4_IO3	-	IR-OUT	SPI1_MISO /I2S1_MCK	USART3_CTS	-	-	TIM4_ CH3	-	-	EVENT OUT
PA14	SWCLK -JTCK	-	-	TSC_ G4_IO4	I2C1_ SDA	-	-	-	-	-	TIM12 _CH1	-	-	EVENT OUT
PA15	JTDI	TIM2_ CH1_ETR	-	TSC_ SYNC	I2C1_ SCL	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	-	-	-	TIM12 _CH2	-	-	EVENT OUT

Table 13. Alternate functions for port PB

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF15
PB0	-	-	TIM3_CH3	TSC_ G3_IO3	-	SPI_MOSI/ I2S1_SD	-	-	-	-	TIM3_ CH2	-	EVENTOUT
PB1	-	-	TIM3_CH4	TSC_ G3_IO4	-	-	-	-	-	-	-	-	EVENTOUT
PB2	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PB3	JTDO-TRACESWO	TIM2_ CH2	TIM4_ETR	TSC_ G5_IO1	-	SPI1_SCK/ I2S1_CK	SPI3_SCK/ I2S3_CK	USART2_TX	-	TIM13_ CH1	TIM3_ ETR	-	EVENTOUT
PB4	NJTRST	TIM16_ CH1	TIM3_CH1	TSC_ G5_IO2	-	SPI1_MISO /I2S1_MCK	SPI3_MISO/ I2S3_MCK	USART2_RX	-	TIM15_ CH1N	TIM17 _BKIN	-	EVENTOUT
PB5	-	TIM16_ BKIN	TIM3_CH2	-	I2C1_ SMBA	SPI1_MOSI /I2S1_SD	SPI3_MOSI /I2S3_SD	USART2_CK	-	-	TIM17 _CH1	TIM19 _ETR	EVENTOUT
PB6	-	TIM16_ CH1N	TIM4_CH1	TSC_ G5_IO3	I2C1_ SCL	-	-	USART1_TX	-	TIM15_ CH1	TIM3_ CH3	TIM19 _CH1	EVENTOUT
PB7	-	TIM17_ CH1N	TIM4_CH2	TSC_ G5_IO4	I2C1_ SDA	-	-	USART1_RX	-	TIM15_ CH2	TIM3_ CH4	TIM19 _CH2	EVENTOUT
PB8	-	TIM16_ CH1	TIM4_CH3	TSC_ SYNC	I2C1_ SCL	SPI2_SCK/ I2S2_CK	CEC	USART3_TX	COMP1 _OUT	CAN_ RX	-	TIM19 _CH3	EVENTOUT
PB9	-	TIM17_ CH1	TIM4_CH4	-	I2C1_ SDA	SPI2_NSS/ I2S2_WS	IR-OUT	USART3_RX	COMP2 _OUT	CAN_ TX	-	TIM19 _CH4	EVENTOUT
PB10	-	TIM2_ CH3	-	TSC_ SYNCH	-	SPI2_SCK/ I2S2_CK	CEC	USART3_TX	-	-	-	-	EVENTOUT
PB14	-	TIM15_ CH1	-	TSC_ G6_IO1	-	SPI2_MISO /I2S2_MCK	-	USART3_RTS	-	TIM12_ CH1	-	-	EVENTOUT
PB15	RTC_REFIN	TIM15_ CH2	TIM15_ CH1N	TSC_ G6_IO2	-	SPI2_MOSI /I2S2_SD	-	-	-	TIM12_ CH2	-	-	EVENTOUT

Table 14. Alternate functions for port PC

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	-	EVENTOUT	TIM5_CH1_ETR	-	-	-	-	-
PC1	-	EVENTOUT	TIM5_CH2	-	-	-	-	-
PC2	-	EVENTOUT	TIM5_CH3	-	-	SPI2_MISO/I2S2_MCK	-	-
PC3	-	EVENTOUT	TIM5_CH4	-	-	SPI2_MOSI/I2S2_SD	-	-
PC4	-	EVENTOUT	TIM13_CH1	TSC_G3_IO1	-	-	-	USART1_TX
PC5	-	EVENTOUT	-	TSC_G3_IO2	-	-	-	USART1_RX
PC6	-	EVENTOUT	TIM3_CH1	-	-	SPI1_NSS/I2S1_WS	-	-
PC7	-	EVENTOUT	TIM3_CH2	-	-	SPI1_SCK/I2S1_CK	-	-
PC8	-	EVENTOUT	TIM3_CH3	-	-	SPI1_MISO/I2S1_MCK	-	-
PC9	-	EVENTOUT	TIM3_CH4	-	-	SPI1_MOSI/I2S1_SD	-	-
PC10	-	EVENTOUT	TIM19_CH1	-	-	-	SPI3_SCK/I2S3_CK	USART3_TX
PC11	-	EVENTOUT	TIM19_CH2	-	-	-	SPI3_MISO/I2S3_MCK	USART3_RX
PC12	-	EVENTOUT	TIM19_CH3	-	-	-	SPI3_MOSI/I2S3_SD	USART3_CK
PC13	-	-	-	-	-	-	-	-
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-

Table 15. Alternate functions for port PD

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	EVENTOUT	TIM19_CH4	-	-	-	-	CAN_RX
PD1	-	EVENTOUT	TIM19_ETR	-	-	-	-	CAN_TX
PD2	-	EVENTOUT	TIM3_ETR	-	-	-	-	-
PD3	-	EVENTOUT	-	-	-	SPI2_MISO/I2S2_MCK	-	USART2_CTS
PD4	-	EVENTOUT	-	-	-	SPI2_MOSI/I2S2_SD	-	USART2_RTS
PD5	-	EVENTOUT	-	-	-	-	-	USART2_TX
PD6	-	EVENTOUT	-	-	-	SPI2_NSS/I2S2_WS	-	USART2_RX
PD7	-	EVENTOUT	-	-	-	SPI2_SCK/I2S2_CK	-	USART2_CK
PD8	-	EVENTOUT	-	TSC_G6_IO3	-	SPI2_SCK/I2S2_CK	-	USART3_TX
PD9	-	EVENTOUT	-	TSC_G6_IO4	-	-	-	USART3_RX
PD10	-	EVENTOUT	-	-	-	-	-	USART3_CK
PD11	-	EVENTOUT	-	-	-	-	-	USART3_CTS
PD12	-	EVENTOUT	TIM4_CH1	TSC_G8_IO1	-	-	-	USART3_RTS
PD13	-	EVENTOUT	TIM4_CH2	TSC_G8_IO2	-	-	-	-
PD14	-	EVENTOUT	TIM4_CH3	TSC_G8_IO3	-	-	-	-
PD15	-	EVENTOUT	TIM4_CH4	TSC_G8_IO4	-	-	-	-

Table 16. Alternate functions for port PE

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE0	-	EVENTOUT	TIM4_ETR	-	-	-	-	USART1_TX
PE1	-	EVENTOUT	-	-	-	-	-	USART1_RX
PE2	TRACECLK	EVENTOUT	-	TSC_G7_IO1	-	-	-	-
PE3	TRACED0	EVENTOUT	-	TSC_G7_IO2	-	-	-	-
PE4	TRACED1	EVENTOUT	-	TSC_G7_IO3	-	-	-	-
PE5	TRACED2	EVENTOUT	-	TSC_G7_IO4	-	-	-	-
PE6	TRACED3	EVENTOUT	-	-	-	-	-	-
PE7	-	EVENTOUT	-	-	-	-	-	-
PE8	-	EVENTOUT	-	-	-	-	-	-
PE9	-	EVENTOUT	-	-	-	-	-	-
PE10	-	EVENTOUT	-	-	-	-	-	-
PE11	-	EVENTOUT	-	-	-	-	-	-
PE12	-	EVENTOUT	-	-	-	-	-	-
PE13	-	EVENTOUT	-	-	-	-	-	-
PE14	-	EVENTOUT	-	-	-	-	-	-
PE15	-	EVENTOUT	-	-	-	-	-	USART3_RX

Table 17. Alternate functions for port PF

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	-	-	-	-	I2C2_SDA	-	-	-
PF1	-	-	-	-	I2C2_SCL	-	-	-
PF2	-	EVENTOUT	-	-	I2C2_SMBA	-	-	-
PF4	-	EVENTOUT	-	-	-	-	-	-
PF6	-	EVENTOUT	TIM4_CH4	-	I2C2_SCL	SPI1_MOSI/I2S1_SD	-	USART3_RTS
PF7	-	EVENTOUT	-	-	I2C2_SDA	-	-	USART2_CK
PF9	-	EVENTOUT	TIM14_CH1	-	-	-	-	-
PF10	-	EVENTOUT	-	-	-	-	-	-

5 Memory mapping

Figure 6. STM32F373xx memory map

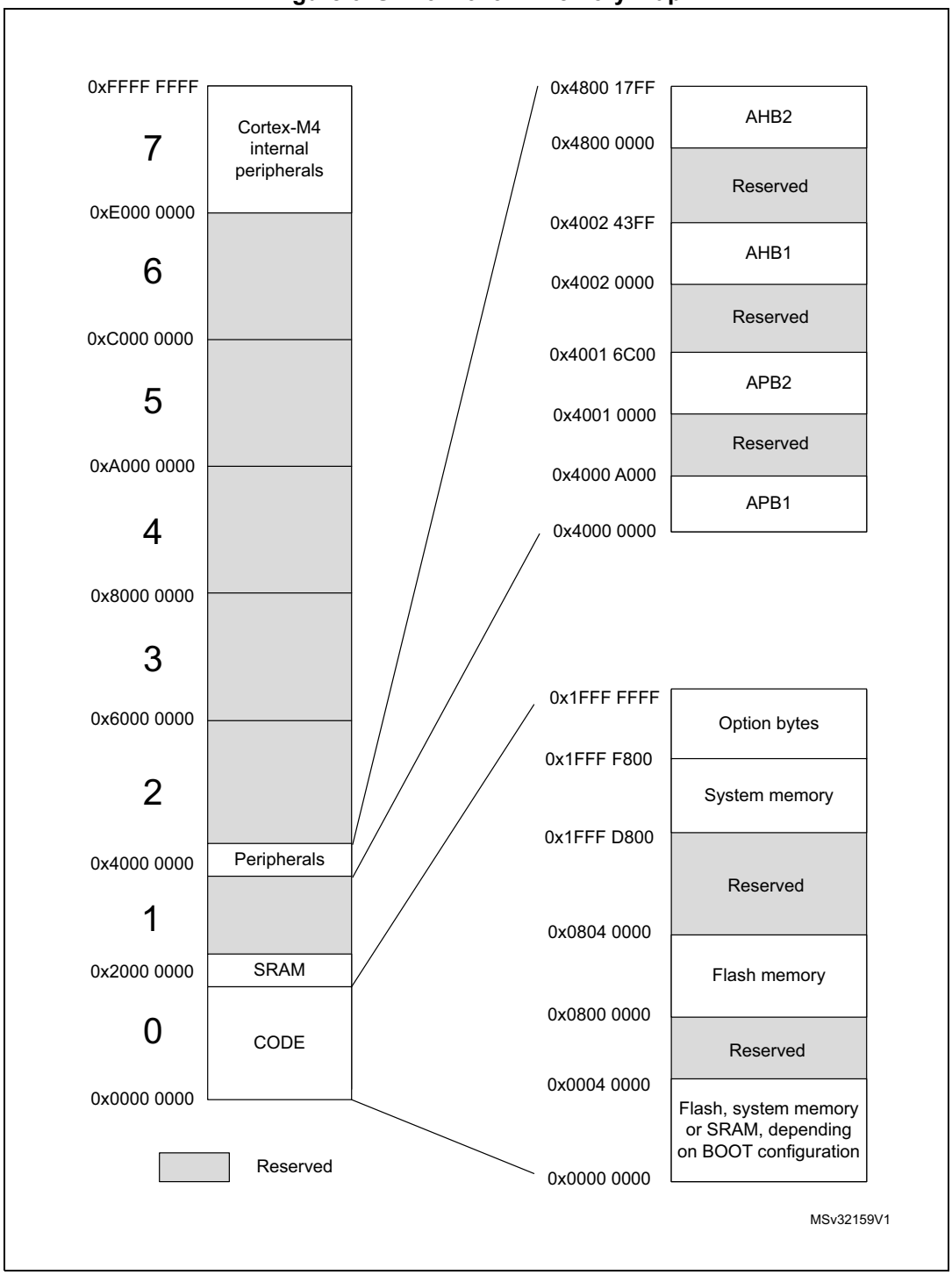


Table 18. STM32F373xx peripheral register boundary addresses(1)

Bus	Boundary address	Size	Peripheral
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800- 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1
-	0x4001 6C00 - 0x4001 FFFF	37 KB	Reserved

Table 18. STM32F373xx peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size	Peripheral
APB2	0x4001 6800 - 0x4001 6BFF	1 KB	SDADC3
	0x4001 6400 - 0x4001 67FF	1 KB	SDADC2
	0x4001 6000 - 0x4001 63FF	1 KB	SDADC1
	0x4001 5C00 - 0x4001 5FFF	1 KB	TIM19
	0x4001 4C00 - 0x4001 5BFF	4 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
	0x4001 2800 - 0x4001 2FFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG + COMP
-	0x4000 4000 - 0x4000 FFFF	24 KB	Reserved
APB1	0x4000 9C00 – 0x4000 9FFF	1 KB	TIM18
	0x4000 9800 - 0x4000 9BFF	1 KB	DAC2
	0x4000 7C00 - 0x4000 97FF	8 KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC
	0x4000 7400 - 0x4000 77FF	1 KB	DAC1
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6800 - 0x4000 6FFF	2 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	CAN
	0x4000 6000 - 0x4000 63FF	1 KB	USB packet SRAM
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB FS

Table 18. STM32F373xx peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size	Peripheral
APB1	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4C00 - 0x4000 53FF	2 KB	Reserved
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1C00 - 0x4000 1FFF	1 KB	TIM13
	0x4000 1800 - 0x4000 1BFF	1 KB	TIM12
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. Cells in gray indicate Reserved memory locations.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = V_{DDSDx} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC and SDADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 7. Pin loading conditions

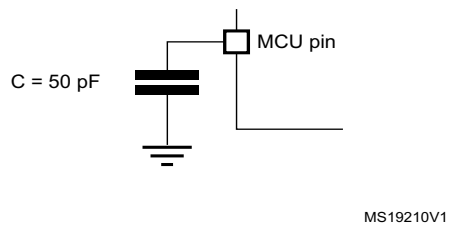
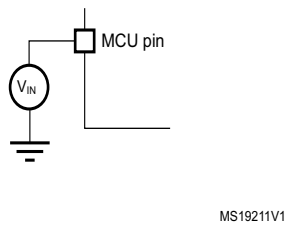
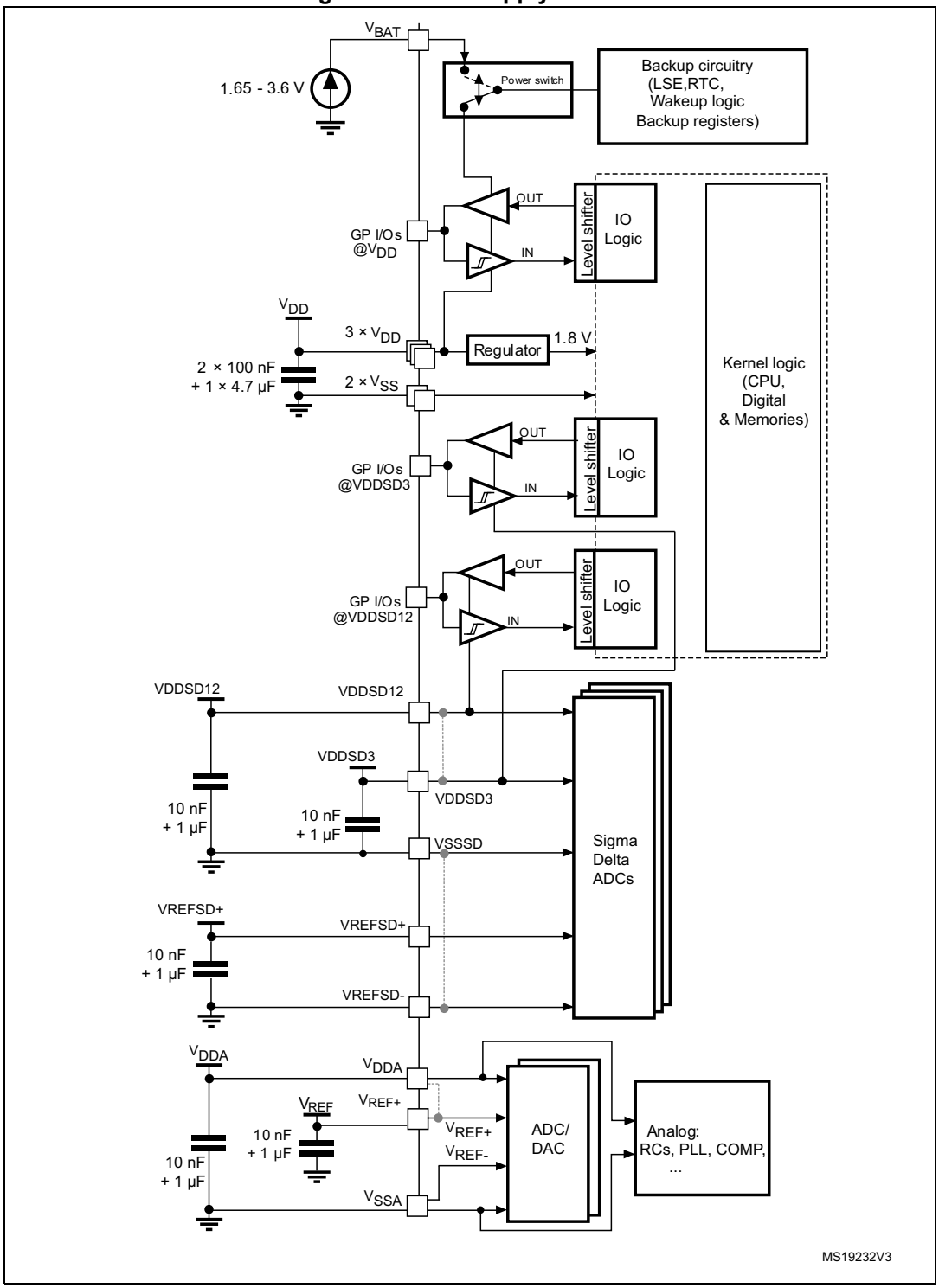


Figure 8. Pin input voltage



6.1.6 Power supply scheme

Figure 9. Power supply scheme

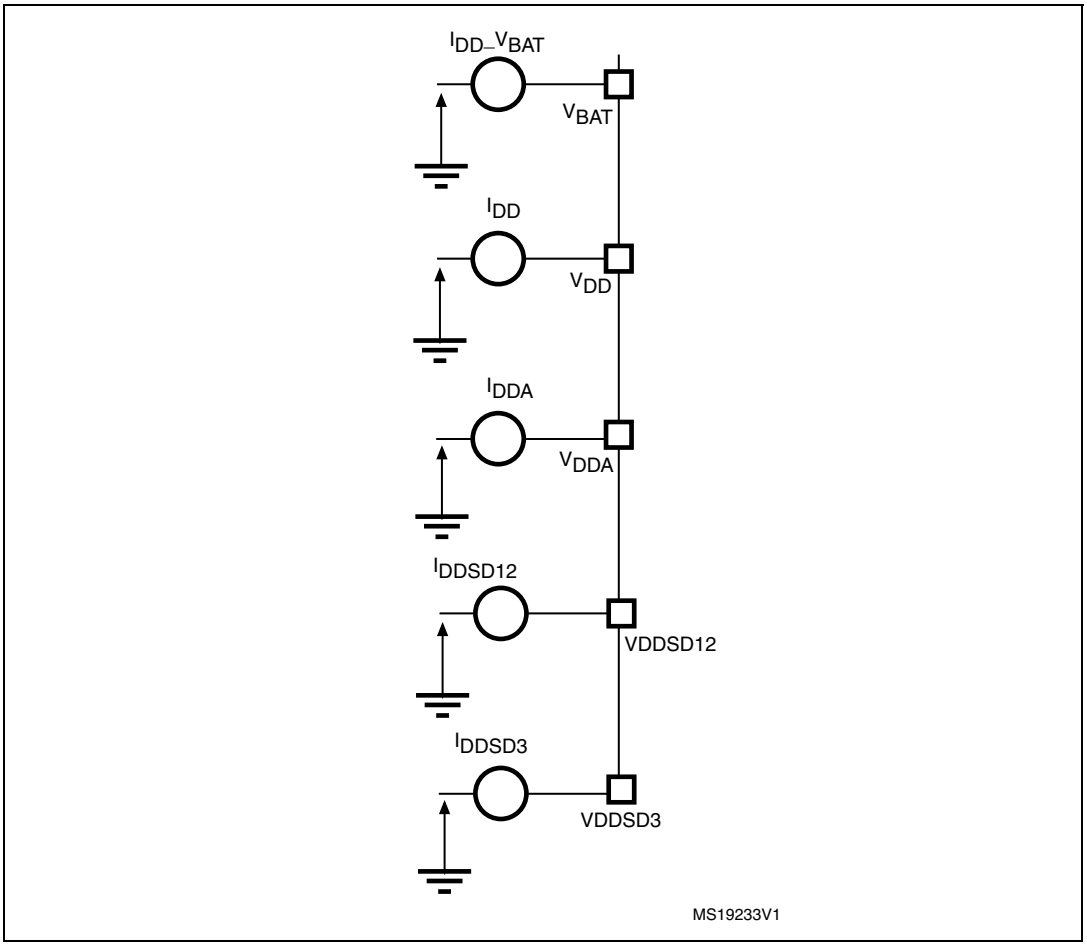


1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics*, and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
$V_{DD}–V_{SS}$	External main supply voltage (including V_{DDA}, V_{DDSDx}, V_{BAT} and V_{DD})	–0.3	4.0	V
$V_{DD}–V_{DDA}$	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	
$V_{DDSDx} – V_{DDA}$	Allowed voltage difference for $V_{DDSDx} > V_{DDA}$	-	0.4	
$V_{REFSD+} – V_{DDSD3}$	Allowed voltage difference for $V_{REFSD+} > V_{DDSD3}$	-	0.4	
$V_{REF+} – V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DD} + 4.0	
	Input voltage on TTa pins	V_{SS} –0.3	4.0	
	Input voltage on TC pins on SDADCx channels inputs(3)	V_{SS} –0.3	4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|V_{SSX} – V_{SS}\|$	Variations between all the different ground pins	-	50	mV
$\|V_{REFSD} – V_{SSx}\|$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 20: Current characteristics* for the maximum allowed injected current values.
3. VDDSD12 is the external power supply for PB2, PB10, and PE7 to PE15 I/O pins (I/O ground pin is internally connected to V_{SS}). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (I/O ground pin is internally connected to V_{SS}).

All main power (V_{DD}, V_{DDSD12}, V_{DDSD3} and V_{DDA}) and ground (V_{SS}, V_{SSSD}, and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

The following relationship must be respected between V_{DDA} and V_{DD}: V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence. V_{DDA} must be greater than or equal to V_{DD}.

The following relationship must be respected between V_{DDA} and V_{DDSD12}: V_{DDA} must power on before or at the same time as V_{DDSD12} or V_{DDSD3} in the power up sequence. V_{DDA} must be greater than or equal to V_{DDSD12} or V_{DDSD3}.

The following relationship must be respected between V_{DDSD12} and V_{DDSD3}: V_{DDSD3} must power on before or at the same time as V_{DDSD12} in the power up sequence.
After power up (V_{DDSD12} > Vrefint = 1.2 V) V_{DDSD3} can be higher or lower than V_{DDSD12}.

The following relationship must be respected between V_{REFSD+} and V_{DDSD12}, V_{DDSD3}: V_{REFSD+} must be lower than V_{DDSD3}.
Depending on the SDADCx operation mode, there can be more constraints between V_{REFSD+}, V_{DDSD12} and V_{DDSD3} which are described in reference manual RM0313.

Table 20. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x and VDDSDx power lines (source)(1)	160	mA
ΣI_{VSS}	Total current out of sum of all VSS_x and VSSSD ground lines (sink)(1)	-160	
$I_{VDD(PIN)}$	Maximum current into each VDD_x or VDDSDx power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS_x or VSSSD ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on FT, FTf and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. VDDSD12 is the external power supply for the PB2, PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to V_{SS}). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to V_{SS}). V_{DD} (VDD_x) is the external power supply for all remaining I/O pins (the I/O pin ground is internally connected to V_{SS}).
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 19: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN}>V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 62*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	Must have a potential equal to or lower than V_{DDA}	2.0	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC and DAC used)	Must have a potential equal to or higher than V_{DD}	2.4	3.6	V
	Analog operating voltage (ADC and DAC not used)		2.0	3.6	
V_{DDSD12}	VDDSD12 operating voltage (SDADC used)	Must have a potential equal to or lower than V_{DDA}	2.2	3.6	V
	VDDSD12 operating voltage (SDADC not used)		2.0	3.6	
V_{DDSD3}	VDDSD3 operating voltage (SDADC used)	Must have a potential equal to or lower than V_{DDA}	2.2	3.6	V
	VDDSD3 operating voltage (SDADC not used)		2.0	3.6	
V_{REF+}	Positive reference voltage (ADC and DAC used)	Must have a potential equal to or lower than V_{DDA}	2.4	3.6	V
	Positive reference voltage (ADC and DAC not used)		2.0	3.6	
V_{REFSD+}	SDADCx positive reference voltage	Must have a potential equal to or lower than any V_{DDSDx}	1.1	3.6	V
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	Input voltage on FT and FTf pins(2)	-	- 0.3	5.5	V
	Input voltage on TTa pins		- 0.3	V_{DDA} + 0.3	
	Input voltage on TC pins on SDADCx channels inputs(3)		- 0.3	V_{DDSDx} + 0.3	
	Input voltage on BOOT0 pin		0	5.5	
	Input voltage on any other pin		- 0.3	V_{DD} + 0.3	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	LQFP100	-	434	mW
		LQFP64	-	444	
		LQFP48	-	364	
		BGA100	-	338	

Table 22. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(5)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(5)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 60: ADC characteristics*.
2. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
3. VDDSD12 is the external power supply for the PB2, PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to VSS). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to VSS).
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 23* are derived from tests performed under the ambient temperature condition summarized in *Table 22*.

Table 23. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge	1.80(2)	1.88	1.96	V
		Rising edge	1.84	1.92	2.00	V
$V_{PDRhyst}$(3)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(3)	POR reset temporization	-	1.50	2.50	4.50	ms

1. The PDR detector monitors V_{DD}, V_{DDA} and V_{DDSD12} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design, not tested in production.

Table 25. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.10	2.18	2.26	V
		Falling edge	2.00	2.08	2.16	V
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3.00	V
		Falling edge	2.66	2.78	2.90	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
IDD(PVD)(2)	PVD current consumption	-	-	0.15	0.26	µA

1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 27* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 26. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

Table 27. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.21	1.26	V
		–40 °C < T_A < +85 °C	1.16	1.20	1.24(1)	
$T_{S_vrefint}$(2)	ADC sampling time when reading the internal reference voltage	-	17.10	-	-	µs
V_{REFINT_s}(3)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10	mV
T_{Coeff}(3)	Temperature coefficient	-	-	-	100	ppm/°C
t_{START}(3)	Startup time	-	-	-	10	µs

1. Data based on characterization results, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.
3. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{APB1} = f_{AHB}/2$, $f_{APB2} = f_{AHB}$
- When f_{HCLK} > 8 MHz PLL is ON and PLL inputs is equal to HSI/2 = 4 MHz (if internal clock is used) or HSE = 8 MHz (if HSE bypass mode is used)

The parameters given in *Table 28* to *Table 34* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 28. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V(1)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from Flash	HSE bypass, PLL on	72 MHz	63.1	70.7	71.5	73.4	29.2	31.1	31.7	34.2	mA
			64 MHz	56.3	63.3	64.1	64.9	26.1	27.8	28.4	30.4	
			48 MHz	42.5	48.5	48.0	50.1	19.9	22.6	21.9	23.1	
			32 MHz	28.8	31.4	32.2	34.3	13.1	16.1	14.9	16.2	
			24 MHz	21.9	24.4	24.4	25.8	10.1	10.9	11.9	12.4	
		HSE bypass, PLL off	8 MHz	7.3	8.0	9.3	9.3	3.7	4.1	4.4	5.0	
			1 MHz	1.1	1.5	1.8	2.3	0.8	1.1	1.4	1.9	
		HSI clock, PLL on	64 MHz	51.7	57.7	58.0	60.4	25.8	27.6	28.1	30.1	
			48 MHz	38.6	45.9	43.5	46.9	19.8	21.9	21.7	22.8	
			32 MHz	26.4	31.1	29.7	31.9	13.1	15.7	14.8	16.2	
			24 MHz	20.3	22.6	22.6	23.7	6.9	7.5	8.1	8.8	
		HSI clock, PLL off	8 MHz	7.0	7.6	8.8	8.8	3.7	4.1	4.4	5.0	

Table 28. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V(1)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from RAM	HSE bypass, PLL on	72 MHz	63.6 (3)	70.7(3)	75.7(3)	72.3(3)	30.0 (3)	31.9(3)	32.6(3)	33.8(3)	mA
			64 MHz	56.7	62.5	67.1	64.0	26.7	28.6	29.3	30.0	
			48 MHz	42.0	50.5	47.4	50.1	20.2	21.5	22.1	22.7	
			32 MHz	28.3	32.1	31.8	33.7	13.4	14.6	14.8	15.7	
			24 MHz	21.1	25.0	24.2	25.9	10.0	11.3	11.2	12.6	
		HSE bypass, PLL off	8 MHz	6.9	7.4	8.3	8.7	3.4	3.7	4.1	4.8	
			1 MHz	0.8	1.2	1.5	2.0	0.4	0.6	1.0	1.5	
		HSI clock, PLL on	64 MHz	51.9	59.5	59.4	58.6	26.4	28.1	28.7	29.5	
			48 MHz	38.1	44.7	43.8	45.4	20.0	21.3	21.9	22.3	
			32 MHz	25.9	31.2	29.4	30.5	13.2	14.3	14.6	15.5	
			24 MHz	19.6	22.7	22.6	23.2	6.5	7.0	7.9	8.2	
		HSI clock, PLL off	8 MHz	6.6	7.1	8.0	8.4	3.3	3.7	4.0	4.7	
	Supply current in Sleep mode, code executing from Flash or RAM	HSE bypass, PLL on	72 MHz	43.2	46.9	48.7	52.5	6.7	7.2	7.6	8.3	
			64 MHz	38.5	41.6	43.7	46.6	5.9	6.5	6.8	7.5	
			48 MHz	29.1	31.3	32.5	34.1	4.5	4.9	5.3	5.9	
			32 MHz	19.4	21.1	24.6	23.0	3.0	3.4	3.8	4.4	
			24 MHz	14.7	16.1	18.5	17.6	2.4	2.6	3.0	3.6	
		HSE bypass, PLL off	8 MHz	4.9	5.3	6.1	6.6	0.8	1.0	1.4	1.9	
			1 MHz	0.6	0.9	1.3	1.8	0.1	0.3	0.6	1.2	
		HSI clock, PLL on	64 MHz	34.5	37.1	39.6	42.0	5.6	6.1	6.5	7.1	
			48 MHz	26.1	28.0	29.0	30.7	4.2	4.6	5.0	5.6	
			32 MHz	17.4	19.1	21.1	20.8	2.9	3.2	3.6	4.2	
			24 MHz	13.3	14.6	16.1	16.0	1.5	1.8	2.2	2.6	
		HSI clock, PLL off	8 MHz	4.5	4.9	5.5	6.1	0.7	0.9	1.3	1.8	

1. To calculate complete device consumption there must be added consumption from VDDA (*Table 29.*).
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production with code executing from RAM.

Table 29. Typical and maximum current consumption from V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA}= 2.4 V				V_{DDA}= 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash or RAM	HSE bypass, PLL on	72 MHz	228	261	274	280	249	288	304	311	µA
			64 MHz	201	235	247	251	220	257	269	275	
			48 MHz	152	182	190	195	164	196	208	212	
			32 MHz	104	132	137	141	112	141	147	150	
			24 MHz	81	108	112	111	87	115	119	119	
		HSE bypass, PLL off	8 MHz	2	4	4	5	3	5	5	6	
			1 MHz	2	4	5	5	3	5	5	6	
		HSI clock, PLL on	64 MHz	270	307	320	326	298	337	353	361	
			48 MHz	220	254	264	269	243	276	292	297	
			32 MHz	172	203	211	214	191	222	232	235	
			24 MHz	151	181	185	189	166	194	201	204	
		HSI clock, PLL off	8 MHz	70	85	87	87	81	93	96	98	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.

Table 30. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ@V_{DD} (V_{DD}=V_{DDA})						Max			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DD}	Supply current in Stop mode	Regulators in run mode, all oscillators OFF	19.33	19.58	19.68	19.73	19.76	19.84	46.5	480	1019	µA
		Regulators in low-power mode, all oscillators OFF	7.72	7.88	8.01	8.13	8.25	8.27	31.8	451.4	966.0	
	Supply current in Standby mode	LSI ON and IWDG ON	0.78	0.95	1.07	1.21	1.32	1.45	-	-	-	
		LSI OFF and IWDG OFF	0.61	0.72	0.81	0.90	0.98	1.08	2.7	3.5	5.3	

Note: *V_{DDA} monitoring is OFF and V_{DDSD12} monitoring is OFF.*
To calculate complete device consumption there must be added consumption from V_{DDA} (*Table 31.*)

Table 31. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ@V_{DD} (V_{DD}=V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} and V_{DDSD12}	Regulator in run mode, all oscillators OFF	1.99	2.07	2.19	2.33	2.46	2.64	10.8	11.8	12.4	µA
			Regulator in low-power mode, all oscillators OFF	1.99	2.07	2.18	2.32	2.47	2.63	10.6	11.5	12.5	
	Supply current in Standby mode		LSI ON and IWDG ON	2.44	2.53	2.7	2.89	3.09	3.33	-	-	-	
			LSI OFF and IWDG OFF	1.87	1.94	2.06	2.19	2.35	2.51	4.1	4.5	4.8	
IDDAmon	Supply current for V_{DDA} and V_{DDSD12} monitoring	-		0.95	1.02	1.12	1.2	1.27	1.4	-	-	-	

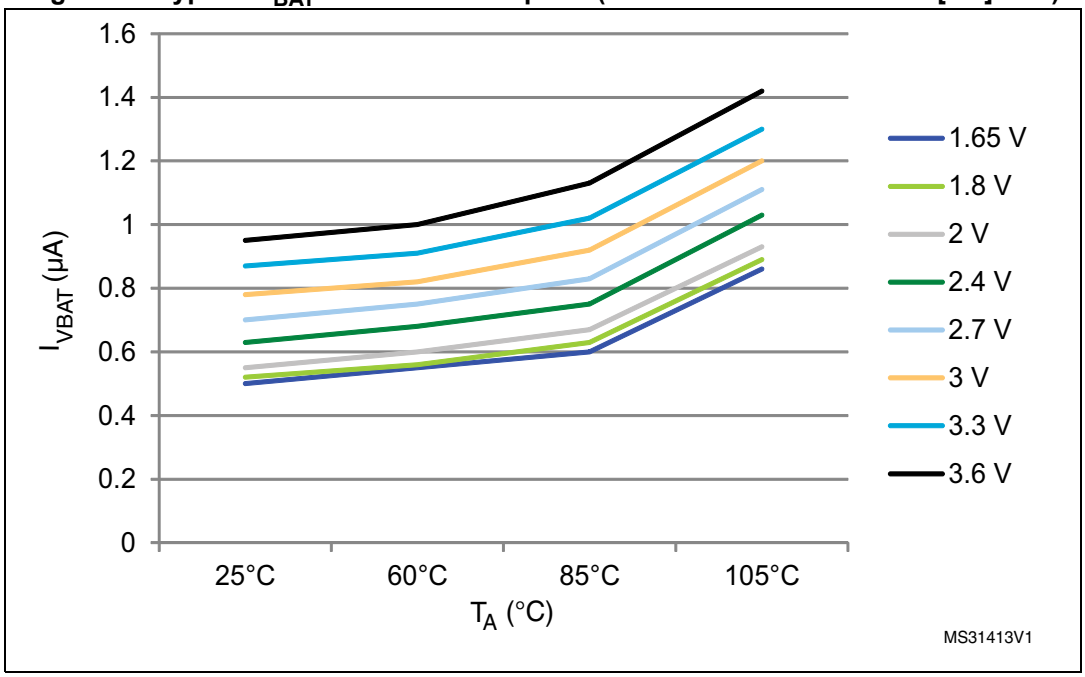
1. Data based on characterization results and tested in production.
2. To obtain data with monitoring OFF is necessary to substract the IDDAmon current.

Table 32. Typical and maximum current consumption from V_{BAT} supply(1)

Symbol	Parameter	Conditions	Typ @ V_{BAT}							Max(2)			Unit
			= 1.65 V	= 1.8 V	= 2.0 V	= 2.4 V	= 2.7 V	= 3.3 V	= 3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.50	0.52	0.55	0.63	0.70	0.87	0.95	1.1	1.6	2.2	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.85	0.90	0.93	1.02	1.10	1.27	1.38	1.6	2.4	3.0	

1. Crystal used: Abracon ABS07-120-32.768kHz-T with 6 pF of CL for typical values.
2. Data based on characterization results, not tested in production.

Figure 11. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0]='00')



Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = V_{DDSD12} = V_{DDSD3} = 3.3$ V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz)
- Prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8, 16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively

Table 33. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash, PLL on	72 MHz	61.4	28.8	mA
			64 MHz	55.4	25.9	
			48 MHz	42.3	20.0	
			32 MHz	28.7	13.8	
			24 MHz	21.9	10.7	
			16 MHz	14.8	7.4	
		Running from HSE crystal clock 8 MHz, code executing from Flash, PLL off	8 MHz	7.8	4.1	
			4 MHz	4.6	2.6	
			2 MHz	2.9	1.8	
			1 MHz	2.0	1.3	
			500 kHz	1.5	1.1	
			125 kHz	1.2	1.0	
I_{DDA}(1)(2)	Supply current in Run mode from V_{DDA} supply	Running from HSE crystal clock 8 MHz, code executing from Flash, PLL on	72 MHz	243.3	242.4	µA
			64 MHz	214.3	213.3	
			48 MHz	159.3	158.3	
			32 MHz	107.7	107.3	
			24 MHz	82.8	82.6	
			16 MHz	58.4	58.2	
		Running from HSE crystal clock 8 MHz, code executing from Flash, PLL off	8 MHz	1.2	1.2	
			4 MHz	1.2	1.2	
			2 MHz	1.2	1.2	
			1 MHz	1.2	1.2	
			500 kHz	1.2	1.2	
			125 kHz	1.2	1.2	
$I_{SDADC12}$ + I_{SDADC3}	Supply currents in Run mode from V_{DDSD12} and V_{DDSD3} (SDADCs are off)	-	-	2.5	1	µA

1. V_{DDA} monitoring is off, V_{DDSD12} monitoring is off.
2. When peripherals are enabled, power consumption of the analog part of peripherals such as ADC, DACs, Comparators, etc. is not included. Refer to those peripherals characteristics in the subsequent sections.

Table 34. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL on	72 MHz	42.8	6.9	mA
			64 MHz	38.2	6.2	
			48 MHz	28.9	4.8	
			32 MHz	19.5	3.4	
			24 MHz	14.7	2.7	
			16 MHz	10.2	2.0	
		Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL off	8 MHz	5.2	1.2	
			4 MHz	3.4	1.1	
			2 MHz	2.2	0.9	
			1 MHz	1.6	0.9	
			500 kHz	1.4	0.8	
			125 kHz	1.1	0.8	
I_{DDA}(1)	Supply current in Sleep mode from V_{DDA} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL on	72 MHz	242.9	241.5	µA
			64 MHz	213.7	212.7	
			48 MHz	158.8	158.0	
			32 MHz	107.6	107.3	
			24 MHz	82.7	82.6	
			16 MHz	58.3	58.2	
		Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL off	8 MHz	1.2	1.2	
			4 MHz	1.2	1.2	
			2 MHz	1.2	1.2	
			1 MHz	1.2	1.2	
			500 kHz	1.2	1.2	
			125 kHz	1.2	1.2	

1. V_{DDA} monitoring is off, V_{DDSD12} monitoring is off.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 52: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC and SDADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode. Under reset conditions all I/Os are configured in input floating mode - so if some inputs do not have a defined voltage level then they can generate additional consumption. This consumption is visible on V_{DD} supply and also on V_{DDSDx} supply because some I/Os are powered from SDADCx supply (all I/Os which have SDADC analog input functionality).

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 36: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 35. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{ext} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.77	mA
			4 MHz	0.87	
			8 MHz	0.95	
			18 MHz	1.59	
			36 MHz	2.57	
			48 MHz	3.11	
		V_{DD} = 3.3 V C_{ext} = 10 pF $C = C_{INT} + C_{EXT} + CS$	2 MHz	0.96	
			4 MHz	1.0	
			8 MHz	1.08	
			18 MHz	2.17	
			36 MHz	3.42	
			48 MHz	5.50	
		V_{DD} = 3.3 V C_{ext} = 22 pF $C = C_{INT} + C_{EXT} + CS$	2 MHz	0.98	
			4 MHz	1.23	
			8 MHz	1.48	
			18 MHz	2.93	
			36 MHz	6.59	
			48 MHz	7.03	
		V_{DD} = 3.3 V C_{ext} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.03	mA
			4 MHz	1.3	
			8 MHz	1.81	
			18 MHz	3.42	
			36 MHz	8.27	
		V_{DD} = 3.3 V C_{ext} = 47 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.09	
			4 MHz	1.55	
			8 MHz	2.18	
			18 MHz	4.38	
			36 MHz	9.65	

1. C_S = 5 pF (estimated value).

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off;
  - with only one peripheral clocked on.
- Ambient operating temperature at 25°C and $V_{DD} = V_{DDA}$= 3.3 Volts.

Table 36. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
AHB peripherals		-
BusMatrix(2)	6.9	µA/MHz
DMA1	18.3	
DMA2	4.8	
CRC	2.6	
GPIOA	12.2	
GPIOB	11.9	
GPIOC	4.3	
GPIOD	12.0	
GPIOE	4.4	
GPIOF	3.7	
TSC	5.7	
APB2 peripherals		
APB2-Bridge(3)	4.2	
SYSCFG & COMP	2.8	
ADC1	17.7	
SPI1	12.3	
USART1	22.9	
TIM15	15.7	
TIM16	12.2	
TIM17	12.1	
TIM19	18.5	
SDAC1	10.8	
SDAC2	10.5	
SDAC3	10.3	

Table 36. Peripheral current consumption (continued)

Peripheral	Typical consumption[1]	Unit
APB1 peripherals		µA/MHz
APB1-Bridge[3]	6.9	
TIM2	47.9	
TIM3	36.8	
TIM4	36.9	
TIM5	45.5	
TIM6	8.4	
TIM7	8.2	
TIM12	21.3	
TIM13	14.2	
TIM14	14.4	
TIM18	10.1	
WWDG	4.7	
SPI2	24.3	
SPI3	25.3	
USART2	45.3	
USART3	43.1	
I2C1	14.0	
I2C2	13.9	
USB	27.9	
CAN	38.1	
DAC2	7.7	
PWR	5.4	
DAC1	14.8	
CEC	5.4	

1. When peripherals are enabled, power consumption of the analog part of peripherals such as ADC, DACs, Comparators, etc. is not included. Refer to those peripherals characteristics in the subsequent sections.
2. The BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).
3. The APBx Bridge is automatically active when at least one peripheral is ON on the same Bus.

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 37* are measured from the wakeup event trigger to the first instruction executed by the CPU. The clock source used to wake up the device depends from the current operating mode:

- Stop or sleep mode: the wakeup event is WFE.
- The WKUP1 (PA0) pin is used to wakeup from standby, stop and sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 37. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V_{DD} = V_{DDA}					Max	Unit
			= 2.0 V	= 2.4 V	= 2.7 V	= 3 V	= 3.3 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.1	3.9	3.8	3.7	3.6	4.5	µs
		Regulator in low power mode	7.9	6.7	6.1	5.7	5.4	8.6	
$t_{WUSTANDBY}$	Wakeup from Standby mode	LSI and IWDG off	62.6	53.7	49.2	45.7	42.7	100	
$t_{WUSLEEP}$	Wakeup from Sleep mode	After WFE instruction	6						CPU clock cycles

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

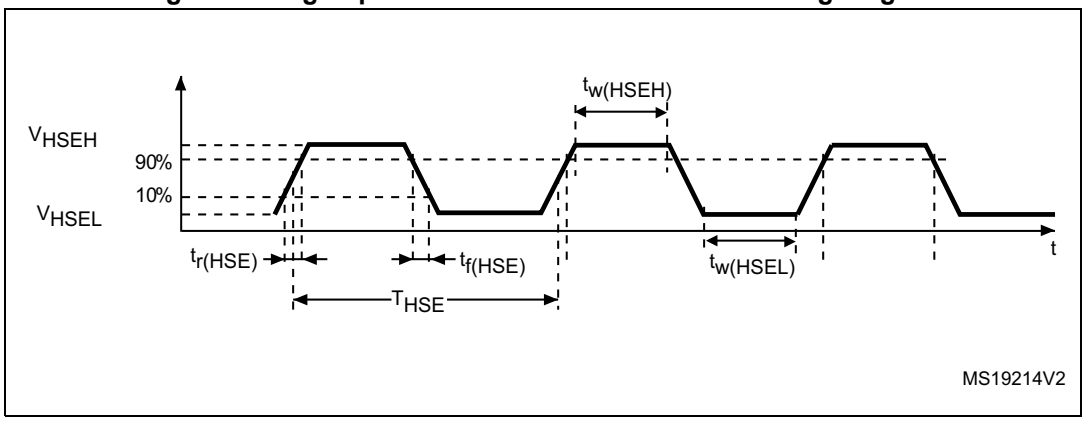
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 12*.

Table 38. High-speed external user clock characteristics

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0			
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DD}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	-	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	-	20	

1. Guaranteed by design, not tested in production.

Figure 12. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

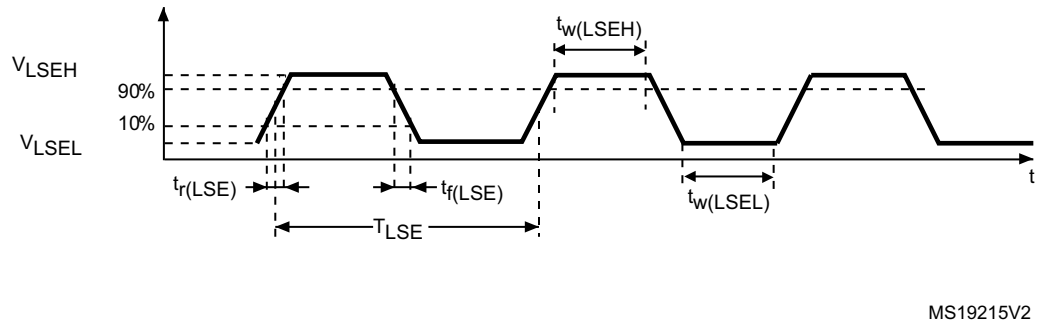
The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 13*.

Table 39. Low-speed external user clock characteristics

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	-	50	

1. Guaranteed by design, not tested in production.

Figure 13. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. HSE oscillator characteristics

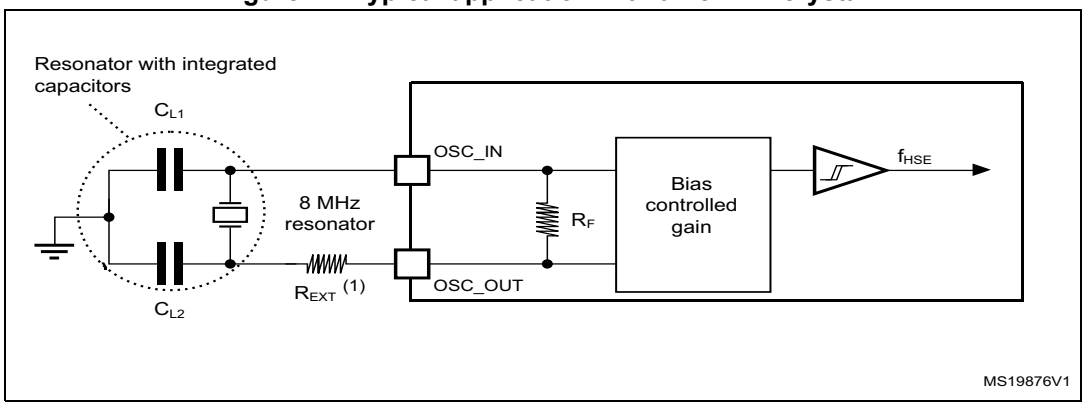
Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD} = 3.3 V, Rm= 30 Ω, CL= 10 pF@8 MHz	-	0.4	-	
		V_{DD} = 3.3 V, Rm= 45 Ω, CL= 10 pF@8 MHz	-	0.5	-	
		V_{DD} = 3.3 V, Rm= 30 Ω, CL=5 pF@32 MHz	-	0.8	-	
		V_{DD} = 3.3 V, Rm= 30 Ω, CL= 10 pF@32 MHz	-	1	-	
		V_{DD} = 3.3 V, Rm= 30 Ω, CL= 20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 14*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on electing the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 14. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

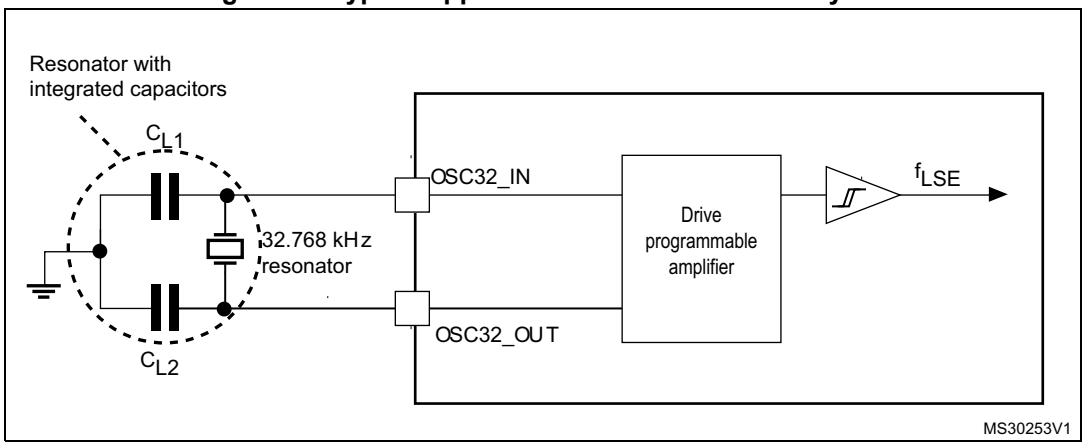
Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]= 01 medium low driving capability	-	-	1	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	8	-	-	
		LSEDRV[1:0] = 10 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 15. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

The provided curves are chararacterization results, not tested in production.

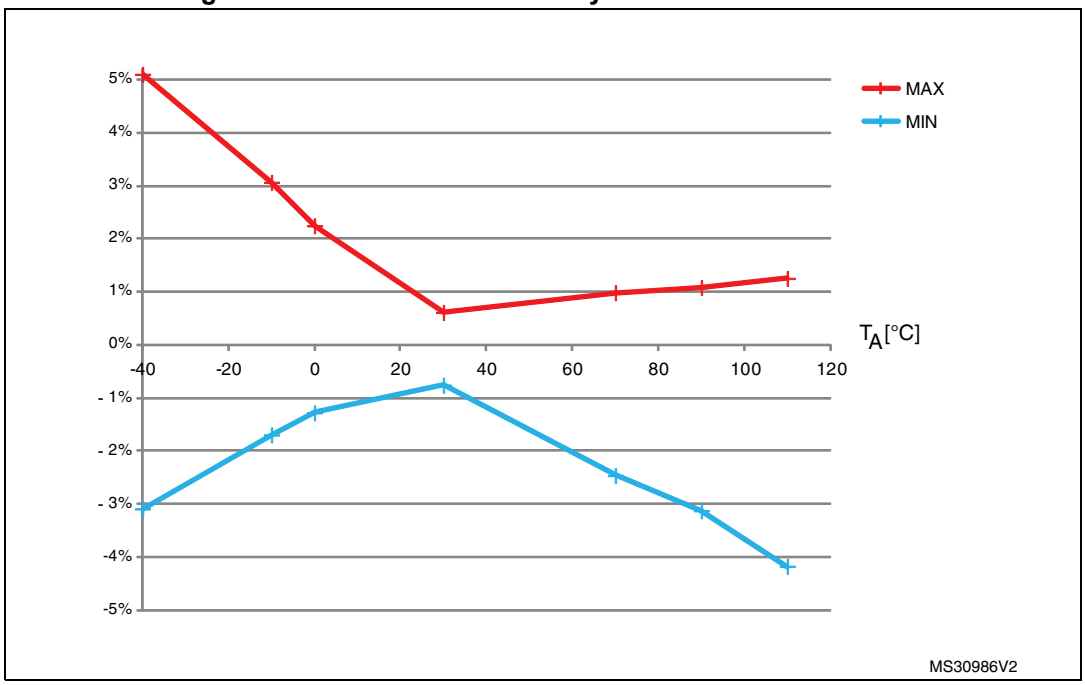
High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = –40 to 105 °C	–3.8(3)	-	4.6(3)	%
		T_A = –10 to 85 °C	–2.9(3)	-	2.9(3)	%
		T_A = 0 to 70 °C	–2.3(3)	-	–2.2(3)	%
		T_A = 25 °C	–1	-	1	%
$t_{su(HSI)}$	HSI oscillator startup time	-	1(3)	-	2(3)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	80	100(3)	µA

1. V_{DDA} =3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 16. HSI oscillator accuracy characterization results



Low-speed internal (LSI) RC oscillator

Table 43. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 44* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 44. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
Jitter	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 45. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 kB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 46. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 47*. They are based on the EMS levels and classes defined in application note AN1709.

Table 47. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 48. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	9	dBµV
			30 to 130 MHz	26	
			130 MHz to 1 GHz	30	
			SAE EMI Level	4	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 49. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1, LQFP100, LQFP64, LQFP48 and BGA100 packages	II	500	

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 50. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 51*.

Table 51. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 pin	-0	NA	mA
	Injected current on PC0 pin	-0	+5	
	Injected current on TC type I/O pins on VDDSD12 power domain: PB2, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB10 with induced leakage current on other pins from this group less than -50 µA	-5	+5	
	Injected current on TC type I/O pins on VDDSD3 power domain: PB14, PB15, PD8, PD9, PD10, PD12, PD13, PD14, PD15 with induced leakage current on other pins from this group less than -50 µA	-5	+5	
	Injected current on TTa type pins: PA4, PA5, PA6 with induced leakage current on adjacent pins less than -10 µA	-5	+5	
	Injected current on any other FT and FTf pins	-5	NA	
	Injected current on any other pins	-5	+5	

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under the conditions summarized in *Table 22*. All I/Os are CMOS and TTL compliant.

Table 52. I/O static characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3V_{DD}+0.07$(2)	V
		FT and FTf I/O	-	-	$0.475V_{DD}-0.2$(2)	
		BOOT0	-	-	$0.3V_{DD}-0.3$(2)	
		All I/Os except BOOT0 pin	-	-	$0.3V_{DD}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445V_{DD}+0.398$(2)	-	-	
		FT and FTf I/O	$0.5V_{DD+0.2}$(2)	-	-	
		BOOT0	$0.2V_{DD}+0.95$(2)	-	-	
		All I/Os except BOOT0 pin	$0.7V_{DD}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200(2)	-	mV
		FT and FTf I/O	-	100(2)	-	
		BOOT0	-	300(2)	-	
I_{lkg}	Input leakage current (3)	TC, FT and FTf I/O TTa in digital mode $V_{SS} < V_{IN} < V_{DD}$	-	-	±0.1	µA
		TTa in digital mode $V_{DD} \leq V_{IN} \leq V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	-	-	±0.2	
		FT and FTf I/O (3) $V_{DD} \leq V_{IN} \leq 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor(4)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)	$V_{IN} = V_{DD}$	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. VDDSD12 is the external power supply for the PB2, PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to VSS). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to VSS). For those pins all V_{DD} supply references in this table are related to their given VDDSDx power supply.
2. Data based on design simulation only. Not tested in production.
3. Leakage could be higher than maximum value, if negative current is injected on adjacent pins.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Note: I/O pins are powered from V_{DD} voltage except pins which can be used as SDADC inputs:

- The PB2, PB10 and PE7 to PE15 I/O pins are powered from V_{DDSD12}.

- PB14 to PB15 and PD8 to PD15 I/O pins are powered from V_{DDSD3}. All I/O pin ground is internally connected to V_{SS}.

V_{DD} mentioned in the Table 52 represents power voltage for a given I/O pin (V_{DD} or V_{DDSD12} or V_{DDSD3}).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 17* and *Figure 18* for standard I/Os, and in *Figure 19* and *Figure 20* for 5 V tolerant I/Os.

Figure 17. TC and TTa I/O input characteristics - CMOS port

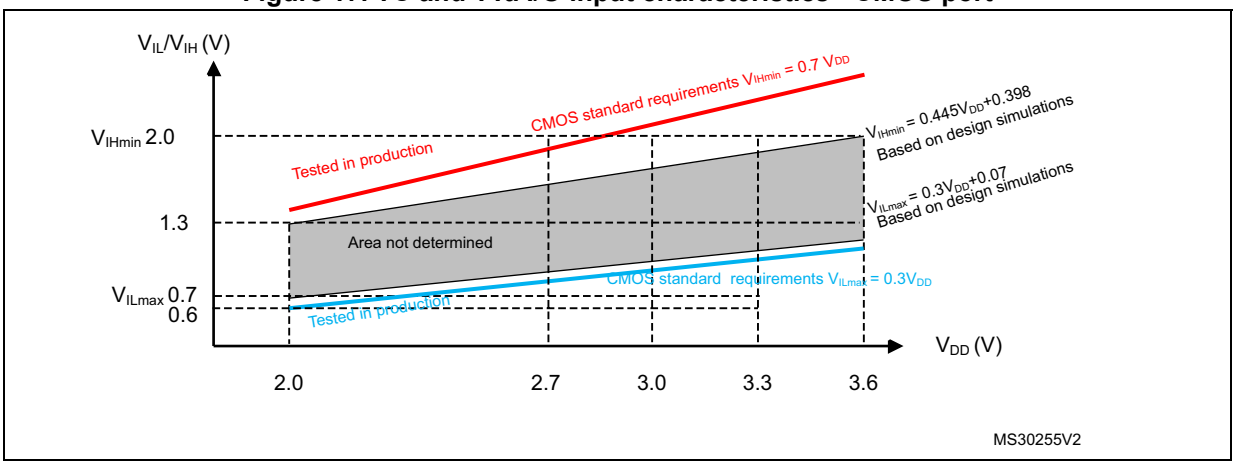


Figure 18. TC and TTa I/O input characteristics - TTL port

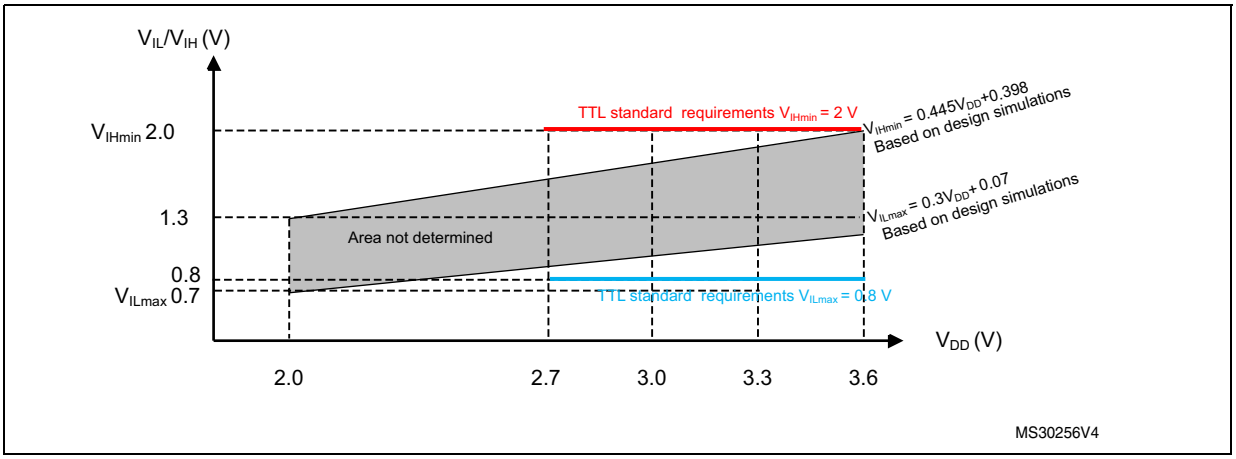


Figure 19. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port

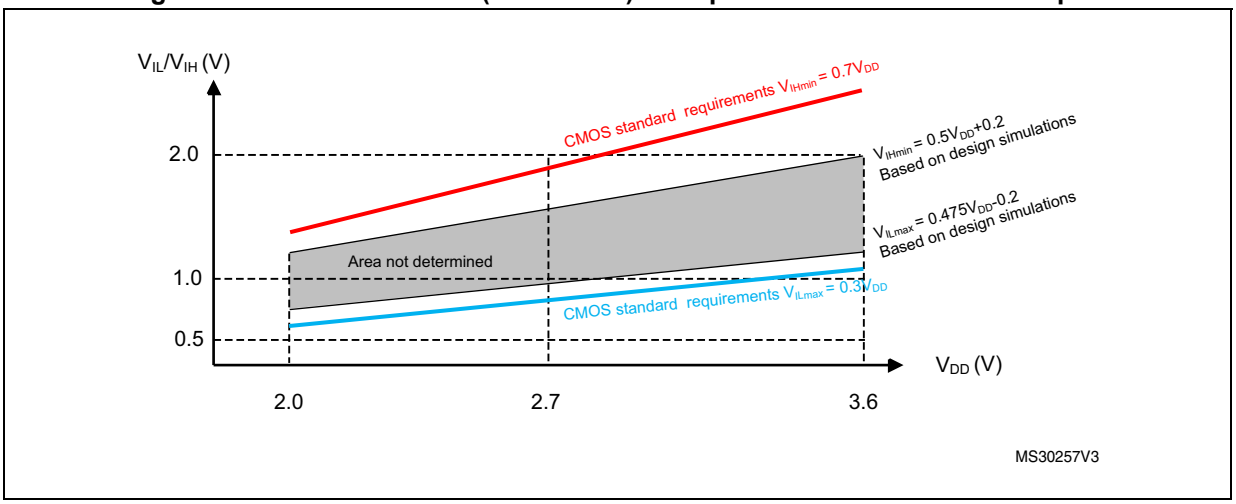
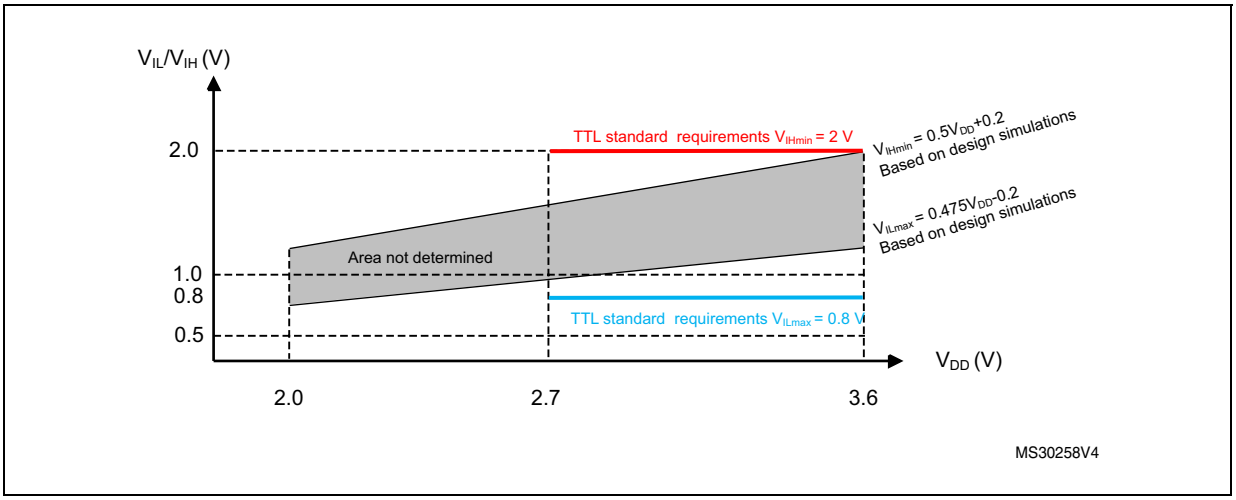


Figure 20. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on all VDD_x and VDDSDx, plus the maximum Run consumption of the MCU sourced on V_{DD} cannot exceed the absolute maximum rating SI_{VDD} (see *Table 20*).
- The sum of the currents sunk by all the I/Os on all VSS_x and VSSSD, plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating SI_{VSS} (see *Table 20*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*. All I/Os are CMOS and TTL compliant (FT, TTa or TC unless otherwise specified).

Table 53. Output voltage characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O pin	CMOS port(3) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(4)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL}(2)	Output low level voltage for an I/O pin	TTL port(3) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH}(4)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(2)(5)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH}(4)(5)	Output high level voltage for an I/O pin		V_{DD}–1.3	-	
V_{OL}(2)(5)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH}(4)(5)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OLFM+}(2)	Output low level voltage for a FTf I/O pins in FM+ mode	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	

1. VDDSD12 is the external power supply for PB2, PB10, and PE7 to PE15 I/O pins (the I/O ground pin is internally connected to VSS). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O ground pin is internally connected to VSS). For those pins all V_{DD} supply references in this table are related to their given VDDSDx power supply.
2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 20* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
4. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 20* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
5. Data based on design simulation.

Note: I/O pins are powered from V_{DD} voltage except pins which can be used as SDADC inputs:

- The PB2, PB10 and PE7 to PE15 I/O pins are powered from V_{DDSD12}.

- PB14 to PB15 and PD8 to PD15 I/O pins are powered from V_{DDSD3}. All I/O pin ground is internally connected to V_{SS}.

V_{DD} mentioned in the Table 53 represents power voltage for a given I/O pin (V_{DD} or V_{DDSD12} or V_{DDSD3}).

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 21* and *Table 54*, respectively.

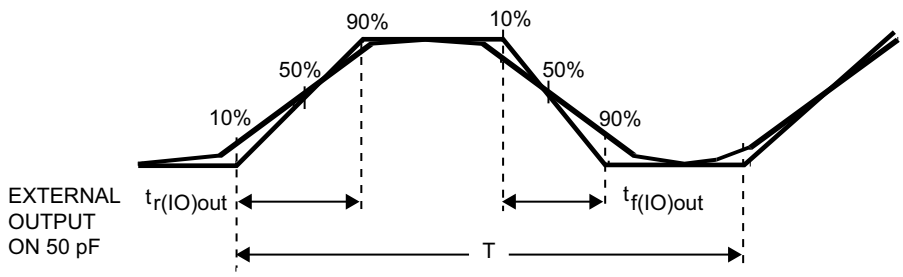
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 54. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)(3)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
FM+ configuration(4)	$f_{max(IO)out}$	Maximum frequency(2)	CL = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	12	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	34	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0313 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 21*.
3. Guaranteed by design, not tested in production.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F37xx reference manual RM0313 for a description of FM+ I/O mode configuration

Figure 21. I/O AC characteristics definition



Maximum frequency is achieved if ($t_r + t_f$ (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by 50 pF

MS32132V1

6.3.15 NRST characteristics

NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 52*).

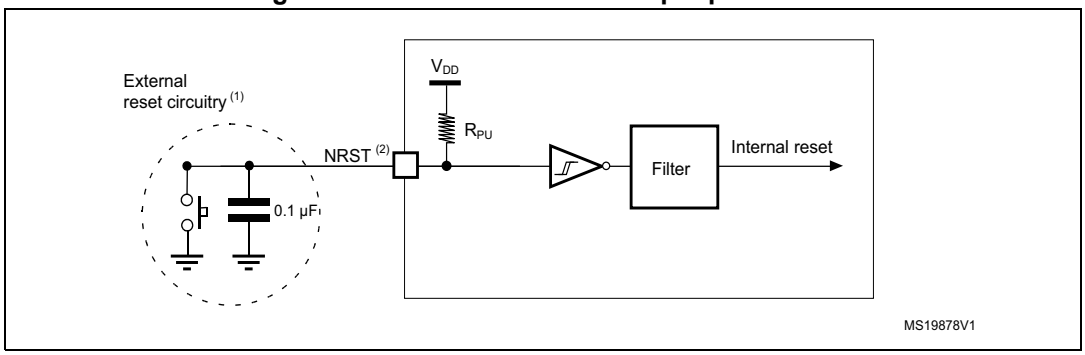
Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 55. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	-	-	$0.3V_{DD} + 0.07$(1)	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	$0.445V_{DD} + 0.398$(1)	-	-	
$V_{hys(NRST)}$(1)	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	500	-	-	ns

1. Data based on design simulation only, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 22. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 55*. Otherwise the reset will not be taken into account by the device.

6.3.16 Communications interfaces

I²C interface characteristics

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 56*. Refer also to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 56. I²C characteristics(1)

Symbol	Parameter	Standard		Fast mode		Fast mode +		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	High Period of the SCL clock	4	-	0.6	-	0.26	-	µs
tr	Rise time of both SDA and SCL signals	-	1000	-	300	-	120	ns
tf	Fall time of both SDA and SCL signals	-	300	-	300	-	120	ns
$t_{HD;DAT}$	Data hold time	0	-	0	-	0	-	µs
$t_{VD;DAT}$	Data valid time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	50	-	ns
$t_{HD;STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	0.5	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	-	550	pF

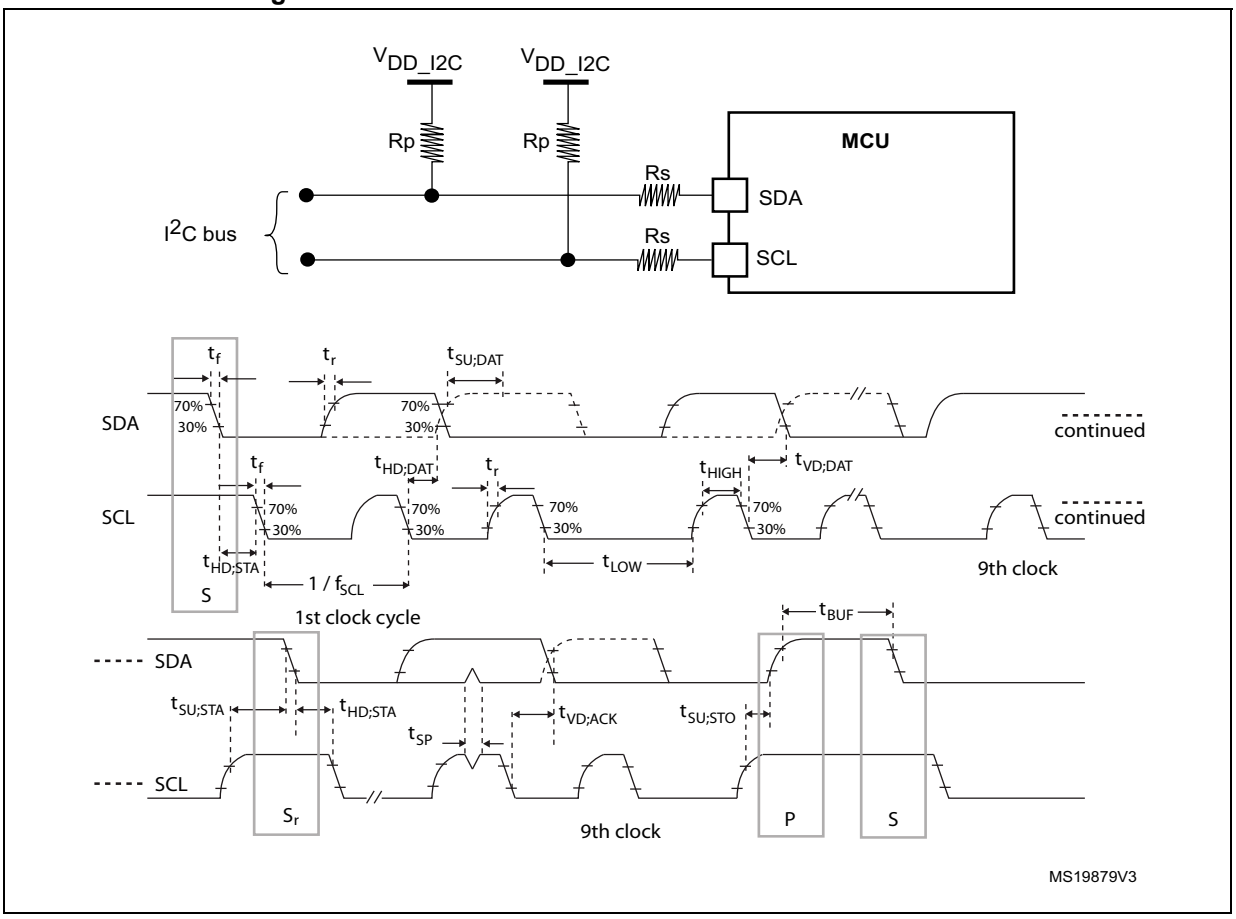
1. The I2C characteristics are the requirements from the I2C bus specification rev03. They are guaranteed by design when the I2Cx_TIMING register is correctly programmed (refer to reference manual). These characteristics are not tested in production.
2. The maximum $t_{HD;DAT}$ could be 3.45 µs, 0.9 µs and 0.45 µs for standard mode, fast mode and fast mode plus, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time.

Table 57. I²C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes width below t_{AF}(min) are filtered.
3. Spikes width above t_{AF}(max) are not filtered.

Figure 23. I²C bus AC waveforms and measurement circuit



1. Legend: Rs: Series protection resistors. Rp: Pull-up resistors. V_{DD_I2C}: I2C bus supply.

SPI/I^{2}S characteristics

Unless otherwise specified, the parameters given in *Table 58* for SPI or in *Table 59* for I^{2}S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^{2}S).

Table 58. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$(1)	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$(1)	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)(1)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$(1)	NSS setup time	Slave mode	2Tpclk	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	4Tpclk	-	
$t_{w(SCKH)}$(1) $t_{w(SCKL)}$(1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 - 3	Tpclk/2 + 3	
$t_{su(MI)}$(1) $t_{su(SI)}$(1)	Data input setup time	Master mode	5.5	-	
		Slave mode	6.5	-	
$t_{h(MI)}$(1)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$(1)		Slave mode	5	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK} = 24 MHz	0	4Tpclk	
$t_{dis(SO)}$(1)(3)	Data output disable time	Slave mode	0	24	
$t_{v(SO)}$(1)	Data output valid time	Slave mode (after enable edge)	-	39	
$t_{v(MO)}$(1)	Data output valid time	Master mode (after enable edge)	-	3	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(1)		Master mode (after enable edge)	4	-	

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 24. SPI timing diagram - slave mode and CPHA = 0

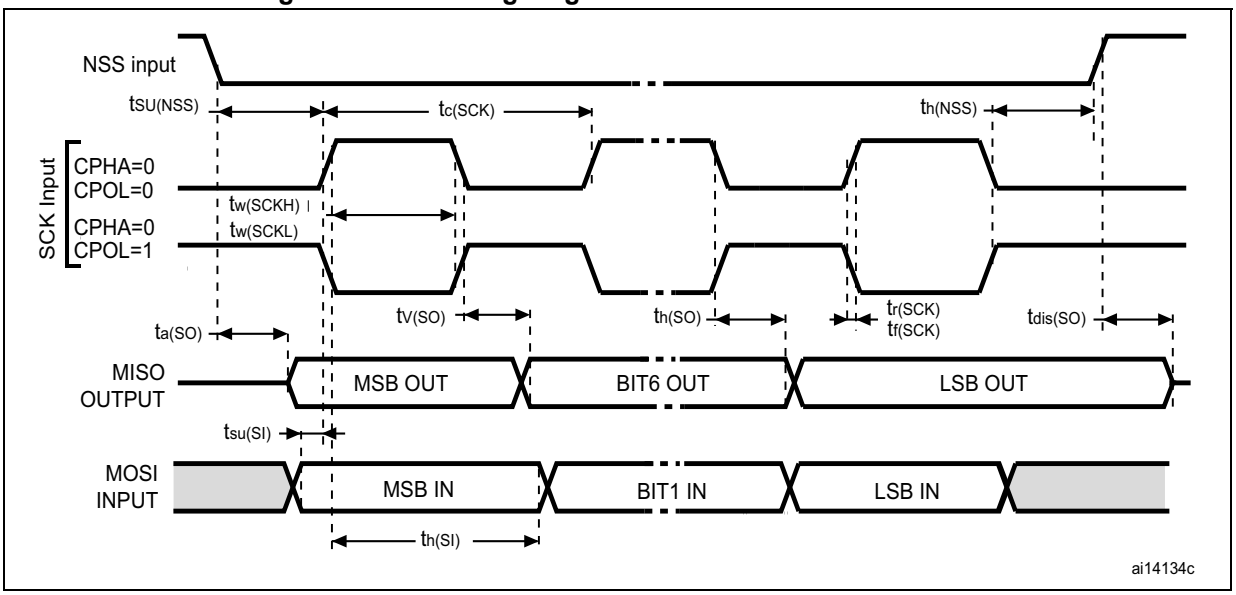
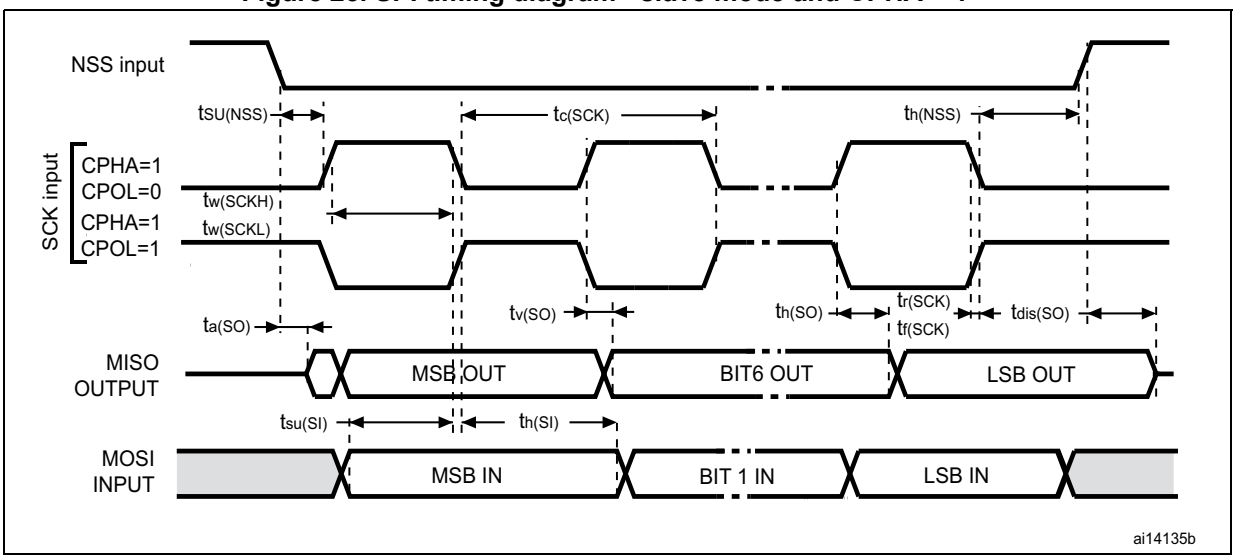
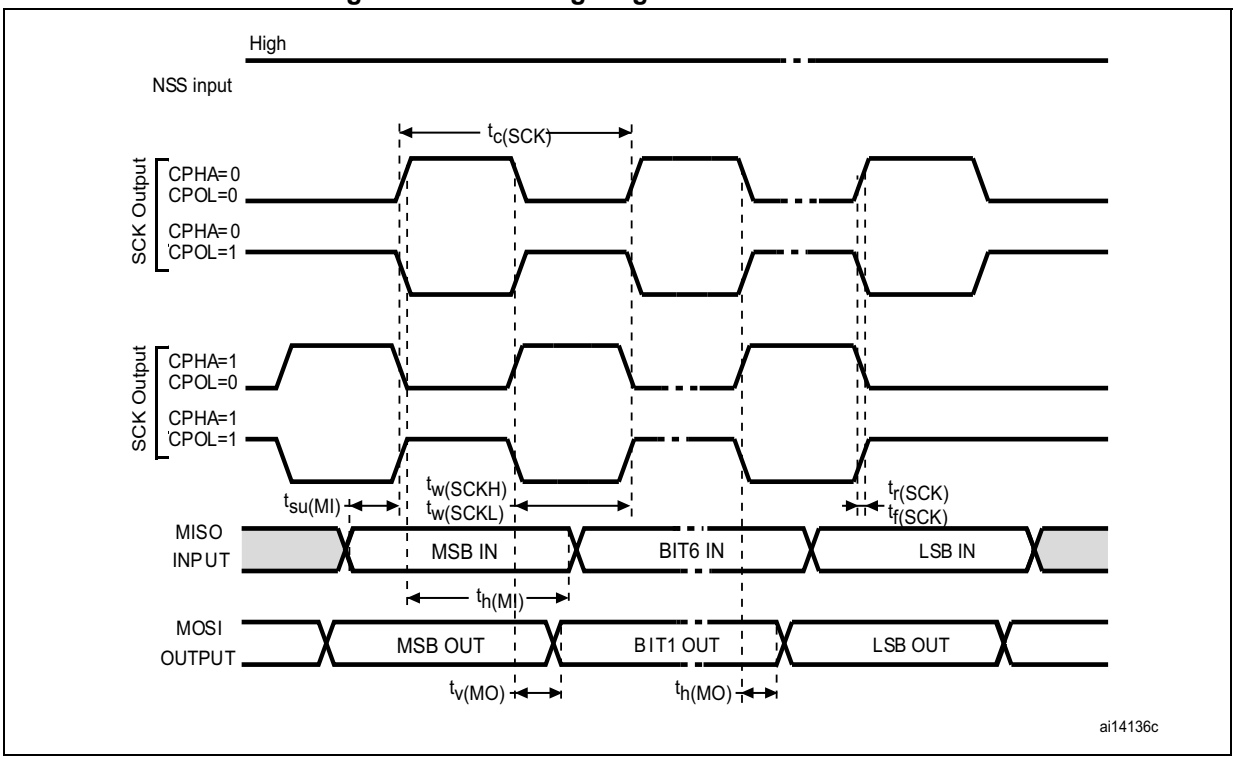


Figure 25. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ level and with external C_L = 30 pF.

Figure 26. SPI timing diagram - master mode(1)



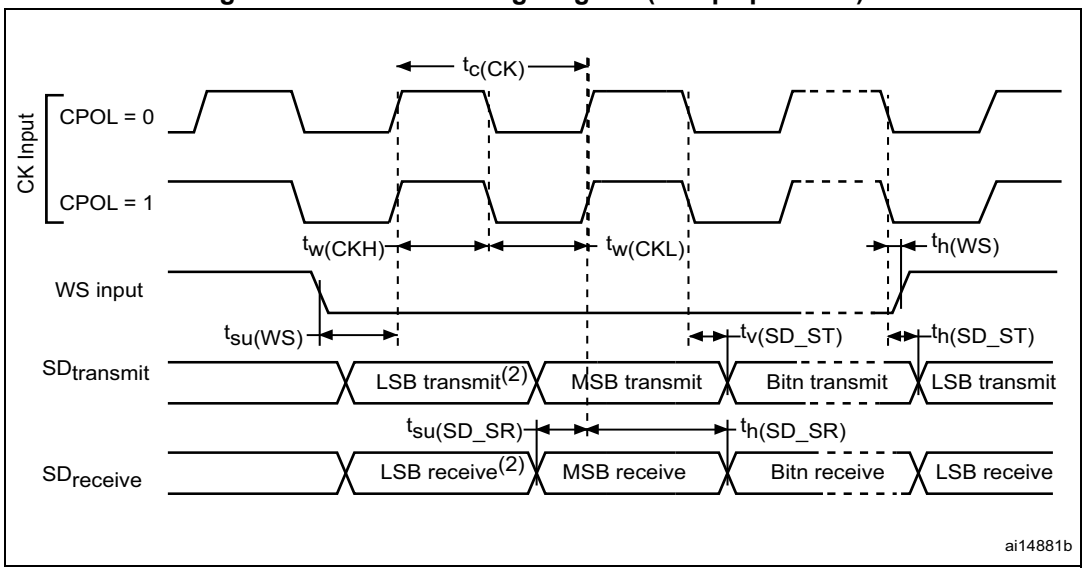
1. Measurement points are done at $0.5V_{DD}$ level and with external C_L = 30 pF.

Table 59. I^2S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
DuCy(SCK)(1)	I2S slave input clock duty cycle	Slave mode	30	70	%
f_{CK}(1) $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.528	1.539	MHz
		Slave mode	0	12.288	
$t_{r(CK)}$(1) $t_{f(CK)}$	I^2S clock rise and fall time	Capacitive load C_L = 30 pF	-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode	4	-	
$t_{h(WS)}$ (1)	WS hold time	Master mode	4	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	2	-	
$t_{h(WS)}$ (1)	WS hold time	Slave mode	-	-	
$t_{w(CKH)}$ (1)	I2S clock high time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$ (1)	I2S clock low time		312	-	
$t_{su(SD_MR)}$ (1)	Data input setup time	Master receiver	6	-	
$t_{su(SD_SR)}$ (1)		Slave receiver	3	-	
$t_{h(SD_MR)}$(1)	Data input hold time	Master receiver	1.5	-	
$t_{h(SD_SR)}$ (1)		Slave receiver	1.5	-	
$t_{v(SD_ST)}$ (1)	Data output valid time	Slave transmitter (after enable edge)	-	16	
$t_{h(SD_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)	16	-	
$t_{v(SD_MT)}$ (1)	Data output valid time	Master transmitter (after enable edge)	-	2	
$t_{h(SD_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)	0	-	

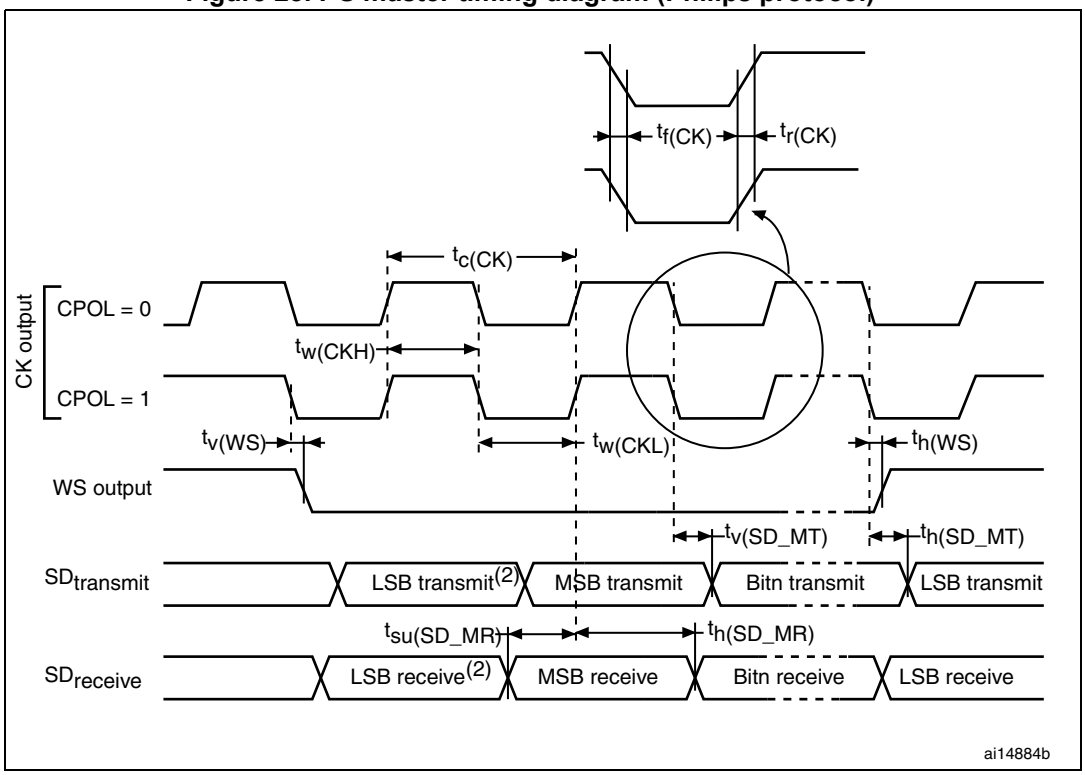
1. Data based on design simulation, not tested in production.

Figure 27. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at 0.5 V_{DD} level and with external C_L = 30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 28. I²S master timing diagram (Philips protocol)(1)



1. Measurement points are done at 0.5 V_{DD} level and with external C_L = 30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 60* are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 22*.

Note: It is recommended to perform a calibration after each power-up.

Table 60. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
$I_{DDA(ADC)}$(1)	Current consumption from V_{DDA}	$V_{DD} = V_{DDA} = 3.3$ V	-	0.9	-	mA
I_{VREF}	Current on the V_{REF} input pin	-	-	160(2)	220(2)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(3)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(3)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{SRC}(3)	Signal source impedance	See *Equation 1* and *Table 61* for details	-	-	50	kΩ
R_{ADC}(3)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(3)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(3)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_{latr}(3)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(3)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(3)	Power-up time	-	-	-	1	µs
t_{CONV}(3)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} is present
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 60*

Equation 1: R_{SRC} max formula

$$R_{SRC} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external signal source impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 61. R_{SRC} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{SRC} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	50
239.5	17.1	50

1. Guaranteed by design, not tested in production.

Table 62. ADC accuracy(1)(2) (3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{ADC} = 14 MHz, R_{SRC} < 10 kΩ, V_{DDA} = 3 V to 3.6 V, T_A = 25 °C	±1.3	±3	LSB
EO	Offset error		±1	±2	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f_{ADC} = 14 MHz, R_{SRC} < 10 kΩ, V_{DDA} = 2.7 V to 3.6 V, T_A = -40 to 105 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error	f_{ADC} = 14 MHz, R_{SRC} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V, T_A = 25 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

1. ADC DC accuracy values are measured after internal calibration.

2. ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Figure 29. ADC accuracy characteristics

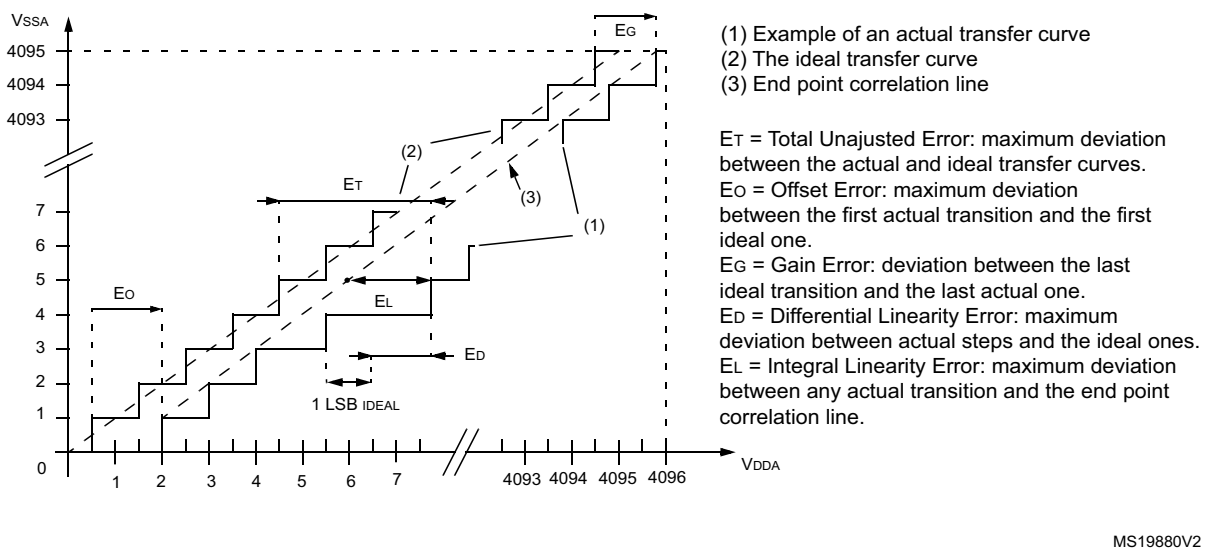
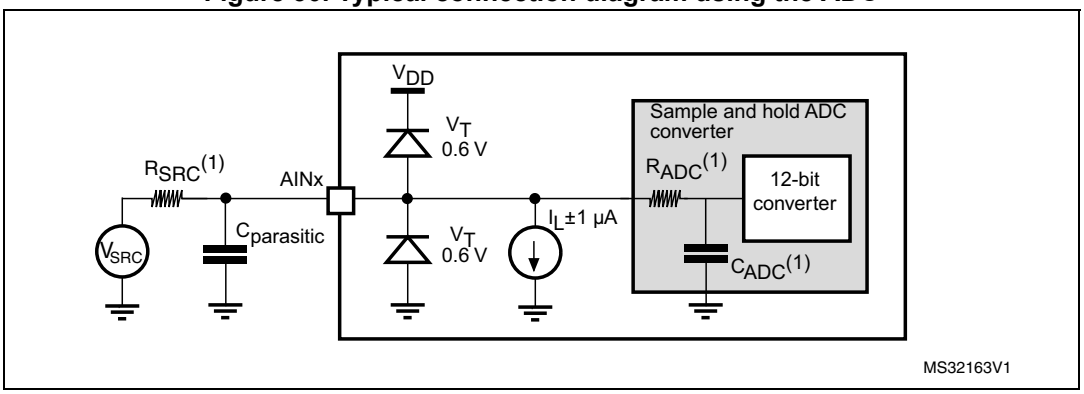


Figure 30. Typical connection diagram using the ADC



1. Refer to *Table 60* for the values of R_{SRC}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 9*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.18 DAC electrical specifications

Table 63. DAC characteristics

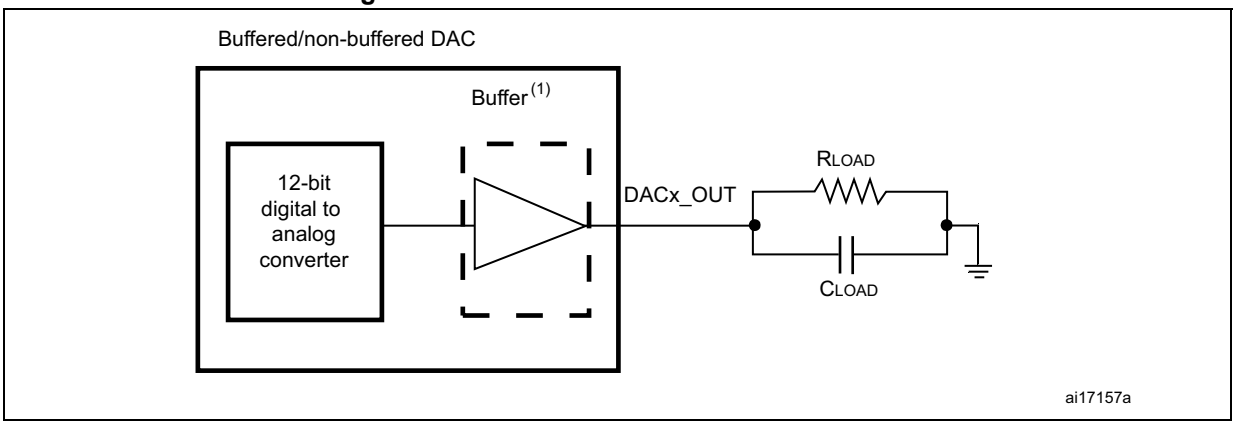
Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V_{REF+}	Reference supply voltage	2.4	-	3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(1)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(1)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x155) and (0xEAB) at V_{REF+} = 2.4 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} – 1LSB	V	
$I_{DDVREF+}$(3)	DAC DC current consumption in quiescent mode (Standby mode)	-	-	220	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}(3)	DAC DC current consumption in quiescent mode(2)	-	-	380	µA	With no load, middle code (0x800) on the inputs
		-	-	480	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(3)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
		-	-	±2	LSB	Given for the DAC in 12-bit configuration
INL(3)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration
		-	-	±4	LSB	Given for the DAC in 12-bit configuration

Table 63. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	±10	mV	-
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(3)	Gain error	-	-	±0.5	%	Given for the DAC in 12bit configuration
$t_{SETTLING}$(3)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	-67	-40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by design, not tested in production.
2. Quiescent mode refers to the state of the DAC keeping a steady value on the output, so no dynamic consumption is involved.
3. Guaranteed by characterization, not tested in production.

Figure 31. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.19 Comparator characteristics

Table 64. Comparator characteristics

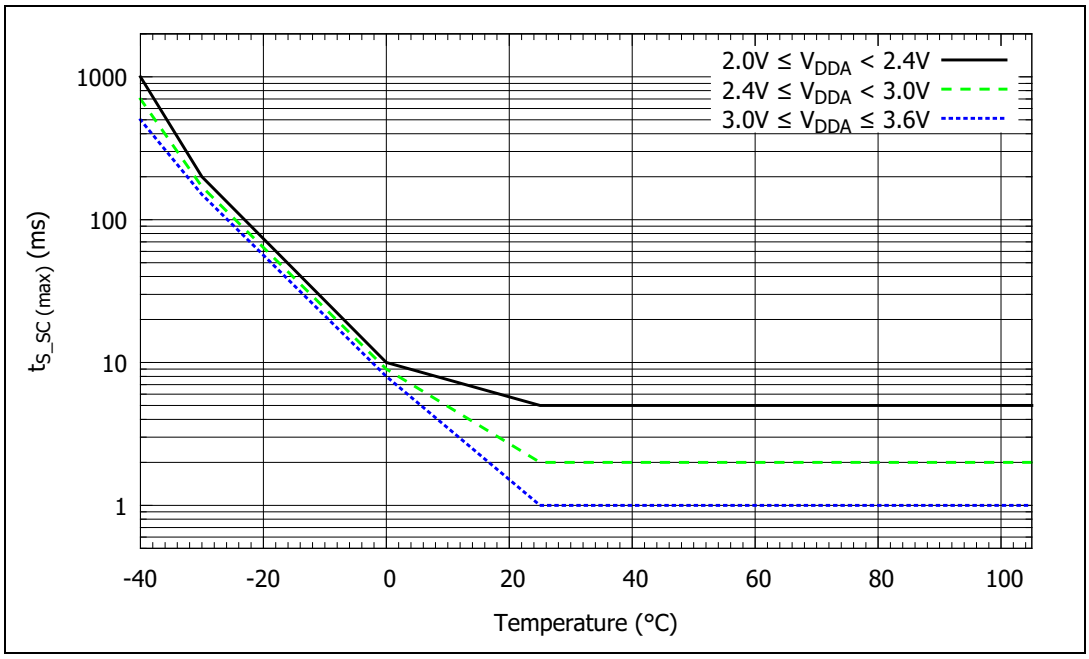
Symbol	Parameter	Conditions		Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-		2	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	V
V_{BG}	V_{REFINT} scaler input voltage	-		-	1.2	-	V
V_{SC}	V_{REFINT} scaler offset voltage	-		-	±5	±10	mV
t_{S_SC}	Scaler startup time from power down	First V_{REFINT} scaler activation after device power on		-	-	1000(2)	ms
		Next activations				0.2	
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode		-	2	4.5	µs
		Low power mode		-	0.7	1.5	
		Medium power mode		-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low power mode		-	2	7	µs
		Low power mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	
V_{offset}	Comparator offset error	-		-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-		-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low power mode		-	1.2	1.5	µA
		Low power mode		-	3	5	
		Medium power mode		-	10	15	
		High speed mode		-	75	100	

Table 64. Comparator characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max(1)	Unit
V_{hys}	Comparator hysteresis	No hysteresis (COMPxHYST[1:0]=00)	-	-	0	-	mV
		Low hysteresis (COMPxHYST[1:0]=01)	High speed mode	3	8	13	
			All other power modes	5		10	
		Medium hysteresis (COMPxHYST[1:0]=10)	High speed mode	7	15	26	
			All other power modes	9		19	
		High hysteresis (COMPxHYST[1:0]=11)	High speed mode	18	31	49	
			All other power modes	19		40	

1. Guaranteed by design, not tested in production.
2. For more details and conditions see *Figure 32: Maximum VREFINT scaler startup time from power down*

Figure 32. Maximum V_{REFINT} scaler startup time from power down



6.3.20 Temperature sensor characteristics

Table 65. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

Table 66. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(2)(1)	ADC sampling time when reading the temperature	17.1	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.21 V_{BAT} monitoring characteristics

Table 67. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	-
Er(1)	Error on Q	-1	-	+1	%
T_{S_vbat}(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	5	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.22 Timer characteristics

The parameters given in *Table 68* are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 68. TIMx(1) (2)characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	24	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s

1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, TIM12, TIM13, TIM14, TIM15, TIM16 , TIM17, TIM18 and TIM19 timers.
2. Data based on characterization results, not tested in production.

Table 69. IWDG min/max timeout period at 40 kHz (LSI) (1)(2)

Prescaler divider	PR[2:0] bits	Min timeout (ms) RL[11:0]= 0x000	Max timeout (ms) RL[11:0]= 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.
2. Data based on characterization results, not tested in production.

Table 70. WWDG min-max timeout value @72 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

6.3.23 USB characteristics

Table 71. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 72. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity (for USB compliance)	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F3xxx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design, not tested in production.
5. R_L is the load connected on the USB drivers

Figure 33. USB timings: definition of data signal rise and fall time

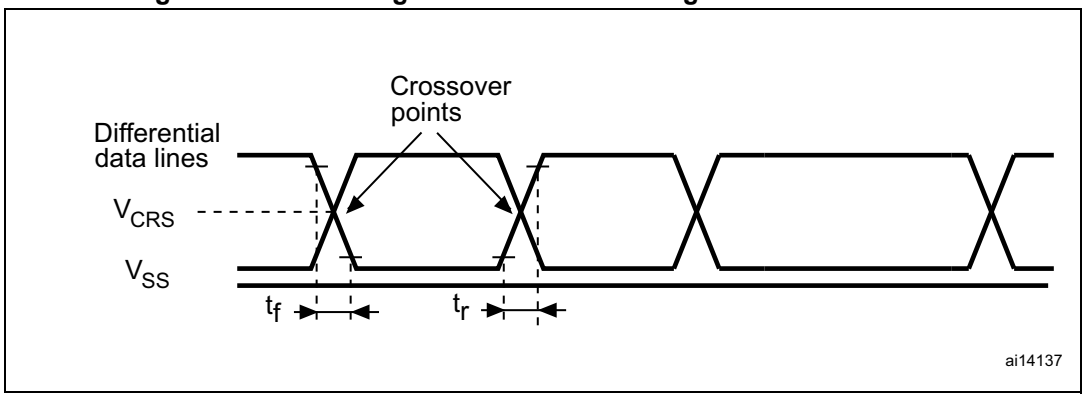


Table 73. USB: Full-speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_r	Rise time(2)	C_L = 50 pF	4	-	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	-	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	-	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	-	2.0	V
Output driver Impedance(3)	Z_{DRV}	driving high and low	28	40	44	Ω

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-), the matching impedance is already included in the embedded driver.

6.3.24 CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.25 SDADC characteristics

Table 74. SDADC characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
V_{DDSDx}	Power supply	Slow mode (f_{ADC} = 1.5 MHz)	2.2	-	V_{DDA}	V	-
		Normal mode (f_{ADC} = 6 MHz)	2.4	-	V_{DDA}		-
f_{ADC}	SDADC clock frequency	Slow mode (f_{ADC} = 1.5 MHz)	0.5	1.5	1.65	MHz	-
		Normal mode (f_{ADC} = 6 MHz)	0.5	6	6.3		-
V_{REFSD+}	Positive ref. voltage	-	1.1	-	V_{DDSDx}	V	-

Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
V_{REFSD-}	Negative ref. voltage	-	-	V_{SSA}	-	V	-
I_{DDSDx}	Supply current (V_{DDSDx} = 3.3 V)	Normal mode (f_{ADC} = 6 MHz)	-	800	1200	µA	-
		Slow mode (f_{ADC} = 1.5 MHz)	-	-	600		-
		Standby	-	-	200		-
		Power down	-	-	2.5		-
		SD_ADC off	-	-	1		-
V_{AIN}	Common input voltage range	Single ended mode (zero reference)	V_{REF-}	-	V_{REFSD+} /gain	V	Voltage on AINP or AINN pin
		Single ended offset mode	V_{REF-}	-	V_{REFSD+}/ (gain*2)		
		Differential mode	V_{SSA}	-	V_{DDSDx}		
V_{DIFF}	Differential input voltage	Differential mode only	$-V_{REFSD+}$/ (gain*2)	-	V_{REFSD+}/ (gain*2)	-	Differential voltage between AINP and AINN
f_S	Sampling rate	Slow mode (f_{ADC} = 1.5 MHz)	-	4.166	-	kHz	f_{ADC}/360
		Slow mode one channel only (f_{ADC} = 1.5 MHz)	-	12.5	-		f_{ADC}/120
		Normal mode multiplexed channel (f_{ADC} = 6 MHz)	-	16.66	-		f_{ADC}/360
		Normal mode one channel only, FAST= 1 (f_{ADC} = 6 MHz)	-	50	-		f_{ADC}/120
t_{CONV}	Conversion time	-	-	1/fs	-	s	-
Rain	Analog input impedance	One channel, gain = 0.5, f_{ADC} = 1.5 MHz	-	540	-	kΩ	see reference manual for detailed description
		One channel, gain = 0.5, f_{ADC} = 6 MHz	-	135	-		
		One channel, gain = 8, f_{ADC} = 6 MHz	-	47	-		
t_{CALIB}	Calibration time	f_{ADC} = 6 MHz, one offset calibration	-	5120	-	µs	30720/f_{ADC}
t_{STAB}	Stabilization time	From power down f_{ADC} = 6 MHz	-	100	-	µs	600/f_{ADC}, 75/f_{ADC} if SLOWCK = 1
$t_{STANDBY}$	Wakeup from standby time	f_{ADC} = 6 MHz	-	50	-	µs	300/f_{ADC}
		f_{ADC} = 1.5 MHz	-	50	-		75/f_{ADC} if SLOWCK = 1

Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions					Min	Typ	Max	Unit	Note
EO	Offset error	Differential mode	gain = 1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3	-	-	110	uV	after offset calibration
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2	-	-	110		
						V_{REFSD+} = 3.3	-	-	100		
			gain = 8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2	-	-	70		
						V_{REFSD+} = 3.3	-	-	100		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3	-	-	90		
		Single ended mode	gain = 1	-		V_{REFSD+} = 1.2	-	-	2100		
						V_{REFSD+} = 3.3	-	-	2000		
			gain = 8			V_{REFSD+} = 1.2	-	-	1500		
						V_{REFSD+} = 3.3	-	-	1800		
$D_{voffsettemp}$	Offset drift with temperature	Differential or single ended mode, gain = 1, V_{DDSDx} = 3.3 V					-	10	15	uV/K	-
EG	Gain error	All gains, differential mode, single ended mode					-2.4	-2.7	-3.1	%	negative gain error = data result are greater than ideal
EGT	Gain drift with temperature	gain = 1, differential mode, single ended mode					-	0	-	ppm /K	-

Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions				Min	Typ	Max	Unit	Note
EL	Integral linearity error	Differential mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2	-	-	16	LSB	-
					V_{REFSD+} = 3.3	-	-	14		
			gain = 8		V_{REFSD+} = 1.2	-	-	26		
					V_{REFSD+}= 3.3	-	-	14		
		Single ended mode	gain = 1		V_{REFSD+} = 1.2	-	-	31		
					V_{REFSD+}= 3.3	-	-	23		
			gain = 8		V_{REFSD+}= 1.2	-	-	80		
					V_{REFSD+} = 3.3	-	-	35		
ED	Differential linearity error	Differential mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2	-	-	2.4	LSB	-
					V_{REFSD+} = 3.3	-	-	1.8		
			gain = 8		V_{REFSD+}= 1.2	-	-	3.6		
					V_{REFSD+} = 3.3	-	-	2.9		
		Single ended mode	gain = 1		V_{REFSD+} = 1.2	-	-	3.2		
					V_{REFSD+} = 3.3	-	-	2.8		
			gain = 8		V_{REFSD+}= 1.2	-	-	4.1		
					V_{REFSD+} = 3.3	-	-	3.3		

Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions					Min	Typ	Max	Unit	Note
SNR(4)	Signal to noise ratio	Differential mode	gain = 1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3(2)	84	85	-	dB	-
				f_{ADC} = 6 MHz		V_{REFSD+}= 1.2(3)	86	88	-		
						V_{REFSD+} = 3.3	88	92	-		
			gain = 8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	76	78	-		
						V_{REFSD+} = 3.3	82	86	-		
				f_{ADC} = 1.5 MHz		V_{REFSD+}= 3.3(2)	76	80	-		
		Single ended mode	gain = 1	f_{ADC} = 1.5MHz		V_{REFSD+} = 3.3	80	84	-		
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	77	81	-		
						V_{REFSD+} = 3.3	85	90	-		
			gain = 8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	66	71	-		
						V_{REFSD+} = 3.3	74	78	-		

Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions					Min	Typ	Max	Unit	Note
SINAD(4)	Signal to noise and distortion ratio	Differential mode	gain =1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3(2)	76	77	-	dB	ENOB = SINAD/ 6.02 -0.292
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	75	76	-		
						V_{REFSD+} = 3.3	76	77	-		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	70	74	-		
						V_{REFSD+} = 3.3	79	85	-		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3(2)	75	81	-		
		Single ended mode	gain =1	f_{ADC} = 1.5MHz		V_{REFSD+} = 3.3	72	73	-		
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	68	71	-		
						V_{REFSD+} = 3.3	72	73	-		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	60	64	-		
						V_{REF} = 3.3	67	72	-		
THD(4)	Total harmonic distortion	Differential mode	gain =1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3(2)	-	-77	-76	dB	-
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	-	-77	-76		
						V_{REFSD+} = 3.3	-	-77	-76		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	-	-85	-70		
						V_{REFSD+} = 3.3	-	-93	-80		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3(2)	-	-93	-83		
		Single ended mode	gain =1	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	-	-72	-68		
						V_{REFSD+} = 3.3	-	-74	-72		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(3)	-	-66	-61		
						V_{REFSD+} = 3.3	-	-75	-70		

1. Data based on characterization results, not tested in production.

2. For f_{ADC} lower than 5 MHz, there will be a performance degradation of around 2 dB due to flicker noise increase.
3. If the reference value is lower than 2.4 V, there will be a performance degradation proportional to the reference supply drop, according to this formula: 20*log10(V_{REF}/2.4) dB
4. SNR, THD, SINAD parameters are valid for frequency bandwidth 20Hz - 1kHz. Input signal frequency is 300Hz (for f_{ADC}=6MHz) and 100Hz (for f_{ADC}=1.5MHz).

Table 75. VREFSD+ pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
V_{REFINT}	Internal reference voltage	Buffered embedded reference voltage (1.2 V)	-	1.2	-	V	See *Section 6.3.4: Embedded reference voltage on page 60*
		Embedded reference voltage amplified by factor 1.5	-	1.8	-	V	-
$C_{VREFSD+}$(2)	Reference voltage filtering capacitor	$V_{REFSD+} = V_{REFINT}$	1000	-	10000	nF	-
$R_{VREFSD+}$	Reference voltage input impedance	Normal mode (f_{ADC} = 6 MHz)	-	238	-	kΩ	See RM0313 reference manual for detailed description
		Slow mode (f_{ADC} = 1.5 MHz)	-	952	-		

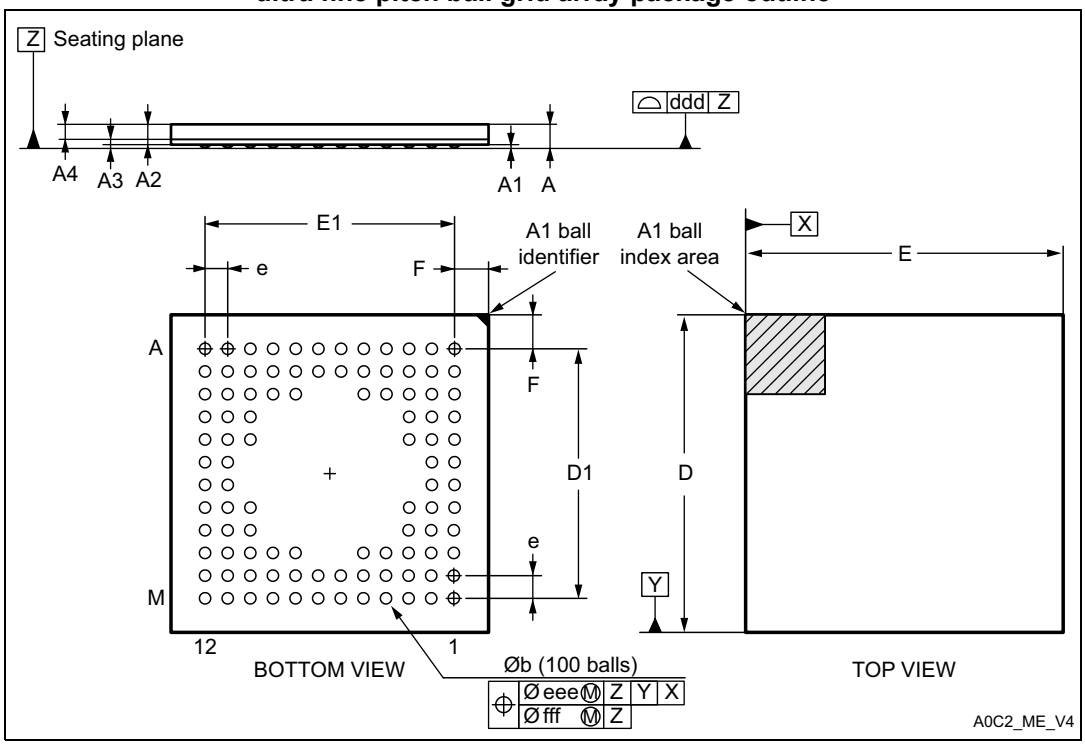
1. Data based on characterization results, not tested in production.
2. If internal reference voltage is selected then this capacitor is charged through internal resistance - typ. 300 ohm. If internal reference source is selected through the reference voltage selection bits (REFV<>"00" in SDADC_CR1 register), the application must first configure REFV bits and then wait for capacitor charging. Recommended waiting time is 3 ms if 1 µF capacitor is used.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 UFBGA100 package information

Figure 34. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 76. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.200	0.250	0.300	0.0079	0.0098	0.0118

Table 76. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.450	5.500	5.550	0.2146	0.2165	0.2185
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.450	5.500	5.550	0.2146	0.2165	0.2185
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

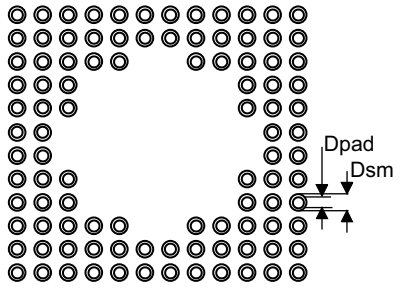


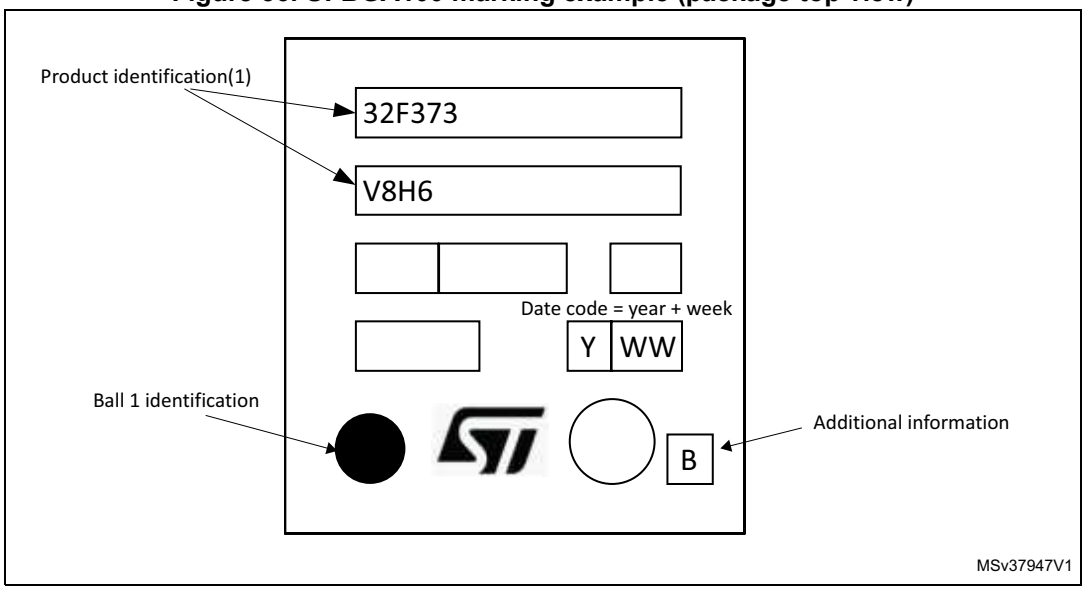
Table 77. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Device Marking for UFBGA100

The following figure gives an example of topside marking orientation versus ball 1 identifier location.

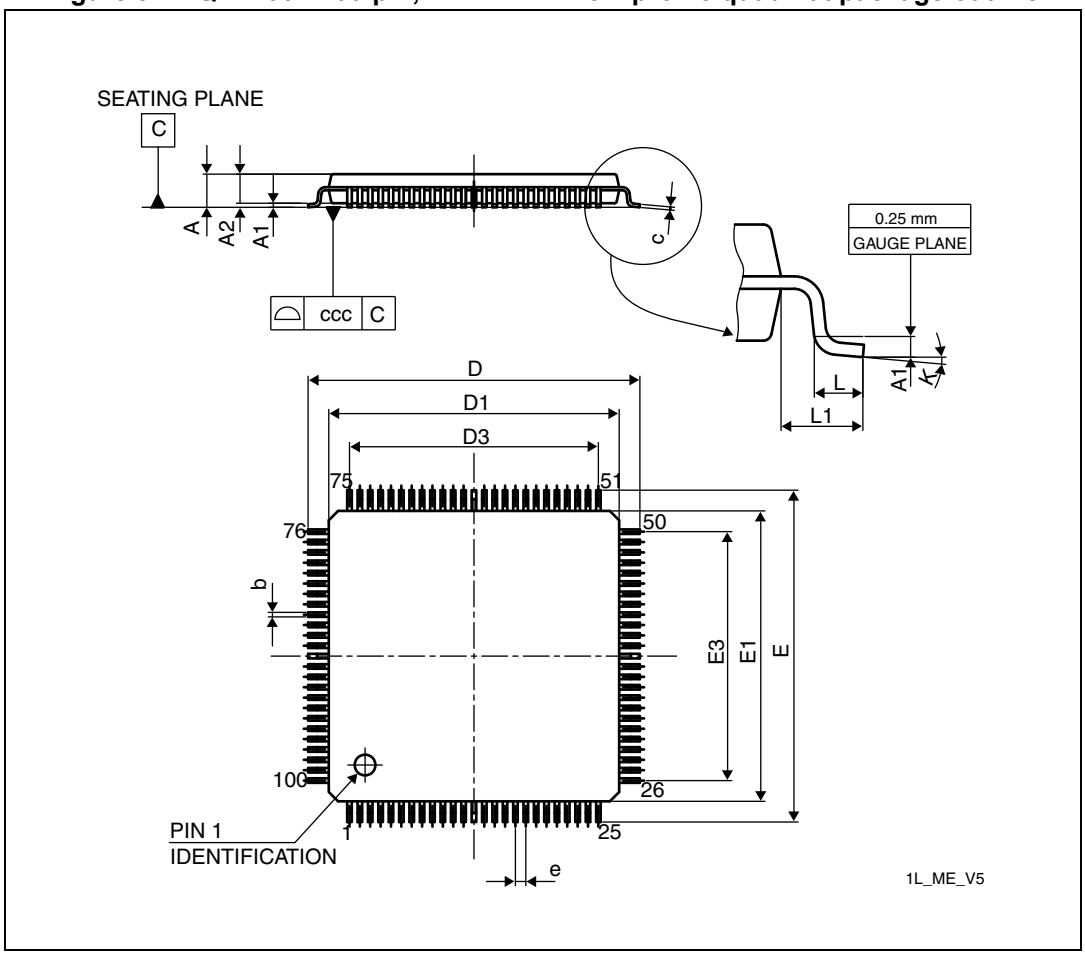
Figure 36. UFBGA100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.2 LQFP100 package information

Figure 37. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



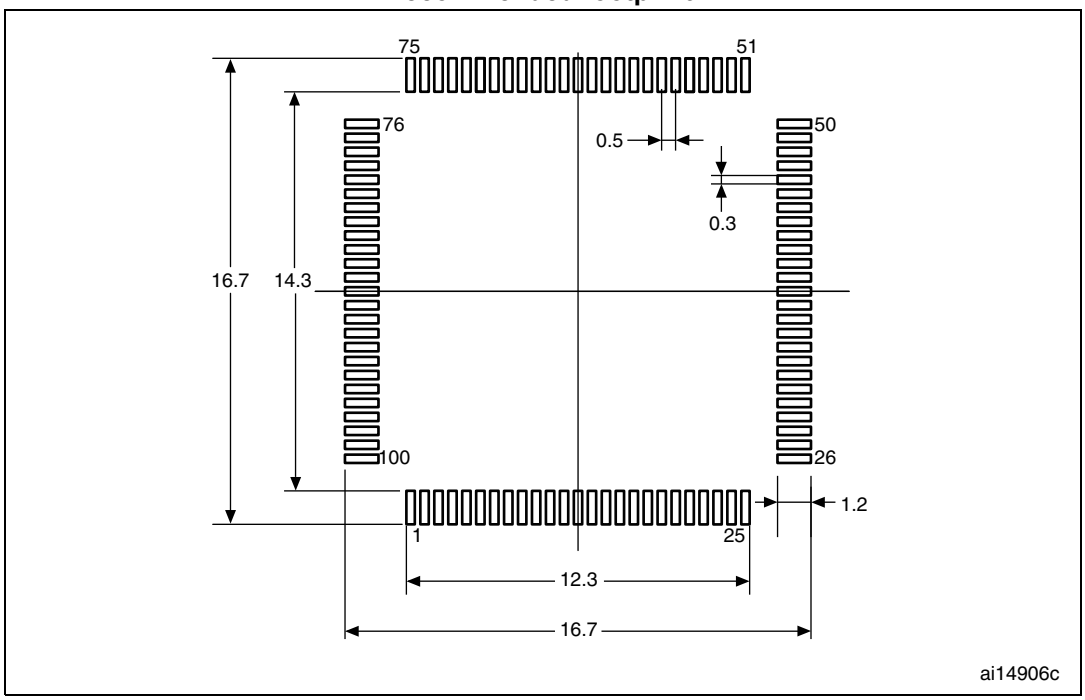
1. Drawing is not to scale.

Table 78. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

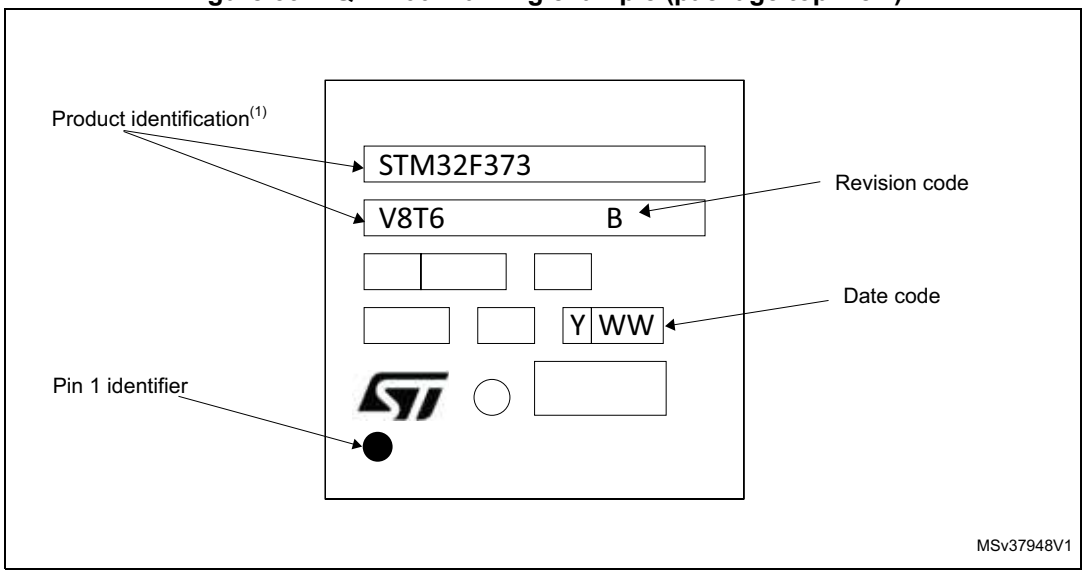


1. Dimensions are expressed in millimeters.

Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

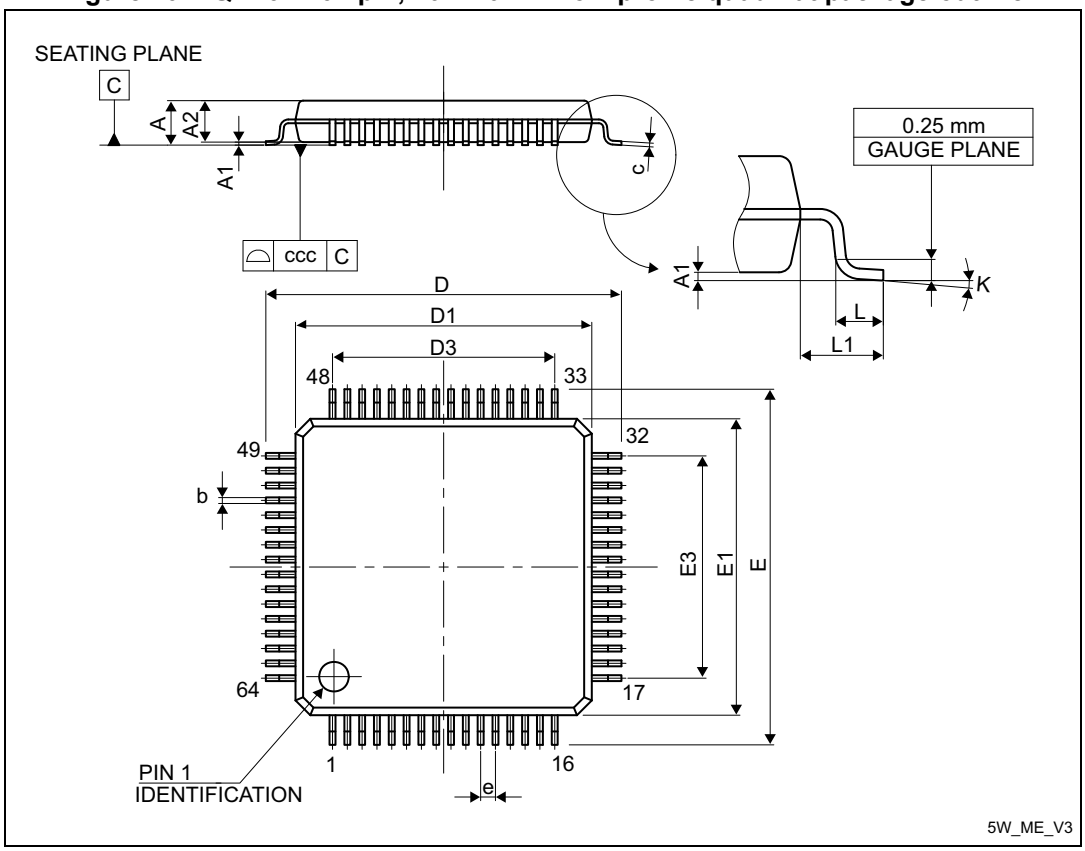
Figure 39. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.3 LQFP64 package information

Figure 40. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



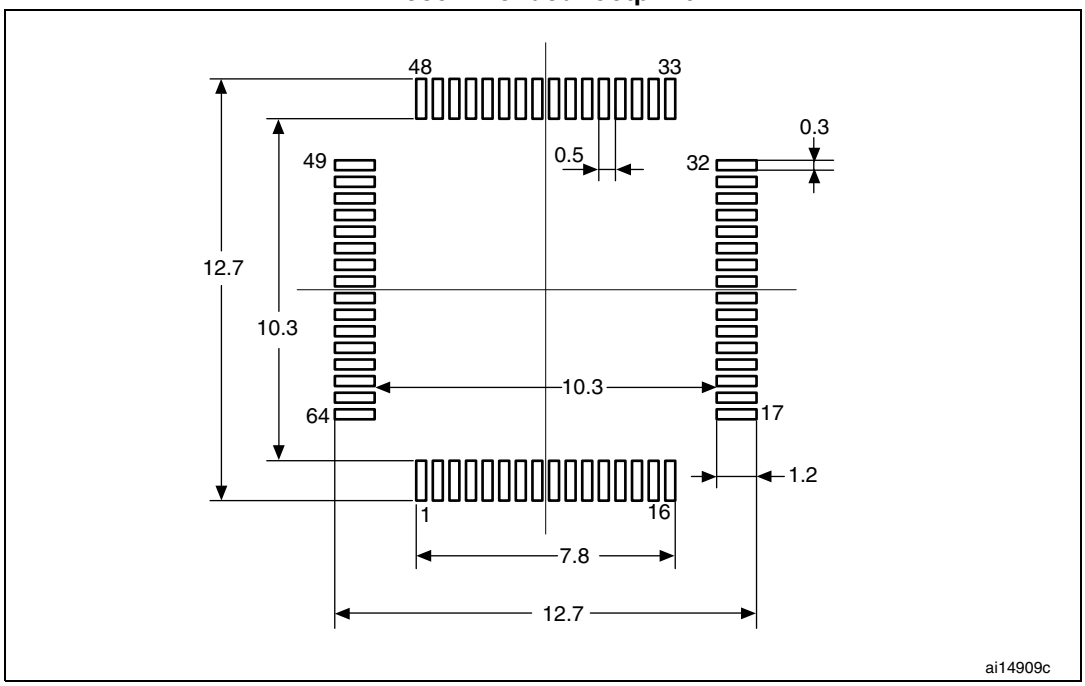
1. Drawing is not to scale.

Table 79. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 41. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint

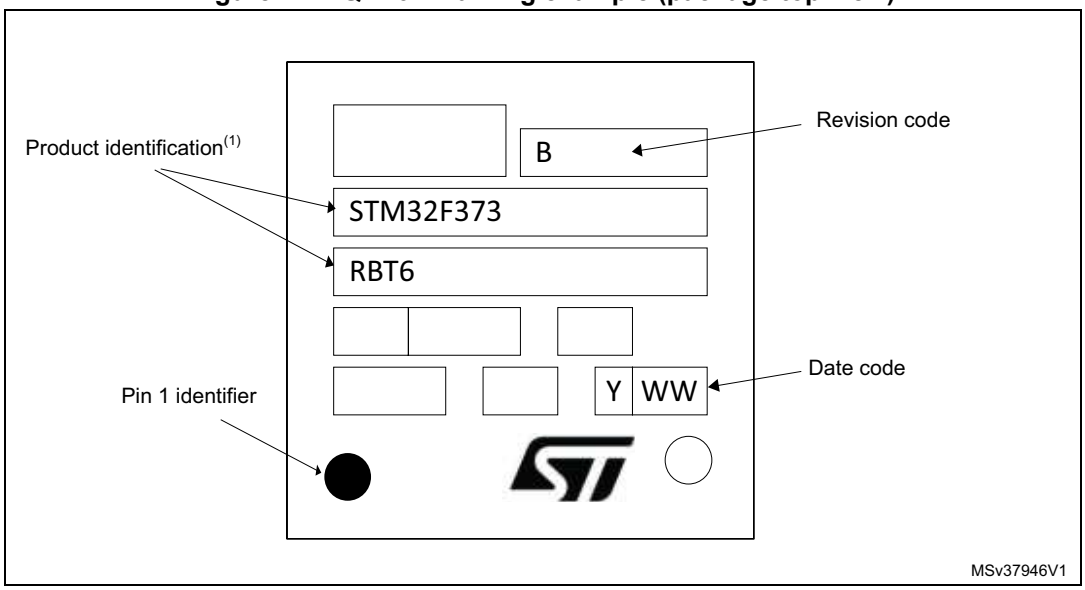


1. Dimensions are expressed in millimeters.

Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

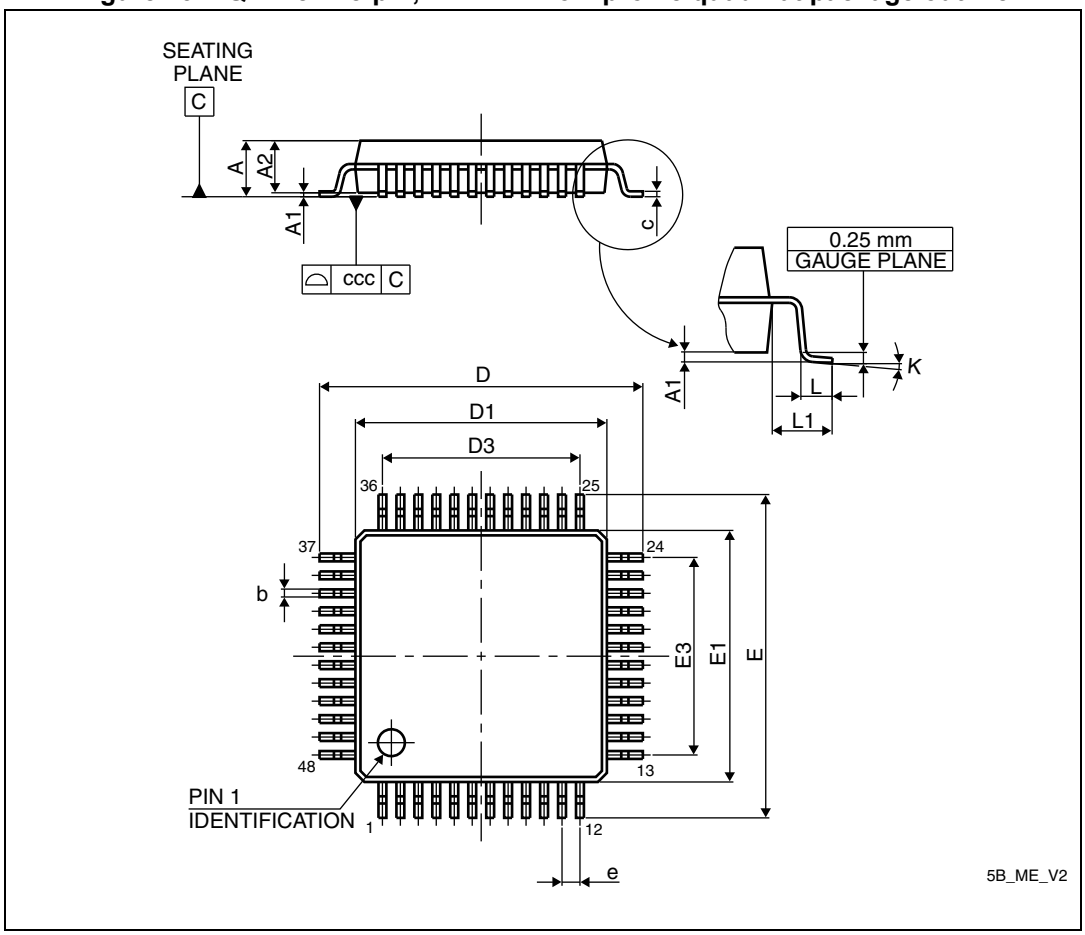
Figure 42. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.4 LQFP48 package information

Figure 43. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



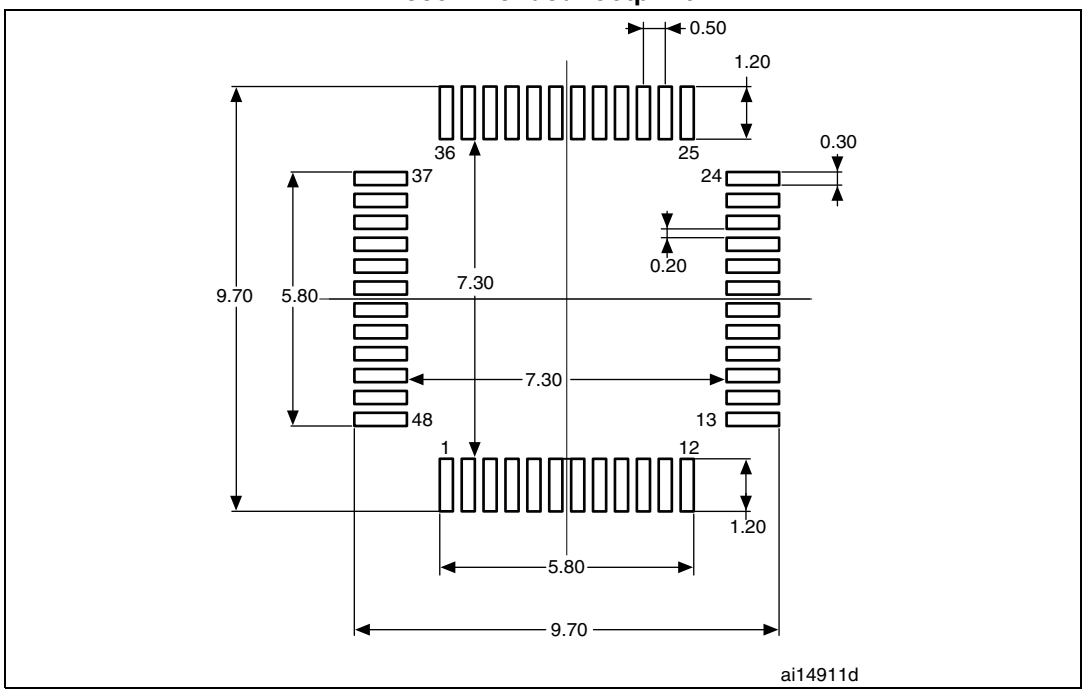
1. Drawing is not to scale.

Table 80. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

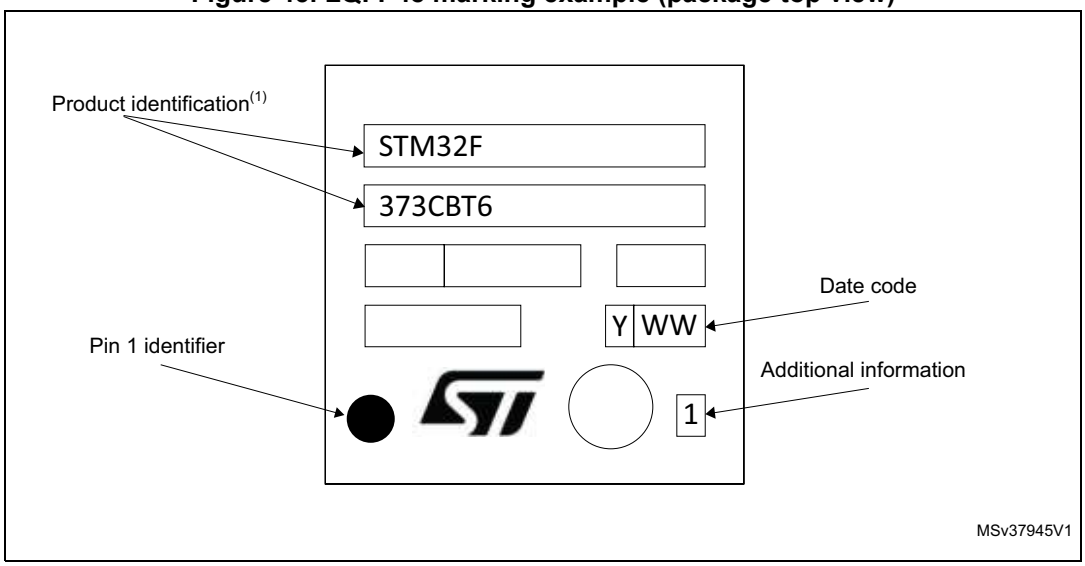


1. Dimensions are expressed in millimeters.

Device marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 45. LQFP48 marking example (package top view)



1. Samples marked “ES” are to be considered as “Engineering Samples”: i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

7.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 22: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times Q_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Q_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = S\,(V_{OL} \times I_{OL}) + S((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 81. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient BGA100 - 7 x 7 mm	59	

7.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F373xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 3 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 2 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 3 × 8 mA × 0.4 V + 2 × 20 mA × 1.3 V = 61.6 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 61.6 mW:

P_{Dmax} = 175+ 61.6 = 236.6 mW

Thus: P_{Dmax} = 236.6 mW

Using the values obtained in *Table 81* T_{Jmax} is calculated as follows:

– For LQFP64, 45°C/W

T_{Jmax} = 82 °C + (45°C/W × 236.6 mW) = 82 °C + 10.65 °C = 92.65 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Part numbering*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 9 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 9 × 8 mA × 0.4 V = 28.8 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 28.8 mW:

P_{Dmax} = 70 + 28.8 = 98.8 mW

Thus: P_{Dmax} = 98.8 mW

Using the values obtained in *Table 81* T_{Jmax} is calculated as follows:

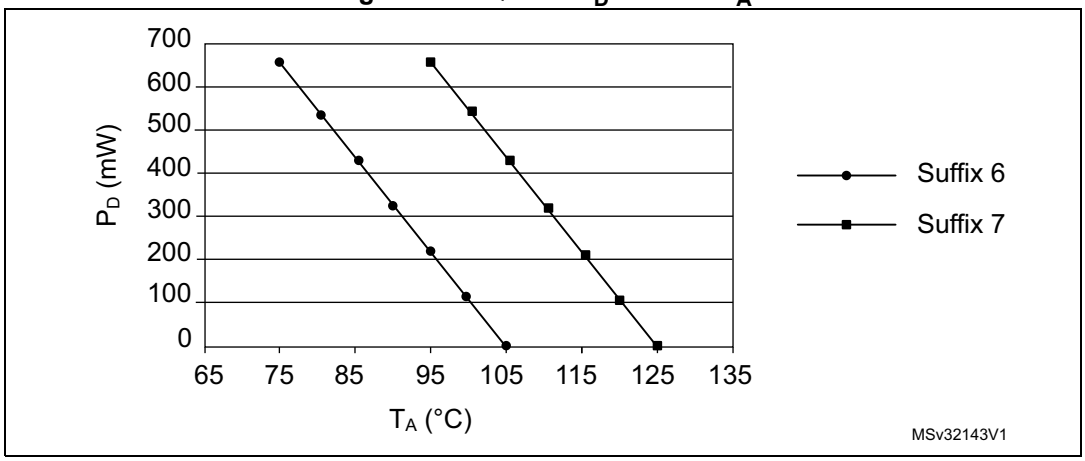
– For LQFP100, 46°C/W

T_{Jmax} = 115 °C + (46°C/W × 98.8 mW) = 115 °C + 4.54 °C = 119.5 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*).

Figure 46. LQFP64 P_D max vs. T_A



8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 82. Ordering information scheme

Example: STM32 F 373 R 8 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

373 = STM32F373xx

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Code size

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

Package

T = LQFP

H = BGA

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts

TR = tape and reel

9 Revision history

Table 83. Document revision history

Date	Revision	Changes
18-Jun-2012	1	Initial release.
07-Sep-2012	2	Added ‘F’ to all ‘Cortex-M4’ occurrences Modified the shapes of *Figure 2: STM32F373xx LQFP48 pinout* to *Figure 4: STM32F373xx LQFP100 pinout* Added two rows ‘VREFSD+ - VDDSD3’ and ‘VREF+ - VDDA’ in *Table 19: Voltage characteristics* Removed PB0 in footnote of *Table 19: Voltage characteristics* and in *Section 6.3.14: I/O port characteristics* Added a paragraph after ‘...power up sequence’ in *Section 6.2: Absolute maximum ratings* and after ‘...in output mode’ in *I/O system current consumption* Corrected SDAC_VREF+ in *Figure 9: Power supply scheme* Modified *Table 20: Current characteristics* Added BGA100 in *Table 22: General operating conditions* Added values in *Table 27: Embedded internal reference voltage* Filled values in *Table 28: Typical and maximum current consumption from VDD supply at VDD = 3.6 V* Filled values in *Table 29: Typical and maximum current consumption from VDDA supply* Filled values in *Table 30: Typical and maximum VDD consumption in Stop and Standby modes* Removed table: “Typical and maximum VDDA consumption in Stop modes” Filled values in *Table 31: Typical and maximum VDDA consumption in Stop and Standby modes* Added VBAT values in *Table 32: Typical and maximum current consumption from VBAT supply* Added typ values in *Table 33: Typical current consumption in Run mode, code with data processing running from Flash* and *Table 34: Typical current consumption in Sleep mode, code running from Flash or RAM* Added max value in *Table 41: LSE oscillator characteristics (fLSE = 32.768 kHz)* Modified min and max values in *Table 42: HSI oscillator characteristics* Added values in *Table 37: Low-power mode wakeup timings* Added Class values in *Table 47: EMS characteristics* Modified values in *Table 48: EMI characteristics* Added values in *Table 49: ESD absolute maximum ratings* Added class value in *Table 50: Electrical sensitivities* Modified values and descriptions in *Table 51: I/O current injection susceptibility*

Table 83. Document revision history (continued)

Date	Revision	Changes
07-Sep-2012	2 (cont'd)	Filled values in *Table 70: WWDG min-max timeout value @72 MHz (PCLK)* Filled values in *Table 58: SPI characteristics* Filled values in *Table 59: I2S characteristics* Replaced *Table 60: ADC characteristics* Added values in *Table 74: SDADC characteristics* Modified footnote in *Table 75: VREFSD+ pin characteristics* Replaced 'AIN' with 'SRC' in *Table 61: RSRC max for fADC = 14 MHz* and *Figure 30: Typical connection diagram using the ADC* Reordered chapters and Cover page features. Added subsection to GPIOS in *Table 2: Device overview* Aligned SRAM with USB in *Figure 1: Block diagram* Added "Do not reconfigure..." sentence in *Section 3.9: General-purpose input/outputs (GPIOs)* Added *Table 7: STM32F373xx I2C implementation* Added *Table 8: STM32F373xx USART implementation* Merged SPI and I2S into one section Reshaped *Figure 5: STM32F373xx BGA100 ballout* and removed ADC10 Added notes column, modified I/O structure values and pin, function names, removed TIM1_TX & TIM1_RX in *Table 11: STM32F373xx pin definitions* Added the note "do not reconfigure..." after *Table 11: STM32F373xx pin definitions* Modified "x_CK" occurrences to "I2Sx_CK" in *Table 12: Alternate functions for port PA* to *Table 17: Alternate functions for port PF* Added two GP I/Os in *Figure 9: Power supply scheme* Added Caution after *Figure 9: Power supply scheme* Added Max values in *Table 23: Operating conditions at power-up / power-down* Modified (1) footnote in *Table 24: Embedded reset and power control block characteristics* Added row to *Table 27: Embedded internal reference voltage* Added the note " It is recommended..." under *Table 51: I/O current injection susceptibility* Modified *Table 51: I/O current injection susceptibility* Modified temperature and current values in *Section 7.5.2: Selecting the product temperature range* Added crystal EPSON-TOYOCOM bullet under *Typical current consumption* Modified *Figure 9: Power supply scheme* Removed Boot 0 section Modified *Table 73: USB: Full-speed electrical characteristics*

Table 83. Document revision history (continued)

Date	Revision	Changes
21-Dec-2012	3	Updated *Table 2: Device overview*, capacitive sensing channels peripheral added. Updated *Table 3: Capacitive sensing GPIOs available on STM32F373xx devices* Updated *Section 3.19: Inter-integrated circuit interface (I2C)* Updated the function names in *Table 11: STM32F373 pin definitions* Updated *Table 20: Current characteristics* Updated *Table 22: General operating conditions* Updated *Table 30: Typical and maximum VDD consumption in Stop and Standby modes* Updated *Table 32: Typical and maximum current consumption from VBAT supply* Added *Figure 11: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0]='00')* Updated *Table 33: Typical current consumption in Run mode, code with data processing running from Flash* and *Table 34: Typical current consumption in Sleep mode, code running from Flash or RAM* Added *Table 35: Switching output I/O current consumption* Added *Table 36: Peripheral current consumption*, *Figure 16: HSI oscillator accuracy characterization results* Updated *Section 6.3.6: Wakeup time from low-power mode* Updated *Table 37: Low-power mode wakeup timings* Updated *Table 47: EMS characteristics* Updated *Table 51: I/O current injection susceptibility* Updated *Table 52: I/O static characteristics* Updated , *Figure 18: TC and TTa I/O input characteristics - TTL port*, *Figure 19: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port* and *Figure 20: Five volt tolerant (FT and FTf) I/O input characteristics - TTL port* Updated *Table 53: Output voltage characteristics* Updated *Table 54: I/O AC characteristics* Updated *Table 55: NRST pin characteristics* Updated *Table 63: DAC characteristics* Updated *Table 74: SDADC characteristics* Updated *Figure 32: LQFP100 –14 x 14 mm 100-pin low-profile quad flat package outline*, *Figure 35: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Figure 38: LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package outline* Updated *Table 72: LQPF100 – 14 x 14 mm low-profile quad flat package mechanical data*, *Table 73: LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data* and *Table 74: LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data* Added *Figure 16: HSI oscillator accuracy characterization results*

Table 83. Document revision history (continued)

Date	Revision	Changes
19-Sep-2013	4	Replaced “Cortex-M4F” with “Cortex-M4” throughout the document. Removed part number STM32F372xx. Added “1.25 DMIPS/MHz (Dhrystone 2.1)” in *Features*. Updated *Introduction*. Added reference to the STMTouch touch sensing firmware library in *Section 3.16: Touch sensing controller (TSC)*. Added “All I2S interfaces can operate in half-duplex mode only.” in *Section 3.21: Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)*. Added row “I2S full-duplex mode” to *Table 9: STM32F373xx SPI/I2S implementation*. Modified introduction of *I2C interface characteristics*. Added alternate function RTC_REFIN and removed additional function RTC_REF_CLK_IN to pins PA1 and PB15. Replaced alternate function JNTRST with NJTRST for pin PB4. In *Table 12: Alternate functions for port PA*: replaced alternate function JTMS-SWDIO with SWDIO-JTMS for pin PA13, and JTCK-SWCLK with SWCLK-JTCK for pin PA14. Added rows V_{REF+} and V_{REFSD+} to *Table 22: General operating conditions*. Replaced "$f_{APB1} = f_{AHB/2}$" with "$f_{APB1} = f_{AHB}$" for “When the peripherals are enabled...” in *Typical current consumption*. Added COMP in *Table 36: Peripheral current consumption* Added conditions for f_{HSE_ext} in *Table 38: High-speed external user clock characteristics*. Added Min and Max values for ACC_{HISI} in *Table 42: HSI oscillator characteristics*. Replaced reference "JESD22-C101" with "ANSI/ESD STM5.3.1" in *Table 49: ESD absolute maximum ratings*. Removed pins PB0 and PB1 in description of I_{INJ} in *Table 51: I/O current injection susceptibility*. Updated *Table 56: I2C characteristics*. Replaced all occurrences of “gain/2” with “gain*2” in *Table 74: SDADC characteristics*. Corrected typo in *Figure 21: I/O AC characteristics definition*. Replaced *Figure 23: I2C bus AC waveforms and measurement circuit*.. Added $I_{DDA(ADC)}$ and footnote 1 in *Table 60: ADC characteristics*

Table 83. Document revision history (continued)

Date	Revision	Changes
18-Mar-2014	5	Renamed part number STM32F37x to STM32F373xx Added note1 in *Table 28: Typical and maximum current consumption from VDD supply at VDD = 3.6 V* Updated *Chapter 3.14: Digital-to-analog converter (DAC)* Updated, added note 2 and 3 in *Table 57: I2C analog filter characteristics* Renamed t_{SP} symbol with $t_{AF.}$ Added note for EG Symbol in *Table 74: SDADC characteristics* Added all packages top view
21-Jul-2015	6	Updated *Section 7* Updated *Section 3.13* Updated *Section 3.7.1*, *Section 3.7.4* Updated *Table 11: STM32F373xx pin definitions*, *Table 19: Voltage characteristics*, *Table 49: ESD absolute maximum ratings*, *Table 74: SDADC characteristics*, *Table 76: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data*, and *Table 78: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data* Updated *Figure 2: STM32F373xx LQFP48 pinout*, *Figure 9: Power supply scheme*, *Figure 34: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline*, *Figure 36: UFBGA100 marking example (package top view)*, *Figure 38: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 39: LQFP100 marking example (package top view)*, *Figure 40: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline*, *Figure 41: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint*, *Figure 42: LQFP64 marking example (package top view)*, *Figure 44: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint*, *Figure 45: LQFP48 marking example (package top view)*. Added *Table 32: Typical and maximum current consumption from VBAT supply*, *Table 49: ESD absolute maximum ratings*, *Table 64: Comparator characteristics*, *Table 77: UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)*. Added *Figure 11: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0]='00')*, *Figure 32: Maximum VREFINT scaler startup time from power down*, *Figure 35: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint*.

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