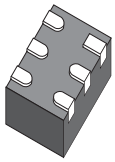
HSP062-2

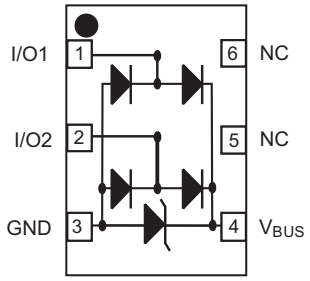
2-line ESD protection for high speed lines

Datasheet - production data



HSP062-2M6
µQFN-6L package

Figure 1. Functional schematic (top view)



µQFN 6 leads

Features

- Flow-through routing to keep signal integrity
- Ultralarge bandwidth: 4.6 GHz
- Ultralow capacitance: 0.6 pF
- Low leakage current: 100 nA at 25 °C
- Extended operating junction temperature range: -40 °C to 150 °C
- RoHS compliant

Benefits

- High ESD robustness of the equipment
- Suitable for high density boards

Complies with following standards

- MIL-STD 883G Method 3015-7 Class 3B:
  - 8 kV
- IEC 61000-4-2 level 4:
  - 15 kV (air discharge)
  - 8 kV (contact discharge)

Applications

The HSP062-2M6 is designed to protect against electrostatic discharge on sub micron technology circuits driving:

- HDMI 1.3 and 1.4
- Digital Video Interface
- Display Port
- USB 3.0
- Serial ATA
- Ethernet
- HMI

Description

The HSP062-2 is a 2-channel ESD array with a rail to rail architecture designed specifically for the protection of high speed differential lines.

The ultralow variation of the capacitance ensures very low influence on signal-skew. The large bandwidth makes it compatible with 5 Gbps.

The device is packaged in µQFN-6L (1.45 x 1.0 mm) with a 500 µm pitch.

This is information on a product in full production. www.st.com

1 Characteristics

Table 1. Absolute maximum ratings T_{amb} = 25 °C

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 contact discharge	8	kV
		IEC 61000-4-2 air discharge	15	
I_{pp}	Repetitive peak pulse current (8/20 µs)		3	A
T_j	Operating junction temperature range		-40 to +150	°C
T_{stg}	Storage temperature range		-65 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

Table 2. Electrical characteristics T_{amb} = 25 °C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	Breakdown voltage	I_R = 1 mA	6			V
I_{RM}	Leakage current	V_{RM} = 3 V			100	nA
V_{CL}	Clamping voltage	IEC 61000-4-2, +8 kV contact (I_{PP} = 30 A), measured at 30 ns		18		V
$C_{I/O - GND}$	Capacitance (input/output to ground)	$V_{I/O}$ = 0 V, F = 200 to 3000 MHz, V_{OSC} = 30 mV		0.6	0.9	pF
$\Delta C_{I/O - GND}$	Capacitance variation (input/output to ground)	$V_{I/O}$ = 0 V F = 200 to 3000 MHz, V_{OSC} = 30 mV		0.09	0.17	pF
f_C	Cut-off frequency	-3 dB		4.6		GHz

Figure 2. Leakage current versus junction temperature (typical values)

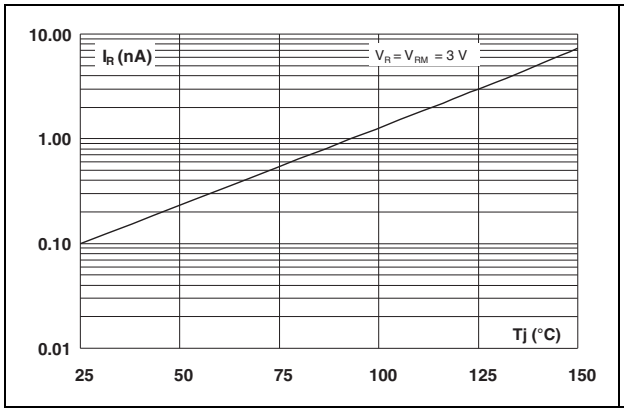


Figure 3. S21 attenuation measurement

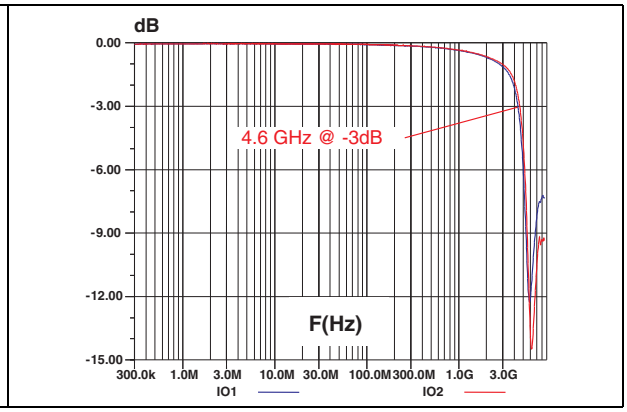


Figure 4. Eye diagram - HDMI mask at 3.4 Gbps per channel(1) (HSP062-2M6)

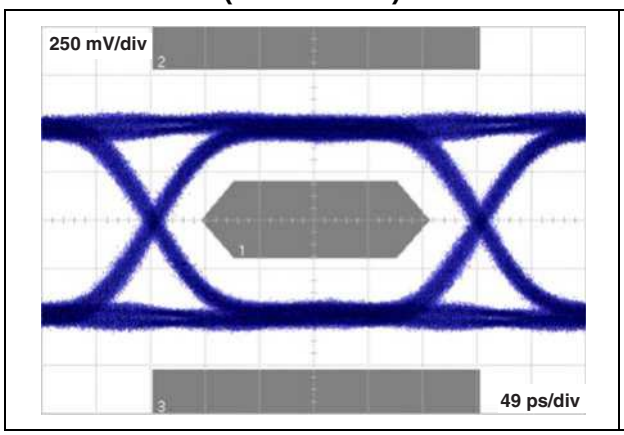
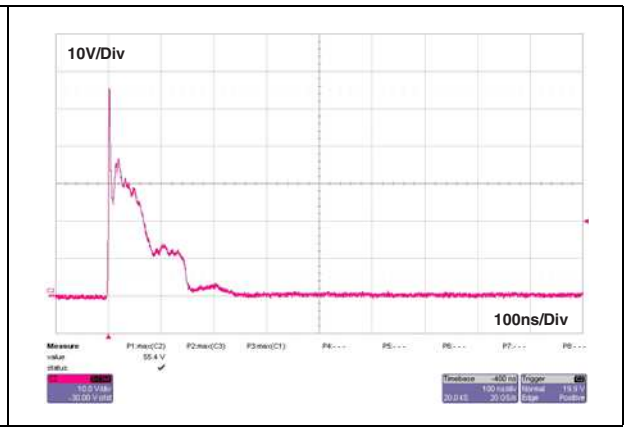
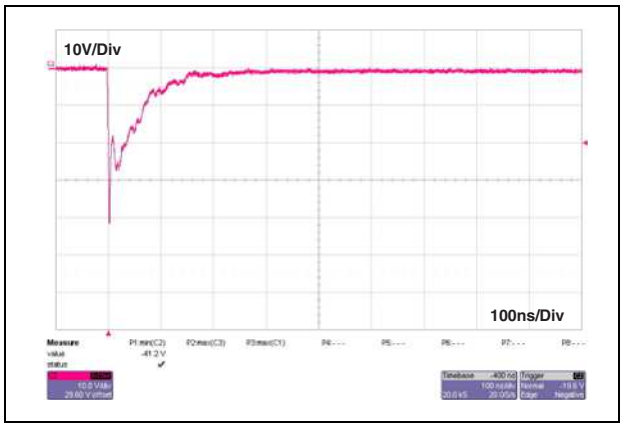


Figure 5. ESD response to IEC 61000-4-2 (+8 kV contact discharge)



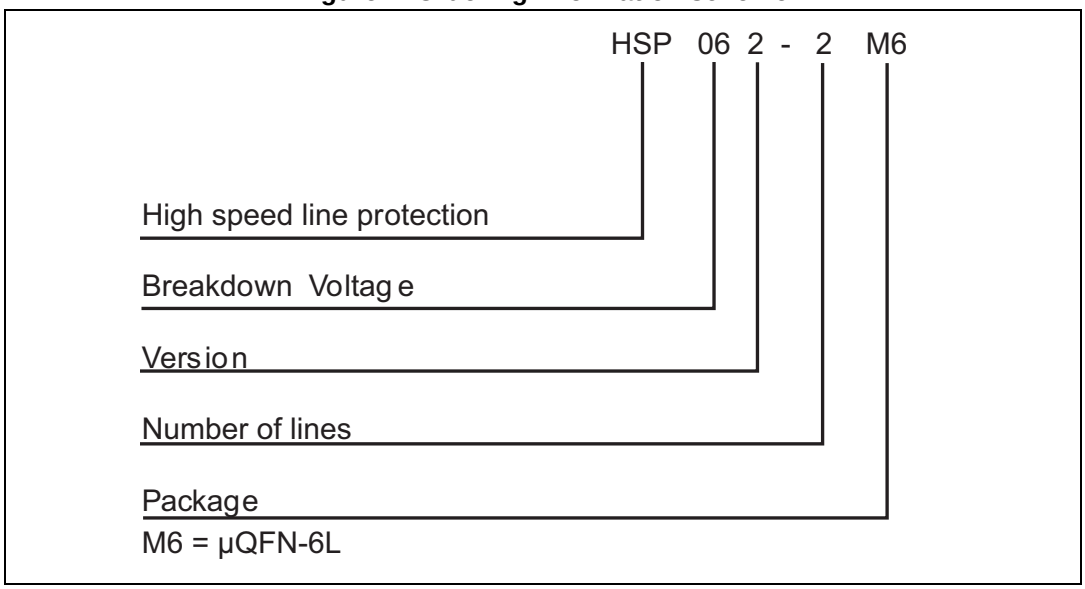
1. HDMI specification conditions. This information can be provided for other applications. Please contact your local ST office.

Figure 6. ESD response to IEC 61000-4-2 (-8 kV contact discharge)



2 Ordering information scheme

Figure 7. Ordering information scheme

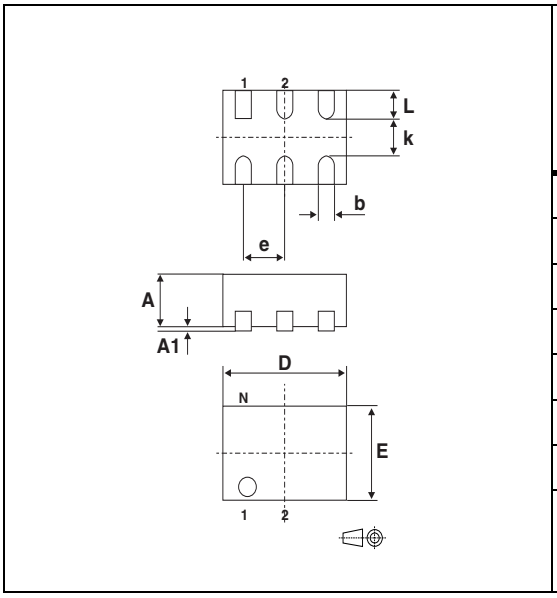


3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. Micro QFN 1.45x1.00 6L dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
D		1.45			0.057	
E		1.00			0.039	
e		0.50			0.020	
K	0.20			0.008		
L	0.30	0.35	0.40	0.012	0.014	0.016

Figure 8. Footprint recommendations dimensions in mm (inches)

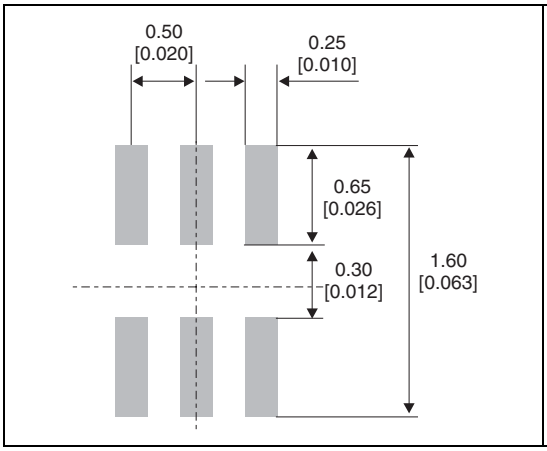


Figure 9. Marking for Micro QFN 1.45x1.00 6L



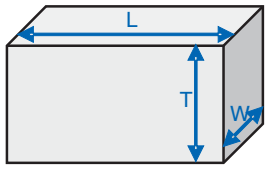
Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 10. Stencil opening dimensions



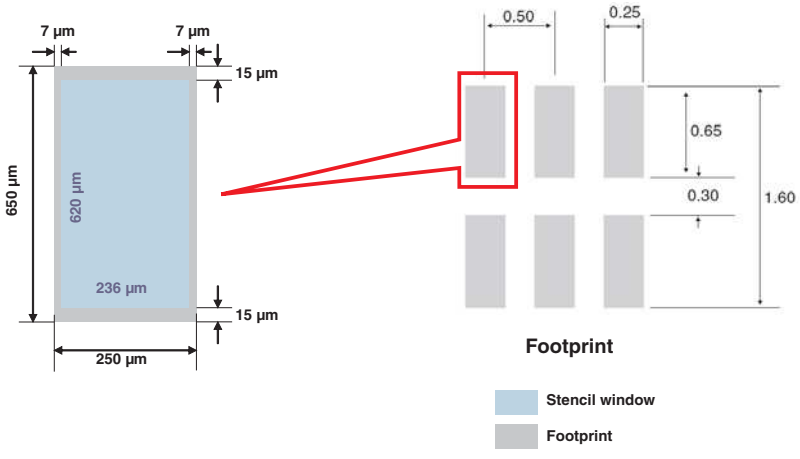
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 11. Recommended stencil window position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

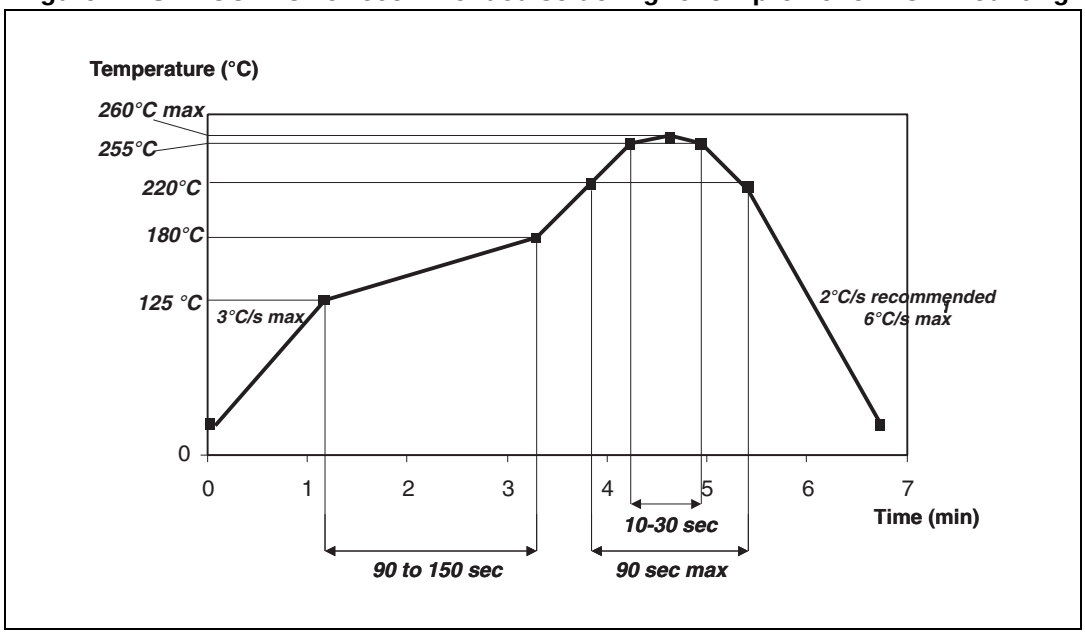
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 12. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
HSP062-2M6	S(1)	µQFN-6L	2.3 mg	3000	Tape and reel (7”)

1. The marking can be rotated by multiple of 90° to differentiate assembly location

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
07-Feb-2012	1	Initial release.
19-Mar-2014	2	Minor text changes.
07-Oct-2015	3	Removed device in SOT-666. Updated document accordingly.

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