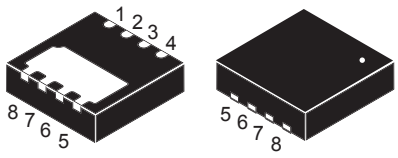
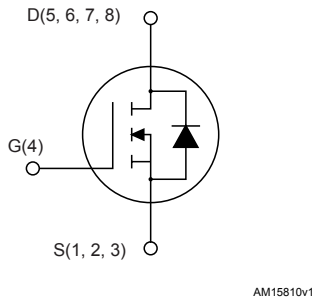
STL3NM60N

Datasheet

N-channel 600 V, 1.5 Ω typ., 2.2 A MDmesh II Power MOSFET in a PowerFLAT 3.3x3.3 HV package



PowerFLAT 3.3x3.3 HV



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL3NM60N	600 V	1.8 Ω	2.2 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Product status link
STL3NM60N

Product summary	
Order code	STL3NM60N
Marking	3NM60
Package	PowerFLAT 3.3x3.3 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	2.2	A
	Drain current (continuous) at T_C = 100 °C	1.7	
	Drain current (continuous) at T_A = 25 °C	0.65	
	Drain current (continuous) at T_A = 100 °C	0.5	
I_{DM} (1)	Drain current pulsed	2.6	A
P_{TOT}	Total power dissipation at T_A = 25 °C	2	W
	Total power dissipation at T_C = 25 °C	22	W
I_{AS}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max)	1	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AS}, V_{DD} = 50 V)	119	mJ
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 2.2 A, di/dt ≤ 400 A/µs, V_{DS} (peak) ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	5.6	°C/W
R_{thJA}(1)	Thermal resistance, junction-to-ambient	62.5	°C/W

1. *When mounted on an 1-inch² FR-4, 2 Oz copper board, t < 10 s .*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1 A		1.5	1.8	Ω

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	188	-	pF
C_{oss}	Output capacitance		-	13	-	pF
C_{rss}	Reverse transfer capacitance		-	1.1	-	pF
$C_{oss\ eq.}$(1)	Equivalent capacitance energy related	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	100	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 2.2 A	-	9.5	-	nC
Q_{gs}	Gate-source charge	V_{GS} = 0 to 10 V	-	1.6	-	nC
Q_{gd}	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	5.3	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 1.1 A,	-	8.6	-	ns
t_r	Rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	6.2	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	20.8	-	ns
t_f	Fall time		-	20	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.2	A
I_{SDM}(1)	Source-drain current (pulsed)		-		2.6	A
V_{SD}(2)	Forward on voltage	I_{SD} = 2.2 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 2.2 A, di/dt = 100 A/µs,	-	168		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	672		nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	8		A
t_{rr}	Reverse recovery time	I_{SD} = 2.2 A, di/dt = 100 A/µs,	-	2.3		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_J = 150 °C	-	913		nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

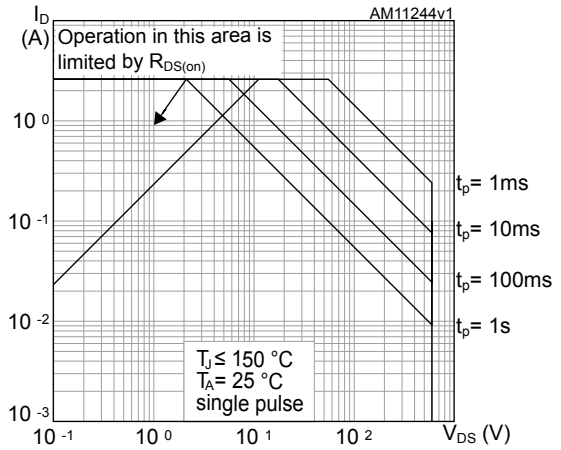


Figure 2. Normalized transient thermal impedance

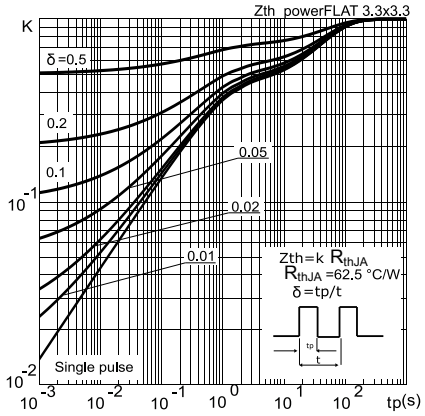


Figure 3. Typical output characteristics

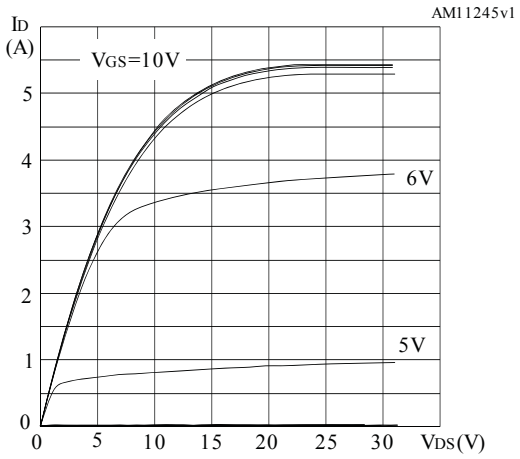


Figure 4. Typical transfer characteristics

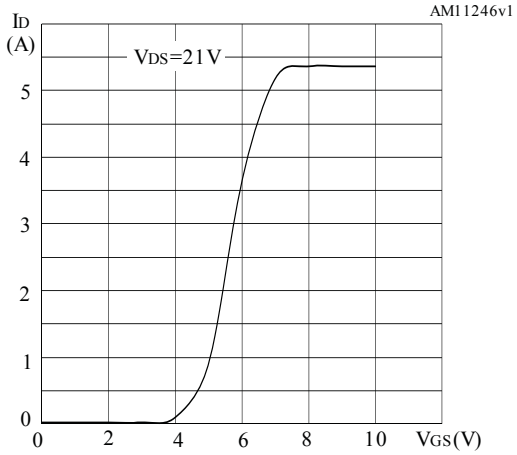


Figure 5. Typical gate charge characteristics

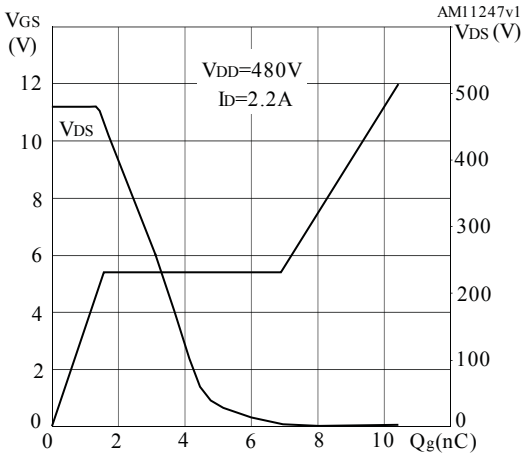


Figure 6. Typical drain-source on-resistance

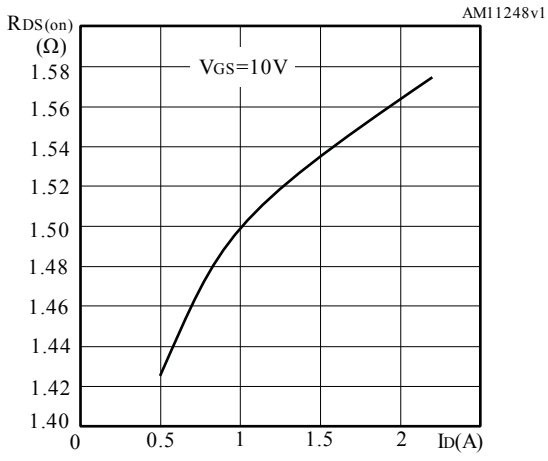


Figure 7. Typical capacitance characteristics

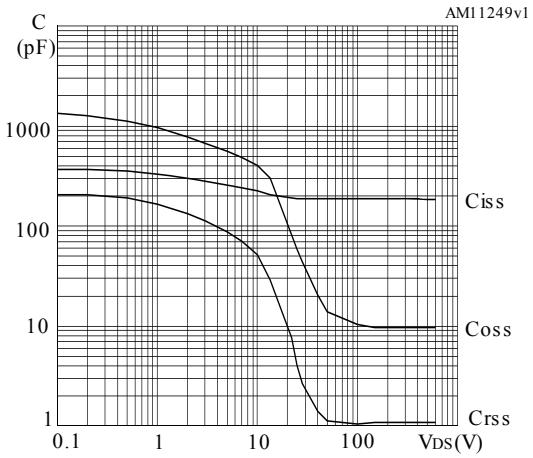


Figure 8. Typical output capacitance stored energy

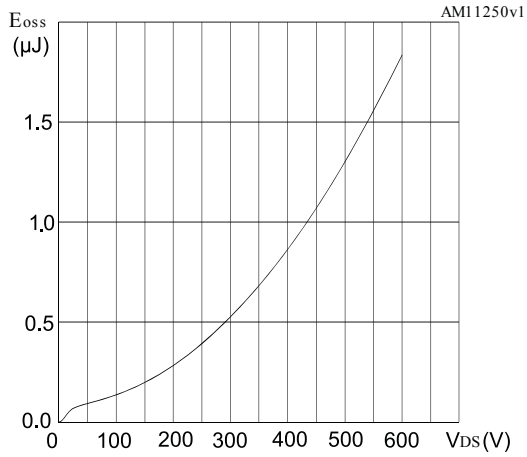


Figure 9. Normalized gate threshold vs temperature

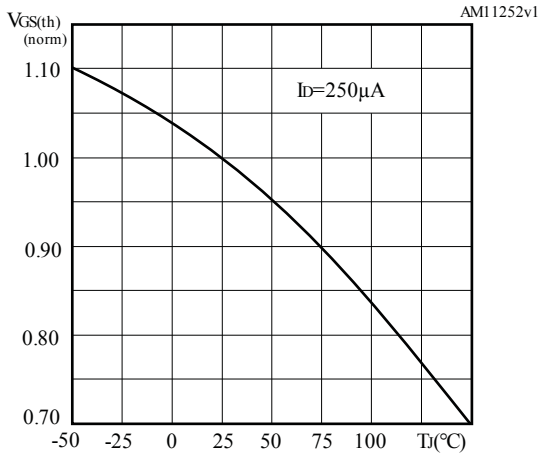


Figure 10. Normalized on-resistance vs temperature

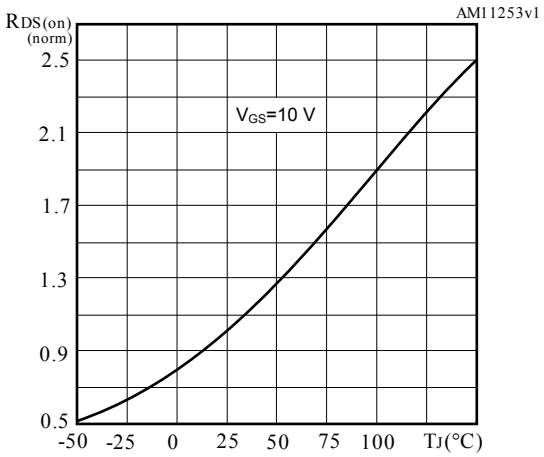


Figure 11. Normalized breakdown voltage vs temperature

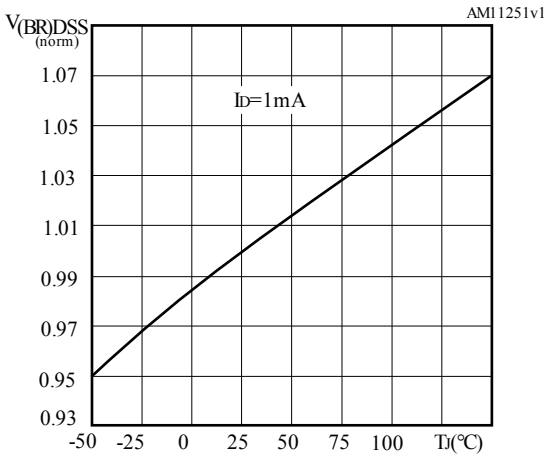
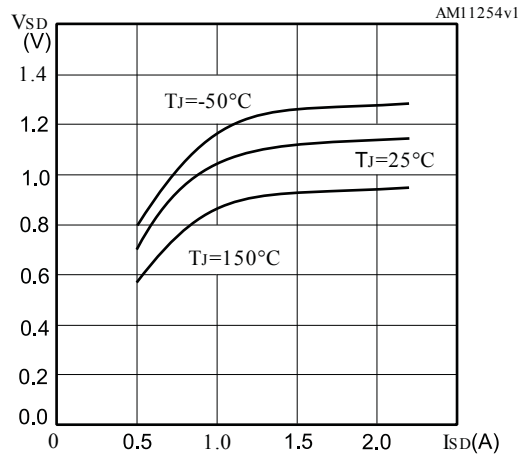
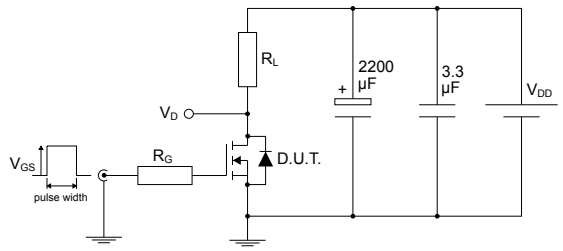


Figure 12. Typical reverse diode forward characteristics



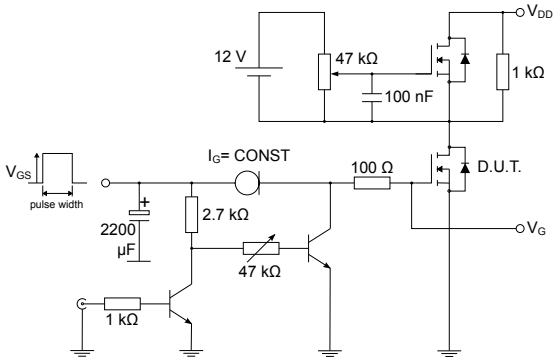
3 Test circuits

Figure 13. Test circuit for resistive load switching times



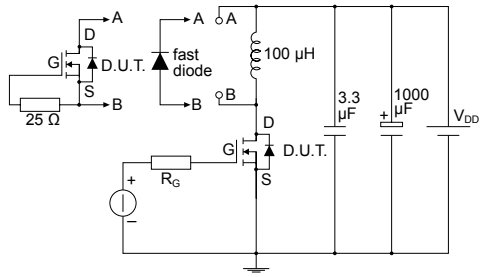
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Figure 14. Test circuit for gate charge behavior



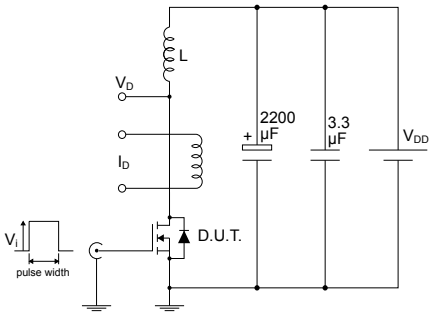
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Figure 15. Test circuit for inductive load switching and diode recovery times



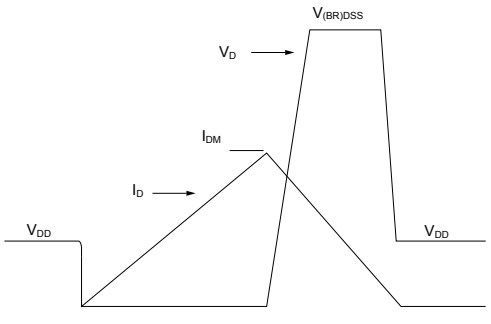
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Figure 16. Unclamped inductive load test circuit



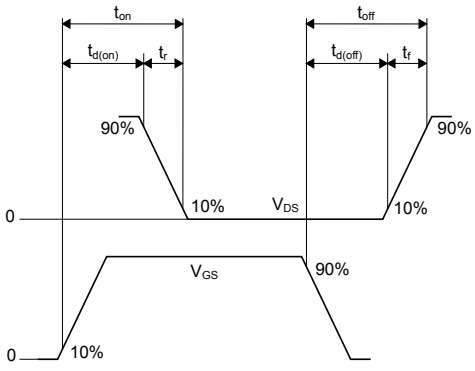
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



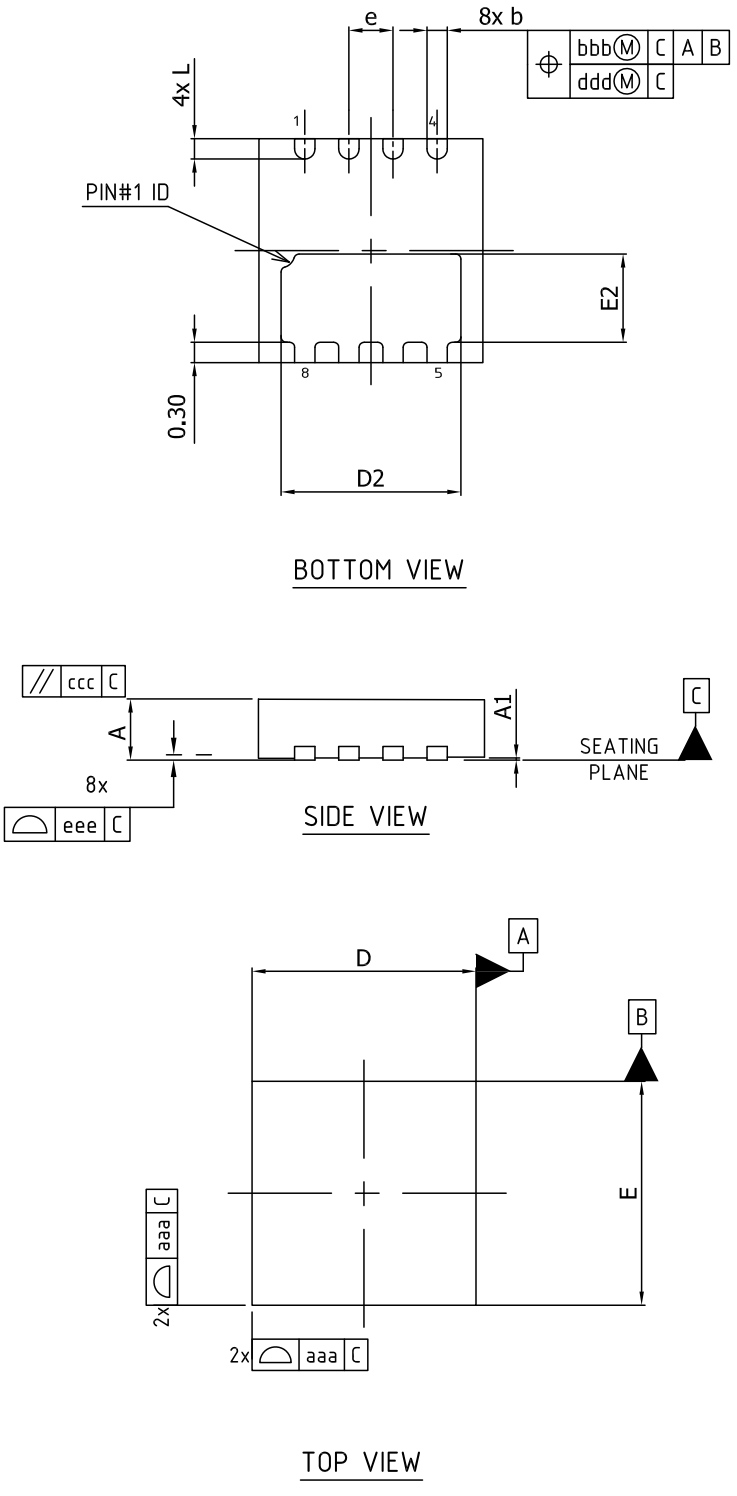
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 3.3x3.3 HV package information

Figure 19. **PowerFLAT 3.3x3.3 HV package outline**

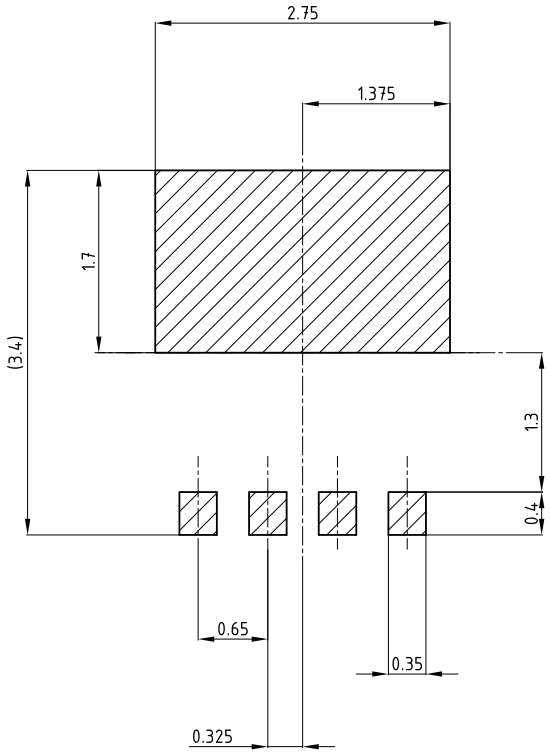


8374983_Rev_2

Table 7. PowerFLAT 3.3x3.3 HV package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
b	0.25	0.30	0.40
D		3.30	
D2	2.50	2.65	2.75
E		3.30	
E2	1.15	1.30	1.40
e		0.65	
L	0.20	0.30	0.40
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Figure 20. PowerFLAT 3.3x3.3 HV recommended footprint (dimensions are in mm)



Revision history

Table 8. **Document revision history**

Date	Version	Changes
12-Mar-2012	1	First release.
19-Nov-2014	2	Document status changed from preliminary to production data. Updated *Figure 1.: Internal schematic diagram*, *Figure 2.: Safe operating area*, *Figure 3.: Thermal impedance* and *Figure 12.: Normalized $V_{(BR)DSS}$ vs temperature.* Updated *Table 5.: Dynamic* and *Table 7.: Source drain diode*. Minor text changes.
26-May-2022	3	Modified marking on cover page Updated Figure 1. Safe operating area Modified I_{SDM} value in Table 6. Source-drain diode Updated Section 4.1 PowerFLAT 3.3x3.3 HV package information Minor text changes.

Contents

1 **Electrical ratings** 2

2 **Electrical characteristics** 3

2.1 Electrical characteristics (curves) 5

3 **Test circuits** 7

4 **Package information** 8

4.1 PowerFLAT 3.3x3.3 HV package information 9

Revision history 11

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