M95128-A125 M95128-A145

Datasheet

Automotive 128-Kbit serial SPI bus EEPROMs with high-speed clock



SO8N

(150 mil width)



TSSOP8

(169 mil width)



WFDFPN8 (MF)

DFN8 - 2 x 3 mm

Product status
M95128-A125
M95128-A145

Product label
LONGEVITY 15 YEARS COMMITMENT

Features

Grade

- AEC-Q100 grade 0 conform qualification

SPI interface

- Compatible with the serial peripheral interface (*SPI*) bus

Memory

- 128-Kbit (16-Kbyte) *EEPROM*
- Page size: 64 bytes
- Additional 64-byte lockable identification page

Supply voltage

- 1.7 V to 5.5 V

Temperature

- Extended operating temperature range:
  - -40 °C up to +125 °C for range 3
  - -40 °C up to +145 °C for range 4

Clock frequency

- Up to 20 MHz

Fast write cycle time

- Byte and page write within 4 ms (typically 3.4 ms)

Advanced features

- Schmitt trigger inputs for noise filtering
- Software write protection by quarter block
- Hardware write protection of the whole memory array
- Enhanced *ESD* and latch-up protection
- *ESD* human body model 4000 V

Write cycle performance

- More than 4 million write cycles at 25 °C
- More than 1.2 million write cycles at 85 °C
- More than 0.6 million write cycles at 125 °C
- More than 0.4 million write cycles at 145 °C

Data retention performance

- More than 50 years at 125 °C
- More than 100 years at 25 °C

Packages

- SO8N, TSSOP8, and WFDFPN8 (ECOPACK2-compliant)

1 Description

The M95128-A125 and M95128-A145 are 128-Kbit serial electrically erasable programmable memory (*EEPROM*) automotive grade devices capable of operating up to 145°C. They are compliant with the very high level of reliability defined by the automotive standard AEC-Q100 grade 0.

The devices are accessed by a simple serial SPI compatible interface running up to 20 MHz.

The memory array is based on advanced true *EEPROM* technology. The M95128-A125 and M95128-A145 are byte-alterable memories (16384 × 8 bits) organized as 256 pages of 64 bytes in which the data integrity is significantly improved with an embedded error correction code logic.

The M95128-A125 and M95128-A145 offer an additional identification page (64 bytes), in which the ST device identification can be read. This page can also store sensitive application parameters, which can later be permanently locked in read-only mode.

Figure 1. Logic diagram

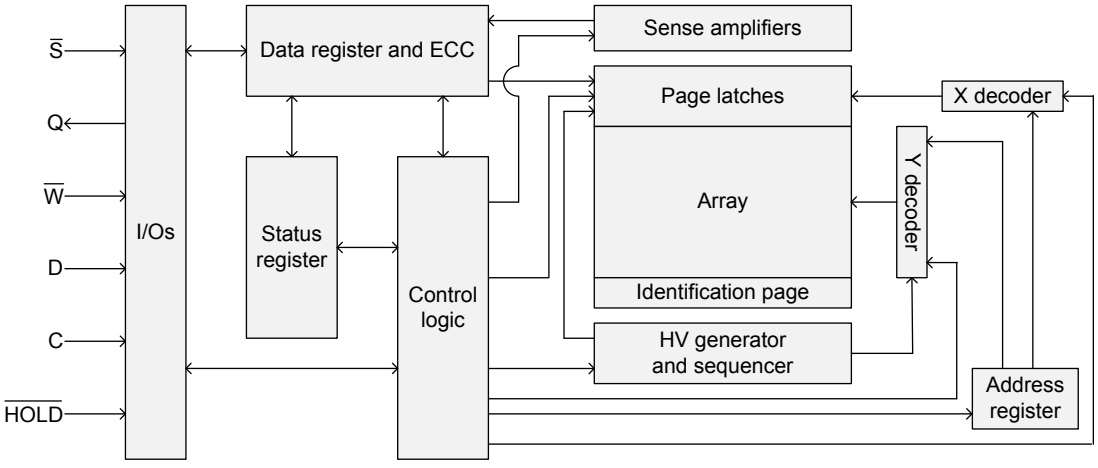
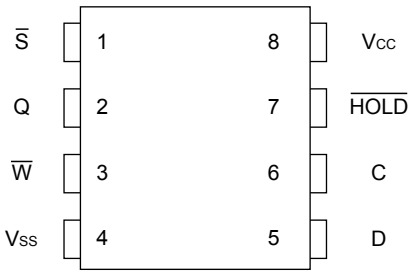


Figure 2. 8-pin package connections



1. See Section 9: Package mechanical data for package dimensions and how to identify pin 1.

Table 1. **Signal names**

Signal name	Description
C	Serial clock
D	Serial data input
Q	Serial data output
$\overline{S}$	Chip select
$\overline{W}$	Write protect
$\overline{HOLD}$	Hold
V_{CC}	Supply voltage
V_{SS}	Ground

2 Signal description

All input signals must be held high or low (according to voltages of V_{IH} or V_{IL}, as specified in Table 12 and Table 13). These signals are described below.

2.1 Serial data output (Q)

This output signal is used to transfer data serially out of the device during a read operation. Data are shifted out on the falling edge of the serial clock (C), the most significant bit (MSB) first. In all other cases, the serial data output is in high impedance.

2.2 Serial data input (D)

This input signal is used to transfer data serially into the device. D input receives instructions, addresses, and the data to be written. Values are latched on the rising edge of the serial clock (C), the most significant bit (MSB) first.

2.3 Serial clock (C)

This input signal allows to synchronize the timing of the serial interface. Instructions, addresses, or data present at serial data input (D) are latched on the rising edge of the serial clock (C). Data on serial data output (Q) changes after the falling edge of the serial clock (C).

2.4 Chip select ($\overline{S}$)

Driving chip select ($\overline{S}$) low selects the device in order to start communication. Driving chip select ($\overline{S}$) high deselects the device and serial data output (Q) enters the high impedance state.

After power-up, instructions only start following falling edge of the chip select ($\overline{S}$) signal.

2.5 Hold ($\overline{HOLD}$)

The hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting it.

During the hold condition, the serial data output (Q) is high impedance, while the states of the serial data input (D) and serial clock (C) are *don't care*.

To start the hold condition, the device must be selected, with chip select ($\overline{S}$) driven low.

2.6 Write protect ($\overline{W}$)

This pin is used to write-protect the status register.

2.7 V_{SS} ground

V_{SS} is the reference for all signals, including the V_{CC} supply voltage.

2.8 V_{CC} supply voltage

V_{CC} is the supply voltage pin. Refer to Section 3.1: Active power and standby power modes and to Section 5.1: Supply voltage (V_{CC}).

3 Operating features

3.1 Active power and standby power modes

When chip select ($\overline{S}$) is low, the device is selected and in the active power mode.

When chip select ($\overline{S}$) is high, the device is deselected. If a write cycle is not in progress, the device goes in standby power mode, and its consumption drops to I_{CC1}, as specified in Table 12 and Table 13.

3.2 SPI modes

The device can be driven by a microcontroller with its SPI peripheral running in one of the two following modes:

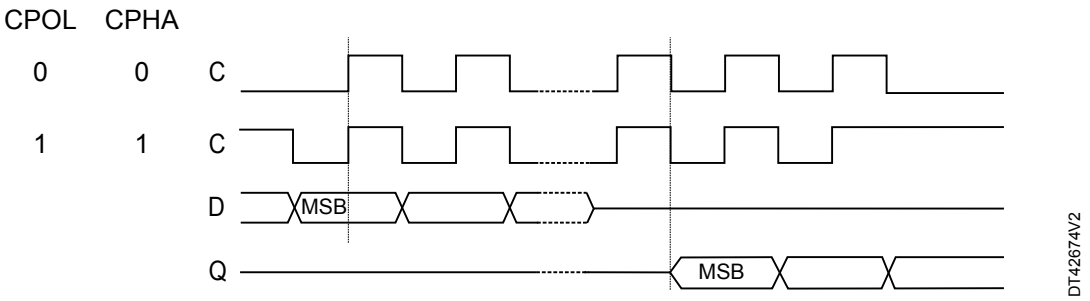
- CPOL = 0, CPHA = 0
- CPOL = 1, CPHA = 1

For these two modes, the input data are latched on the rising edge of the serial clock (C), and the output data are available from the falling edge of the serial clock (C).

The difference between the two modes, as shown in Figure 3, is the clock polarity when the bus controller is in standby mode and not transferring data:

- C remains at 0 for (CPOL = 0, CPHA = 0)
- C remains at 1 for (CPOL = 1, CPHA = 1)

Figure 3. Supported SPI modes

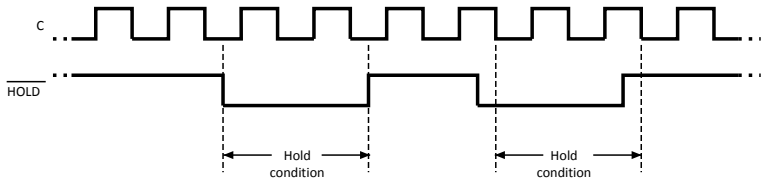


3.3 Hold mode

The hold ($\overline{\text{HOLD}}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

The hold mode starts when the hold ($\overline{\text{HOLD}}$) signal is driven low and the serial clock (C) is low (as shown in Figure 4). During the hold mode, the serial data output (Q) is high impedance, and the signals present on serial data input (D) and serial clock (C) are not decoded. The hold mode ends when the hold ($\overline{\text{HOLD}}$) signal is driven high and the serial clock (C) is or becomes low.

Figure 4. Hold mode activation



Deselecting the device while it is in hold mode resets the paused communication.

3.4 Protocol control and data protection

3.4.1 Protocol control

The chip select ($\overline{\text{S}}$) input offers a built-in safety feature, as the $\overline{\text{S}}$ input is edge-sensitive as well as level-sensitive: after power-up, the device is not selected until a falling edge has first been detected on chip select ($\overline{\text{S}}$). This ensures that chip select ($\overline{\text{S}}$) must have been high prior to going low, to start the first operation.

To ensure that the write commands (WRITE, WRSR, WRID, LID) are accepted and executed correctly, the following conditions must be met:

- A write enable (WREN) instruction sets the write enable latch (WEL) bit.
- During the entire command, a falling edge followed by a low state on chip select ($\overline{\text{S}}$) must be decoded.
- The instruction, address, and input data must be sent as multiples of eight bits.
- The command must include at least one data byte.
- The chip select ($\overline{\text{S}}$) must be driven high exactly after a data byte boundary.

Write commands can be discarded at any time by a rising edge on chip select ($\overline{\text{S}}$) outside of a byte boundary.

To execute read commands (READ, RDSR, RDID, RDLS), the device must decode:

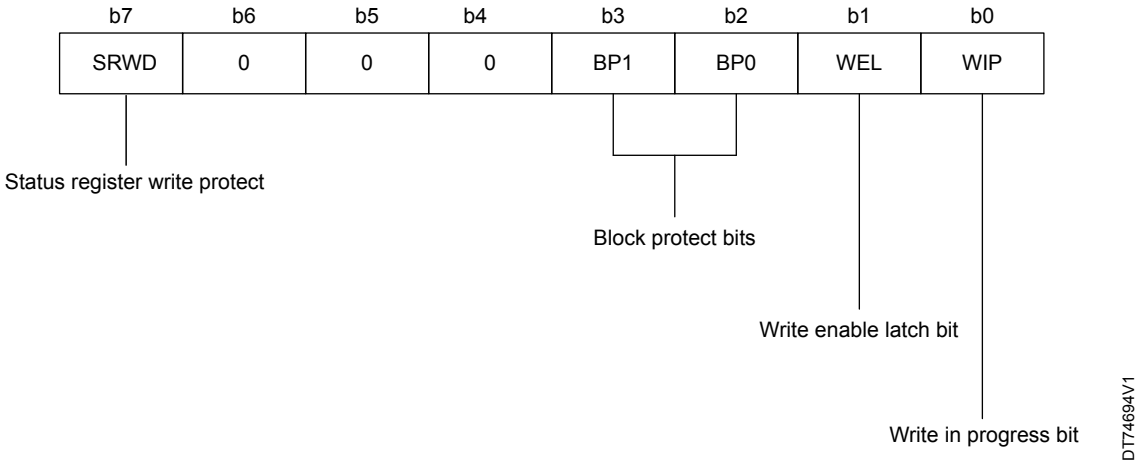
- A falling edge and a low level on chip select ($\overline{\text{S}}$) during the entire command
- The instruction and address as multiples of eight bits (byte)

From this step, data bits are shifted out until the rising edge on chip select ($\overline{\text{S}}$).

3.4.2 Status register and data protection

The status register format is shown in Figure 5.

Figure 5. Status register format



Note: The bits b6, b5, b4 are always read as 0.

WIP bit

The write in progress bit (WIP) is a read-only flag that indicates the ready/busy state of the device. When a write command (WRITE, WRSR, WRID, LID) is decoded and a write cycle (t_W) is in progress, the device is busy, and the WIP bit is set to 1. When WIP = 0, the device is ready to decode a new command.

During a write cycle, continuously reading the WIP bit detects when the device becomes ready (WIP = 0) to decode a new command.

Note: During a write lock ID operation, the device is busy, but the WIP bit remains set to 0.

WEL bit

The write enable latch (WEL) bit is a flag that indicates the status of the internal write enable latch.

When WEL is:

- 1: the write instructions (WRITE, WRSR, WRID, and LID) are executed
- 0: any decoded write instruction is not executed

The WEL bit is set to 1 with the WREN instruction. The WEL bit is reset to 0 after the following events:

- Completion of the write disable (WRDI) instruction
- Completion of write instructions (WRITE, WRSR, WRID, and LID), including the write cycle time (t_W)
- Power-up

BP1 and BP0 bits

The block protect bits (BP1, BP0) are nonvolatile. BP1 and BP0 bits define the size of the memory block to protect against write instructions, as defined in Figure 5. These bits are written using the write status register (WRSR) instruction, provided that the status register is not protected (refer to SRWD bit and W input signal)

Table 2. **Write-protected block size**

Status register bits		Protected block	Protected array addresses
BP1	BP0		
0	0	None	None
0	1	Upper quarter	3000h-3FFFh
1	0	Upper half	2000h-3FFFh
1	1	Whole memory	0000h - 3FFFh plus Identification page

SRWD bit and $\overline{W}$ input signal

The status register write disable (SRWD) bit operates with the write protect pin ($\overline{W}$) signal. When the SRWD bit is written to 0, it is possible to write to the status register, regardless of whether the write protect pin ($\overline{W}$) is high or low.

When the SRWD bit is 1, two cases have to be considered, depending on the state of the $\overline{W}$ input pin:

- Case 1: if pin $\overline{W}$ is driven high, it is possible to write the status register.
- Case 2: if pin $\overline{W}$ is driven low, it is not possible to write the status register (WRSR is discarded), and therefore SRWD, BP1, BP0 bits cannot be changed (the size of the protected memory block defined by BP1 and BP0 bits is frozen).

Case 2 can be entered in either sequence:

- Writing SRWD bit to 1 after driving pin $\overline{W}$ low

or

- Driving pin $\overline{W}$ low after writing SRWD bit to 1.

The only way to exit case 2 is to pull pin $\overline{W}$ high.

Note: If the pin $\overline{W}$ is permanently tied high, the status register cannot be write-protected.

The protection features of the device are summarized in Table 3

Table 3. **Protection modes**

SRWD bit	$\overline{W}$ signal	Status
0	X	Status register is writable
1	1	
1	0	Status register is write-protected

3.5 Identification page

The M95128-A125 and M95128-A145 offer an identification page (64 bytes) in addition to the 128-Kbit memory. The identification page contains two fields:

- Device identification: the first three bytes are programmed by STMicroelectronics with the device identification code, as shown in Table 4.
- Application parameters: the byte after the device identification code is available for application-specific data.

Note: If the end application does not need to read the device identification code, this field can be overwritten and used to store application-specific data. Once these data are written, the whole identification page should be permanently locked in read-only mode.

The READ, WRITE, LID instructions are detailed in Section 4: Instructions.

Table 4. Device identification bytes

Address in identification page	Content	Value
00h	ST manufacturer code	20h
01h	SPI family code	00h
02h	Memory density code	0Eh (128-Kbit)

4 Instructions

Each command is composed of bytes (the most significant bit, *MSB*, is transmitted first), initiated with the instruction byte, as summarized in Table 5.

If an invalid instruction is sent (one not contained in Table 5), the device automatically enters a wait state until deselected.

Table 5. Instruction set

Instruction	Description	Instruction format
WREN	Write enable	0000 0110
WRDI	Write disable	0000 0100
RDSR	Read status register	0000 0101
WRSR	Write status register	0000 0001
READ	Read from memory array	0000 0011
WRITE	Write to memory array	0000 0010
RDID	Read identification page	1000 0011
WRID	Write identification page	1000 0010
RDLS	Reads the identification page lock status	1000 0011
LID	Locks the identification page in read-only mode	1000 0010

For read and write commands to memory array and identification page, the address is defined by two bytes as explained in Table 6.

Table 6. Significant bits within the two address bytes

Instruction	Most significant byte (*MSB*)[1]								Less significant byte (*LSB*)[1]							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
READ or WRITE	x	x	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RDID or WRID	0	0	0	0	0	0	0	0	0	0	A5	A4	A3	A2	A1	A0
RDLS or LID	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

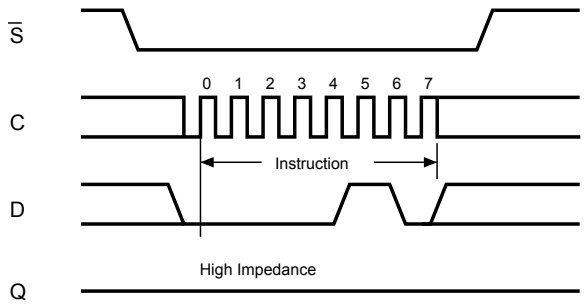
1. *A: Significant address bit.*

4.1 Write enable (WREN)

The WREN instruction must be decoded by the device before a write instruction (WRITE, WRSR, WRID or LID).

As shown in Figure 6, to send this instruction to the device, chip select ($\overline{S}$) is driven low, the bits of the instruction byte are shifted in (MSB first) on serial data input (D) after what the chip select ($\overline{S}$) input is driven high and the WEL bit is set (status register bit).

Figure 6. Write enable (WREN) sequence



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4.2 Write disable (WRDI)

One way of resetting the WEL bit (in the status register) is to send a write disable instruction to the device.

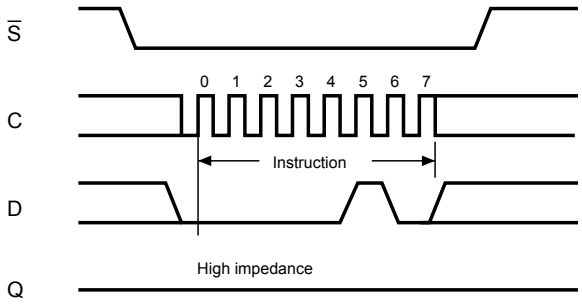
As shown in Figure 7, to send this instruction to the device, chip select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in (MSB first), on serial data input (D), after what the chip select ($\overline{S}$) input is driven high and the WEL bit is reset (status register bit).

If a write cycle is currently in progress, the WRDI instruction is decoded and executed and the WEL bit is reset to 0 with no effect on the ongoing write cycle.

In fact, the Write Enable Latch (WEL) bit is reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion

Figure 7. Write disable (WRDI) sequence



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4.3 Read status register (RDSR)

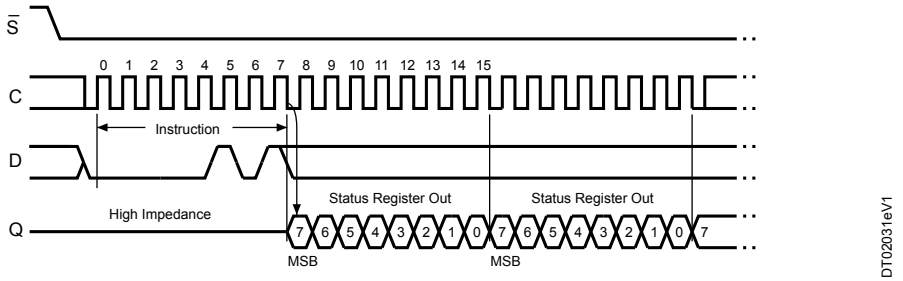
The read status register (RDSR) instruction is used to read the content of the status register.

As shown in Figure 8, to send this instruction to the device, chip select ($\overline{S}$) is first driven low. The bits of the instruction byte are shifted in (MSB first) on serial data input (D), the status register content is then shifted out (MSB first) on serial data output (Q).

If chip select ($\overline{S}$) continues to be driven low, the status register content is continuously shifted out.

The status register can always be read, even if a write cycle (t_W) is in progress. The status register functionality is detailed in Section 3.4.2: Status register and data protection.

Figure 8. Read status register (RDSR) sequence



4.4 Write status register (WRSR)

The write status register (WRSR) instruction allows new values to be written to the status register. Before it can be accepted, a write enable (WREN) instruction must previously have been executed.

The write status register (WRSR) instruction is entered (MSB first) by driving chip select ($\overline{S}$) low, sending the instruction code followed by the data byte on serial data input (D), and driving the chip select ($\overline{S}$) signal high.

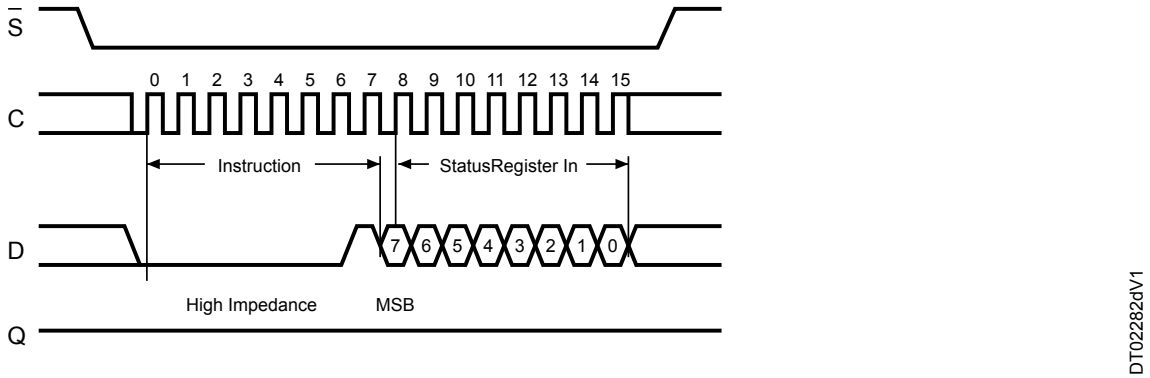
The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the write cycle (t_W).

The write status register (WRSR) instruction has no effect on bits b6, b5, b4, b1, and b0 bits in the status register (see Figure 5. Status register format).

The status register functionality is detailed in Section 3.4.2: Status register and data protection.

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 9. Write status register (WRSR) sequence



4.5 Read from memory array (READ)

The READ instruction is used to read the content of the memory.

As shown in Figure 10, to send this instruction to the device, chip select ($\overline{S}$) is first driven low.

The bits of the instruction byte and address bytes are shifted in (MSB first) on serial data input (D) and the addressed data byte is then shifted out (MSB first) on serial data output (Q). The first addressed byte can be any byte within any page.

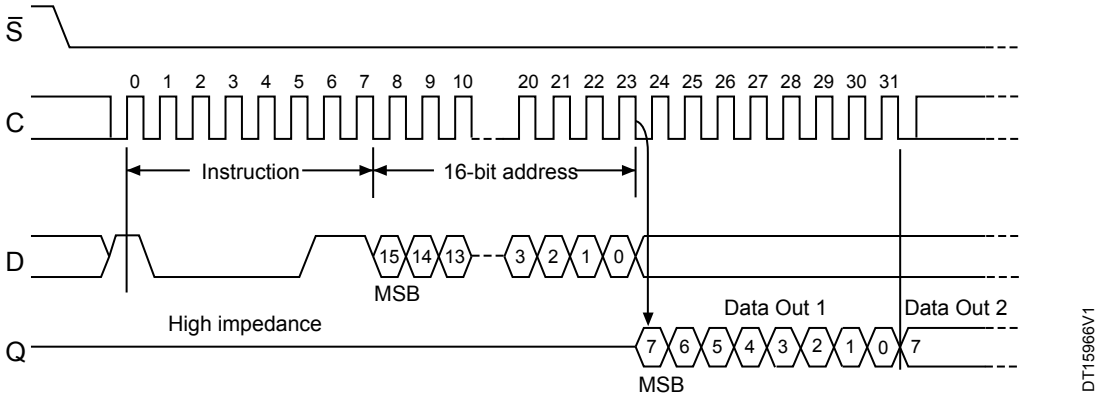
If chip select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented, and the next byte of data is shifted out. The whole memory can therefore be read with a single READ instruction.

When the highest address is reached, the address counter rolls over to zero, allowing the read cycle to continue indefinitely.

The read cycle is terminated by driving chip select ($\overline{S}$) high at any time when the data bits are shifted out on serial data output (Q).

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 10. Read from memory array (READ) sequence



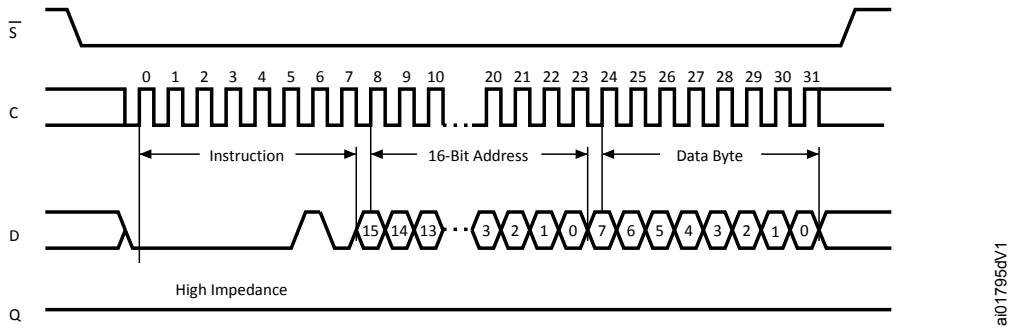
1. *Depending on the memory size, as shown in Table 6, the most significant address bits are don't care.*

4.6 Write to memory array (WRITE)

The WRITE instruction is used to write new data in the memory.

As shown in Figure 11, to send this instruction to the device, chip select ($\overline{S}$) is first driven low. The bits of the instruction byte, address bytes, and at least one data byte are then shifted in (MSB first), on serial data input (D). The instruction is terminated by driving chip select ($\overline{S}$) high at a data byte boundary. Figure 11 shows a single byte write.

Figure 11. Byte write (WRITE)



Note: 1. Depending on the memory size, as shown in Table 6, the most significant address bits are Don't Care.

A page write is used to write several bytes inside a page, with a single internal write cycle.

For a page write, chip select ($\overline{S}$) has to remain low, as shown in Figure 12, so that the next data byte are shifted in. Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the address counter exceeds the page boundary (the page size is 64 bytes), the internal address pointer rolls over to the beginning of the same page where the next data bytes are written. If more than 64 bytes are received, only the last 64 bytes are written.

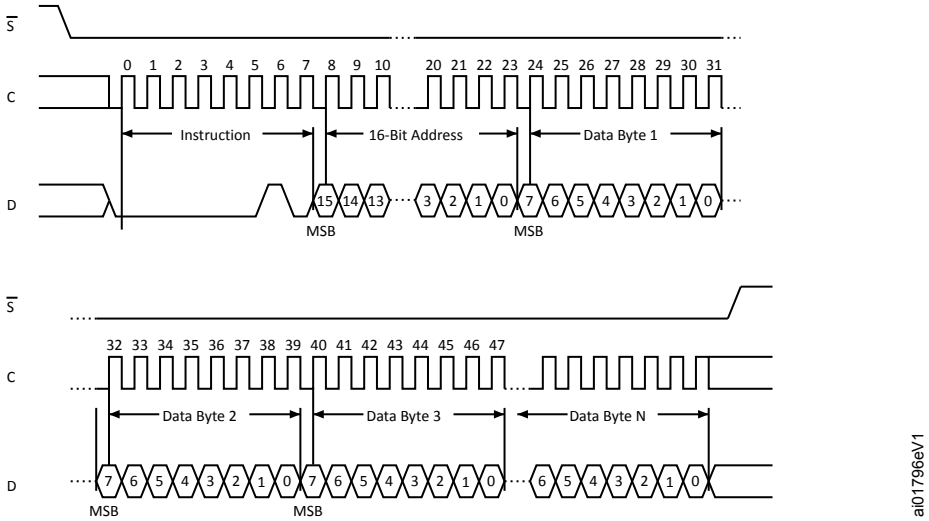
For both byte write and page write, the self-timed write cycle starts from the rising edge of chip select ($\overline{S}$), and continues for a period t_W (as specified in Table 14).

The instruction is discarded, and is not executed, under the following conditions:

- If a write cycle is already in progress
- If the addressed page is in the region protected by the block protect (BP1 and BP0) bits
- If one of the conditions defined in Section 3.4.1: Protocol control is not satisfied

Note: The self-timed write cycle (t_W) is internally executed as a sequence of two consecutive events: [erase addressed byte(s)], followed by [program addressed byte(s)]. An erased bit is read as 0 and a programmed bit is read as 1.

Figure 12. **Page write (WRITE) sequence**



Note: *1. Depending on the memory size, as shown in Table 6, the most significant address bits are Don't Care.*

4.7 Read identification page (RDID)

The read identification page instruction is used to read the identification page (additional page of 64 byte which can be written and later permanently locked in Read-only mode).

The chip select ($\overline{S}$) signal is first driven low. The bits of the instruction byte and address byte are then shifted in (MSB first) on serial data input (D). Address bit A10 must be 0 and the other upper address bits are *don't care* (it might be easier to define these bits as 0, as shown in Table 6). The data byte pointed to by the lower address bits [A5:A0] is shifted out (MSB first) on serial data output (Q).

The first byte addressed can be any byte within the identification page.

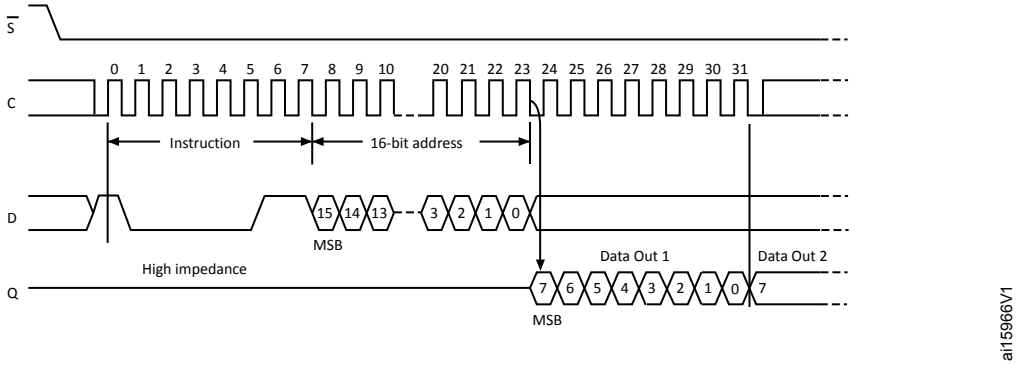
If chip select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented and the byte of data at the new address is shifted out.

Note: *There is no roll-over feature in the identification page. The address of the byte to read must not exceed the page boundary.*

The read cycle is terminated by driving chip select ($\overline{S}$) high. The rising edge of the chip select ($\overline{S}$) signal can occur at any time when the data bits are shifted out.

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 13. **Read identification page sequence**



The first three bytes of the identification page offer information about the device itself. Refer to Section 3.5: Identification page for more information.

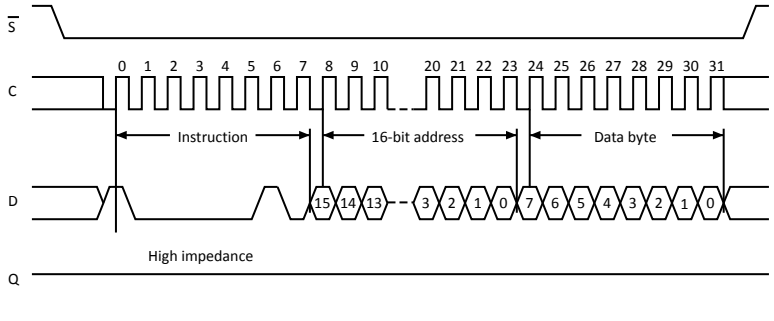
4.8 Write identification page (WRID)

The write identification page instruction is used to write the identification page (additional page of 64 bytes which can also be permanently locked in read-only mode).

The chip select ($\overline{S}$) signal is first driven low, and then the bits of the instruction byte, address byte, and at least one data byte are shifted in (MSB first) on serial data input (D). The address bit A10 must be 0 and the other upper address bits are *don't care* (it might be easier to define these bits as 0, as shown in Table 6. Significant bits within the two address bytes). The lower address bits [A5:A0] define the byte address inside the identification page.

The self-timed write cycle starts from the rising edge of chip select ($\overline{S}$), and continues for a period t_W (as specified in Table 14).

Figure 14. Write identification page sequence



Note: The first three bytes of the identification page offer the device identification code (refer to Section 3.5: Identification page for more information). Using the WRID command on the first three bytes overwrites the device identification code.

The instruction is discarded, and is not executed, under the following conditions:

- If a write cycle is already in progress
- If the block protect bits (BP1,BP0) = (1,1)
- If one of the conditions defined in Section 3.4.1: Protocol control is not satisfied.

4.9 Read lock status (RDLS)

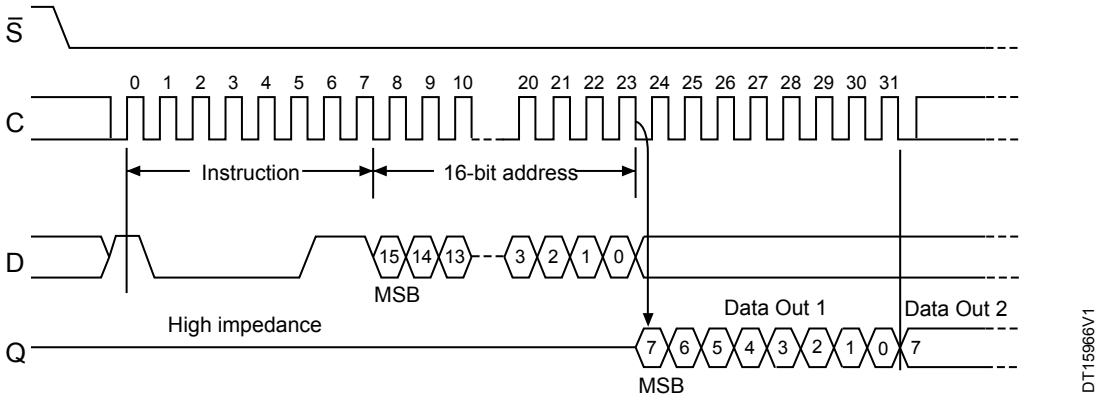
The read lock status instruction is used to read the lock status.

To send this instruction to the device, chip select ($\overline{S}$) first has to be driven low. The bits of the instruction byte and address byte are then shifted in (MSB first) on serial data input (D). Address bit A10 must be 1; all other address bits are *don't care* (it might be easier to define these bits as 0, as shown in Table 6). The lock bit is the LSB (least significant bit) of the byte read on serial data output (Q). It is at '1' when the lock is active and at '0' when the lock is not active. If chip select ($\overline{S}$) continues to be driven low, the same data byte is shifted out.

The read cycle is terminated by driving chip select ($\overline{S}$) high. The instruction sequence is shown in Figure 15.

The read lock status instruction is not accepted and not executed if a write cycle is currently in progress.

Figure 15. Read lock status sequence

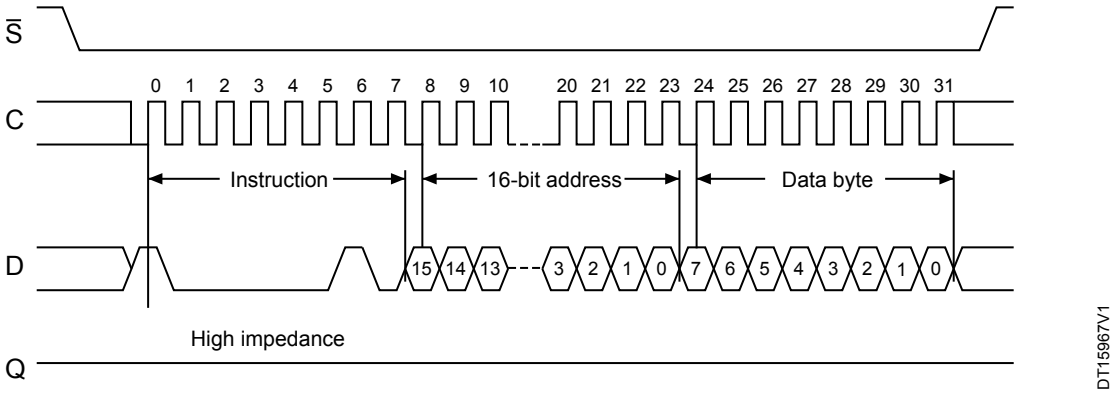


4.10 Lock identification page (LID)

The lock identification (LID) command is used to permanently lock the identification page in read-only mode.

The LID instruction is issued by driving chip select ($\overline{S}$) low , sending (MSB first) the instruction code, the address and a data byte on serial data input (D), and driving chip select ($\overline{S}$) high. In the address sent, A10 must be equal to 1. All other address bits are *don't care* (it might be easier to define these bits as 0, as shown in Table 6). The data byte sent must be equal to the binary value xxxx xx1x, where x = *don't care*. The LID instruction is terminated by driving chip select ($\overline{S}$) high at a data byte boundary, otherwise, the instruction is not executed.

Figure 16. Lock ID sequence



Driving chip select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed write cycle which duration is t_W (specified in Table 14). The instruction sequence is shown in Figure 16.

The instruction is discarded, and is not executed, under the following conditions:

- If a write cycle is already in progress
- If the block protect bits (BP1, BP0) = (1,1)
- If one of the conditions defined in Section 3.4.1: Protocol control is not satisfied.

5 Application design recommendations

5.1 Supply voltage (V_{CC})

5.1.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [$V_{CC(min)}$, $V_{CC(max)}$] range must be applied (see Table 9, and Table 10).

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

5.1.2 Power-up conditions

When the power supply is turned on, V_{CC} continuously rises from V_{SS} to V_{CC}. During this time, the chip select ($\overline{S}$) line is not allowed to float but must follow the V_{CC} voltage. The chip select ($\overline{S}$) line must be connected to V_{CC} via a suitable pull-up resistor (see Figure 17).

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in Table 12, and Table 13.

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} reaches the internal threshold voltage (this threshold is defined in Table 12, and Table 13 as V_{RES}).

When V_{CC} passes over the POR threshold, the device is reset and in the following state:

- Standby power mode
- Deselected
- Status register values:
  - Write enable latch (WEL) bit is reset to 0.
  - Write in progress (WIP) bit is reset to 0.
  - SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits).
- Not in the hold condition

As soon as the V_{CC} has reached a stable value within the [V_{CC}(min), V_{CC}(max)] range, the device is ready to operate.

5.1.3 Power-down

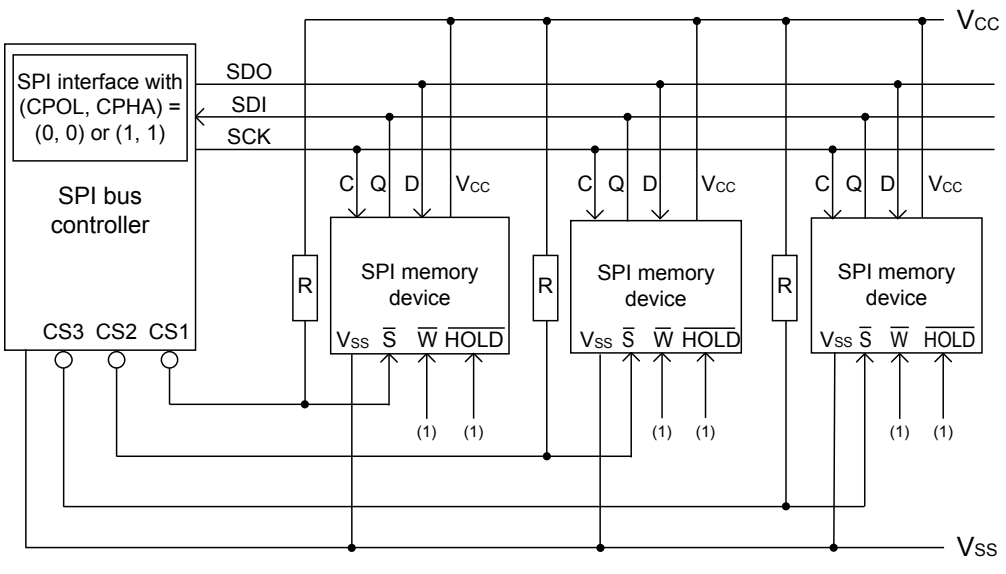
During power-down (continuous decrease in V_{CC} supply voltage below the minimum V_{CC} operating voltage defined in Table 12, and Table 13), the device must be:

- Deselected (chip select ($\overline{S}$) should be allowed to follow the voltage applied on V_{CC})
- Standby power mode (there should not be any internal write cycle in progress).

5.2 Implementing devices on SPI bus

Figure 17 shows an example of three devices, connected to the *SPI* bus controller. Only one device is selected at a time, so that only the selected device drives the serial data output (Q) line. All the other devices outputs are then in high impedance.

Figure 17. Bus controller and memory devices on the SPI bus



1. *The write protect ($\overline{W}$) and hold ($\overline{HOLD}$) signals must be driven high or low as appropriate.*

A pull-up resistor connected on each chip select ($\overline{S}$) input (represented in Figure 17) ensures that each device is not selected if the bus controller leaves the chip select ($\overline{S}$) line in the high impedance state.

5.3 Cycling with error correction code (*ECC* x 4)

The error correction code (*ECC*) is an internal logic function which is transparent for the *SPI* communication protocol.

The *ECC* logic is implemented on each group of four bytes. This byte is located at:

$$[4N, 4N + 1, \quad 4N + 2, \quad 4N + 3]$$

Where N is an integer.

Within a group, if a single bit happens to be erroneous during a read operation, the *ECC* detects and replaces it with the correct value. The read reliability is therefore much improved.

Even if the *ECC* function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the *ECC* function also writes/cycles the three other bytes located in the same group. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the four bytes of the group: the sum of the cycles seen by byte 0, byte 1, byte 2, and byte 3 of the same group must remain below the maximum value defined in Table 8.

Example 1 : Maximum cycling limit reached with one million cycles per byte

Each byte of a group can be equally cycled one million times (at 25 °C), so that the group cycling budget is four million cycles.

Example 2 : Maximum cycling limit reached with unequal byte cycling

Within a group, byte 0 can be cycled two million times, byte 1 can be cycled one million times, byte 2 and byte 3 can be cycled 500.000 times, making a total cycling budget of four million cycles for the group.

6 Delivery state

The device is delivered with:

- The memory array set to all 1s (each byte = FFh)
- The status register: bit SRWD =0, BP1 =0 and BP0 =0
- The identification page: the first three bytes define the device identification code (value defined in Table 4). The content of the following bytes is *don't care*.

7 Absolute maximum ratings

Stressing the device outside the ratings listed in Table 7 can permanently damage it. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	-65	150	°C
T_{AMB}	Ambient operating temperature	-40	150	
T_{LEAD}	Lead temperature during soldering	See note (1)		
V_O	Output voltage on Q pin	-0.50	V_{CC} + 0.6	V
V_I	Input voltage	-0.50	6.5	
I_{OL}	*DC* output current (Q = 0)	-	5	mA
I_{OH}	*DC* output current (Q = 1)	-	5	
V_{CC}	Supply voltage	-0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(2)	-	4000	V

1. *Compliant with JEDEC standard J-STD-020 (for small-body, Sn-Pb or Pb-free assembly), the ST ECOPACK 7191395 specification, and the European directive on restrictions on hazardous substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses are applied to pin pairs in accordance with AEC-Q100-002, compliant with ANSI/ESDA/JEDEC JS-001-2012, C1 = 100 pF, R1 = 1500 Ω , R2 = 500 Ω).*

8 DC and AC parameters

This section summarizes the operating conditions and the DC and AC characteristics of the device.

Table 8. Cycling performance by groups of 4 bytes

Symbol	Parameter	Test condition	Min.	Max.	Units
Ncycle	Write cycle endurance(1)	$T_A \le 25$ °C, 1.7 V < V_{CC} < 5.5 V	-	4,000,000	Write cycle(2)
		T_A = 85 °C, 1.7 V < V_{CC} < 5.5 V	-	1,200,000	
		T_A = 125 °C, 1.7 V < V_{CC} < 5.5 V	-	600,000	
		T_A = 145 °C(3), 2.5 V < V_{CC} < 5.5 V	-	400,000	

1. *The write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer, or for the status register byte (refer to Section 5.3: Cycling with error correction code (ECC x 4)). The write cycle endurance is defined by characterization and qualification.*
2. *A write cycle is executed when either a page write, a byte write, a WRSR, a WRID or an LID instruction is decoded.*

   When using the byte write, the page write or the WRID, refer also to Section 5.3: Cycling with error correction code (ECC x 4).
3. *For temperature range 4 only.*

Table 9. Operating conditions (voltage range W, temperature range 4)

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Supply voltage	-	2.5	5.5	V
T_A	Ambient operating temperature	-	–40	145	°C
f_C	Operating clock frequency	5.5 V ≥ V_{CC} ≥ 2.5 V capacitive load on Q pin ≤ 100pF	-	10	MHz

Table 10. Operating conditions (voltage range R, temperature range 3)

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Supply voltage	-	1.7	5.5	V
T_A	Ambient operating temperature	-	–40	125	°C
f_C	Operating clock frequency	V_{CC} ≥ 2.5 V, capacitive load on Q pin ≤ 100pF	-	10	MHz
		V_{CC} ≥ 1.7 V, capacitive load on Q pin ≤ 100pF	-	5	

Table 11. Operating conditions (voltage range R, temperature range 3) for high-speed communications

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Supply voltage	-	4.5	5.5	V
T_A	Ambient operating temperature	-	–40	85	°C
f_C	Operating clock frequency	V_{CC} ≥ 4.5 V, capacitive load on Q pin ≤ 60 pF	-	20	MHz

Table 12. DC characteristics (voltage range W, temperature range 4)

Symbol	Parameter	Specific test conditions (in addition to conditions specified in Table 9)	Min.	Max.	Units
C_{OUT}(1)	Output capacitance (Q)	V_{OUT} = 0 V	-	8	pF
C_{IN}(1)	Input capacitance	V_{IN} = 0 V	-	6	
I_{LI}	Input leakage current	V_{IN} = V_{SS} or V_{CC}	-	2	µA
I_{LO}	Output leakage current	$\overline{S}$ = V_{CC}, V_{OUT} = V_{SS} or V_{CC}	-	3	
I_{CC}	Supply current (Read)	V_{CC} = 2.5 V, f_C = 10 MHz, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	2	mA
		V_{CC} = 5.5 V, f_C = 10 MHz, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	4	
I_{CC0}(2)	Supply current (Write)	2.5 V < V_{CC} < 5.5 V, during t_W, $\overline{S}$ = V_{CC}	-	2(1)	
I_{CC1}(2)	Supply current (Standby power mode)	t° = 85 °C, V_{CC} = 2.5 V, $\overline{S}$ = V_{CC} V_{IN} = V_{SS} or V_{CC}	-	2	µA
		t° = 85 °C, V_{CC} = 5.5 V, $\overline{S}$ = V_{CC} V_{IN} = V_{SS} or V_{CC}	-	3	
		t° = 125 °C, V_{CC} = 2.5 V, $\overline{S}$ = V_{CC} V_{IN} = V_{SS} or V_{CC}	-	15	
		t° = 125 °C, V_{CC} = 5.5 V, $\overline{S}$ = V_{CC} V_{IN} = V_{SS} or V_{CC}	-	20	
		t° = 145 °C, V_{CC} = 2.5 V, $\overline{S}$ = V_{CC} V_{IN} = V_{SS} or V_{CC}	-	25	
		t° = 145 °C, V_{CC} = 5.5 V, $\overline{S}$ = V_{CC} V_{IN} = V_{SS} or V_{CC}	-	40	
V_{IL}	Input low voltage	-	– 0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage	-	0.7 V_{CC}	V_{CC}+1	
V_{OL}	Output low voltage	I_{OL} = 2 mA	-	0.4	
V_{OH}	Output high voltage	I_{OH} = –2 mA	0.8 V_{CC}	-	
V_{RES}(1)	Internal reset threshold voltage	-	0.5	1.5	

1. *Evaluated by characterization, not tested in production.*
2. *Averaged value during the write cycle (t_W)*

Table 13. DC characteristics (voltage range R, temperature range 3)

Symbol	Parameter	Test conditions (in addition to conditions specified in Table 10)	Min.	Max.	Units
C_{OUT}(1)	Output capacitance (Q)	V_{OUT} = 0 V	-	8	pF
C_{IN}(1)	Input capacitance	V_{IN} = 0 V	-	6	pF
I_{LI}	Input leakage current	V_{IN} = V_{SS} or V_{CC}	-	2	µA
I_{LO}	Output leakage current	$\overline{S}$ = V_{CC}, V_{OUT} = V_{SS} or V_{CC}	-	3	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.7 V, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open, f_C = 5 MHz	-	2	mA
		V_{CC} = 2.5 V, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open, f_C = 10 MHz	-	2	mA
		V_{CC} = 5.5 V, f_C = 20 MHz(2) C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	5	mA
I_{CC0}(3)	Supply current (Write)	1.7 V ≤ V_{CC} < 5.5 V during t_W, $\overline{S}$ = V_{CC}	-	2(1)	mA
I_{CC1}	Supply current (Standby mode)	t° = 85 °C, V_{CC} = 1.7 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	1	µA
		t° = 85 °C, V_{CC} = 2.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	2	µA
		t° = 85 °C, V_{CC} = 5.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	3	µA
		t° = 125 °C, V_{CC} = 1.7 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	15	µA
		t° = 125 °C, V_{CC} = 2.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	15	µA
		t° = 125 °C, V_{CC} = 5.5 V, $\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	20	µA
V_{IL}	Input low voltage	1.7 V ≤ V_{CC} < 2.5 V	-0.45	0.25 V_{CC}	V
		2.5 V ≤ V_{CC} < 5.5 V	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage	1.7 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+ 1	V
		2.5 V ≤ V_{CC} < 5.5 V	0.7 V_{CC}	V_{CC}+ 1	V
V_{OL}	Output low voltage	V_{CC} = 1.7 V, I_{OL} = 1 mA	-	0.3	V
		V_{CC} ≥ 2.5 V, I_{OL} = 2 mA	-	0.4	V
V_{OH}	Output high voltage	V_{CC} = 1.7 V, I_{OH} = 1 mA	0.8 V_{CC}	-	V
		V_{CC} ≥ 2.5 V, I_{OH} = -2 mA	0.8 V_{CC}	-	V
V_{RES}(1)	Internal reset threshold voltage	-	0.5	1.5	V

1. *Evaluated by characterization, not tested in production.*
2. *When –40 °C < t° < 85 °C*
3. *Average value during the Write cycle (t_W)*

Table 14. AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
			Test conditions specified in Table 10		Test conditions specified in Table 9 and Table 10		Test conditions specified in Table 11		
f_C	f_{SCK}	Clock frequency	-	5	-	10	-	20	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	60	-	30	-	15	-	ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	60	-	30	-	15	-	
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	90	-	40	-	20	-	
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	60	-	30	-	15	-	
t_{CHSL}	-	$\overline{S}$ not active hold time	60	-	30	-	15	-	
t_{CH}(1)	t_{CLH}	Clock high time	80	-	40	-	20	-	
t_{CL}(1)	t_{CLL}	Clock low time	80	-	40	-	20	-	
t_{CLCH}(2)	t_{RC}	Clock rise time	-	2	-	2	-	2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time	-	2	-	2	-	2	
t_{DVCH}	t_{DSU}	Data in setup time	20	-	10	-	5	-	ns
t_{CHDX}	t_{DH}	Data in hold time	20	-	10	-	10	-	
t_{HHCH}	-	Clock low hold time after $\overline{HOLD}$ not active	60	-	30	-	15	-	
t_{HLCH}	-	Clock low hold time after $\overline{HOLD}$ active	60	-`	30	-	15	-	
t_{CLHL}	-	Clock low set-up time before $\overline{HOLD}$ active	0	-	0	-	0	-	
t_{CLHH}	-	Clock low set-up time before $\overline{HOLD}$ not active	0	-	0	-	0	-	
t_{SHQZ}(2)	t_{DIS}	Output disable time	-	80	-	40	-	20	
t_{CLQV}(3)	t_V	Clock low to output valid	-	80	-	40	-	20	
t_{CLQX}	t_{HO}	Output hold time	0	-	0	-	0	-	
t_{QLQH}(2)	t_{RO}	Output rise time	-	20	-	20	-	20	
t_{QHQL}(2)	t_{FO}	Output fall time	-	20	-	20	-	20	
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid	-	80	-	40	-	20	
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z	-	80	-	40	-	20	
t_W	t_{WC}	Write time	-	4	-	4	-	4	ms

1. *t_{CH} + t_{CL} must never be lower than the shortest possible clock period, $1/f_C$(max).*
2. *Evaluated by characterization, not tested in production.*
3. *t_{CLQV} must be compatible with t_{CL} (clock low time): if t_{SU} is the Read setup time of the SPI bus controller, t_{CL} must be equal to (or greater than) t_{CLQV}+t_{SU}.*

Figure 18. **AC measurement I/O waveform**

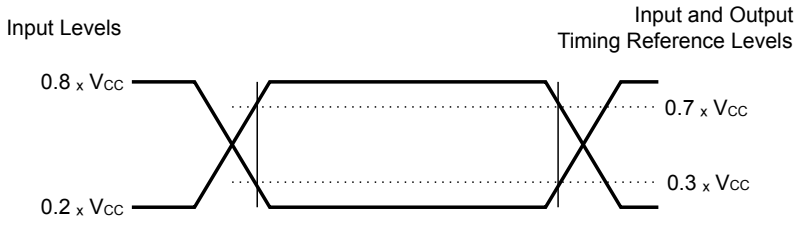


Figure 19. **Serial input timing**

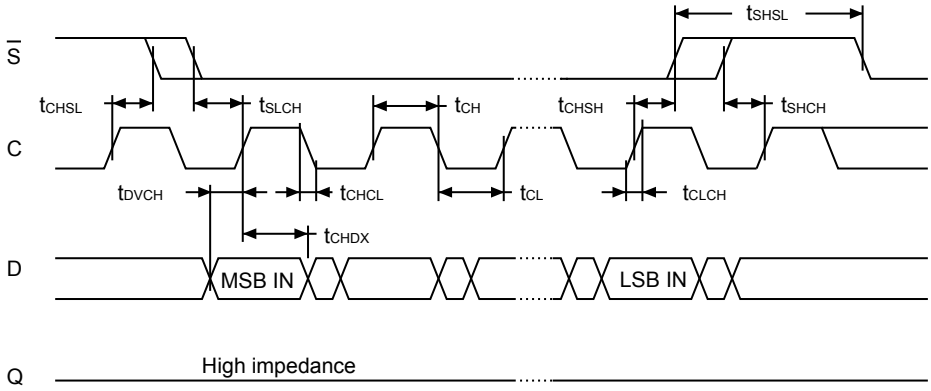


Figure 20. **Hold timing**

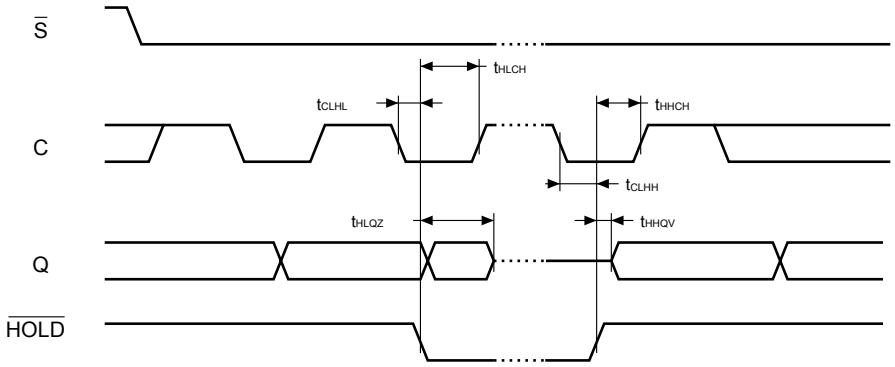
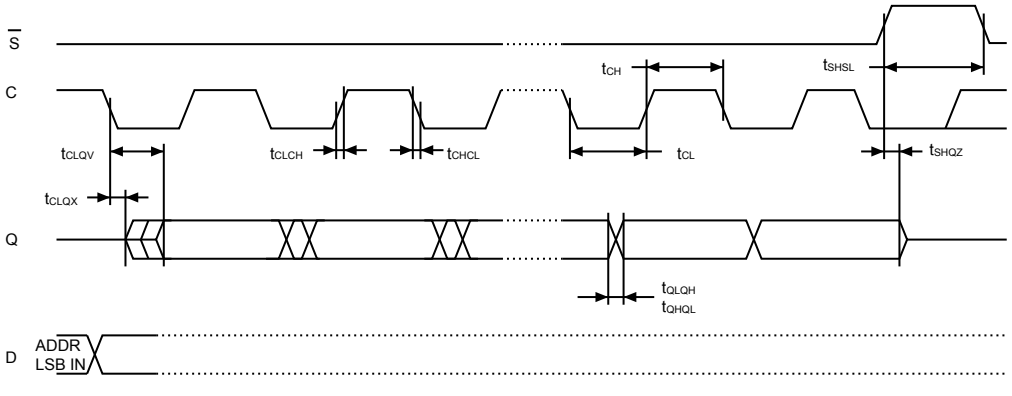


Figure 21. **Serial output timing**



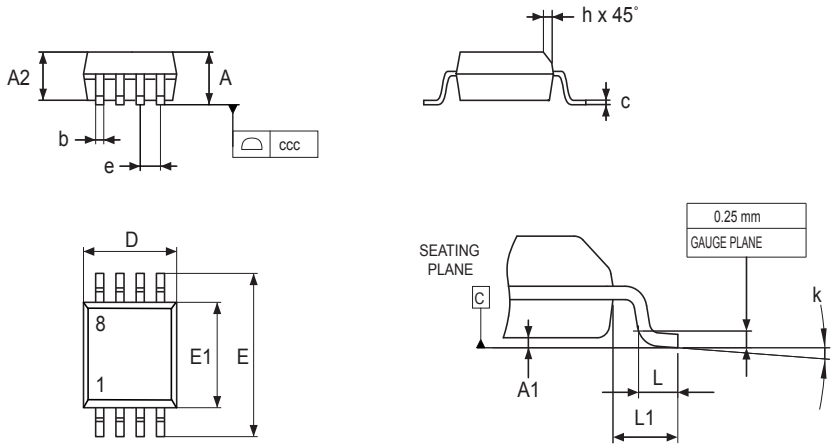
9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 SO8N package information

This SO8N is an 8-lead, 4.9 x 6 mm, plastic small outline, 150 mil body width package.

Figure 22. SO8N - Outline



1. *Drawing is not to scale.*

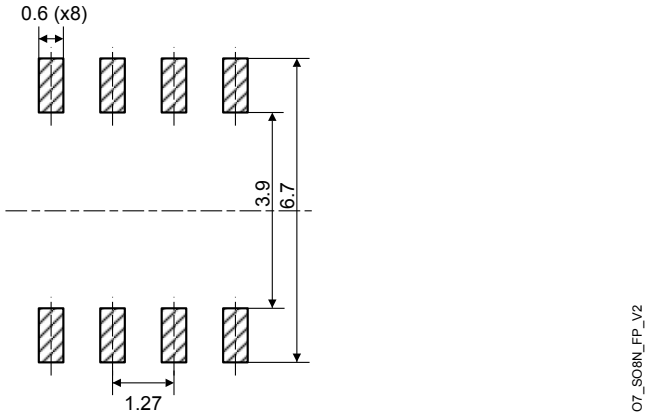
Table 15. SO8N - Mechanical data

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.170	-	0.230	0.0067	-	0.0091
D[2]	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1[3]	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side*
3. *Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Note: The package top may be smaller than the package bottom. Dimensions D and E1 are determinated at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interleads flash, but including any mismatch between the top and bottom of the plastic body. The measurement side for mold flash, protusions, or gate burrs is the bottom side.

Figure 23. SO8N - Footprint example

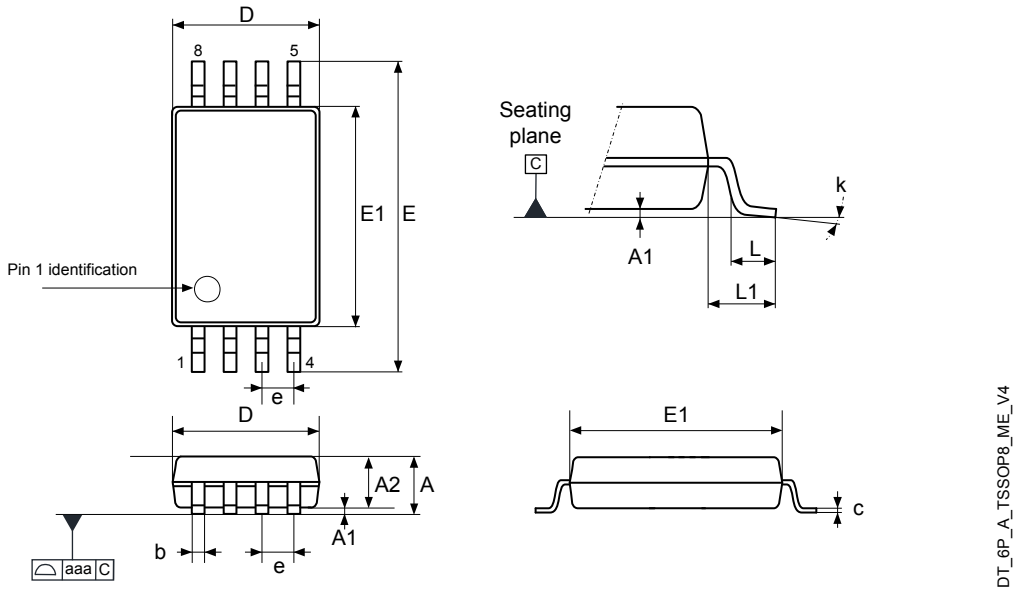


1. *Dimensions are expressed in millimeters.*

9.2 TSSOP8 package information

This TSSOP is an 8-lead, 3 x 6.4 mm, 0.65 mm pitch, thin shrink small outline package.

Figure 24. TSSOP8 – Outline



1. *Drawing is not to scale.*

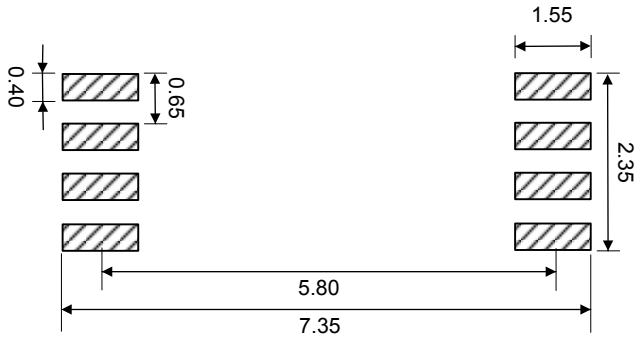
Table 16. TSSOP8 - Mechanical data

Symbol	millimeters			inches (1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D(2)	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1(3)	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.*
3. *Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Note: The package top may be smaller than the package bottom. Dimensions D and E1 are determinated at the outermost extremes of the plastic body exclusive of the mold flash, tie bar burrs, gate burrs, and interleads flash, but including any mismatch between the top and bottom of the plastic body. The measurement side for the mold flash, protrusions, or gate burrs is the bottom side.

Figure 25. TSSOP8 – Footprint example

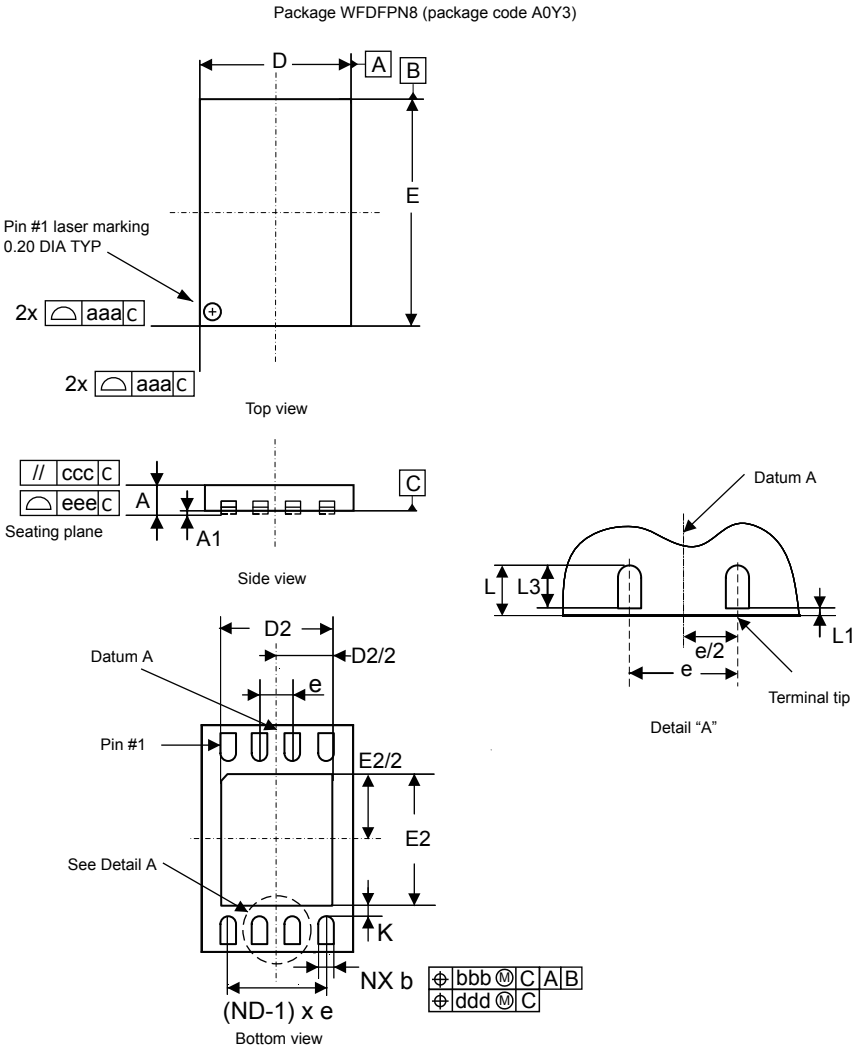


1. *Dimensions are expressed in millimeters.*

9.3 WFDFPN8 (DFN8) package information

This WFDFPN is an 8-lead, 2 x 3 mm, 0.5 mm pitch very thin fine pitch dual flat package.

Figure 26. WFDFPN8 (DFN8) – Outline



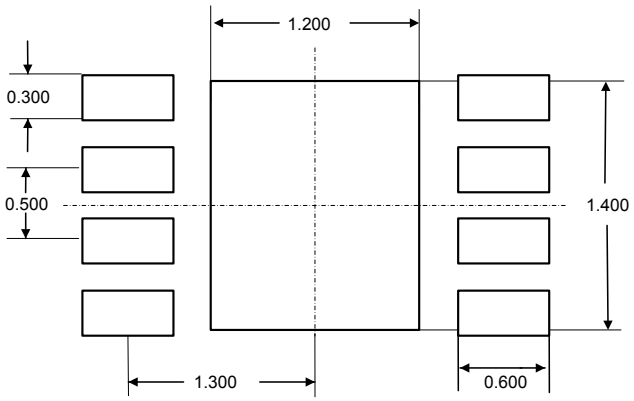
1. *Drawing is not to scale.*
2. *Exposed copper is not systematic and can appear partially or totally according to the cross section.*
3. *The central pad (the area E2 by D2 in the above illustration) must be either connected to Vss or left floating (not connected) in the end application.*

Table 17. WFDFPN8 (DFN8) – Mechanical data

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.700	0.750	0.800	0.0276	0.0295	0.0315
A1	0.025	0.045	0.065	0.0010	0.0018	0.0026
b[2]	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	1.900	2.000	2.100	0.0748	0.0787	0.0827
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.500	-	-	0.0197	-
L1	-	-	0.150	-	-	0.0059
L3	0.300	-	-	0.0118	-	-
D2	1.400	-	1.600	0.0551	-	0.0630
E2	1.200	-	1.400	0.0472	-	0.0551
K	0.400	-	-	0.0157	-	-
L	0.300	-	0.500	0.0118	-	0.0197
NX [3]	8					
ND [3]	4					
aaa	-	-	0.150	-	-	0.0059
bbb[4]	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee [5]	-	-	0.080	-	-	0.0031

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension b applies to the plated terminal and is measured between 0.15 and 0.30 mm from the terminal tip.*
3. *N is the number of terminals. ND is the number of terminals on the “D” sides.*
4. *The max package warpage is 0.05 mm.*
5. *Applied for exposed die paddle and terminals. Exclude embedding part of the exposed die paddle from measuring.*

Figure 27. WFDFPN8 (DFN8) – Footprint example



10 Ordering information

Table 18. Ordering information scheme

Example: M95 128-D W DW 4 T P /K

Device type

M95 = SPI serial access EEPROM

Device function

128-D = 128 Kbit (16 Kbyte) with additional identification page

Operating voltage

W = V_{CC} = 2.5 to 5.5 V

R = V_{CC} = 1.7 to 5.5 V

Package(1)

MN = SO8 (150 mils width)

DW = TSSOP8 (169 mil width)

MF = WFDFPN8 (DFN8 2 x 3 mm)

Device grade

3 = -40 to 125 °C. Automotive grade

4 = -40 to 145 °C. Automotive grade

Option

Blank = Tube packing

T = Tape and reel packing

Plating technology

P or G = ECOPACK2®

Process

/K = Manufacturing technology code

1. *All packages are ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimony-oxide flame retardants).*

Note: For a list of available options (speed, package, etc.) or for further information on any aspect of this device, contact your nearest ST sales office.

Engineering samples

Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 19. **Document revision history**

Date	Revision	Changes
17-Apr-2012	1	Initial release.
04-Oct-2012	2	Deleted line “128 = 128 Kbit (16 Kbytes x 8)” in section “Device function” of Table 19: Ordering information scheme.
30-Jan-2013	3	Changed datasheet status from “Preliminary data” to “Production data”. Updated VRES maximum value in Table 13: DC characteristics (voltage range W, temperature range 4) and Table 14: DC characteristics (voltage range R, temperature range 3). Rephrased introduction of Section 3.5: Identification page and information about Identification page in Section 6: Delivery state. Deleted note(1) under Table 6: Instruction set.
04-Dec-2013	4	Updated note (1) under Table 8: Absolute maximum ratings. Replaced UFDFPN8 package (MC) by WFDFPN8 package (MF). Modified the Data retention from “40 years at 50 °C” to “50 years at 125 °C”
24-Oct-2014	5	Updated Note 2 below Table 8: Absolute maximum ratings Updated Table 14: DC characteristics (voltage range R, temperature range 3). Updated Table 18: WFPN8 (MLP8) – 8-lead, 2 x 3 mm, 0.5 mm pitch very very thin fine pitch dual flat package mechanical data Updated Table 19: Ordering information scheme. Added Note 2 below Figure 24: WFDFPN8 (MLP8) – 8-lead, 2 x 3 mm, 0.5 mm pitch very very thin fine pitch dual flat package outline.
15-Jan-2015	6	Updated Table 18: WFPN8 (MLP8) – 8-lead, 2 x 3 mm, 0.5 mm pitch very very thin fine pitch dual flat package mechanical data Updated Figure 24: WFDFPN8 (MLP8) – 8-lead, 2 x 3 mm, 0.5 mm pitch very very thin fine pitch dual flat package outline Added paragraph: Engineering samples on page 41
22-Jan-2016	7	Updated • Section 9: Package mechanical data • V_{CC} min value.
29-Jan-2016	8	Updated • Title of Figure 23: TSSOP8 – 8-lead thin shrink small outline, 3 x 4.4 mm, 0.65 mm pitch, package outline Title of Table 17: TSSOP8 – 8-lead thin shrink small outline, 3 x 4.4 mm, 0.65 mm pitch, package mechanical data
21-Oct-2025	9	Updated the document format and corrected the unnecessary capital letters throughout the document. Over and above the above change the following changes are made: Added: • Product summary and product label Updated: • Features • Cover image • Figure 1. Logic diagram • Section 3.2: SPI modes • Section 3.4.1: Protocol control • Section 3.4.2: Status register and data protection • Section 4.2: Write disable (WRDI) • Section 5.1.2: Power-up conditions

Date	Revision	Changes
		• Figure 17. Bus controller and memory devices on the SPI bus • Section 5.3: Cycling with error correction code (*ECC* x 4) • Section 7: Absolute maximum ratings • Table 8. Cycling performance by groups of 4 bytes • Table 14. AC characteristics • Table 12. DC characteristics (voltage range W, temperature range 4) • Table 13. DC characteristics (voltage range R, temperature range 3) • Table 14. AC characteristics • Table 15. SO8N - Mechanical data • Section 9.2: TSSOP8 package information • Section 9.3: WFDFPN8 (DFN8) package information • Section 10: Ordering information

Glossary

AC Alternating current

CPHA Clock phase bit. Selects the clock phase.

CPOL Clock polarity bit. Selects the clock polarity.

DC Direct current

ECC Error correction code

EEPROM Electrically erasable programmable read-only memory

ESD Electrostatic discharge

LSB Least significant byte

MSB Most significant byte

POR Power-on reset

SPI Serial peripheral interface

V_{IH} Input high voltage

V_{IL} Input low voltage

V_{OH} Output high voltage

V_{OL} Output low voltage

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