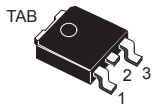
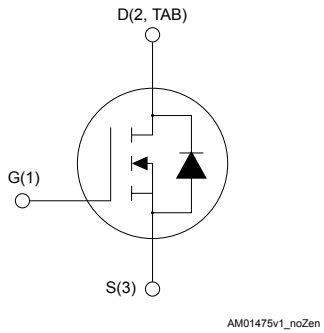
N-channel 650 V, 308 mΩ typ., 11 A MDmesh M5 Power MOSFET in a DPAK package



DPAK



Features

Order code	V_{DS} at T_J max.	$R_{DS(on)}$ max.	I_D
STD15N65M5	710 V	340 mΩ	11 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Product status link
STD15N65M5

Product summary	
Order code	STD15N65M5
Marking	15N65M5
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	11	A
	Drain current (continuous) at T_C = 100 °C	6.9	
I_{DM}(1)	Drain current (pulsed)	44	A
P_{TOT}	Total power dissipation at T_C = 25 °C	85	W
dv/dt(2)	Peak diode recovery voltage slope	10	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 11 A, di/dt ≤ 400 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.47	°C/W
R_{thJA}(1)	Thermal resistance, junction-to-ambient	50	°C/W

1. *When mounted on 1 inch^2 FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	2.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	160	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)			100	
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 5.5 A		308	340	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	816	-	pF
C_{oss}	Output capacitance		-	23	-	pF
C_{rss}	Reverse transfer capacitance		-	2.6	-	pF
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	70	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related		-	21	-	pF
R_g	Gate input resistance	f = 1 MHz, I_D=0 A	-	5	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 5.5 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	22	-	nC
Q_{gs}	Gate-source charge		-	5.5	-	nC
Q_{gd}	Gate-drain charge		-	11	-	nC

1. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 7 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	30	-	ns
$t_{r(v)}$	Voltage rise time		-	8	-	ns
$t_{c(off)}$	Crossing time		-	12.5	-	ns
$t_{f(i)}$	Current fall time		-	11	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
I_{SDM} (1)	Source-drain current (pulsed)		-		44	A
V_{SD} (2)	Forward on voltage	I_{SD} = 11 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs, V_{DD} = 100 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	247		ns
Q_{rr}	Reverse recovery charge		-	2.4		µC
I_{RRM}	Reverse recovery current		-	19.5		A
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs V_{DD} = 100 V, T_J = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	312		ns
Q_{rr}	Reverse recovery charge		-	3		µC
I_{RRM}	Reverse recovery current		-	19		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

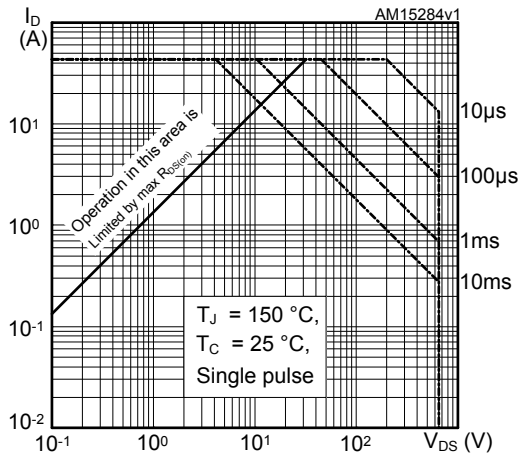


Figure 2. Thermal impedance

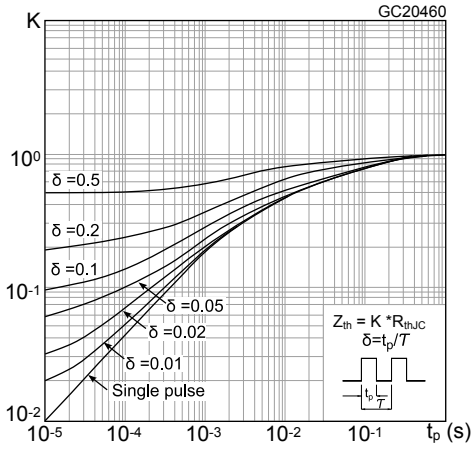


Figure 3. Output characterisics

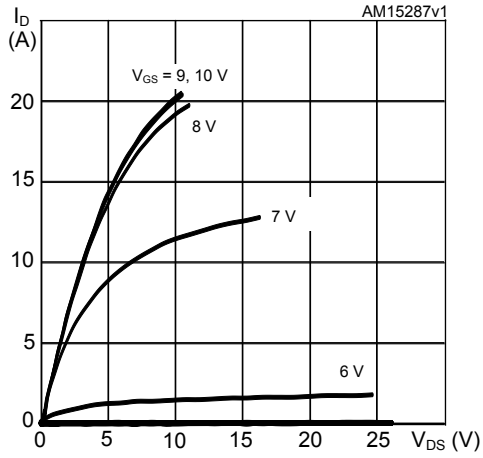


Figure 4. Transfer characteristics

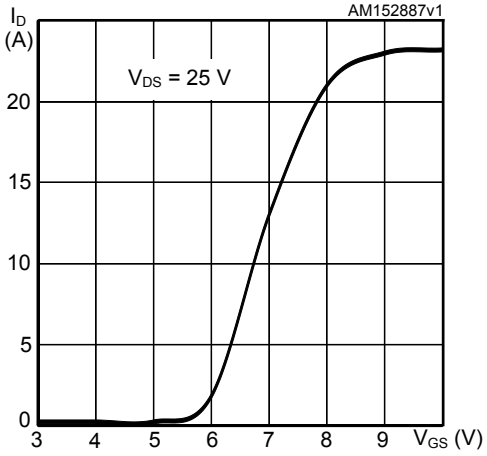


Figure 5. Gate charge vs gate-source voltage

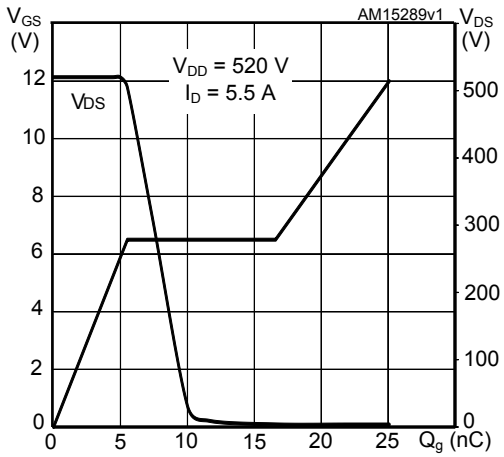


Figure 6. Static drain-source on resistance

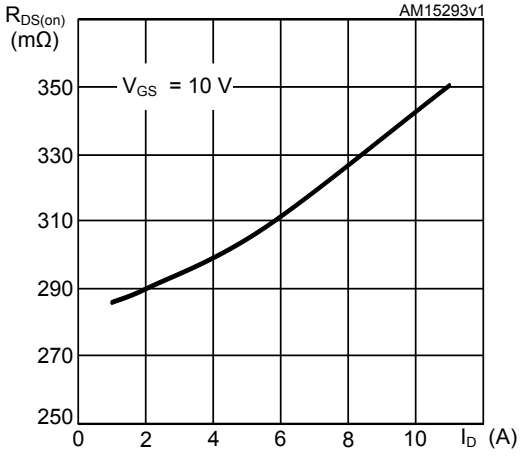


Figure 7. Output capacitance stored energy

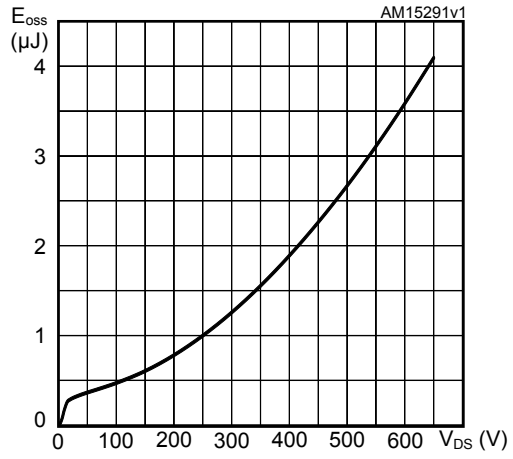


Figure 8. Capacitance variations

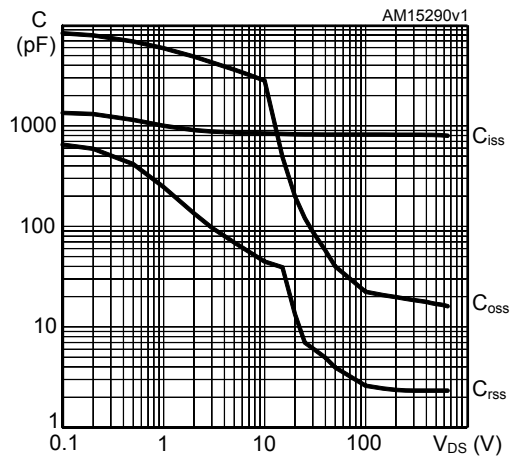


Figure 9. Normalized gate threshold voltage vs temperature

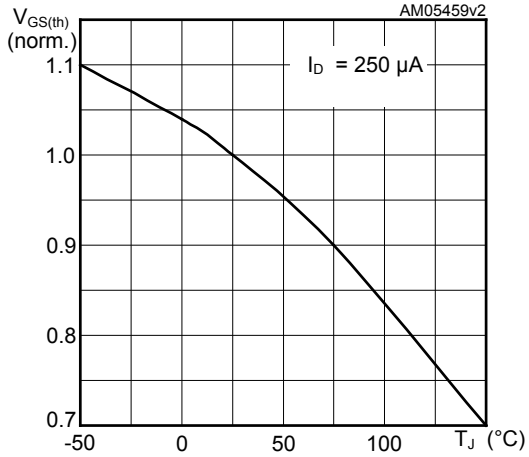


Figure 10. Normalized on-resistance vs temperature

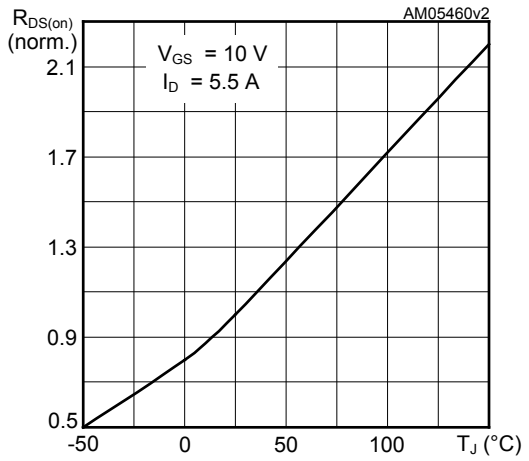


Figure 11. Source-drain diode forward characteristics

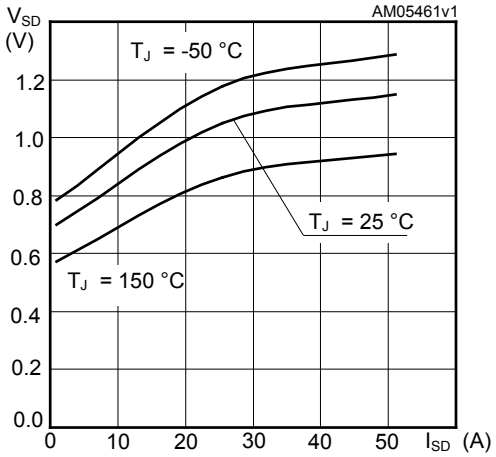


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature

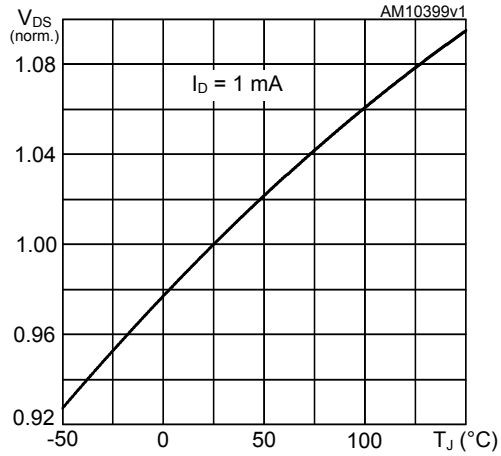
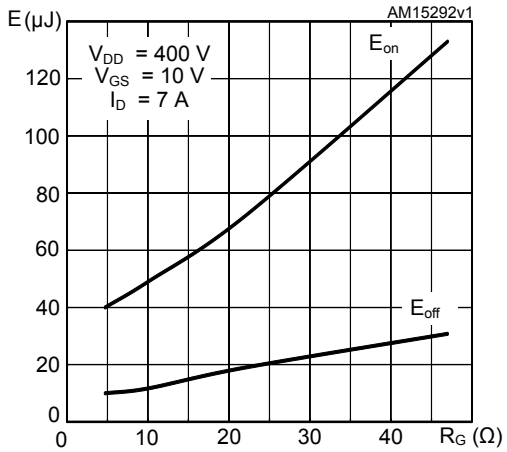
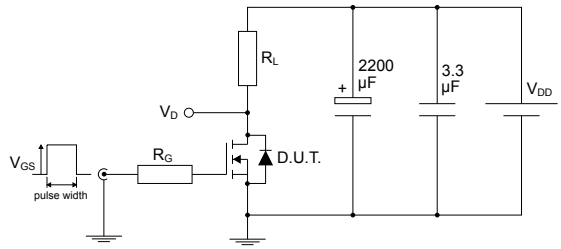


Figure 13. **Switching losses vs gate resistance**



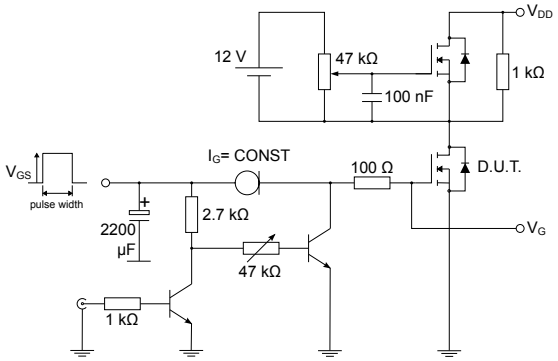
3 Test circuits

Figure 14. Test circuit for resistive load switching times



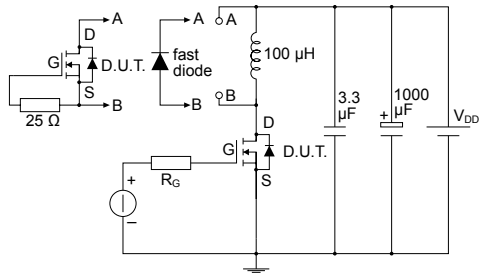
AM01468v1

Figure 15. Test circuit for gate charge behavior



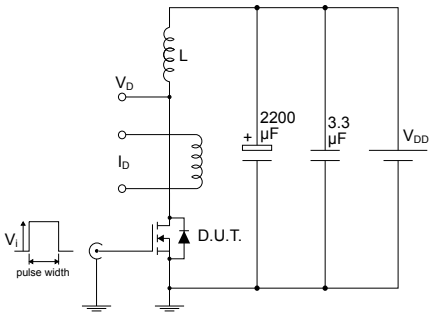
AM01469v1

Figure 16. Test circuit for inductive load switching and diode recovery times



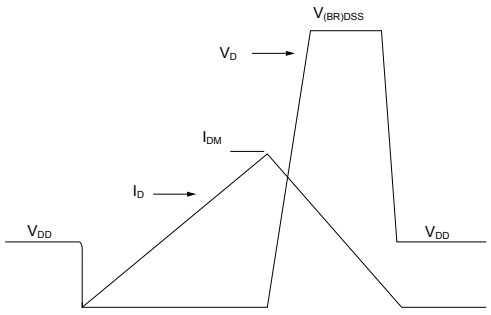
AM01470v1

Figure 17. Unclamped inductive load test circuit



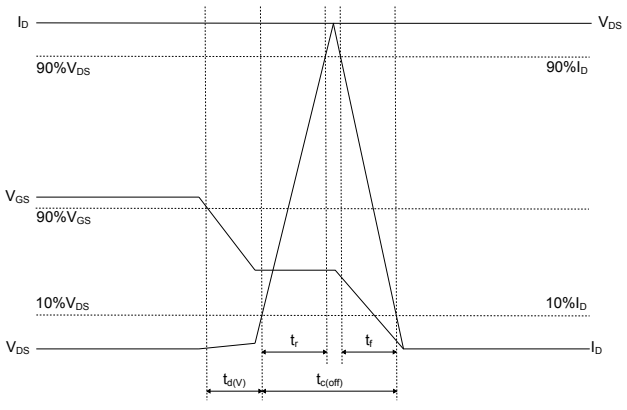
AM01471v1

Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



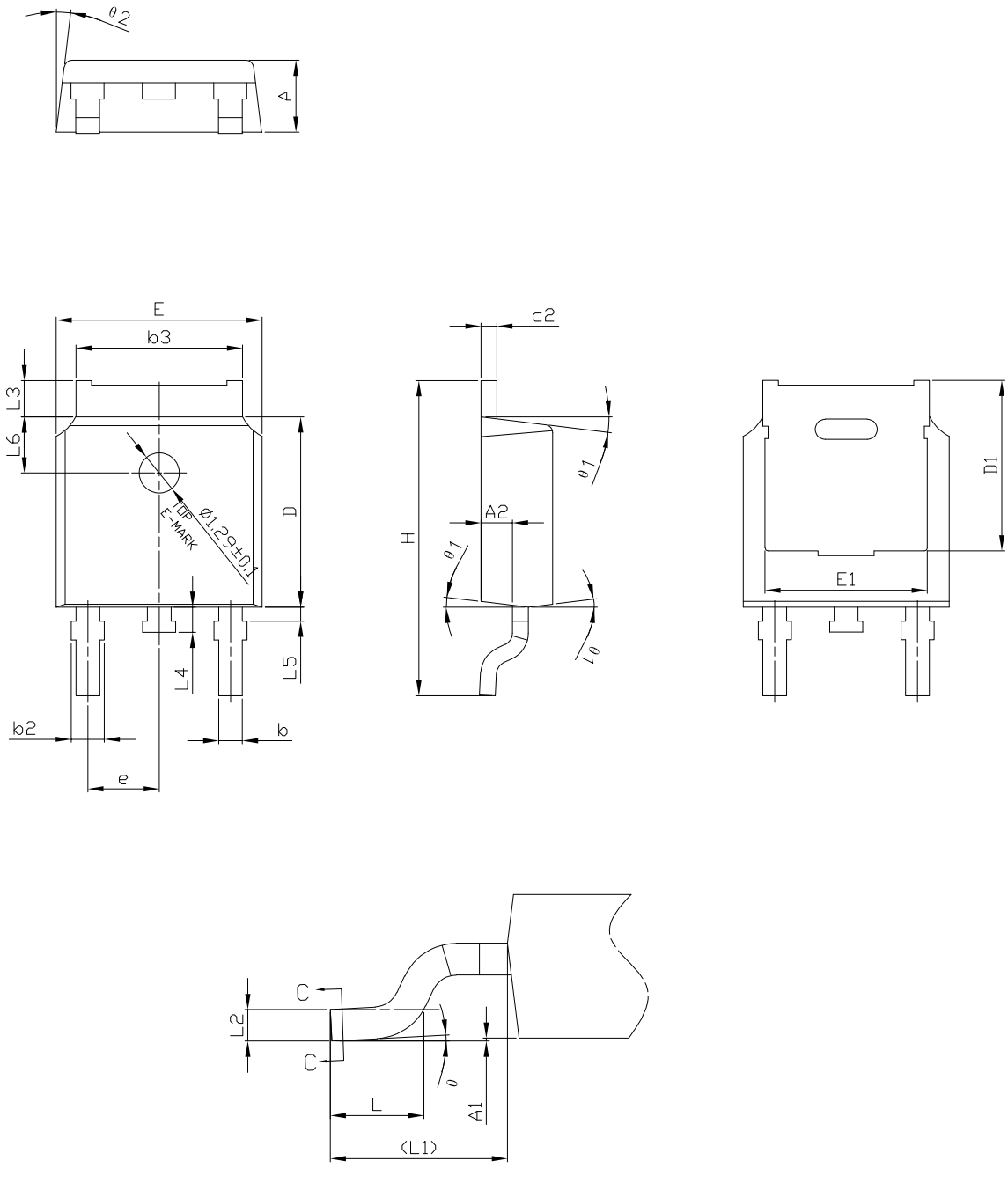
AM05540v2

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type C3 package information

Figure 20. DPAK (TO-252) type C3 package outline

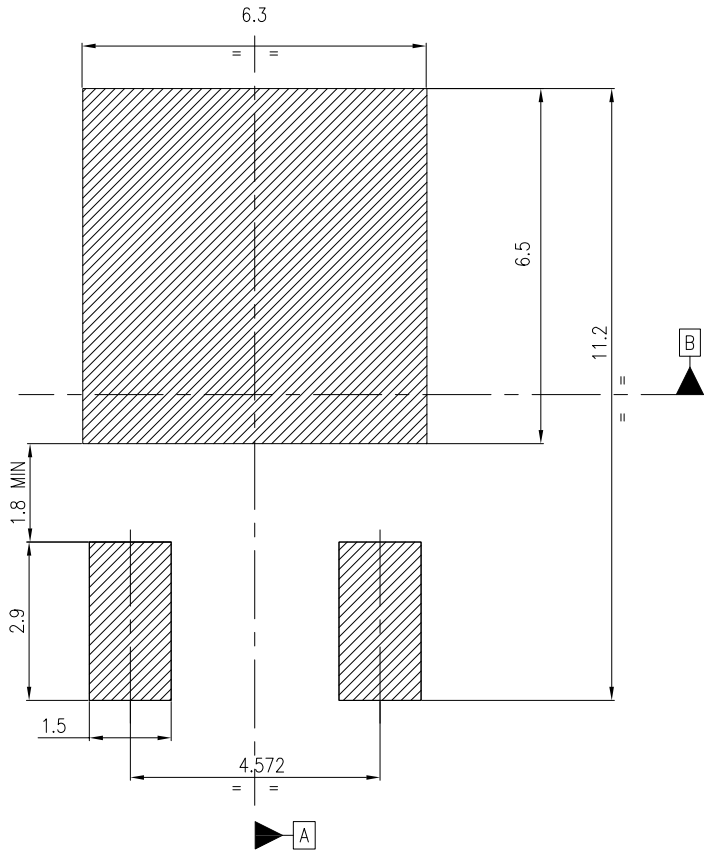


0068772_type-C3_rev34

Table 8. **DPAK (TO-252) type C3 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.10
A2	0.90	1.01	1.10
b	0.72		0.85
b2	0.72		1.10
b3	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.20	5.45	5.70
E	6.50	6.60	6.70
E1	5.00	5.20	5.40
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.51 BSC		
L3	0.90		1.25
L4	0.60	0.80	1.00
L5	0.15		0.75
L6	1.80 REF		
θ	0°		8°
θ1	5°	7°	9°
θ2	5°	7°	9°

Figure 21. DPAK (TO-252) recommended footprint (dimensions are in mm)



Notes:

1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664−1)

2) The device must be positioned within ⌖ 0.05 A B

FP_0068772_34

4.2 DPAK (TO-252) packing information

Figure 22. **DPAK (TO-252) tape outline**

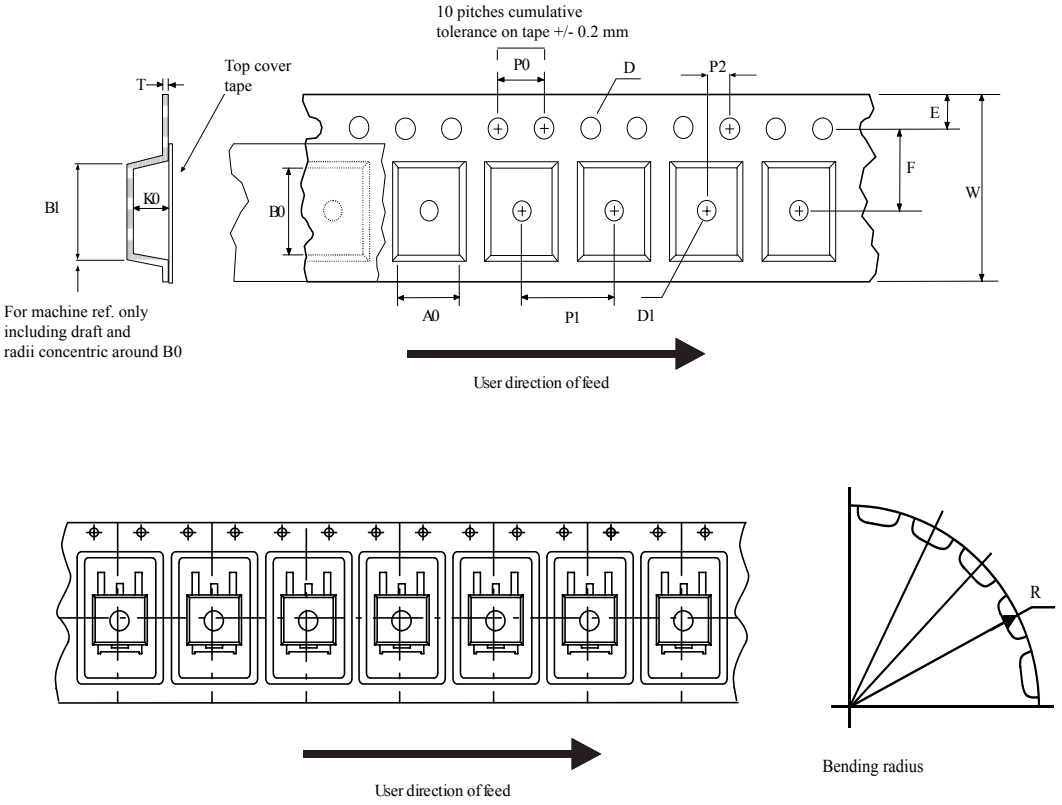
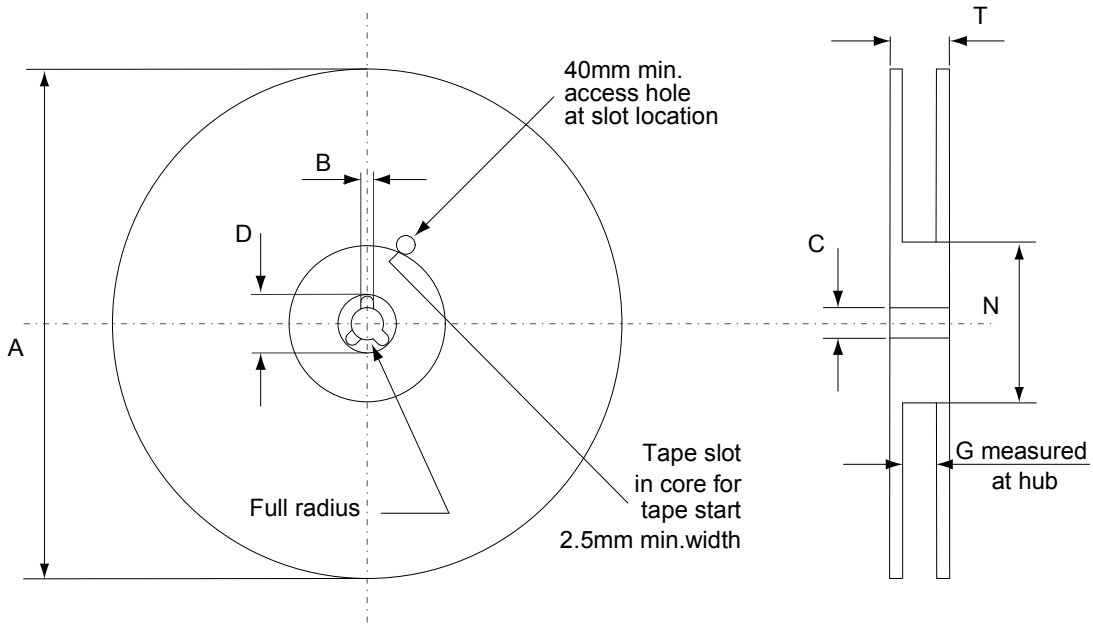


Figure 23. **DPAK (TO-252) reel outline**



AM06038v1

Table 9. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
09-Nov-2012	1	First release.
15-May-2018	2	Removed maturity status indication from cover page. The document status is production data. Updated *Section 1 Electrical ratings*, *Section 2 Electrical characteristics* and *Section 2.1 Electrical characteristics curves*. Minor text changes.
14-Jul-2023	3	The part number STB15N65M5 has been moved to a separate datasheet and the document has been updated accordingly. Removed "*Section 4.2 DPAK (TO-252) type A2 package information*" and replaced "*Section 4.3 DPAK (TO-252) type C2 package information*" with Section 4.1 DPAK (TO-252) type C3 package information. Minor text changes.

Contents

1 **Electrical ratings** 2
2 **Electrical characteristics** 3
2.1 Electrical characteristics (curves) 5
3 **Test circuits** 8
4 **Package information** 9
4.1 DPAK (TO-252) type C3 package information 9
4.2 DPAK (TO-252) packing information 12
Revision history 14

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved