M95M01-A125 M95M01-A145 M95M01-A150

Datasheet

Automotive 1-Mbit serial SPI bus EEPROM



SO8N

(150 mil width)



TSSOP8

(169 mil width)



WFDFPN8 (MF)

DFN8 - 2 x 3 mm

Product status
M95M01-A125
M95M01-A145
M95M01-A150

Product label



Features

Functional safety

- Follows ASIL-B ready requirement



Grade

- AEC-Q100 grade 0 conform qualification



SPI interface

- Compatible with the serial peripheral interface (*SPI*) bus

Memory

- 1-Mbit (128-Kbyte) *EEPROM*
- Page size: 256 bytes
- Additional 256-byte lockable identification page

Supply voltage

- 2.5 V to 5.5 V for CMOSF8H products
- 1.7 V to 5.5 V for CMOSF9V products

Temperature

- Operating temperature range:
  - -40°C up to +125°C for range 3
  - -40°C up to +145°C for range 4 for CMOSF8H
  - -40°C up to +150°C for range 4 for CMOSF9V

Clock frequency

- Up to 16 MHz

Fast write cycle time

- Byte and page write within 5 ms (typically 4 ms) for CMOSF8H products
- Byte and page write within 3.5 ms (typically 2.6 ms) for CMOSF9V products

Advanced features

- Schmitt trigger inputs for noise filtering
- Software write protection by quarter block
- Hardware write protection of the whole memory array
- Enhanced *ESD*/latch-up protection
- *ESD* human body model 4000 V

Write cycle performance

- For CMOSF8H products
  - More than 4 million write cycles at +25°C
  - More than 1.2 million write cycles at +85°C
  - More than 600 k write cycles at +125°C
  - More than 400 k write cycles at +145°C
- For CMOSF9V products
  - More than 4 million write cycles at +25°C
  - More than 1.2 million write cycles at +85°C
  - More than 600 k write cycles at +125°C
  - More than 400 k Write cycles at +150°C

Data retention performance

- 100 years at 25°C for CMOSF8H products
- 15 years at 45°C for CMOSF9V products

Ultra-low power current consumption (for CMOSF9V commercial products)

- 0.6 µA (typical) in standby mode
- 650 µA (typical) for read current
- 1 mA (typical) for write current

Packages

- SO8N, TSSOP8, and WFDFPN8 (ECOPACK2-compliant)

1 Description

The M95M01-A125, M95M01-A145 and M95M01-A150 are 1-Mbit serial electrically erasable programmable memory (EEPROM) automotive-grade devices. Those manufactured in CMOSF8H operate up to +145 °C, while those manufactured in CMOSF9V operate up to +150 °C. They are qualified with the high reliability automotive standard AEC-Q100 grade 0, and are accessed through a simple serial SPI-compatible interface running at up to 16 MHz. Moreover,the devices manufactured in CMOSF9V follow the ASIL-B ready requirement.

The devices are byte-alterable memories (131072 × 8 bits), organized as 512 pages of 256 bytes, in which the data integrity is significantly improved thanks to an embedded error correction code logic.

The M95M01-A125, M95M01-A145 and M95M01-A150 offer an additional identification page (256 bytes), where the ST device identification can be read. This page can also store sensitive application parameters, which can later be permanently locked in read-only mode.

Figure 1. Logic diagram

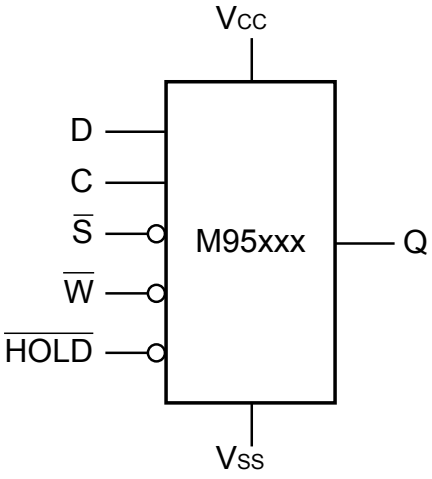
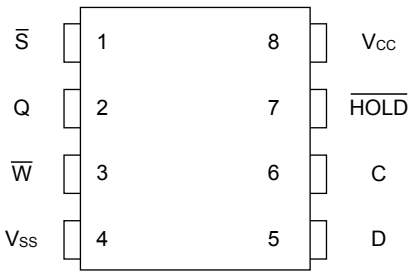


Figure 2. 8-pin package connections



1. *See Section 11: Package information for package dimensions and how to identify pin 1.*

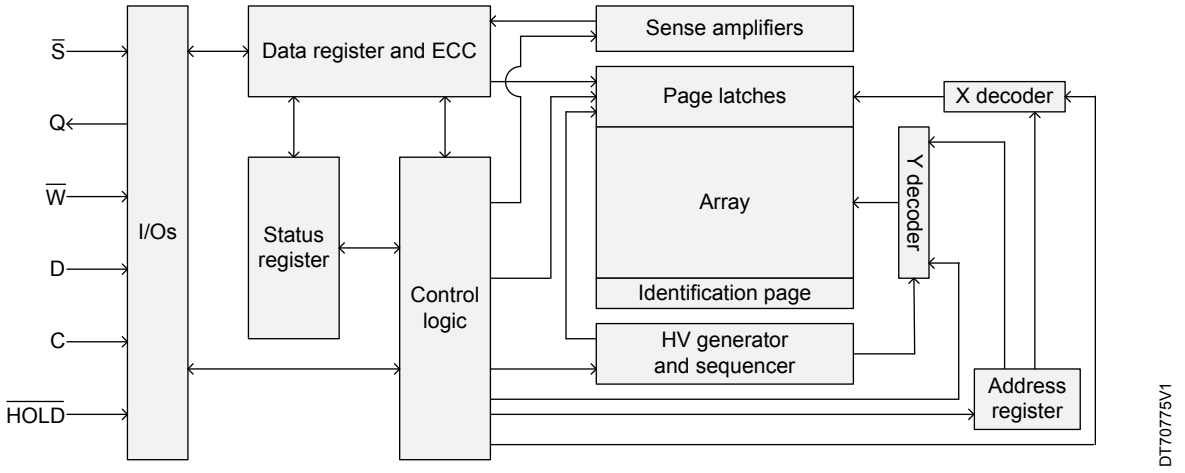
Table 1. Signal names

Signal name	Description	Direction
C	Serial clock	Input
D	Serial data input	Input
Q	Serial data output	Output
$\overline{S}$	Chip select	Input
$\overline{W}$	Write protect	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

2 Memory organization

The memory is organized as shown in the following figure.

Figure 3. Block diagram



3 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals must be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in Section 9: DC and AC parameters). These signals are described in the following subsections.

3.1 Serial data output (Q)

The serial data output (Q) signal is used to transfer data serially out of the device during a read operation. Data are shifted out on the falling edge of the serial clock (C), the most significant bit (*MSB*) first. In all other cases, the serial data output (Q) is in high impedance.

3.2 Serial data input (D)

The serial data input (D) signal is used to transfer data serially into the device. The serial data input (D) receives instructions, addresses, and the data to be written. Values are latched on the rising edge of the serial clock (C), the most significant bit (*MSB*) first.

3.3 Serial clock (C)

This input signal provides the timing for the serial interface. Instructions, addresses, or data present at serial data input (D) are latched on the rising edge of the serial clock (C). Data on serial data output (Q) change after the falling edge.

3.4 Chip select ($\overline{S}$)

When this input signal is high, the device is deselected and the serial data output (Q) is at high impedance. The device is in the standby power mode, unless an internal write cycle is in progress. Driving chip select ($\overline{S}$) low selects the device, placing it in the active power mode.

After power-up, a falling edge is required before the start of any instruction.

3.5 Hold ($\overline{HOLD}$)

The hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting it.

During the hold condition, the serial data output (Q) is high impedance, while the states of the serial data input (D) and serial clock (C) are *don't care*.

To start the hold condition, the device must be selected, with chip select ($\overline{S}$) driven low.

3.6 Write protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory protected against write instructions, as specified by the values of the BP1 and BP0 bits in the status register.

This pin must be driven either high or low and must remain stable during all write instructions.

3.7 V_{SS} ground

V_{SS} is the reference for all signals, including V_{CC}.

3.8 V_{CC} supply voltage

V_{CC} is the supply voltage.

Refer to Section 4.1: Active power and standby power modes and to Section 6.1: Supply voltage (V_{CC}).

4 Operating features

4.1 Active power and standby power modes

When chip select ($\overline{S}$) is low, the device is selected and in the active power mode. When it is high, the device is deselected. If a write cycle is not in progress, the device goes in standby power mode, and its consumption drops to I_{CC1}, as specified in Table 14, Table 15, Table 16, and Table 17.

4.2 SPI modes

The device can be driven by a microcontroller with its *SPI* peripheral running in one of the two following modes:

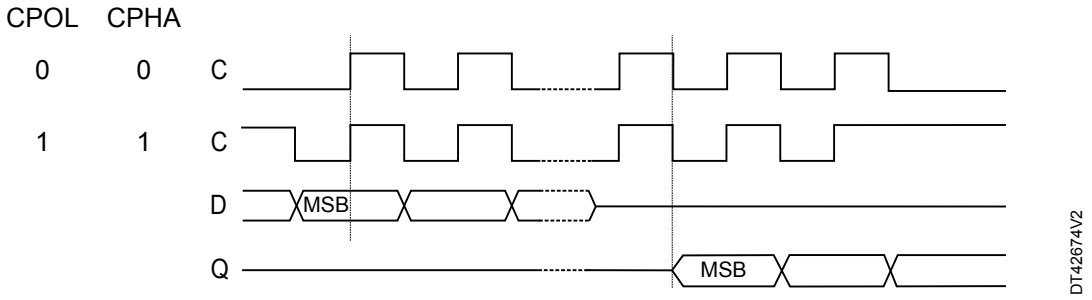
- *CPOL* = 0, *CPHA* = 0
- *CPOL* = 1, *CPHA* = 1

For these two modes, the input data are latched on the rising edge of the serial clock, and the output data are available from the falling edge of the serial clock (C).

The difference between the two modes, as shown in Figure 4, is the clock polarity when the bus controller is in standby mode and not transferring data:

- Serial clock (C) remains at 0 for (*CPOL* = 0, *CPHA* = 0)
- Serial clock (C) remains at 1 for (*CPOL* = 1, *CPHA* = 1)

Figure 4. Supported *SPI* modes



4.3 Hold condition

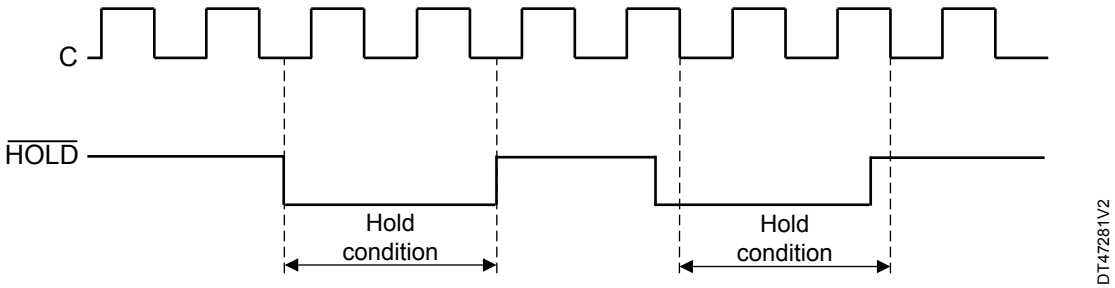
The hold (HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence.

To enter the hold condition, the device must be selected with the chip select (S) low. During this condition, the serial data output (Q) is in high impedance, while the serial data input (D) and the serial clock (C) are *don't care*.

Typically, the device remains selected for the entire duration of the hold condition. Deselecting the device while it is in the hold condition resets the state of the device. This mechanism can be used, if required, to reset the ongoing processes. It resets the internal logic, except the WEL and WIP bits of the status register.

Note: When the device receives a write command (instruction + address + 8-bit data bytes), deselecting it triggers the write cycle of this decoded command.

Figure 5. Hold condition activation



The hold condition starts when the hold (HOLD) signal is driven low while the serial clock (C) is already low (as shown in Figure 5).

Figure 5 also shows what happens if the rising and falling edges do not align with the Serial clock (C) being low.

4.4 Protocol control and data protection

4.4.1 Protocol control

The chip select (S) input offers a built-in safety feature, as it is edge as well as level-sensitive. After power-up, the device is not selected until a falling edge has first been detected. This ensures that the chip select (S) must have been high prior to going low, to start the first operation.

To ensure that the write commands (WRITE, WRSR, WRID, LID) are accepted and executed correctly, the following conditions must be met:

- A write enable (WREN) instruction sets the write enable latch (WEL) bit.
- During the entire command, a falling edge followed by a low state on chip select must be decoded.
- The instruction, address, and input data must be sent as multiples of eight bits.
- The command must include at least one data byte.
- The chip select must be driven high exactly after a data byte boundary.

WRITE commands can be discarded at any time by a rising edge on chip select (S) outside of a byte boundary.

To execute read commands (READ, RDSR, RDID, RDLS), the device must decode:

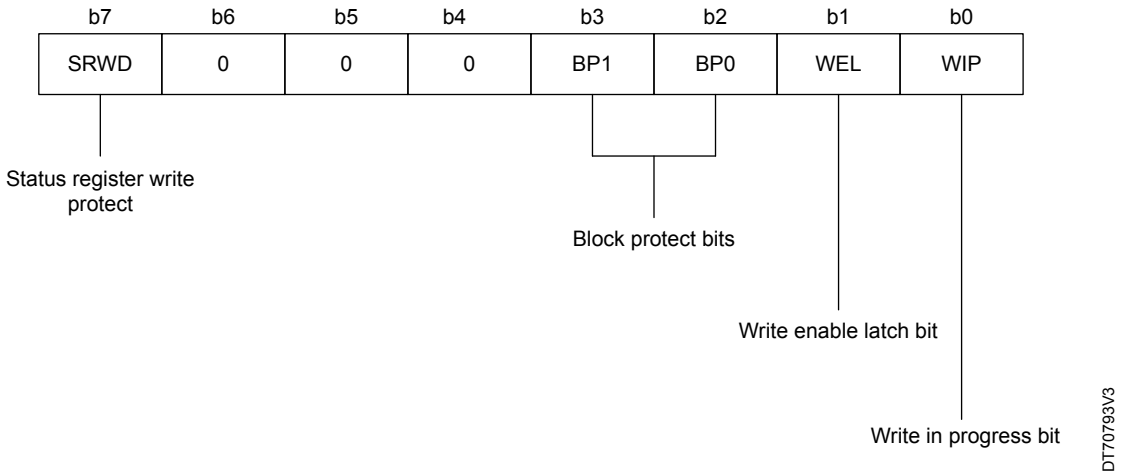
- A falling edge and a low level on chip select during the entire command
- The instruction and address as multiples of eight bits (one byte)

From this step, data bits are shifted out until the rising edge on chip select (S).

4.4.2 Status register and data protection

The status register format is shown in Figure 6.

Figure 6. Status register format



Note: The bits b6 to b4 are always read as 0.

WIP bit

The write in progress (WIP) bit is a read-only flag that indicates the ready/busy state of the device. When a write command (WRITE, WRSR, WRID, LID) is decoded and a write cycle (t_W) is in progress, the device is busy, and the WIP bit is set to 1. When WIP = 0, the device is ready to decode a new command.

During a write cycle, continuously reading the WIP bit detects when the device becomes ready (WIP = 0) to decode a new command.

Note: For CMOSF8H products and during a write lock ID operation, the device is busy, but the WIP bit remains set to 0.

WEL bit

The write enable latch (WEL) bit is a flag that indicates the status of the internal write enable latch.

When WEL is:

- 1: the write instructions (WRITE, WRSR, WRID, and LID) are executed
- 0: any decoded write instruction is not executed

The WEL bit is set to 1 with the WREN instruction, and reset (WEL=0) after the following events:

- Completion of the write disable (WRDI) instruction
- Completion of write instructions (WRITE, WRSR, WRID, and LID), including the write cycle time t_W
- Power-up

BP1 and BP0 bits

The block protect bits (BP1, BP0) are nonvolatile. BP1 and BP0 define the size of the memory block to protect against write instructions, as defined in Table 2. These bits are written using the write status register (WRSR) instruction, provided that the status register is not protected (refer to SRWD bit and $\overline{W}$ input signal).

Table 2. Write-protected block size

Status register bits		Protected block	Protected array addresses
BP1	BP0		
0	0	None	None
0	1	Upper quarter	18000h - 1FFFFh
1	0	Upper half	10000h - 1FFFFh
1	1	Whole memory	00000h - 1FFFFh, and the identification page

SRWD bit and $\overline{W}$ input signal

The status register write disable (SRWD) bit operates in conjunction with the write protect ($\overline{W}$) signal. When the SRWD bit is 0, it is possible to write to the status register, regardless of whether the write protect ($\overline{W}$) signal is high or low.

When the SRWD bit is 1, consider the following two cases, depending on the state of the $\overline{W}$ input pin:

- Case 1: if the write protect ($\overline{W}$) signal is driven high, it is possible to write the status register.
- Case 2: if the write protect ($\overline{W}$) signal is driven low, it is not possible to write the status register (WRSR is discarded), and therefore SRWD, BP1, BP0 bits cannot be changed (the size of the protected memory block defined by BP1 and BP0 bits is frozen).

Case 2 can be entered in using one of the following sequences:

- Writing SRWD bit to 1 after driving the $\overline{W}$ signal low, or
- Driving the $\overline{W}$ signal low after writing SRWD bit to 1.

The only way to exit case 2 is to pull the $\overline{W}$ signal high.

Note: If the $\overline{W}$ pin is permanently tied high, the status register cannot be write-protected.

The protection features of the device are summarized in Table 3 .

Table 3. Protection modes

SRWD bit	$\overline{W}$ signal	Status
0	X	Status register is writable
1	1	
1	0	Status register is write-protected

4.5 Identification page

The M95M01-A125, M95M01-A145 and M95M01-A150 offer an identification page (256 bytes) in addition to the 1-Mbit memory.

The identification page contains:

- A device identification: the first three bytes are programmed by STMicroelectronics with the device identification code, as shown in Table 4.
- Application parameters: the remaining bytes are filled at FFh and are available for application-specific data.

Note: If the end application does not need to read the device identification code, this field can be overwritten and used to store application-specific data. Once these data are written, the whole identification page should be permanently locked in read-only mode.

The RDID, WRID, LID instructions are detailed in Section 5: Instructions.

Table 4. Device identification bytes

Address in identification page	Content	Value
00h	ST manufacturer code	20h
01h	SPI family code	00h
02h	Memory density code	11h (1-Mbit)

5 Instructions

The list of instructions and their operation opcode are summarized in Table 5. All instructions, addresses and data are transferred with the *MSB* first and are initiated with a chip select ($\overline{S}$) driven low. Each command is composed of bytes , initiated with the instruction, as summarized in the following list of instructions. If an invalid instruction is sent, meaning an instruction not contained in Table 5, the device automatically enters a wait state until deselected.

Table 5. Instruction set

Instruction	Description	Reference section	Opcode	Command					
				Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
WREN	Write enable	Section 5.1	0000 0110	06h	-	-	-	-	-
WRDI	Write disable	Section 5.2	0000 0100	04h	-	-	-	-	-
RDSR	Read status register	Section 5.3	0000 0101	05h	D_7 to D_0 (out)	-	-	-	-
WRSR	Write status register	Section 5.4	0000 0001	01h	D_7 to D_0 (in)	-	-	-	-
READ	Read from memory array	Section 5.5	0000 0011	03h	XXXX $XXXA_{16}$(1)	A_{15} to A_8	A_7 to A_0	D_7 to D_0 (out)	Next byte(2)
WRITE	Write to memory array	Section 5.6	0000 0010	02h	XXXX $XXXA_{16}$(1)	A_{15} to A_8	A_7 to A_0	D_7 to D_0 (in)	Next byte(3)
RDID	Read identification page	Section 5.7	1000 0011	83h	XXXX XXXX(1)	XXXX X**0**XX(1)	A_7 to A_0	D_7 to D_0 (out)	Next byte(2)
WRID	Write identification page	Section 5.8	1000 0010	82h	XXXX XXXX(1)	XXXX X**0**XX(1)	A_7 to A_0	D_7 to D_0 (in)	Next byte(3)
RDLS	Read lock status	Section 5.9	1000 0011	83h	XXXX XXXX(1)	XXXX X**1**XX(1)	XXXX XXXX(1)	D_7 to D_0 (out)	-
LID	Lock identification page	Section 5.10	1000 0010	82h	XXXX XXXX(1)	XXXX X**1**XX(1)	XXXX XXXX(1)	XXXX XX1X(1)	-

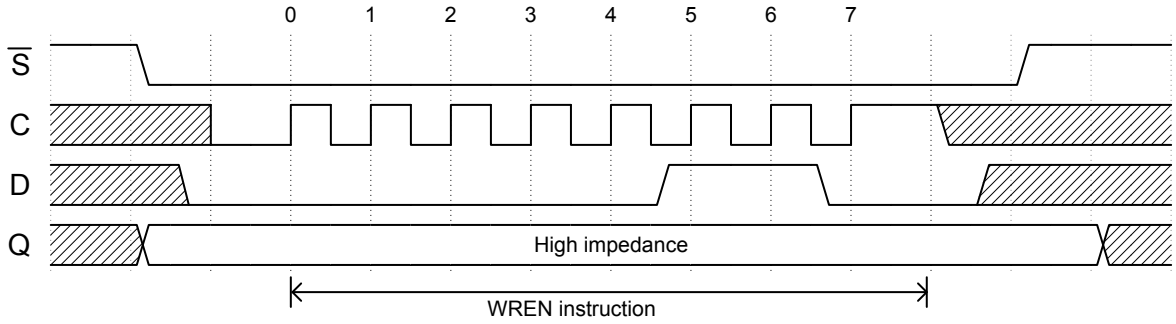
1. *X stands for "Don't care bits"*
2. *Continuously*
3. *Up to one page*

5.1 Write enable (06h)

The write enable (WREN) instruction must be decoded by the device before a write instruction (WRITE, WRSR, WRID or LID).

As shown in the following figure, to send this instruction to the device, chip select ($\overline{S}$) is driven low, the bits of the instruction byte are shifted in (*MSB* first) on serial data input (D) after which the chip select ($\overline{S}$) input is driven high and the write enable latch (WEL) bit is set (status register bit).

Figure 7. Write enable (WREN)



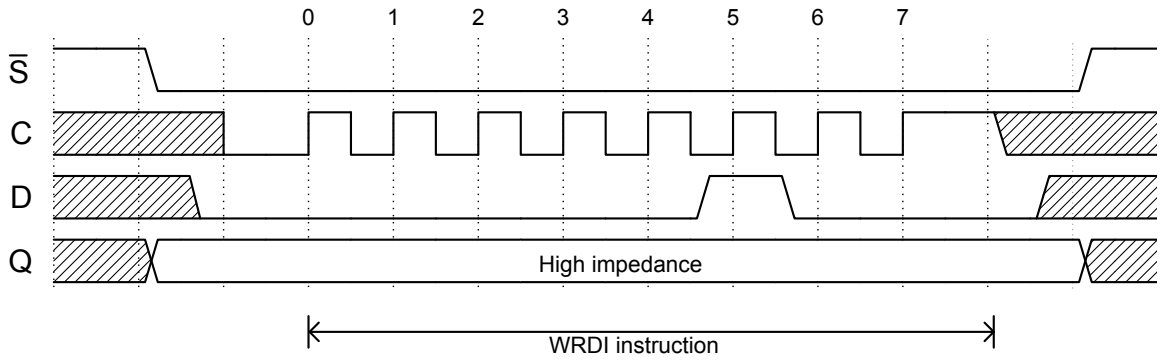
5.2 Write disable (04h)

The write disable (WRDI) instruction resets the write enable latch (WEL) bit in the status register to 0.

As shown in Figure 8, to send this instruction to the device, chip select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in (*MSB* first), on serial data input (D), after what the chip select ($\overline{S}$) input is driven high and the WEL bit is reset (status register bit).

If a write cycle is currently in progress, the WRDI instruction is decoded and executed and the WEL bit is reset to 0 with no effect on the ongoing write cycle.

Figure 8. Write disable (WRDI)



5.3 Read status register (05h)

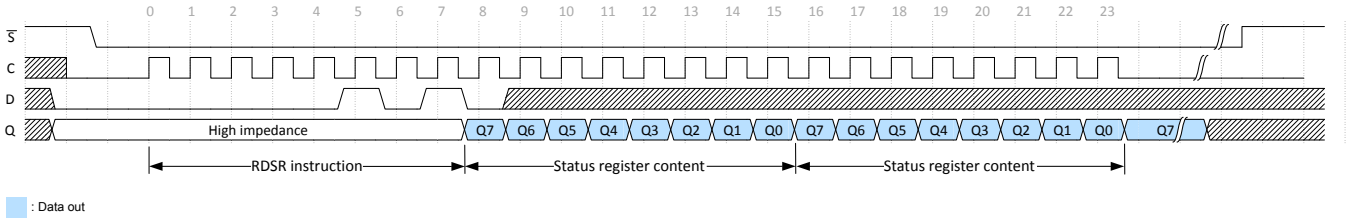
The read status register (RDSR) instruction is used to read the content of the status register.

As shown in Figure 9, to send this instruction to the device, chip select ($\overline{S}$) is first driven low. The bits of the instruction byte are shifted in (*MSB* first) on serial data input (D), the status register content is then shifted out (*MSB* first) on serial data output (Q).

If chip select ($\overline{S}$) continues to be driven low, the status register content is continuously shifted out.

The status register can always be read, even if a write cycle (t_W) is in progress. The status register functionality is detailed in Section 4.4.2: Status register and data protection.

Figure 9. Read status register (RDSR)



5.4 Write status register (01h)

The write status register (WRSR) instruction allows new values to be written to the status register. Before it can be accepted, a write enable (WREN) instruction must previously have been executed.

The write status register (WRSR) instruction is entered (*MSB* first) by driving chip select ($\overline{S}$) low, sending the instruction code followed by the data byte on serial data input (D), and driving the chip select ($\overline{S}$) signal high.

The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the write cycle (t_W).

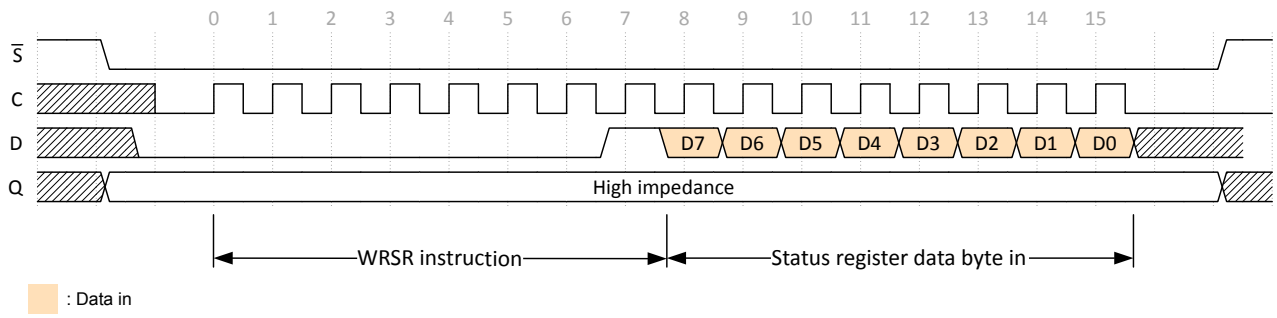
The write status register (WRSR) instruction has no effect on the b6, b5, b4, b1, and b0 bits in the status register (see Section 4.4.2: Status register and data protection).

The status register functionality is detailed in Section 4.4.2: Status register and data protection.

If a write cycle is in progress, the instruction is:

- Not accepted
- Not executed

Figure 10. Write status register (WRSR)



5.5 Read from memory array (03h)

The read from memory array (READ) instruction allows one or more data bytes to be sequentially read from the memory.

As shown in Figure 11, to send this instruction to the device, chip select ($\overline{S}$) is first driven low.

The bits of the instruction byte and address bytes are shifted in (*MSB* first) on serial data input (D) and the addressed data byte is then shifted out (*MSB* first) on serial data output (Q). The first addressed byte can be any byte within any page.

If chip select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented, and the next byte of data is shifted out. The whole memory can therefore be read with a single READ instruction.

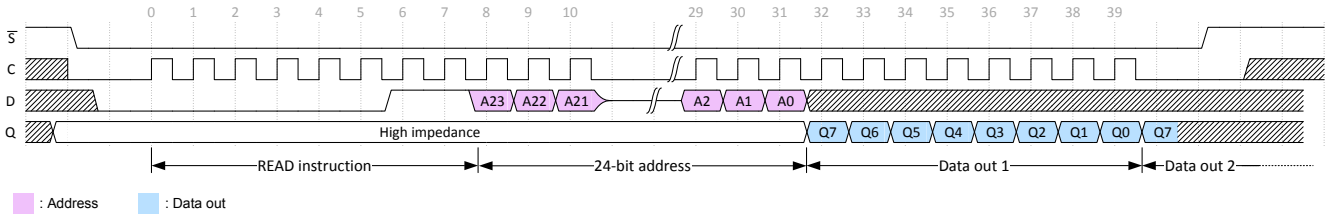
When the highest address is reached, the address counter rolls over to zero, allowing the read cycle to continue indefinitely.

The read cycle is terminated by driving chip select ($\overline{S}$) high at any time when the data bits are shifted out on serial data output (Q).

If a write cycle is in progress, the instruction is:

- Not accepted
- Not executed

Figure 11. Read from memory array (READ)

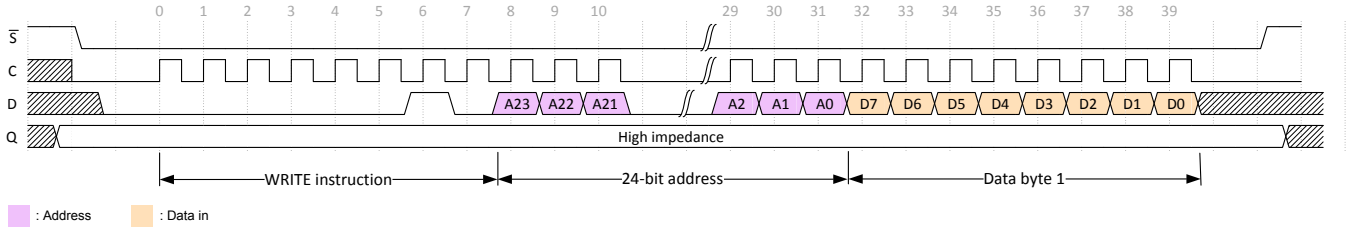


5.6 Write to memory array (02h)

The write to memory array (WRITE) instruction allows from one to 256 bytes of data to be written in a single instruction.

As shown in Figure 12, to send this instruction to the device, chip select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in (MSB first) on the serial data input (D). The instruction is terminated by driving chip select ($\overline{S}$) high at a data byte boundary. Figure 12 shows a single byte write.

Figure 12. Byte write (WRITE)



A page write is used to write several bytes of the same page with a single internal write cycle.

For a page write, chip select ($\overline{S}$) has to remain low, as shown in Figure 13, so that the next data byte are shifted in. Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the address counter exceeds the page boundary (the page size is 256 bytes), the internal address pointer rolls over to the beginning of the same page where the next data bytes are written. If more than 256 bytes are received, only the last 256 bytes are written.

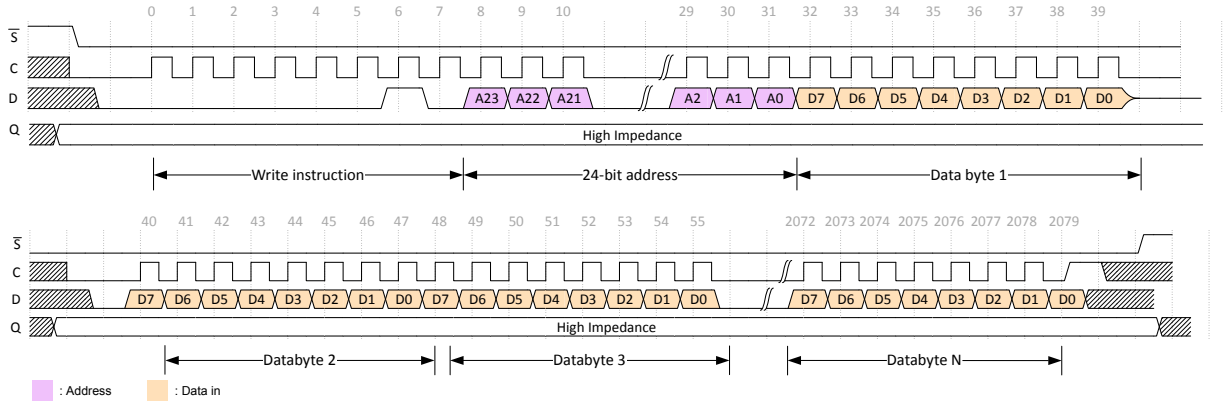
For both byte write and page write, the self-timed write cycle starts from the rising edge of chip select ($\overline{S}$), and continues for a period t_W (as specified in Table 18 and Table 19).

The instruction is discarded, and is not executed, under the following conditions:

- If a write cycle is already in progress
- If the addressed page is in the region protected by the block protect (BP1 and BP0) bits
- If one of the conditions defined in Section 4.4.1: Protocol control is not satisfied

Note: The self-timed write cycle t_W is internally executed as a sequence of two consecutive events: [erase addressed byte(s)], followed by [program addressed byte(s)]. An erased bit is read as 0 and a programmed bit is read as 1.

Figure 13. Page write (WRITE)



Note: N=256 in Figure 13

5.7 Read identification page (83h)

The read identification page (RDID) instruction allows one or more data bytes to be sequentially read from the identification page.

The chip select ($\overline{S}$) signal is first driven low. The bits of the instruction byte and address bytes are then shifted in (*MSB* first) on serial data input (D). The address bit A10 must be 0 and all other address bits, except [A7:A0], are *don't care*. The data byte pointed to by the lower address bits [A7:A0] is shifted out (*MSB* first) on serial data output (Q).

The first byte addressed can be any byte within the identification page.

If chip select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented and the byte of data at the new address is shifted out.

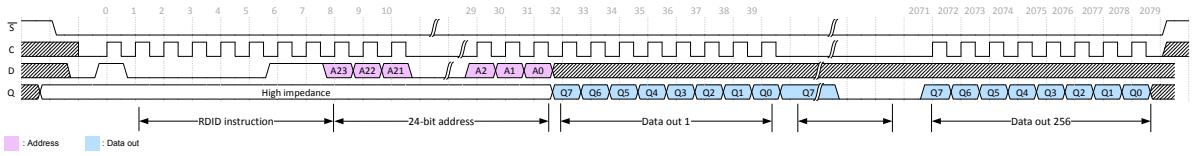
Note: There is no roll-over feature in the identification page. The address of the byte to read must not exceed the page boundary.

The read cycle is terminated by driving chip select ($\overline{S}$) high. The rising edges of the chip select ($\overline{S}$) signal can occur at any time when the data bits are shifted out.

If a write cycle is in progress, the instruction is:

- Not accepted
- Not executed

Figure 14. Read identification page (RDID)



The first three bytes of the identification page provide information about the device itself. Refer to Section 4.5: Identification page for more information.

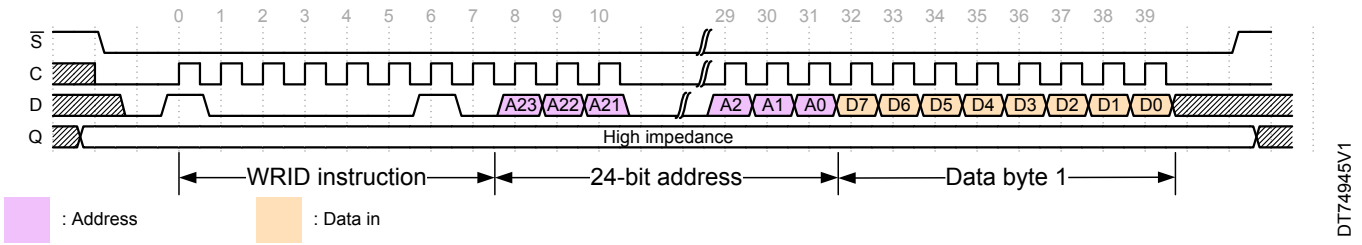
5.8 Write identification page (82h)

The write identification page (WRID) instruction allows from one to 256 bytes of data to be written in a single instruction inside the identification page.

The chip select ($\overline{S}$) is first driven low, and then the bits of the instruction byte, address bytes, and at least one data byte are shifted in (*MSB* first) on serial data input (D). The address bit A10 must be 0 and all other address bits, except [A7:A0], are *don't care*. The lower address bits [A7:A0] define the byte address inside the identification page.

The self-timed write cycle starts from the rising edge of chip select ($\overline{S}$), and continues for a period t_W (as specified in Table 18 and Table 19).

Figure 15. Write identification page (WRID)



Note: The first three bytes of the identification page offer the device identification code (refer to Section 4.5: Identification page for more information). Using the WRID command on the first three bytes overwrites the device identification code.

The instruction is discarded, and is not executed, under the following conditions:

- If a write cycle is already in progress
- If the block protect bits (BP1, BP0) = (1,1)
- If one of the conditions defined in Section 4.4: Protocol control and data protection is not satisfied.

5.9 Read lock status (83h)

The read lock status (RDLS) instruction is used to read the lock status.

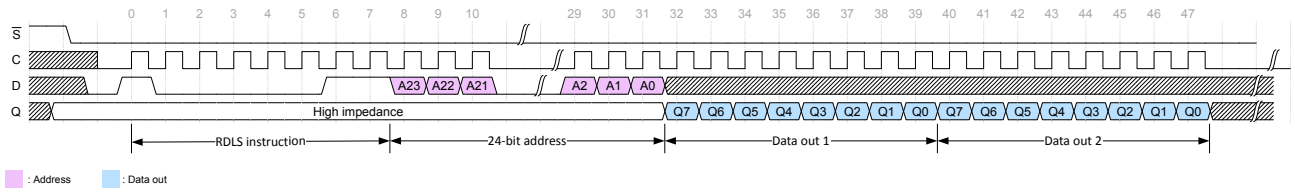
To send this instruction to the device, chip select ($\overline{S}$) first has to be driven low. The bits of the instruction byte and address bytes are then shifted in (*MSB* first) on serial data input (D). Address bit A10 must be 1; all other address bits are *don't care* (see Table 5). The lock bit is the least significant bit (*LSB*) of the byte read on serial data output (Q). It is at 1 when the lock is active and at 0 when the lock is not active. If chip select ($\overline{S}$) continues to be driven low, the same data byte is shifted out.

The read cycle is terminated by driving chip select ($\overline{S}$) high. The instruction sequence is shown in Figure 16.

If a write cycle is in progress, the instruction is:

- Not accepted
- Not executed

Figure 16. Read lock status (RDLS)



5.10 Lock identification page (82h)

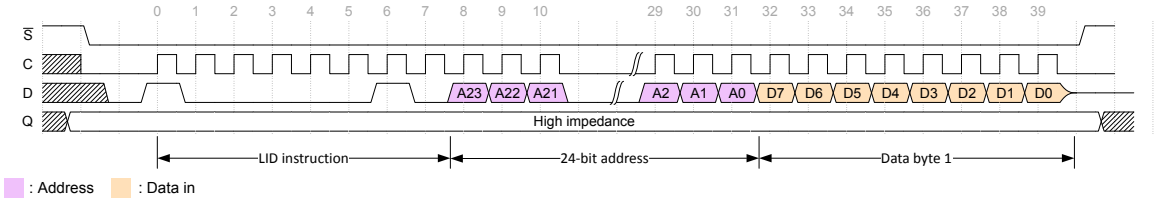
The lock identification page (LID) instruction is used to permanently lock the identification page in read-only mode.

The LID instruction is issued by:

- Driving chip select ($\overline{S}$) low
- Sending (*MSB* first) the instruction code, the address bytes and a data byte on serial data input (D)
- Driving chip select ($\overline{S}$) high

In the address sent, A10 must be equal to 1. All other address bits are *don't care* (see Table 5). The data byte sent must be equal to the binary value xxxx xx1x, where x = *don't care*. The LID instruction is terminated by driving chip select ($\overline{S}$) high at a data byte boundary, otherwise, the instruction is not executed.

Figure 17. Lock ID sequence



Driving chip select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed write cycle which duration is t_W (specified in Table 18 and Table 19). The instruction sequence is shown in Figure 17.

The instruction is discarded, and is not executed, under the following conditions:

- If a write cycle is already in progress
- If (BP1, BP0) = (1,1)
- If one of the conditions defined in Section 4.4: Protocol control and data protection is not satisfied

6 Application design recommendations

6.1 Supply voltage (V_{CC})

6.1.1 Operating supply voltage (V_{CC})

Before selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Table 7, Table 8, Table 9, Table 10, and Table 11).

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W). To secure a stable *DC* supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

6.1.2 Device reset

In order to prevent erroneous instruction decoding and inadvertent write operations during power-up, a power-on-reset (*POR*) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} reaches the *POR* threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see operating conditions in Section 9: DC and AC parameters).

At power-up, when V_{CC} passes over the *POR* threshold, the device is reset and is in the following state:

- in standby power mode,
- deselected,
- Status register values:
  - Write enable latch (WEL) bit is reset to 0
  - Write in progress (WIP) bit is reset to 0
  - Status register write disable (SRWD) , BP1 and BP0 bits remain unchanged (nonvolatile bits).

It is important to note that the device must not be accessed until V_{CC} reaches a valid and stable level within the specified [V_{CC}(min), V_{CC}(max)] range, as defined under operating conditions in Section 9: DC and AC parameters.

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

6.1.3 Power-up conditions

When the power supply is turned on, V_{CC} continuously rises from V_{SS} to V_{CC}. During this time, the chip select ($\overline{S}$) line is not allowed to float but must follow the V_{CC} voltage. The chip select ($\overline{S}$) line must be connected to V_{CC} via a suitable pull-up resistor (see Figure 18).

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in Table 7, Table 8, Table 9, Table 10, and Table 11.

To prevent inadvertent write operations during power-up, a *POR* circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} reaches the internal threshold voltage. Once the V_{CC} is greater than, or equal to, the minimum V_{CC} level, the controller must wait for at least t_{WU} before sending the first command to the device. See Table 18 and Table 19 for the value of the wake-up time parameter.

When V_{CC} passes over the *POR* threshold, the device is reset and in the following state:

- Standby power mode
- Deselected
- Status register values:
  - Write enable latch (WEL) bit is reset to 0.
  - Write in progress (WIP) bit is reset to 0.
  - SRWD, BP1, and BP0 bits remain unchanged (nonvolatile bits).
- Not in the hold condition

When the V_{CC} has reached a stable value within the [V_{CC}(min), V_{CC}(max)] range, the device is ready to operate.

6.1.4 Power-down

During power-down, when V_{CC} continuously decreases below the minimum operating voltage defined in Table 7, Table 8, Table 9, Table 10, and Table 11, the device must be:

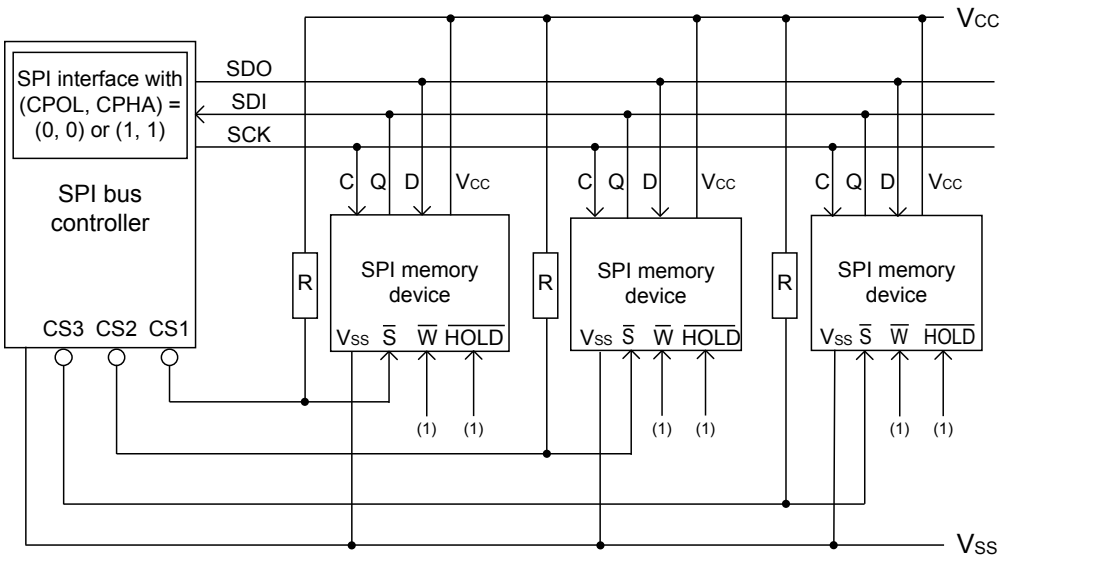
- Deselected (chip select ($\overline{S}$) must be allowed to follow the voltage applied on V_{CC})
- Standby power mode (there must not be any internal write cycle in progress).

6.2 Connecting to the SPI bus

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The serial data input (D) is sampled on the first rising edge of the serial clock (C) after chip select ($\overline{S}$) goes low.

All output data bytes are shifted out of the device, most significant bit first. The serial data output (Q) is latched on the first falling edge of the serial clock (C) after the instruction (such as the read from memory array and read status register instructions) have been clocked into the device.

Figure 18. Bus controller and memory devices on the SPI bus



1. The write protect ($\overline{W}$) and hold ($\overline{HOLD}$) signals must be driven, high or low as appropriate.

Figure 18 shows an example of three memory devices connected to an *SPI* bus controller. Only one device is selected at a given time, so only one of them drives the serial data output (Q) line at that time. The other devices are in a high impedance state. The pull-up resistor R (represented in Figure 18) ensures that a device is not selected if the bus controller leaves the chip select ($\overline{S}$) line in the high impedance state.

In applications where the bus controller leaves all *SPI* bus lines in high impedance at the same time (for example, if the bus controller is reset during the transmission of an instruction), it is recommended to connect the serial clock (C) line to an external pull-down resistor. This ensures that, if all inputs/outputs become high impedance, the serial clock (C) line is pulled low (while the chip select ($\overline{S}$) line is pulled high). This prevents chip select ($\overline{S}$) and serial clock (C) from becoming high at the same time, ensuring that the t_{SHCH} requirement is met. The typical value of R is 100 kΩ.

6.3 Cycling with error correction code (*ECC*)

The error correction code (*ECC*) is an internal logic function, transparent for the *SPI* communication protocol.

The *ECC* logic is implemented on each group of four bytes. This byte is located at:

$$[4N, 4N + 1, \quad 4N + 2, \quad 4N + 3]$$

Where N is an integer.

Within a group, if a single bit happens to be erroneous during a read operation, the *ECC* detects and replaces it with the correct value. The read reliability is therefore much improved.

Even if the *ECC* function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the *ECC* function also writes/cycles the three other bytes located in the same group. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the four bytes of the group: the sum of the cycles seen by byte 0, byte 1, byte 2, and byte 3 of the same group must remain below the maximum value defined in Table 20 and Table 22.

Example 1 : Maximum cycling limit reached with one million cycles per byte

Each byte of a group can be equally cycled one million times (at 25 °C), so that the group cycling budget is four million cycles.

Example 2 : Maximum cycling limit reached with unequal byte cycling

Within a group, byte 0 can be cycled two million times, byte 1 can be cycled one million times, byte 2 and byte 3 can be cycled 500.000 times, making a total cycling budget of four million cycles for the group.

7 Delivery state

The device is delivered with:

- The memory array set to all 1s (each byte = FFh)
- The status register bits set to 0 (byte = 00h)
- The identification page is set with the first three bytes containing the value of the device identification defined in Table 4. The content of the other bytes is *don't care*.

8 Absolute maximum ratings

Stressing the device outside the ratings listed in Table 6 can permanently damage it. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Units
T_{AMB}	Ambient operating temperature	-40	+150	°C
T_{STG}	Storage temperature	-65	+150	
T_{LEAD}	Lead temperature during soldering	See note (1)		
V_O	Output voltage on Q pin	-0.50	V_{CC} + 0.6	V
V_I	Input voltage	-0.50	6.5	
I_{OL}	DC output current (Q = 0)	-	5	mA
I_{OH}	DC output current (Q = 1)	-	5	
V_{CC}	Supply voltage	-0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(2)	-	4000	V

1. *Compliant with JEDEC standard J-STD-020 (for small-body, Sn-Pb or Pb free assembly), the ST ECOPACK 7191395 specification, and the European directive on restrictions on hazardous substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses are applied to pin pairs in accordance with AEC-Q100-002, compliant with ANSI/ESDA/JEDEC JS-001, C1 = 100 pF, R1 = 1500 Ω , R2 = 500 Ω).*

9 DC and AC parameters

This section summarizes the operating conditions and the *DC* and *AC* characteristics.

9.1 DC parameters

9.1.1 Operating conditions for CMOSF8H products

Table 7. Operating conditions for /K commercial products (voltage range W, temperature grade 4)

Symbol	Parameter	Test conditions	Min.	Max.	Units
V_{CC}	Supply voltage	-	2.5	5.5	V
T_A	Operating temperature	-	-40	+145	°C
f_C	Operating clock frequency	V_{CC} ≥ 2.5 V, capacitive load on the Q pin ≤ 100 pF	-	10	MHz

Table 8. Operating conditions for /K commercial products (voltage range W, temperature grade 3)

Symbol	Parameter	Test conditions	Min.	Max.	Units
V_{CC}	Supply voltage	-	2.5	5.5	V
T_A	Operating temperature	-	-40	+125	°C
f_C	Operating clock frequency	V_{CC} ≥ 2.5 V, capacitive load on the Q pin ≤ 100 pF	-	10	MHz

Table 9. Operating conditions for /K commercial products (voltage range W, temperature grade 3) for high-speed communication

Symbol	Parameter	Test conditions	Min.	Max.	Units
V_{CC}	Supply voltage	-	4.5	5.5	V
T_A	Operating temperature	-	-40	+85	°C
f_C	Operating clock frequency	V_{CC} ≥ 4.5 V, capacitive load on the Q pin ≤ 100 pF	-	16	MHz

9.1.2 Operating conditions for CMOSF9V products

Table 10. Operating conditions for /V commercial products (voltage range R, temperature grade 3)

Symbol	Parameter	Test conditions	Min.	Max.	Units
V_{CC}	Supply voltage	-	1.7	5.5	V
T_A	Operating temperature	-	-40	+125	°C
f_C	Operating clock frequency	Capacitive load on the Q pin ≤ 100 pF	-	16	MHz

Table 11. Operating conditions for /V commercial products (voltage range W, temperature grade 4)

Symbol	Parameter	Test conditions	Min.	Max.	Units
V_{CC}	Supply voltage	-	2.5	5.5	V
T_A	Operating temperature	-	-40	+150	°C
f_C	Operating clock frequency	Capacitive load on the Q pin ≤ 100 pF	-	16	MHz

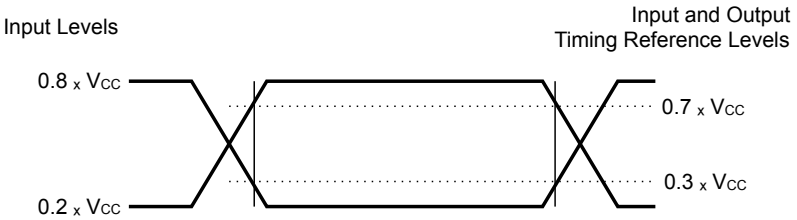
9.2 AC characteristics

9.2.1 AC measurement conditions

Table 12. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	-	100	pF
-	Input rise and fall times	-	25	ns
-	Input pulse voltages	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input and output timing reference voltages	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 19. AC measurement I/O waveform



9.2.2 Capacitance

Table 13. Capacitance

Symbol	Parameter	Test conditions	Min.	Max.	Units
C_{OUT}(1)	Output capacitance (Q)	V_{OUT} = 0 V	-	8	pF
C_{IN}(1)	Input capacitance	V_{IN} = 0 V	-	6	pF

1. *Evaluated by characterization - Not tested in production.*

9.3 DC characteristics

9.3.1 DC characteristics for CMOSF8H products

Table 14. DC characteristics for /K commercial products (voltage range W, temperature grade 4)

Symbol	Parameter	Test conditions (in addition to the conditions specified in Table 7)	Min.	Max.	Units
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}	-	2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}	-	3	
I_{CC}	Supply current (read)	V_{CC} = 2.5 V, f_C = 10 MHz, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	2	mA
		V_{CC} = 5.5 V, f_C = 10 MHz, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	4	
I_{CC0}	Supply current (write)	Averaged value during the write cycle (t_W): 2.5 V ≤ V_{CC} ≤ 5.5 V, $\overline{S} = V_{CC}$	-	2(1)	mA
I_{CC1}	Supply current (Standby mode)	T_A = 85 °C, V_{CC} = 2.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	2	µA
		T_A = 85 °C, V_{CC} = 5.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	3	
		T_A = +125 °C, V_{CC} = 2.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	15	
		T_A = +125 °C, V_{CC} = 5.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	20	
		T_A = 145 °C, V_{CC} = 2.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	25	
		T_A= 145 °C, V_{CC} = 5.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	40	
V_{IL}	Input low voltage	-	-0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage	-	0.7 V_{CC}	V_{CC} + 1	
V_{OL}	Output low voltage	I_{OL} = 2 mA	-	0.4	
V_{OH}	Output high voltage	I_{OH} = -2 mA	0.8 V_{CC}	-	
V_{RES}(1)	Internal reset threshold voltage	-	0.5	1.5	

1. *Evaluated by characterization - Not tested in production.*

Table 15. DC characteristics for /K commercial products (voltage range W, temperature grade 3)

Symbol	Parameter	Test conditions (in addition to the conditions specified in Table 8)	Min.	Max.	Units
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}	-	2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}	-	3	
I_{CC}	Supply current (read)	V_{CC} = 2.5 V, f_C = 10 MHz, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	2	mA
		V_{CC} = 5.5 V, f_C = 16 MHz(1), C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	5	
I_{CC0}	Supply current (write)	Averaged value during the write cycle (t_W): 2.5 V ≤ V_{CC} < 5.5 V, $\overline{S} = V_{CC}$	-	2(2)	mA
I_{CC1}	Supply current (Standby mode)	T_A = 85 °C, V_{CC} = 2.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	2	µA
		T_A = 85 °C, V_{CC} = 5.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	3	
		T_A = +125 °C, V_{CC} = 2.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	15	
		T_A= +125 °C, V_{CC} = 5.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}	-	20	
V_{IL}	Input low voltage	2.5 V ≤ V_{CC} ≤ 5.5 V	-0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage	2.5 V ≤ V_{CC} ≤ 5.5 V	0.7 V_{CC}	V_{CC} + 1	
V_{OL}	Output low voltage	V_{CC} ≥ 2.5 V, I_{OL} = 2 mA	-	0.4	
V_{OH}	Output high voltage	V_{CC} ≥ 2.5 V, I_{OH} = -2 mA	0.8 V_{CC}	-	
V_{RES}(2)	Internal reset threshold voltage	-	0.5	1.5	

1. *When -40 °C < T_A < 85 °C.*
2. *Evaluated by characterization - Not tested in production.*

9.3.2 DC characteristics for CMOSF9V products

Table 16. DC characteristics for /V commercial products (voltage range R, temperature grade 3)

Symbol	Parameter	Test conditions (in addition to the conditions specified in Table 10 and Table 11)	Min.	Max.	Units
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}	-	2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}	-	3	
I_{CC}	Supply current (read)	V_{CC} = 1.7 V, f_C = 5 MHz, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	1	mA
		V_{CC} = 2.5 V, f_C = 10 MHz, C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	1.5(1)	
		V_{CC} = 5.5 V, f_C = 16 MHz C = 0.1 V_{CC}/0.9 V_{CC}, Q = open	-	3	
I_{CC0}(2)	Supply current (write)	Averaged value during the write cycle (t_W): 1.7 V ≤ V_{CC} < 2.5 V, $\overline{S} = V_{CC}$	-	1	mA
		2.5 V ≤ V_{CC} ≤ 5.5 V, $\overline{S} = V_{CC}$	-	2(3)	
I_{CC1}	Supply current (Standby power mode)	T_A = +85 °C, V_{CC} = 1.7 V, $\overline{S} = V_{CC}$ $V_{IN} = V_{SS}$ or V_{CC}	-	1.5(2)	µA
		T_A = +85 °C, V_{CC} = 2.5 V, $\overline{S} = V_{CC}$ $V_{IN} = V_{SS}$ or V_{CC}	-	2(2)(4)	
		T_A = +85 °C, V_{CC} = 5.5 V, $\overline{S} = V_{CC}$ $V_{IN} = V_{SS}$ or V_{CC}	-	4(2)	
		T_A = +125 °C, V_{CC} = 1.7 V, $\overline{S} = V_{CC}$ $V_{IN} = V_{SS}$ or V_{CC}	-	5	
		T_A = +125 °C, V_{CC} = 2.5 V, $\overline{S} = V_{CC}$ $V_{IN} = V_{SS}$ or V_{CC}	-	7	
		T_A = +125 °C, V_{CC} = 5.5 V, $\overline{S} = V_{CC}$ $V_{IN} = V_{SS}$ or V_{CC}	-	11	
V_{IL}	Input low voltage	1.7 V ≤ V_{CC} < 2.5 V	-0.45	0.25 V_{CC}	V
		2.5 V ≤ V_{CC} ≤ 5.5 V	-0.45	0.3 V_{CC}	
V_{IH}	Input high voltage	1.7 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC} + 1	
		2.5 V ≤ V_{CC} ≤ 5.5 V	0.7 V_{CC}	V_{CC} + 1	
V_{OL}	Output low voltage	1.7 V ≤ V_{CC} < 2.5 V, I_{OL} = 1 mA	-	0.3	
		V_{CC} ≥ 2.5 V, I_{OL} = 2 mA	-	0.4	
V_{OH}	Output high voltage	1.7 V ≤ V_{CC} < 2.5 V, I_{OH} = -0.1 mA	0.8 V_{CC}	-	
		2.5 V ≤ V_{CC} ≤ 5.5 V, I_{OH} = -2 mA	0.8 V_{CC}	-	
V_{RES}(2)	Internal reset threshold voltage	-	0.5	1	

1. *Typical value at 3.3 V, +25 °C (evaluated by characterization, not tested in production) is 650 µA.*
2. *Evaluated by characterization - Not tested in production.*
3. *Typical value at 3.3 V, +25 °C (evaluated by characterization, not tested in production) is 1 mA.*
4. *Typical value at 3.3 V, +25 °C (evaluated by characterization, not tested in production) is 0.6 µA*

Table 17. DC characteristics for /V commercial products (operating voltage W, grade 4)

Symbol	Parameter	Test conditions (in addition to the conditions specified in Table 11)	Min.	Max.	Units
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}	-	2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}	-	3	µA
I_{CC}	Supply current (read)	V_{CC} = 2.5 V, f_C = 10 MHz, C = 0.1 V_{CC} /0.9 V_{CC}, Q = open	-	1.5 (1)	mA
		V_{CC} = 5.5 V, f_C = 16 MHz C = 0.1 V_{CC} /0.9 V_{CC}, Q = open	-	3	
I_{CC0}	Supply current (write)	Averaged value during the write cycle (t_W): 2.5 V ≤ V_{CC} ≤ 5.5 V $\overline{S} = V_{CC}$	-	2(2)	mA
I_{CC1}	Supply current (Standby power mode)	T_A = +125 °C, V_{CC} = 2.5 V, $\overline{S} = V_{CC}$ $V_{IN} = V_{SS}$ or V_{CC}	-	7	µA
		T_A = +125 °C, V_{CC} = 5.5 V, $\overline{S} = V_{CC}$ $V_{IN} = V_{SS}$ or V_{CC}	-	11	
		T_A = +150 °C, V_{CC} = 2.5 V, $\overline{S} = V_{CC}$ $V_{IN} = V_{SS}$ or V_{CC}	-	14	
		T_A = +150 °C, V_{CC} = 5.5 V, $\overline{S} = V_{CC}$ $V_{IN} = V_{SS}$ or V_{CC}	-	20	
V_{IL}	Input low voltage	2.5 V ≤ V_{CC} ≤ 5.5 V	-0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage	2.5 V ≤ V_{CC} ≤ 5.5 V	0.7 V_{CC}	V_{CC} + 1	
V_{OL}	Output low voltage	2.5 V ≤ V_{CC} ≤ 5.5 V, I_{OL} = 2 mA	-	0.4	
V_{OH}	Output high voltage	2.5 V ≤ V_{CC} ≤ 5.5 V, I_{OH} = -2 mA	0.8 V_{CC}	-	
V_{RES}(2)	Internal reset threshold voltage	-	0.5	1	

1. *Typical value at 3.3 V, +25 °C (evaluated by characterization, not tested in production) is 650 µA.*
2. *Evaluated by characterization, not tested in production*

9.4 AC tables

9.4.1 AC characteristics for CMOSF8H products

Table 18. AC characteristics for /K commercial products

Symbol	Alt.	Parameter	Min.(1)	Max.(1)	Min.(2)	Max.(2)	Units
f_C	f_{SCK}	Clock frequency	-	10	-	16	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	30	-	20	-	ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	30	-	20	-	ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	40	-	25	-	ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	30	-	20	-	ns
t_{CHSL}	-	$\overline{S}$ not active hold time	30	-	20	-	ns
t_{CH}(3)	t_{CLH}	Clock high time	40	-	25	-	ns
t_{CL}(3)	t_{CLL}	Clock low time	40	-	25	-	ns
t_{CLCH}(4)	t_{RC}	Clock rise time	-	2	-	2	µs
t_{CHCL}(4)	t_{FC}	Clock fall time	-	2	-	2	µs
t_{DVCH}	t_{DSU}	Data in setup time	10	-	10	-	ns
t_{CHDX}	t_{DH}	Data in hold time	10	-	10	-	ns
t_{HHCH}	-	Clock low hold time after $\overline{HOLD}$ not active	30	-	25	-	ns
t_{HLCH}	-	Clock low hold time after $\overline{HOLD}$ active	30	-	20	-	ns
t_{CLHL}	-	Clock low set-up time before $\overline{HOLD}$ active	0	-	0	-	ns
t_{CLHH}	-	Clock low set-up time before $\overline{HOLD}$ not active	0	-	0	-	ns
t_{SHQZ}(4)	t_{DIS}	Output disable time	-	40	-	25	ns
t_{CLQV}(5)	t_V	Clock low to output valid	-	40	-	25	ns
t_{CLQX}	t_{HO}	Output hold time	0	-	0	-	ns
t_{QLQH}(4)	t_{RO}	Output rise time	-	20	-	25	ns
t_{QHQL}(4)	t_{FO}	Output fall time	-	20	-	25	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid	-	40	-	25	ns
t_{HLQZ}(4)	t_{HZ}	$\overline{HOLD}$ low to output high-Z	-	40	-	25	ns
t_W	t_{WC}	Write time	-	4	-	4	ms

1. *Test conditions specified in Table 7 and Table 8*
2. *Test conditions specified in Table 9*
3. *t_{CH} + t_{CL} must never be less than the shortest possible clock period, 1 / f_C(max)*
4. *Evaluated by characterization - not tested in production.*
5. *t_{CLQV} must be compatible with t_{CL} (clock low time). If t_{SU} is the read setup time of the SPI bus controller, then t_{CL} must be equal to or greater than t_{CLQV} + t_{SU}.*

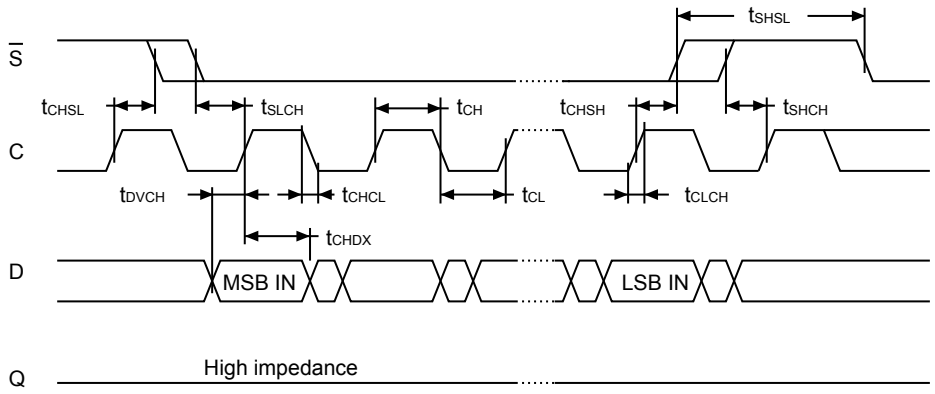
9.4.2 AC characteristics for CMOSF9V products

Table 19. AC characteristics for /V commercial products

Symbol	Alt.	Parameter	Min.	Max.	Min	Max.	Min	Max.	Units
			1.7 V ≤ V_{CC} < 2.5 V		2.5 V ≤ V_{CC} < 4.5 V		4.5 V ≤ V_{CC} < 5.5 V		
f_C	f_{SCK}	Clock frequency	-	5	-	10	-	16	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	60	-	30	-	20	-	ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	60	-	30	-	20	-	
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	90	-	40	-	25	-	
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	60	-	30	-	20	-	
t_{CHSL}	-	$\overline{S}$ not active hold time	60	-	30	-	20	-	
t_{CH}(1)	t_{CLH}	Clock high time	80	-	40	-	25	-	
t_{CL}(1)	t_{CLL}	Clock low time	80	-	40	-	25	-	
t_{CLCH}(2)	t_{RC}	Clock rise time	-	2	-	2	-	2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time	-	2	-	2	-	2	
t_{DVCH}	t_{DSU}	Data in setup time	20	-	10	-	10	-	ns
t_{CHDX}	t_{DH}	Data in hold time	20	-	10	-	10	-	
t_{HHCH}	-	Clock low hold time after $\overline{HOLD}$ not active	60	-	30	-	25	-	
t_{HLCH}	-	Clock low hold time after $\overline{HOLD}$ active	60	-	30	-	25	-	
t_{CLHL}	-	Clock low set-up time before $\overline{HOLD}$ active	0	-	0	-	0	-	
t_{CLHH}	-	Clock low set-up time before $\overline{HOLD}$ not active	0	-	0	-	0	-	
t_{SHQZ}(2)	t_{DIS}	Output disable time	-	80	-	40	-	25	
t_{CLQV}(3)	t_V	Clock low to output valid	-	80	-	40	-	25	
t_{CLQX}	t_{HO}	Output hold time	0	-	0	-	0	-	
t_{QLQH}(2)	t_{RO}	Output rise time	-	80	-	40	-	25	
t_{QHQL}(2)	t_{FO}	Output fall time	-	80	-	40	-	25	
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid	-	80	-	40	-	25	
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z	-	80	-	40	-	25	
t_W	t_{WC}	Write time	-	3.5	-	3.5	-	3.5	ms
t_{WU}(2)(4)	-	Wake up time	-	5	-	5	-	5	µs

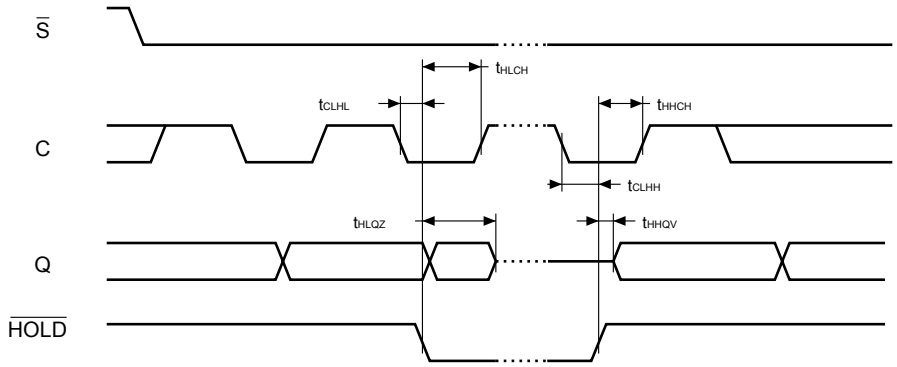
1. *t_{CH} + t_{CL} must never be lower than the shortest possible clock period, $1/f_C$(max).*
2. *Evaluated by characterization - Not tested in production.*
3. *t_{CLQV} must be compatible with t_{CL} (clock low time): if t_{SU} is the Read setup time of the SPI bus controller, t_{CL} must be equal to (or greater than) t_{CLQV}+t_{SU}.*
4. *Wake up time: Delay between the V_{CC}(min) stable and the first accepted command.*

Figure 20. **Serial input timing**



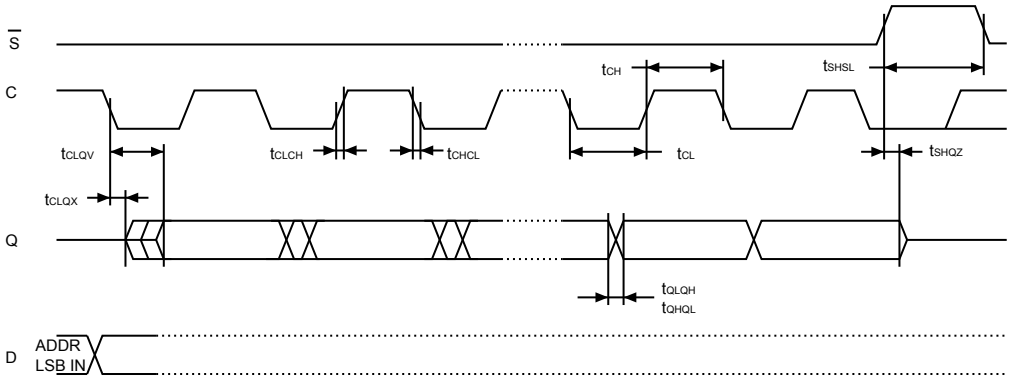
DT01447dV2

Figure 21. **Hold timing**



DT01448cV2

Figure 22. **Serial output timing**



DT01449gV2

10 Endurance and data retention

10.1 Endurance and data retention for CMOSF8H products

Table 20. Cycling performance for /K commercial products by groups of four bytes

Symbol	Parameter	Test conditions	Min.	Max.	Units
Ncycle	Write cycle endurance(1)	T_A ≤ +25 °C, V_{CC} (min) ≤ V_{CC} ≤ V_{CC} (max)	-	4.000.000	Write cycle (2)
		T_A = +85 °C, V_{CC} (min) ≤ V_{CC} ≤ V_{CC} (max)	-	1.200.000	
		T_A = +125°C, V_{CC} (min) ≤ V_{CC} ≤ V_{CC} (max)	-	600.000	
		T_A = +145 °C, V_{CC} (min) ≤ V_{CC} ≤ V_{CC} (max)(3)	-	400.000	

1. *The write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer, or for the status register byte (refer also to Section 6.3: Cycling with error correction code (ECC). The write cycle endurance is defined by characterization and qualification.*
2. *A write cycle is executed when either a page write, a byte write, a WRSR, a WRID, or a LID instruction is decoded. When using the byte write, the page write or the WRID instruction, refer also to Section 6.3: Cycling with error correction code (ECC) for more details.*
3. *For temperature range 4 only.*

Table 21. Memory cell data retention for CMOSF8H products

Parameter	Test conditions	Data retention performance
Data retention(1)	V_{CC}(min) ≤ V_{CC} ≤ V_{CC}(max)	• 100 years at +25 °C after maximum cycling • 200 years at +55°C for read only data

1. *Evaluated by characterization - Not tested in production.*

10.2 Endurance and data retention for CMOSF9V products

Table 22. Cycling performance by groups of four bytes for /V commercial products

Symbol	Parameter	Test conditions	Min.	Max.	Units
Ncycle	Write cycle endurance(1)	T_A ≤ +25 °C, V_{CC} (min) ≤ V_{CC} ≤ V_{CC} (max)	-	4.000.000	Write cycle (2)
		T_A = +85 °C, V_{CC} (min) ≤ V_{CC} ≤ V_{CC} (max)	-	1.200.000	
		T_A = +105 °C, V_{CC} (min) ≤ V_{CC} ≤ V_{CC} (max)	-	900.000	
		T_A = +125 °C, V_{CC} (min) ≤ V_{CC} ≤ V_{CC} (max)	-	600.000	
		T_A = +150 °C, V_{CC} (min) ≤ V_{CC} ≤ V_{CC} (max)	-	400.000	

1. *The write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer, or for the status register byte (refer also to Section 6.3: Cycling with error correction code (ECC). The write cycle endurance is defined by characterization and qualification.*
2. *A write cycle is executed when either a page write, a byte write, a WRSR, a WRID, or a LID instruction is decoded. When using the byte write, the page write or the WRID instruction, refer also to Section 6.3: Cycling with error correction code (ECC) for more details.*

Table 23. Memory cell data retention for CMOSF9V products

Parameter	Test conditions	Data retention performance
Data retention (1)	V_{CC}(min) ≤ V_{CC} ≤ V_{CC}(max)	• 10 years at +55 °C after maximum cycling • 15 years at +40 °C after maximum cycling • 100 years at +55 °C for read only data

1. *Evaluated by characterization - Not tested in production.*

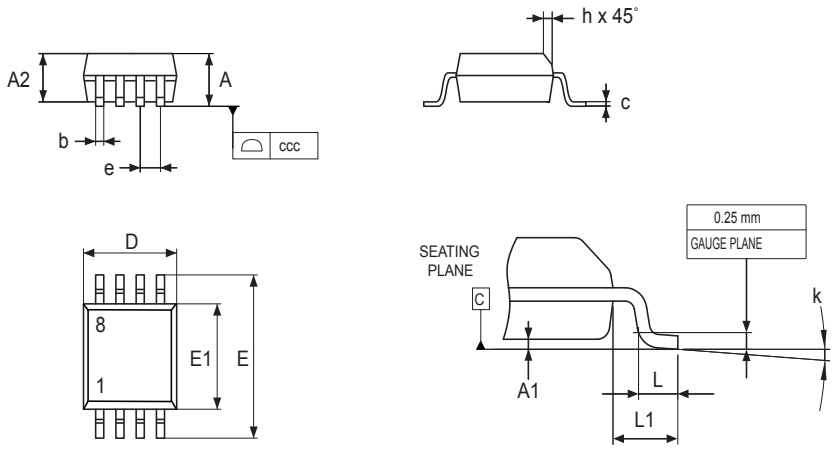
11 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 SO8N package information

This SO8N is an 8-lead, 4.9 x 6 mm, plastic small outline, 150 mil body width package.

Figure 23. SO8N - Outline



1. *Drawing is not to scale.*

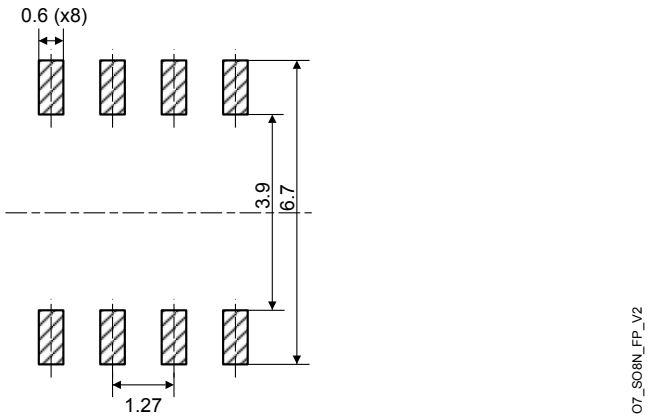
Table 24. SO8N - Mechanical data

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.170	-	0.230	0.0067	-	0.0091
D[2]	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1[3]	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side*
3. *Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Note: The package top may be smaller than the package bottom. Dimensions D and E1 are determinated at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interleads flash, but including any mismatch between the top and bottom of the plastic body. The measurement side for mold flash, protusions, or gate burrs is the bottom side.

Figure 24. SO8N - Footprint example

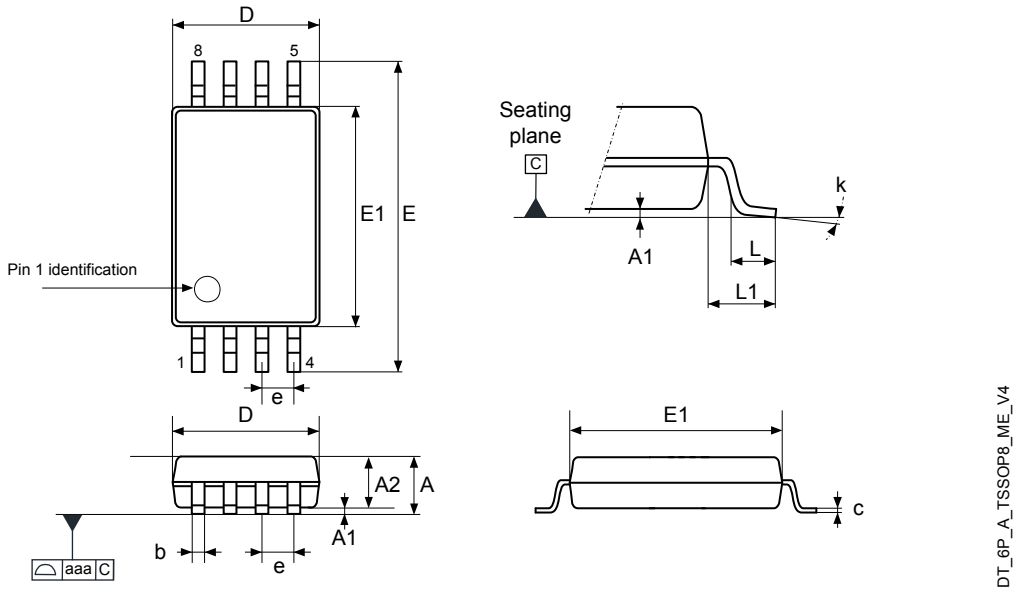


1. *Dimensions are expressed in millimeters.*

11.2 TSSOP8 package information

This TSSOP is an 8-lead, 3 x 6.4 mm, 0.65 mm pitch, thin shrink small outline package.

Figure 25. TSSOP8 – Outline



1. *Drawing is not to scale.*

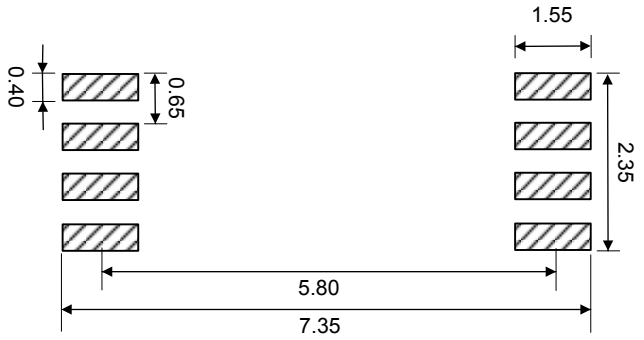
Table 25. TSSOP8 - Mechanical data

Symbol	millimeters			inches (1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D(2)	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.650	-	-	0.0256	-
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1(3)	4.300	4.400	4.500	0.1693	0.1732	0.1772
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.*
3. *Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.*

Note: The package top may be smaller than the package bottom. Dimensions D and E1 are determinated at the outermost extremes of the plastic body exclusive of the mold flash, tie bar burrs, gate burrs, and interleads flash, but including any mismatch between the top and bottom of the plastic body. The measurement side for the mold flash, protrusions, or gate burrs is the bottom side.

Figure 26. TSSOP8 – Footprint example

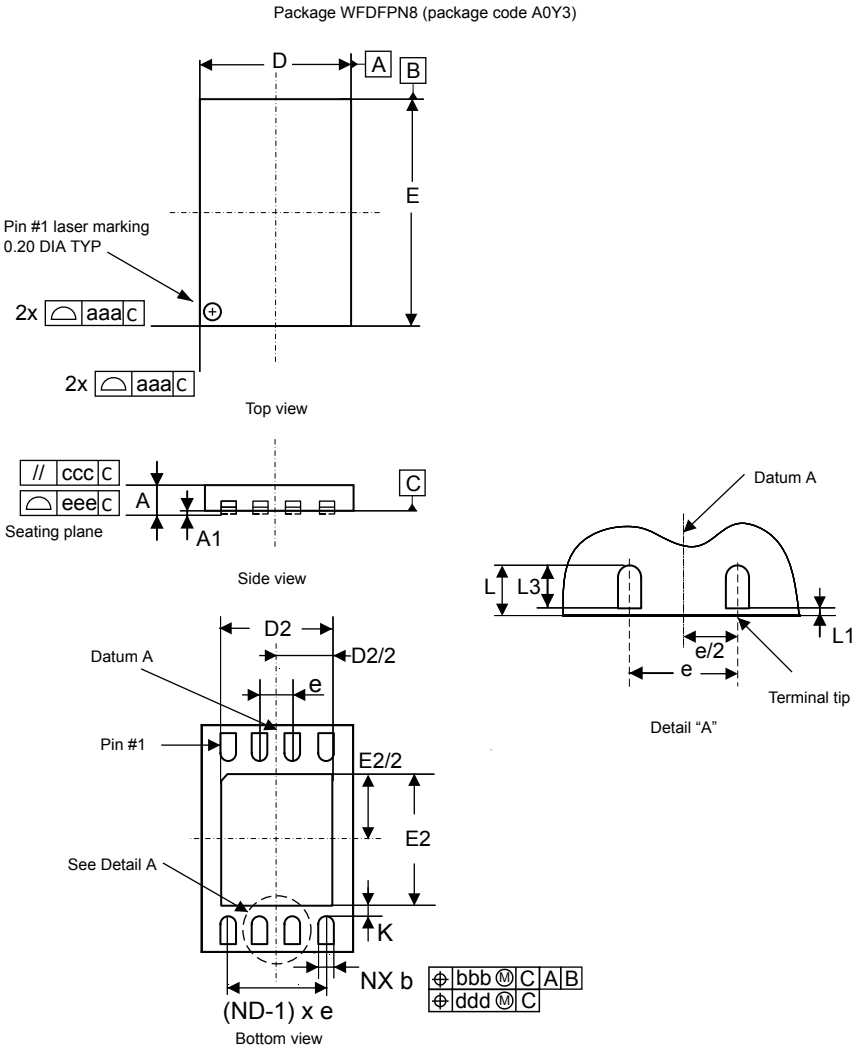


1. *Dimensions are expressed in millimeters.*

11.3 WFDFPN8 (DFN8) package information

This WFDFPN is a 8-lead, 2 x 3 mm, 0.5 mm pitch very very thin fine pitch dual flat package.

Figure 27. WFDFPN8 (DFN8) – Outline



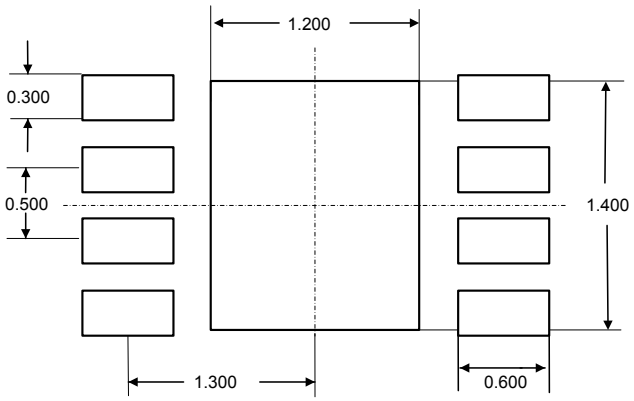
1. *Drawing is not to scale.*
2. *Exposed copper is not systematic and can appear partially or totally according to the cross section.*

Table 26. WFDFPN8 (DFN8) – Mechanical data

Symbol	millimeters			inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.700	0.750	0.800	0.0276	0.0295	0.0315
A1	0.025	0.045	0.065	0.0010	0.0018	0.0026
b[2]	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	1.900	2.000	2.100	0.0748	0.0787	0.0827
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
e	-	0.500	-	-	0.0197	-
L1	-	-	0.150	-	-	0.0059
L3	0.300	-	-	0.0118	-	-
D2	1.400	-	1.600	0.0551	-	0.0630
E2	1.200	-	1.400	0.0472	-	0.0551
K	0.400	-	-	0.0157	-	-
L	0.300	-	0.500	0.0118	-	0.0197
NX [3]	8					
ND [3]	4					
aaa	-	-	0.150	-	-	0.0059
bbb[4]	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee [5]	-	-	0.080	-	-	0.0031

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Dimension b applies to plated terminal and is measured between 0.15 and 0.30 mm from the terminal tip.*
3. *N is the number of terminals, ND is the number of terminals on “D” sides.*
4. *Max package warpage is 0.05 mm.*
5. *Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.*

Figure 28. WFDFPN8 (DFN8) – Footprint example



Note: The central pad (the area E2 by D2 in the Figure 27) must be either connected to V_{SS} or left floating (not connected) in the end application.

12 Ordering information

Table 27. Ordering information scheme

Example: M95 M01-D W MN 3 T P /K

Device type

M95 = SPI serial access EEPROM

Device function

M01-D = 1-Mbit (128-Kbyte) with additional identification page

Operating voltage

W = V_{CC} = 2.5 to 5.5 V

R = V_{CC} = 1.7 V to 5.5 V

Package(1)

MN = SO8 (150 mils width)

DW = TSSOP8 (169 mil width)

MF = WFDFPN8 (DFN8 2 x 3 mm)

Device grade

3 = Temperature range: -40°C to +125°C.

4 = Temperature range: -40°C to +145°C (for \K product)

4 = Temperature range: -40°C to +150°C (for \V product)

Option

Blank = Tube packing

T = Tape and reel packing

Plating technology

P or G = RoHS compliant and halogen-free (ECOPACK2)

Process

/K = Manufacturing technology CMOSF8H

/V = Manufacturing technology CMOSF9V

1. *All packages are ECOPACK2 (RoHS-compliant and free of brominated, chlorinated and antimony-oxide flame retardants).*

Note: For a list of available options (speed, package, etc.) or for further information on any aspect of this device, contact your nearest ST sales office.

Note: Parts marked as “ES” or “E” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 28. **Document revision history**

Date	Revision	Changes
06-Jun-2012	1	Initial release.
30-Jul-2012	2	• V_{CC} range R3 replaced with range W3 • Max clock frequency defined as 16 MHz when V_{CC} > 4.5 V inside the [-40 °C / +85 °C] temperature range
14-Feb-2013	3	• Removed UFDFPN8 (MLP8) package. • Updated V_{RES} maximum value in Table 13: DC characteristics (voltage range W, temperature range 4) and Table 14: DC characteristics (voltage range W, temperature range 3). • Rephrased introduction of Section 3.5: Identification page and information about Identification page in Section 6: Delivery state. • Deleted note(1) under Table 6: Instruction set. • Updated Table 9: Cycling performance by groups of 4 byte
14-Apr-2013	4	• Document reformatted. • Document status changed from “Preliminary data” to “Production data”. • Updated note (1) under Table 8: Absolute maximum ratings.
04-Feb-2014	5	• Changed Data retention from “40 years at 55 °C” to “50 years at +125 °C” in Features. • Removed bullets in Section 4.2: Write Disable (WRDI) (refer to Section : WEL bit). • Removed redundant sentence after Table 5: Device identification bytes.
31-Oct-2014	6	Added: • Updated Note 2 below Table 8: Absolute maximum ratings • Updated Table 14: DC characteristics (voltage range W, temperature range 3) • Updated Table 18: Ordering information scheme
18-May-2026	7	The document has undergone a general update.

Glossary

AC Alternating current

CPHA Clock phase bit. Selects the clock phase.

CPOL Clock polarity bit. Selects the clock polarity.

DC Direct current

ECC Error correction code

EEPROM Electrically erasable programmable read-only memory

ESD Electrostatic discharge

LSB Least significant byte

MSB Most significant byte

POR Power-on reset

SPI Serial peripheral interface

V_{IH} Input high voltage

V_{IL} Input low voltage

V_{OH} Output high voltage

V_{OL} Output low voltage

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