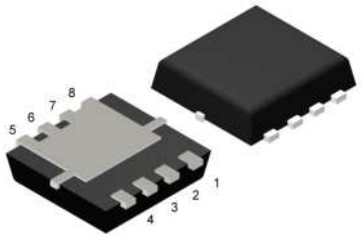
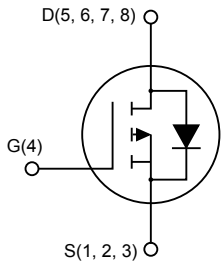
STL6P3LLH6

Datasheet

P-channel 30 V, 24 mΩ typ., 6 A STripFET H6 Power MOSFET in a PowerFLAT 3.3 x 3.3 package



PowerFLAT 3.3x3.3



AM01475v4

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL6P3LLH6	30 V	30 mΩ	6 A	2.9 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Product status link
STL6P3LLH6

Product summary	
Order code	STL6P3LLH6
Marking	6P3L
Package	PowerFLAT 3.3 x 3.3
Packing	Tape and reel

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	±20	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	6	A
	Drain current (continuous) at T_C = 100 °C	3.8	A
I_{DM}(1)(2)	Drain current (pulsed)	24	A
P_{TOT}	Total power dissipation at T_C = 25 °C	2.9	W
T_{stg}	Storage temperature	- 55 to 150	°C
T_J	Max. operating junction temperature	150	°C

1. *The value is rated according $R_{thj\text{-}pcb}$.*
2. *Pulse width limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2.50	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb, single operation	42.8	°C/W

1. *When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec.*

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 30 V			1	µA
		V_{GS} = 0 V, V_{DS} = 30 V, T_C = 125 °C			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3 A		24	30	mΩ
		V_{GS} = 4.5 V, I_D = 3 A		38	50	mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1450	-	pF
C_{oss}	Output capacitance		-	178	-	pF
C_{rss}	Reverse transfer capacitance		-	120	-	pF
Q_g	Total gate charge	V_{DD} = 24 V, I_D = 6 A, V_{GS} = 4.5 V (see Figure 12. Switching times test circuit for resistive load)	-	12	-	nC
Q_{gs}	Gate-source charge		-	4.4	-	nC
Q_{gd}	Gate-drain charge		-	5	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 24 V, I_D = 3 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	15	-	ns
t_r	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	21	-	ns

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage	I_{SD} = 6 A, V_{GS} = 0 V	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 6 A, di/dt = 100 A/µs V_{DD} = 16 V, T_J = 150 °C	-	15		ns
Q_{rr}	Reverse recovery charge		-	6.5		nC
I_{RRM}	Reverse recovery current		-	0.9		A

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

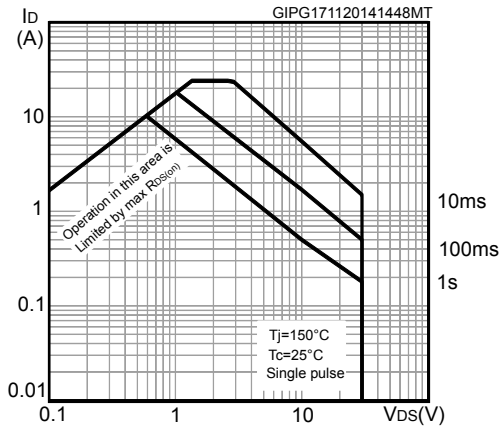


Figure 2. Thermal impedance

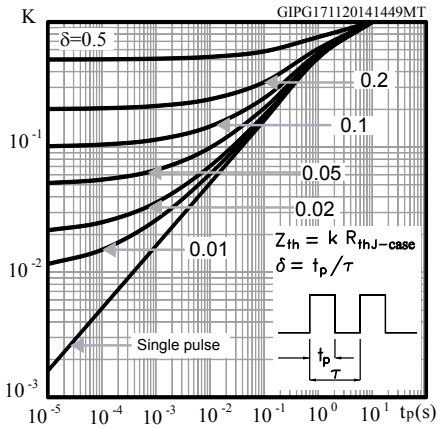


Figure 3. Output characteristics

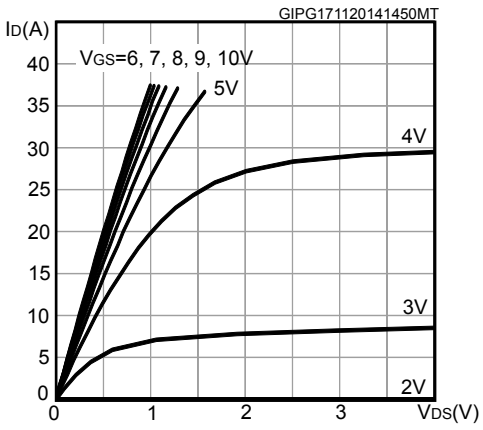


Figure 4. Transfer characteristics

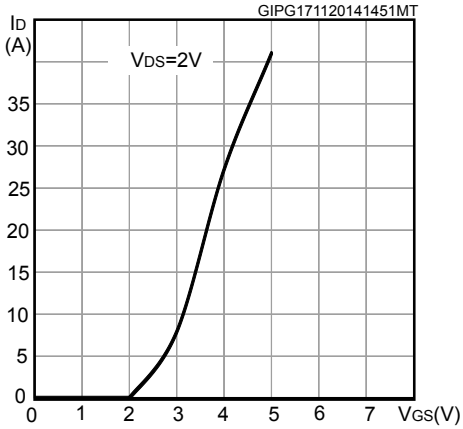


Figure 5. Gate charge vs gate-source voltage

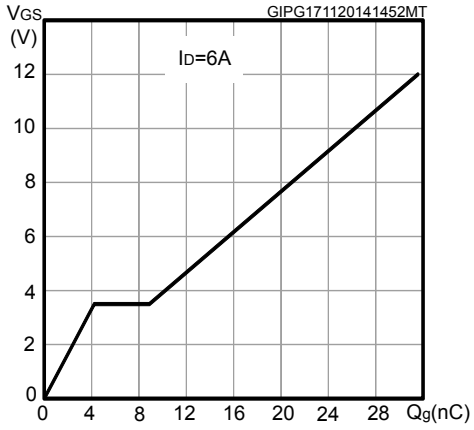


Figure 6. Static drain-source on-resistance

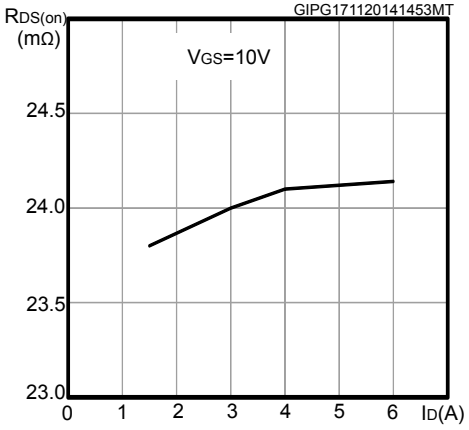


Figure 7. Capacitance variations

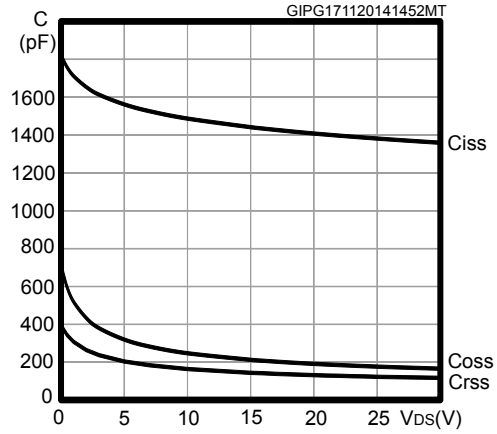


Figure 8. Normalized gate threshold voltage vs temperature

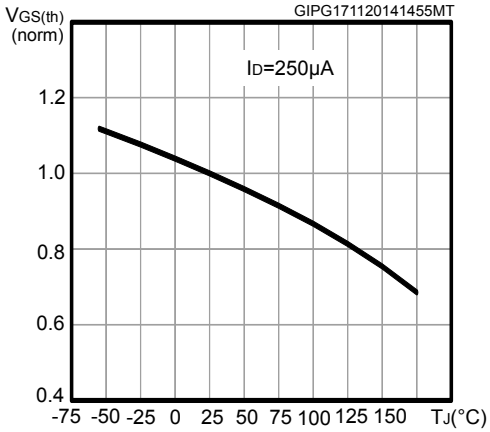


Figure 9. Normalized on-resistance vs temperature

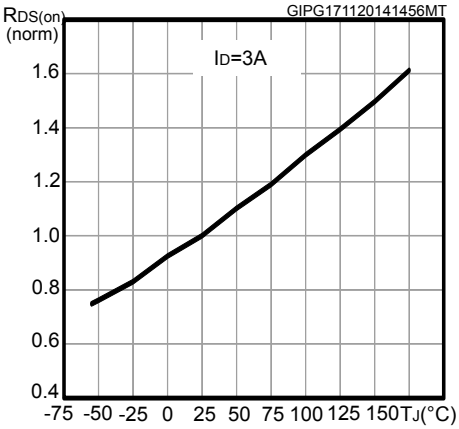


Figure 10. Normalized V_{DS} vs temperature

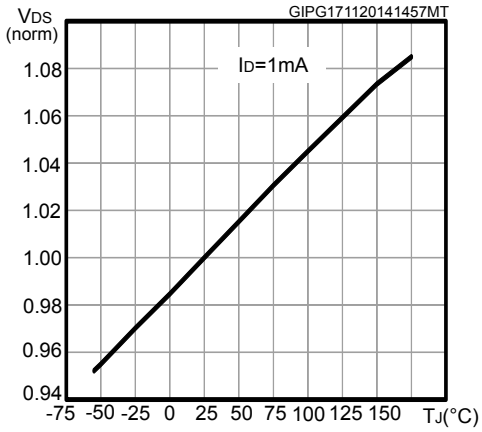
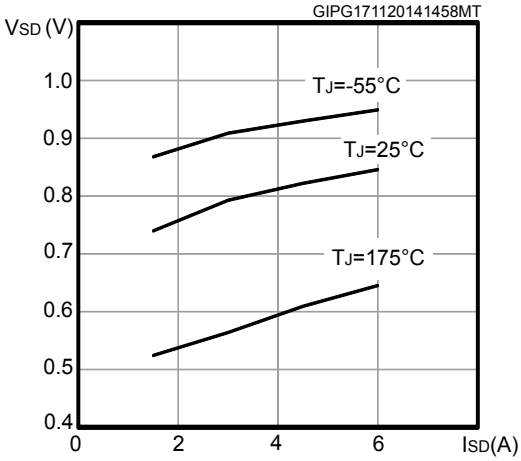


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Switching times test circuit for resistive load

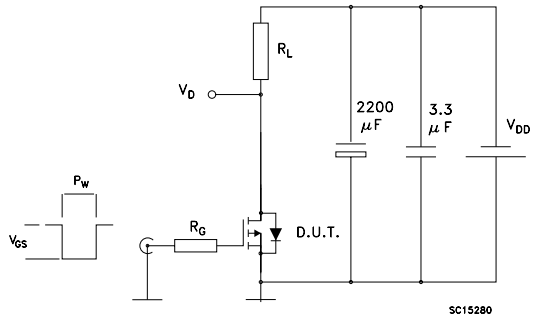


Figure 13. Gate charge test circuit

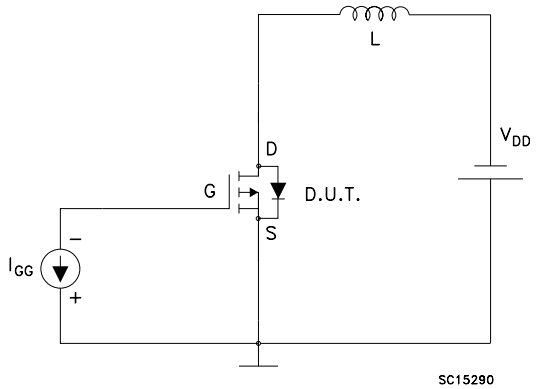
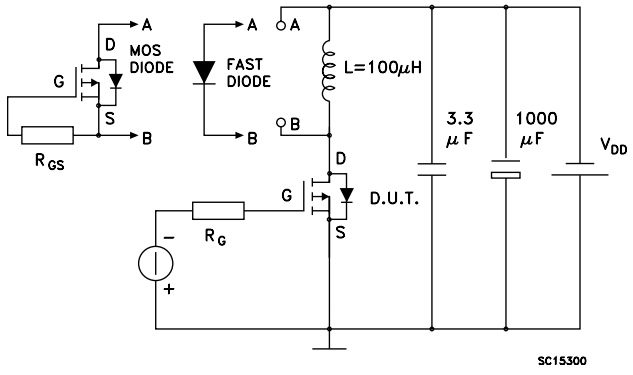


Figure 14. Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 3.3 x 3.3 type F mechanical data

Figure 15. PowerFLAT 3.3 x 3.3 type F drawing

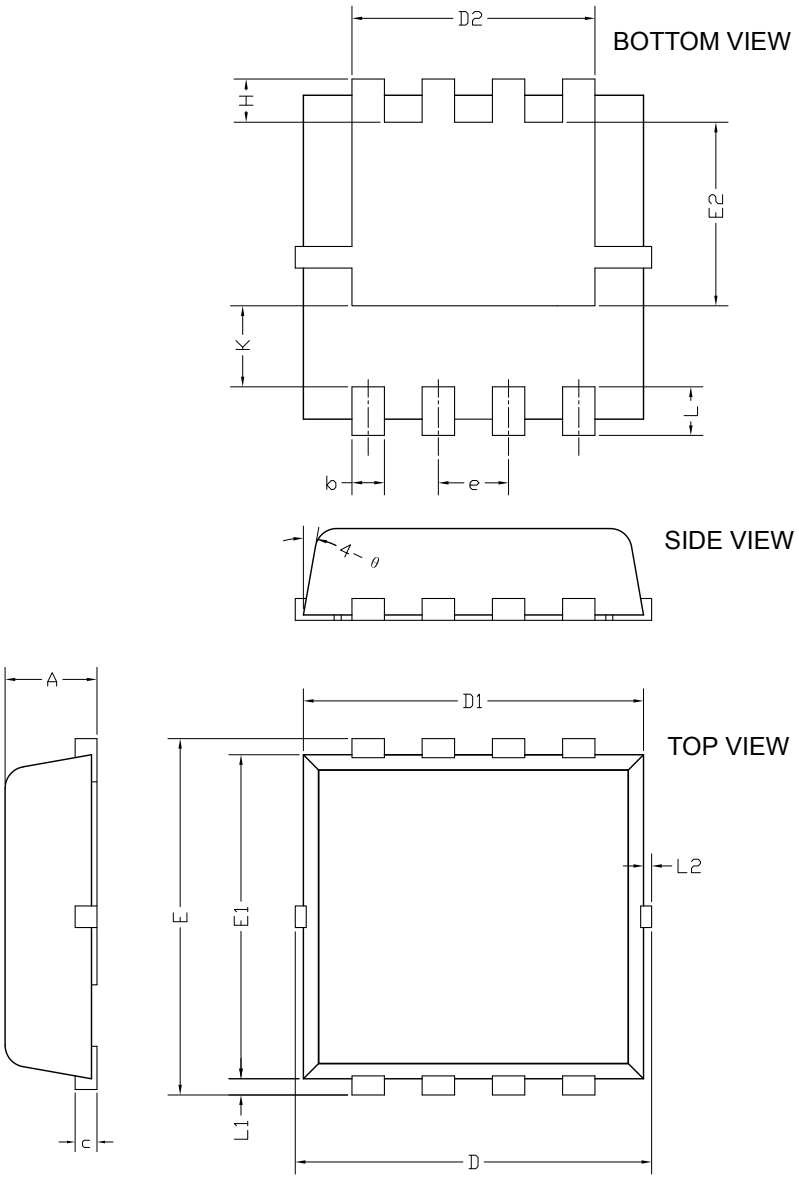
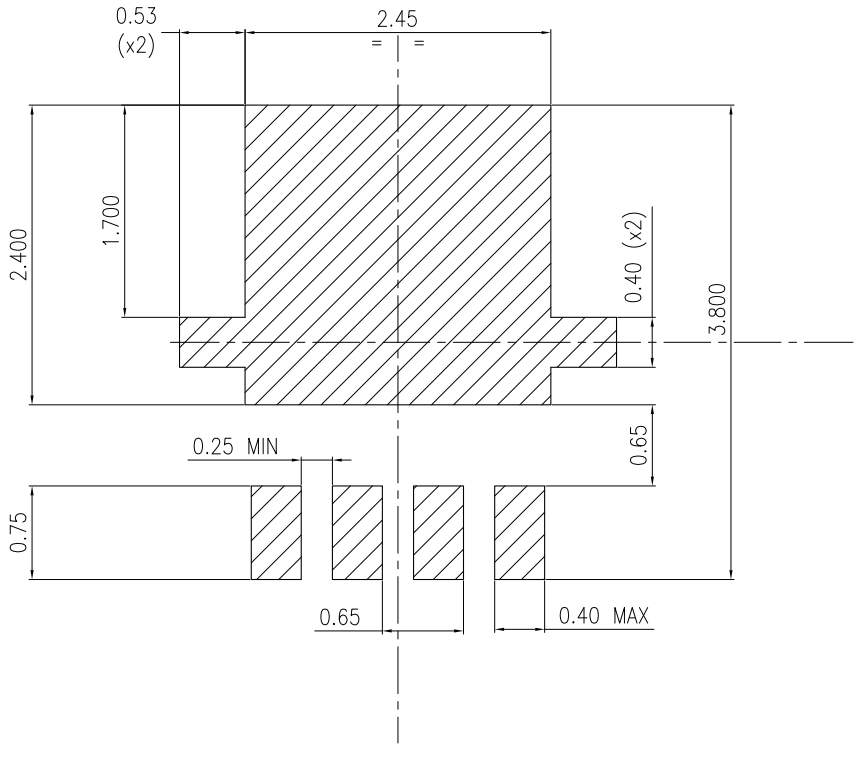


Table 7. PowerFLAT 3.3 x 3.3 type F mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
J	8°	10°	12°

Figure 16. PowerFLAT 3.3 x 3.3 type F recommended footprint



Revision history

Table 8. Document revision history

Date	Revision	Changes
04-Mar-2013	1	First release.
28-Nov-2013	2	• Modified: P_{TOT} value, silhouette and not found in cover page • Modified: V_{GS} and P_{TOT} values in not found • Modified: $R_{thj\text{-}pcb}$ value and note (1) in *Table 3: "Thermal data"* • Modified: I_{GSS} test conditions value • Modified: Q_g in *Table 5: "Dynamic"* • Added: *Table 9: "PowerFLAT™ 3.3 x 3.3 type F mechanical data"*, *Figure 18: "PowerFLAT™ 3.3 x 3.3 type F drawing"* and *Figure 19: "PowerFLAT™ 3.3 x 3.3 type F recommended footprint"*. • Minor text changes
26-Nov-2014	3	Updated *Figure 1: "Internal schematic diagram"*. Added *Section 4.1: "PowerFLAT™ 3.3 x 3.3 type C package information"* and *Section 4.2: "PowerFLAT™ 3.3 x 3.3 type F package information"*. Minor text changes.
09-Mar-2020	4	Updated Section 4 Package information. Minor text changes.

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4 **Package information** 8

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