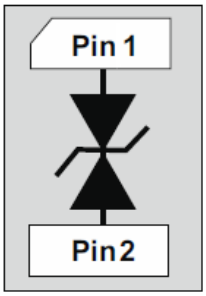
ESDAXLC6-1BT2

Datasheet

Single line ESD protection for high speed lines in 0402



SOD882T(0402)
(QFN-2L 1.0 x 0.6 x 0.35)



Product status link
ESDAXLC6-1BT2

Features

- Flow-through routing to keep signal integrity
- Ultra large bandwidth: 12 GHz
- Ultra low capacitance: 0.4 pF
- Extended operating junction temperature range: -55 °C to 150 °C
- RoHS compliant
- Complies with IEC 61000-4-2 - C = 150 pF, R = 330 Ω
  - ±16 kV (contact discharge)
  - ±30 kV (air discharge)

Application

The ESDAXLC6-1BT2 is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients such as:

- Digital video interface
- Ethernet
- USB 2.0 and USB 3.0
- High speed communication buses
- RF front-end

Description

The ESDAXLC6-1BT2 is an ESD device designed for high-speed lines protection.

For automotive application, an AEC-Q101 qualified version is available see ESDAXLC6-1BT2Y.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 (C = 150 pF, R = 330 Ω): Contact discharge Air discharge	 16 30	kV
P_{PP}	Peak pulse power dissipation (8/20 µs)		40	W
I_{PP}	Peak Pulse current (8/20 µs)		1.3	A
T_{stg}	Storage temperature range		-65 to +150	°C
T_j	Operating junction temperature range		-55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

Figure 1. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
V_{RM}	=	Stand-off voltage
V_{CL}	=	Clamping voltage
I_{RM}	=	Leakage current at V_{RM}
I_{PP}	=	Peak pulse current
R_d	=	Dynamic impedance
C_{LINE}	=	Input capacitance per line

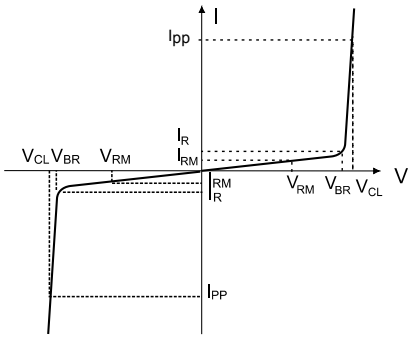


Table 2. Electrical characteristics (values) (T_{amb} = 25° C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	9	11	V
I_R	V_R = 3 V			50	nA
V_{CL}	I_{PP} = 1 A, 8/20 µs			17	V
	IEC 61000-4-2 - C = 150 pF, R = 330 Ω +8 kV contact discharge, measured at 30 ns		37		
	TLP, pulse duration 100 ns, 16 A		41		
R_d	TLP, pulse duration 100 ns, 16 A		2		Ω
$C_{I/O-GND}$	$V_{I/O}$ = 0 V, 200 MHz < f < 3 GHz, V_{OSC} = 30 mV		0.4	0.5	pF
f_C	S_{21} = -3 dB		12		GHz

1.1 Characteristics (curves)

Figure 2. Leakage current versus junction temperature

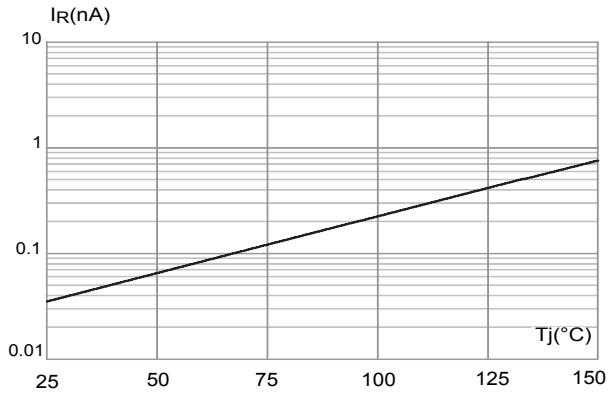


Figure 3. Junction capacitance versus reverse applied voltage

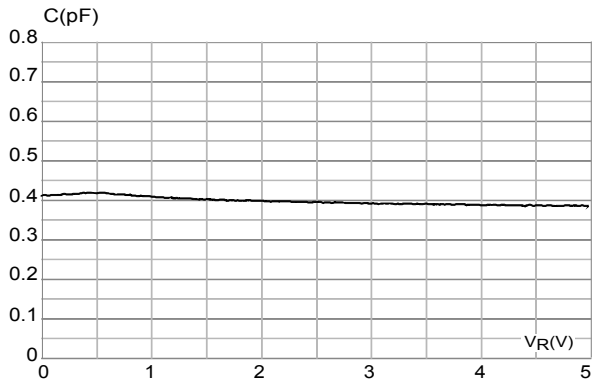


Figure 4. TLP

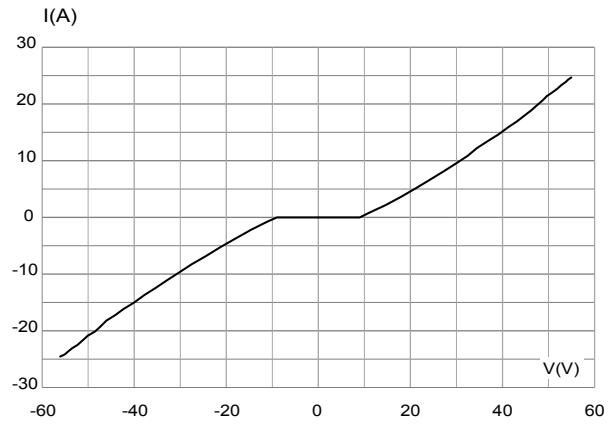


Figure 5. S21 attenuation

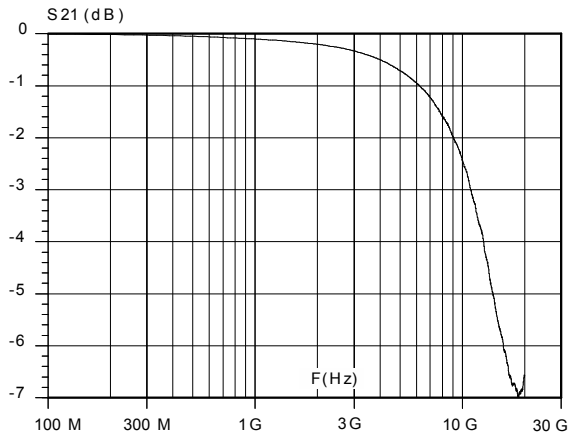


Figure 6. ESD response to IEC 61000-4-2 - C = 150 pF, R = 330 Ω (-8 kV contact discharge)

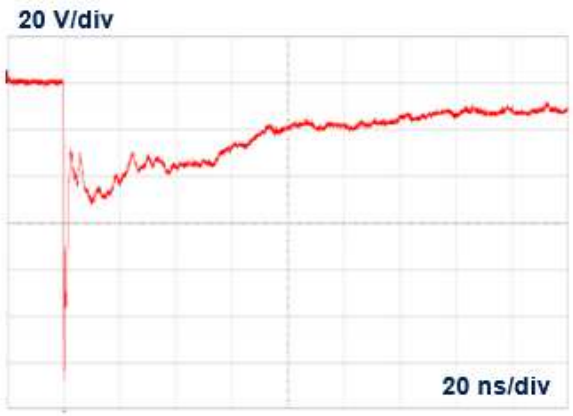


Figure 7. ESD response to IEC 61000-4-2 - C = 150 pF, R = 330 Ω (+8 kV contact discharge)



Figure 8. H2 harmonic versus input power at 710 MHz

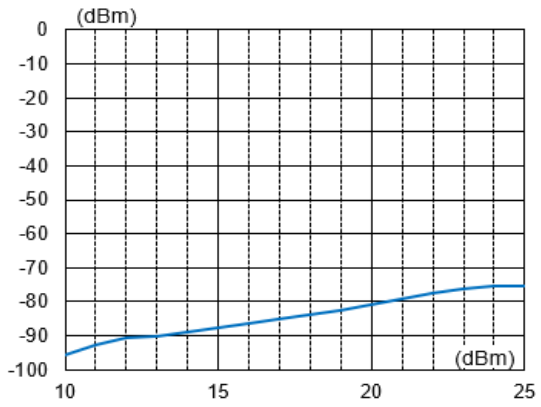


Figure 9. H3 harmonic versus input power at 710 MHz

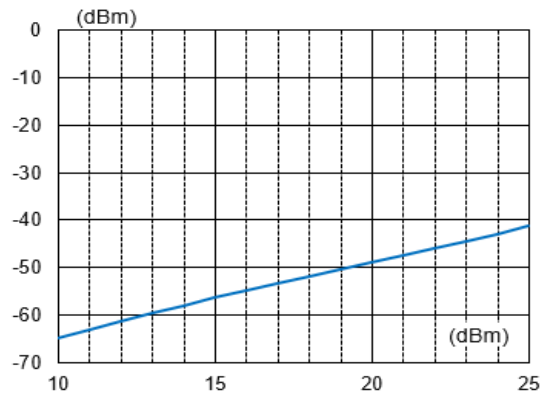


Figure 10. H2 harmonic versus input power at 824 MHz

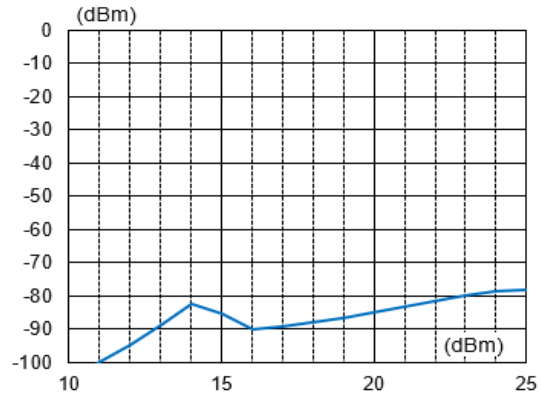


Figure 11. H3 harmonic versus input power at 824 MHz

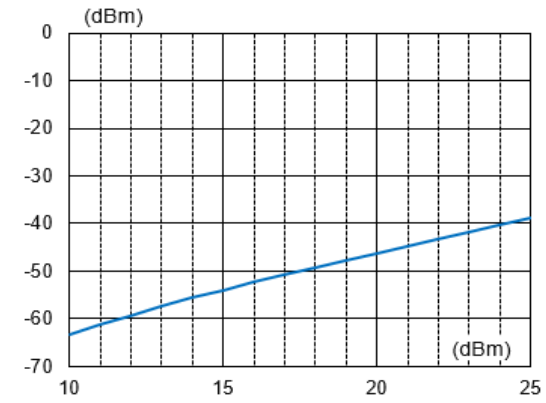


Figure 12. H2 harmonic versus input power at 2400 MHz

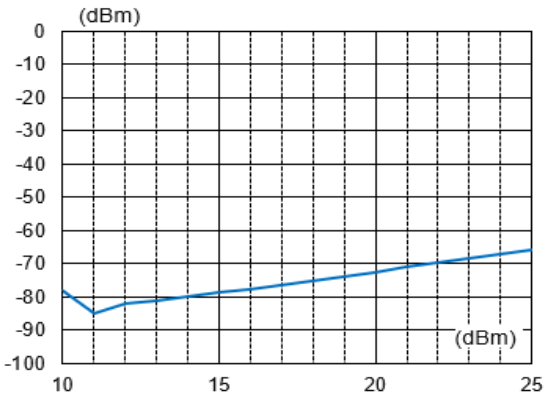
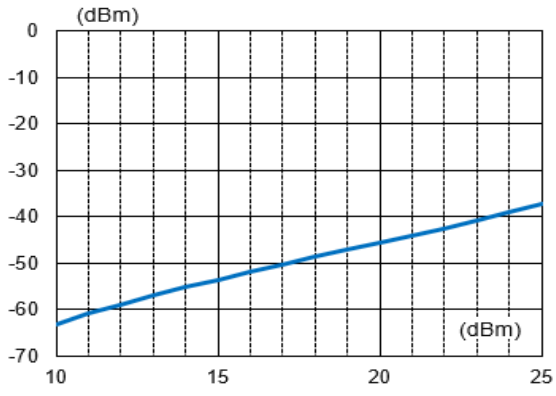


Figure 13. H3 harmonic versus input power at 2400 MHz



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 Package information

Figure 14. Package outline

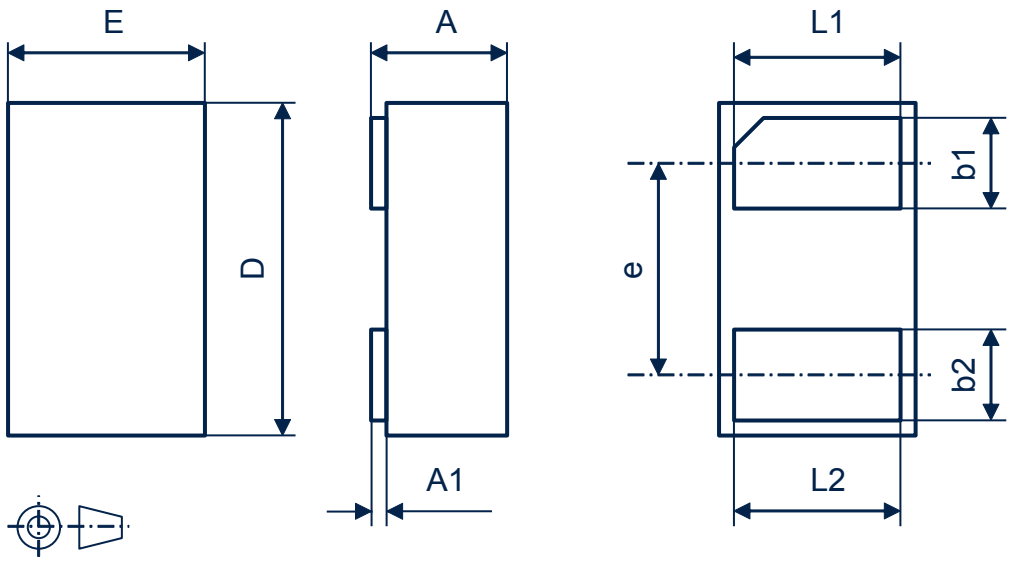
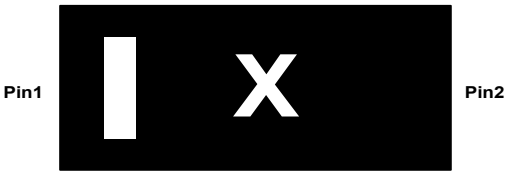


Table 3. Package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.30		0.40
A1	0.00		0.05
L1	0.45	0.50	0.55
L2	0.45	0.50	0.55
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	0.60	0.65	0.70
b1	0.20	0.25	0.30
b2	0.20	0.25	0.30

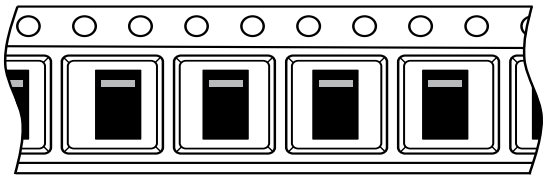
2.2 Packing and marking information

Figure 15. Marking layout



X: Refer to ordering information table for marking.

Figure 16. Package orientation in reel



Taped according to EIA-481

Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package
On bidirectional devices, marking and logo may be not always in the same direction

Figure 17. Tape leader and trailer dimensions

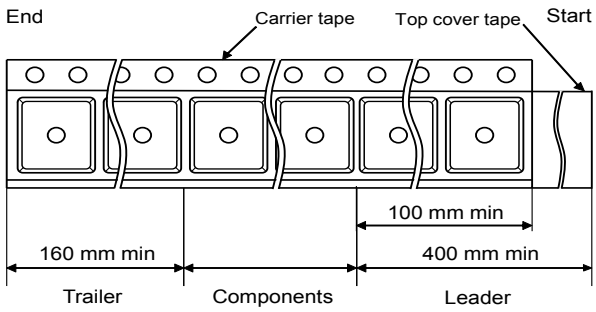


Figure 18. Tape and reel orientation

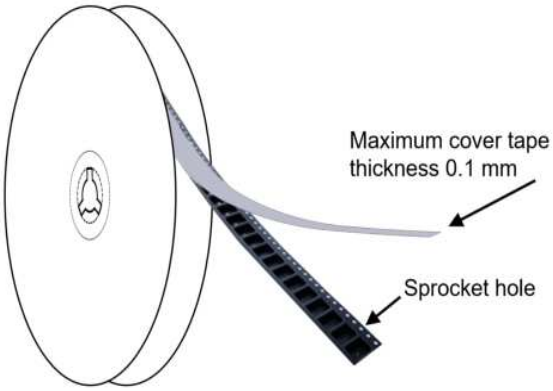


Figure 19. Reel dimensions (mm)

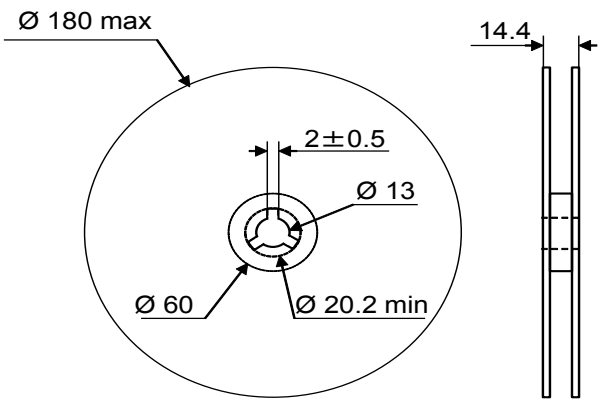


Figure 20. Inner box dimensions (mm)

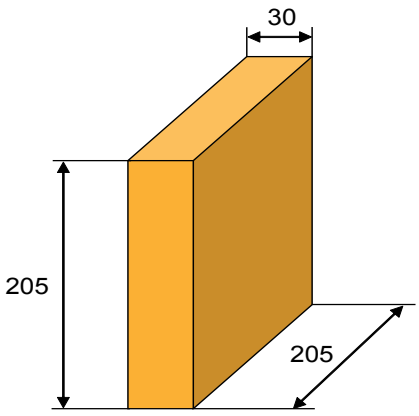
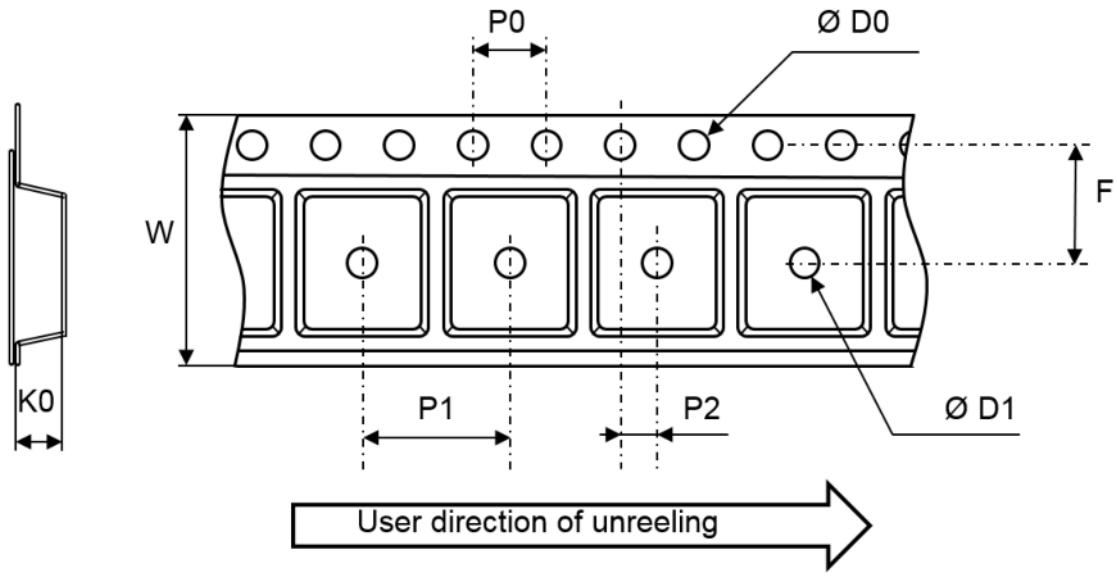


Figure 21. **Tape outline**



Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

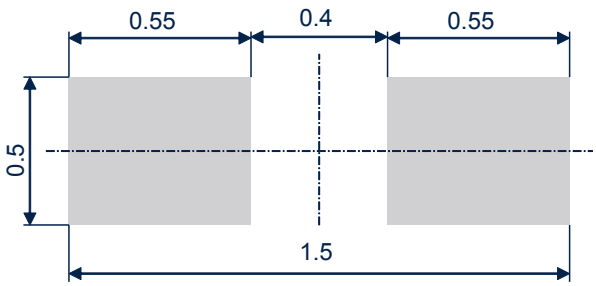
Table 4. **Tape and reel mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.45	1.5	1.6
D1	0.35		
F	3.45	3.5	3.55
K0	0.42	0.47	0.52
P0	3.9	4	4.1
P1	1.95	2	2.05
P2	1.95	2	2.05
W	7.9	8	8.3

3 Assembly recommendations

3.1 Recommended footprint

Figure 22. **Recommended footprint in mm**

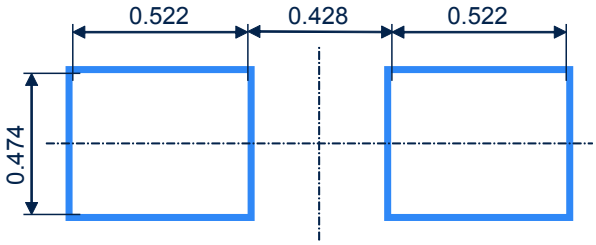


Note: Solder mask defined (SMD) recommended.

3.2 Stencil opening design

Stencil opening thickness: 75 µm / 3 mils

Figure 23. **Stencil opening recommendations**



3.3 Solder paste

1. Halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Tack force high enough to resist component displacement during PCB movement.
4. Particles size 20-38 µm per IPCJ STD-005.

3.4 Placement

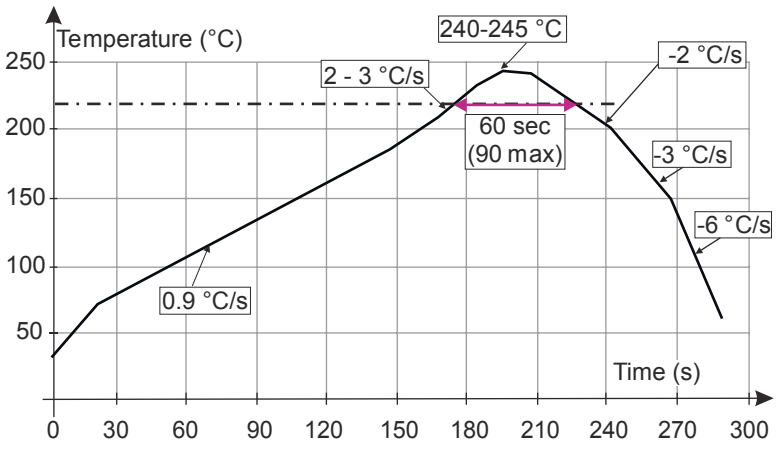
1. It is recommended to use leads recognition instead of package outline for accurate placement on footprint with adequate resolution tool.
2. Tolerance of ±50 µm (25% offset allowed on the smallest dimension of the smallest pad) is recommended.
3. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
4. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. Any via around or inside the footprint area must be closed to avoid solderpaste migration in the via.
2. Position and dimensions of the tracks should be well balanced. A symmetrical layout is recommended to prevent assembly troubles.

3.6 Reflow profile

Figure 24. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. O_2 rate inside the oven must be below 500 ppm. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 25. **Ordering information scheme**

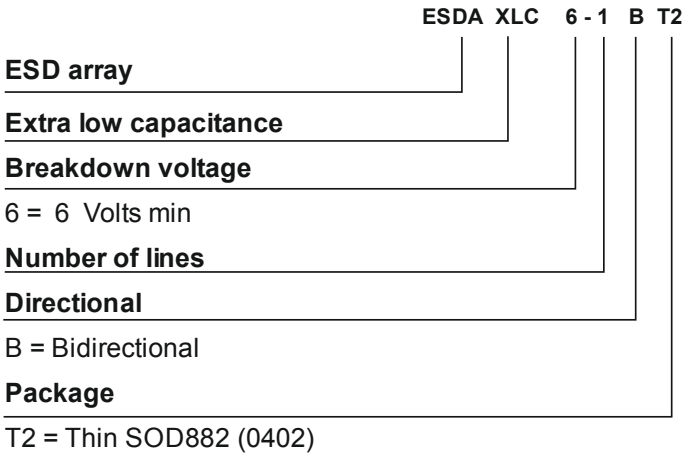


Table 5. **Ordering information**

Order code	Marking[1]	Package	Weight	Base qty.	Delivery mode
ESDAXLC6-1BT2	T	SOD882T (0402)	0.80 mg	12000	Tape and reel

1. *The marking can be rotated by multiples of 90° to differentiate assembly location*

Revision history

Table 6. **Document revision history**

Date	Version	Changes
04-Sep-2012	1	Initial release.
12-Aug-2013	2	Updated Figure 4, Figure 5, Figure 6, Figure 11 and Table 4.
10-May-2021	3	Updated SOD882T (0402) package information. Minor text changes.

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