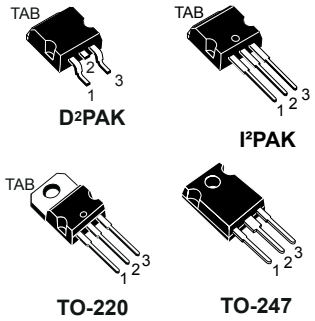
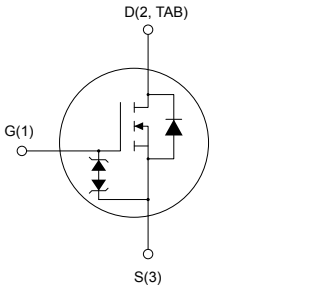
STB24N60M2, STI24N60M2
STP24N60M2, STW24N60M2

Datasheet

N-channel 600 V, 168 mΩ typ., 18 A MDmesh M2 Power MOSFET in a D²PAK, I²PAK, TO-220 and TO-247 packages





Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB24N60M2	600 V	190 mΩ	18 A
STI24N60M2			
STP24N60M2			
STW24N60M2			

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the MDmesh M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high-efficiency converters

Product status links
STB24N60M2
STI24N60M2
STP24N60M2
STW24N60M2

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	18	A
I_D	Drain current (continuous) at T_C = 100 °C	12	A
I_{DM}(1)	Drain current (pulsed)	72	A
P_{TOT}	Total power dissipation at T_C = 25 °C	150	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 18 A, di/dt ≤ 400 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
3. *V_{DS} = 480 V.*

Table 2. Thermal data

Symbol	Parameter	Value				Unit
		D^2PAK	I^2PAK	TO-220	TO-247	
R_{thJC}	Thermal resistance, junction-to-case	0.83				°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	30(1)	62.5		50	°C/W

1. *When mounted on a standard 1 inch^2 area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	3.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	180	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	600	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)	-	-	100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V	-	-	±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 9 A	-	168	190	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1060	-	pF
C_{oss}	Output capacitance		-	55	-	pF
C_{rss}	Reverse transfer capacitance		-	2.2	-	pF
$C_{oss\ eq.}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	258	-	pF
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 17 A, V_{GS} = 0 to 10 V (see the Figure 16. Test circuit for gate charge behavior)	-	29	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	12	-	nC
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7	-	Ω

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 9 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	14	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
t_f	Fall time		-	15	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	18	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	72	A
V_{SD}(2)	Forward on voltage	I_{SD} = 18 A, V_{GS} = 0 V	-	-	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs, V_{DD} = 60 V (see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	332	-	ns
Q_{rr}	Reverse recovery charge		-	4	-	µC
I_{RRM}	Reverse recovery current		-	24	-	A
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	450	-	ns
Q_{rr}	Reverse recovery charge		-	5.5	-	µC
I_{RRM}	Reverse recovery current		-	25	-	A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for D²PAK, I²PAK and TO-220

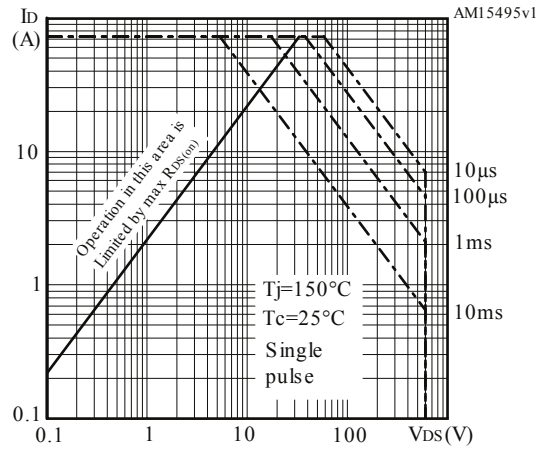


Figure 2. Normalized transient thermal impedance for D²PAK, I²PAK and TO-220

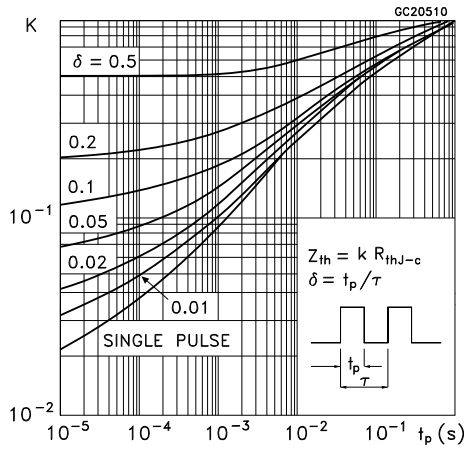


Figure 3. Safe operating area for TO-247

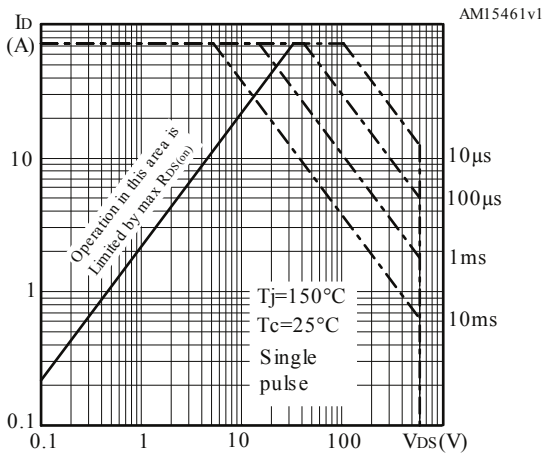


Figure 4. Normalized transient thermal impedance for TO-247

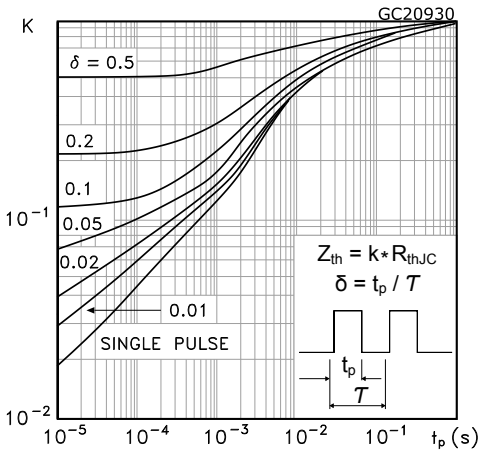


Figure 5. Typical output characteristics

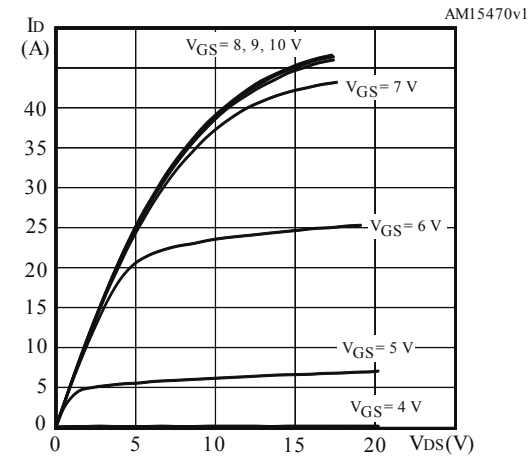


Figure 6. Typical transfer characteristics

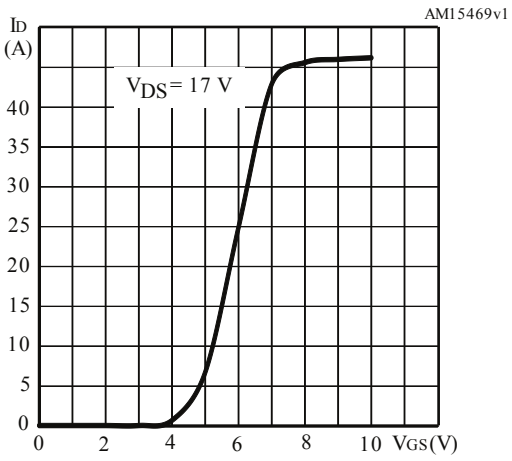


Figure 7. Typical gate charge characteristics

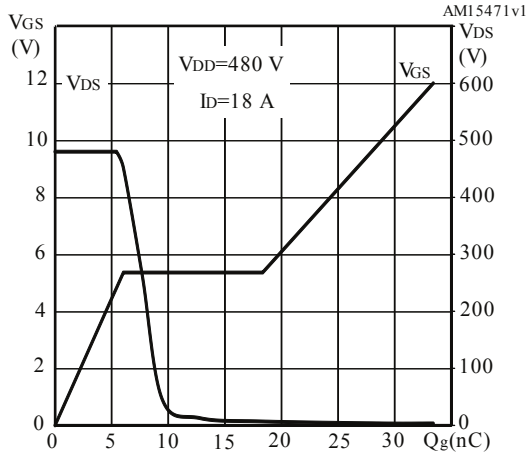


Figure 8. Typical capacitance characteristics

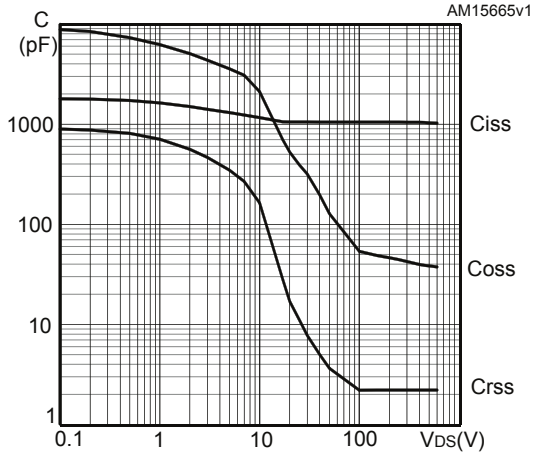


Figure 9. Typical drain-source on-resistance

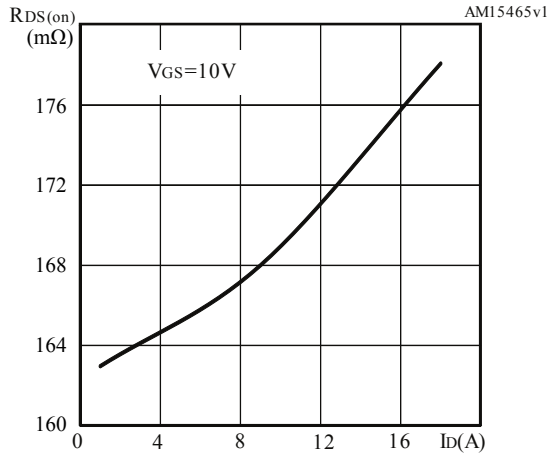


Figure 10. Normalized breakdown voltage vs temperature

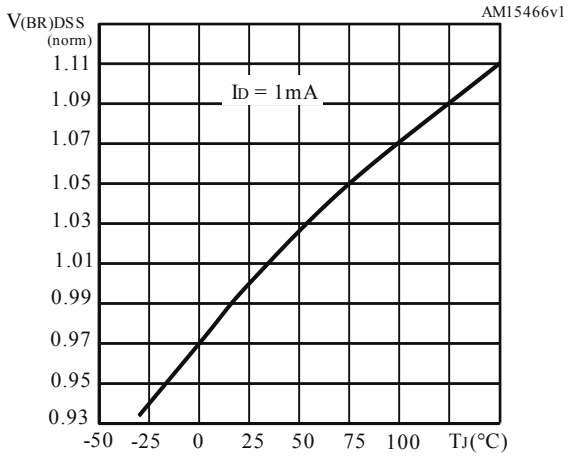


Figure 11. Normalized gate threshold vs temperature

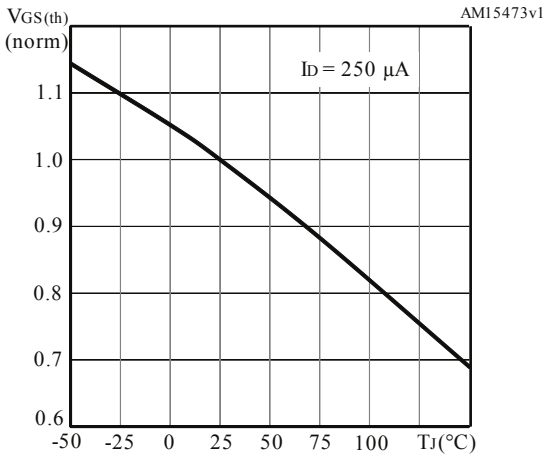


Figure 12. Normalized on-resistance vs temperature

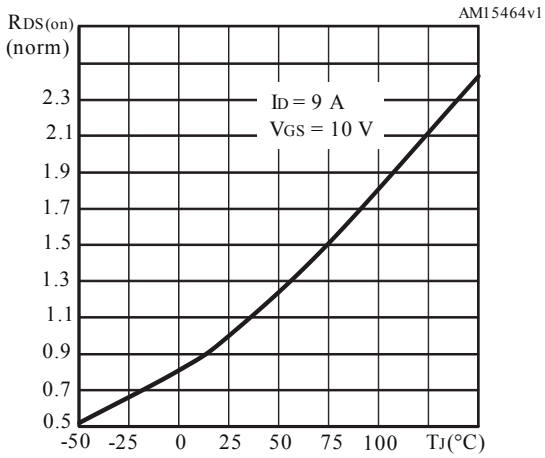


Figure 13. Typical reverse diode forward characteristics

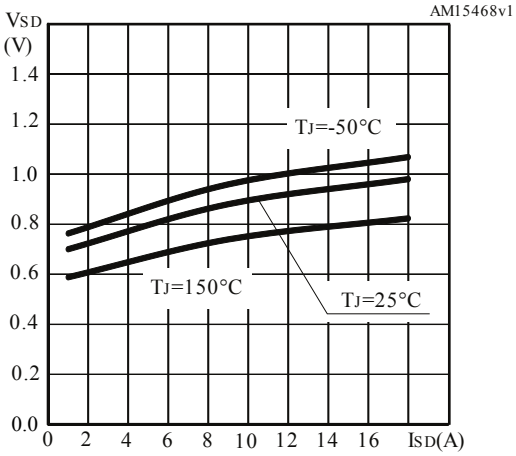
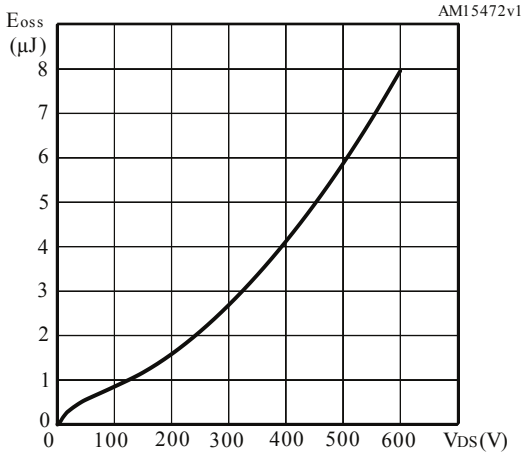
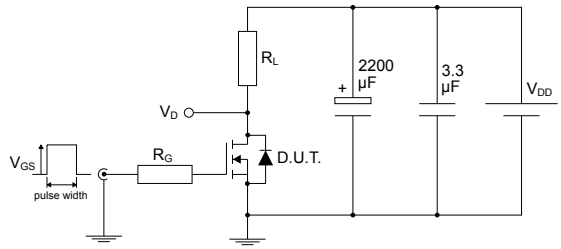


Figure 14. Output capacitance stored energy



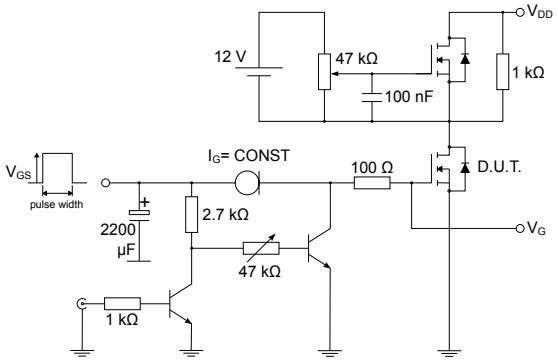
3 Test circuits

Figure 15. Test circuit for resistive load switching times



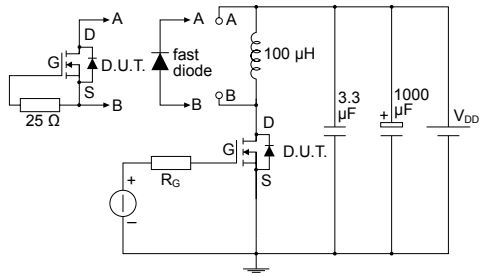
AM01468v1

Figure 16. Test circuit for gate charge behavior



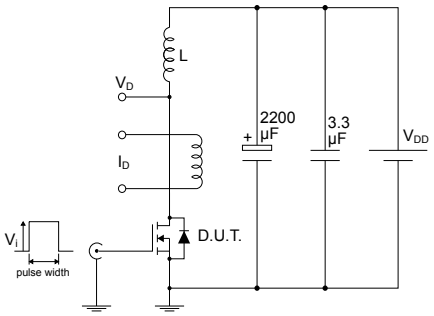
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Figure 17. Test circuit for inductive load switching and diode recovery times



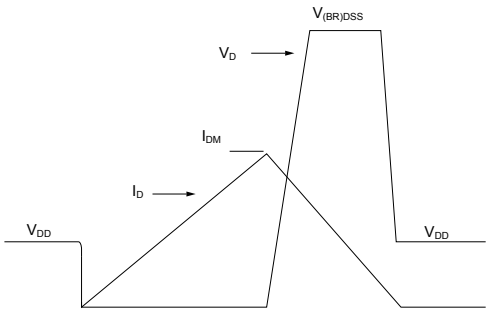
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Figure 18. Unclamped inductive load test circuit



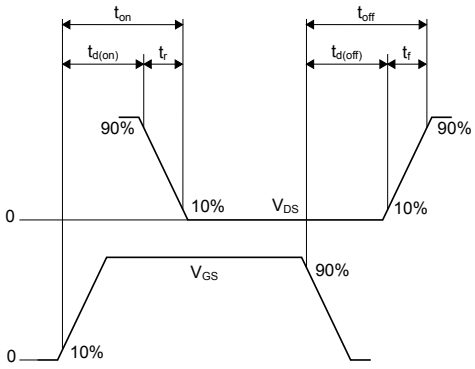
AM01471v1

Figure 19. Unclamped inductive waveform



AM01472v1

Figure 20. Switching time waveform



AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 21. **D²PAK (TO-263) type A package outline**

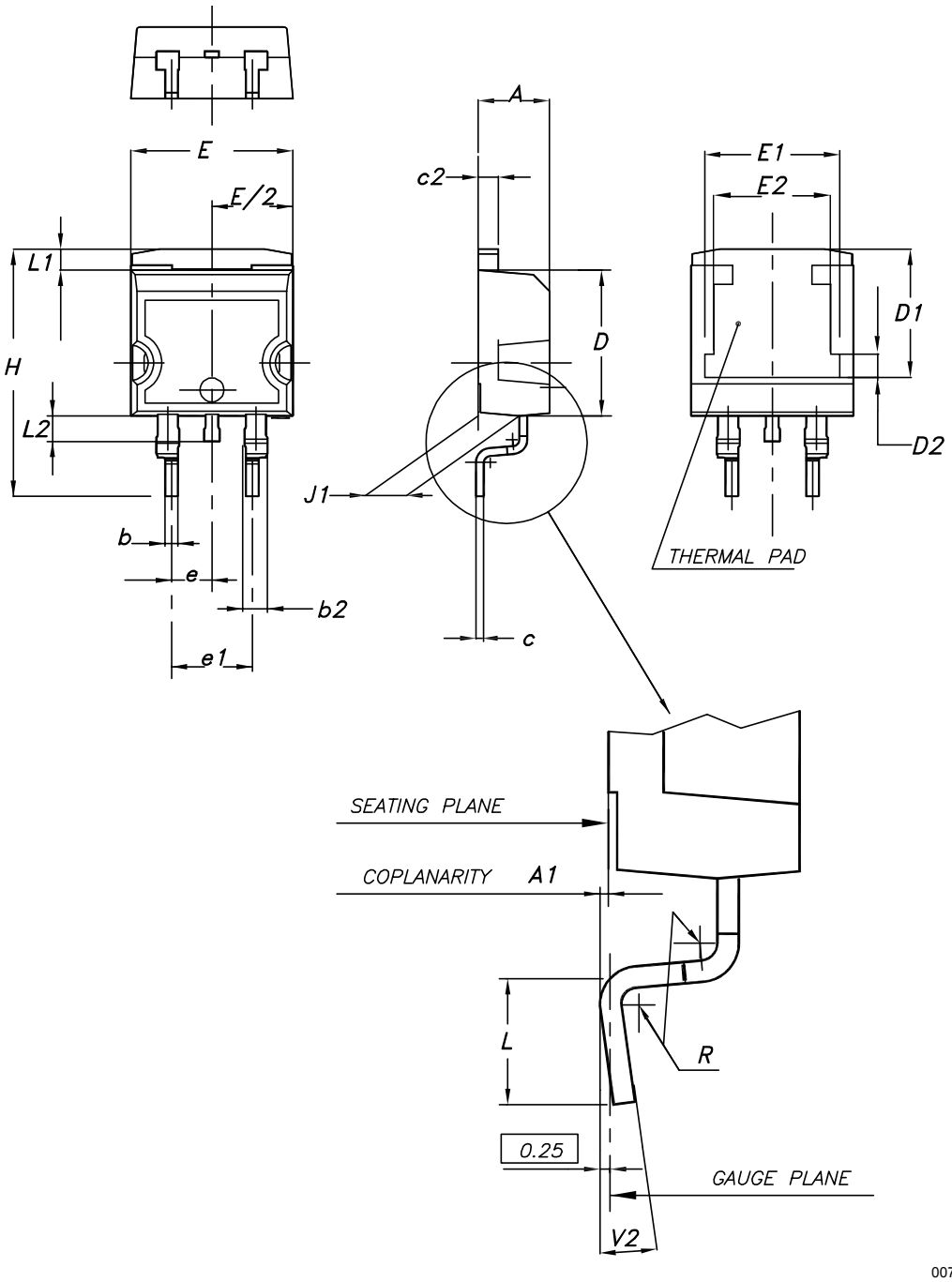
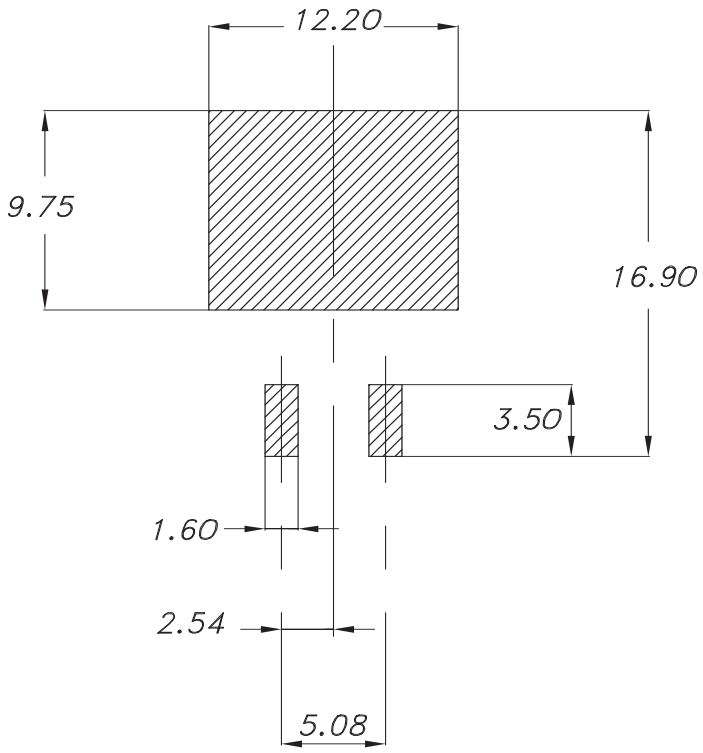


Table 8. D²PAK (TO-263) type A package mechanical data

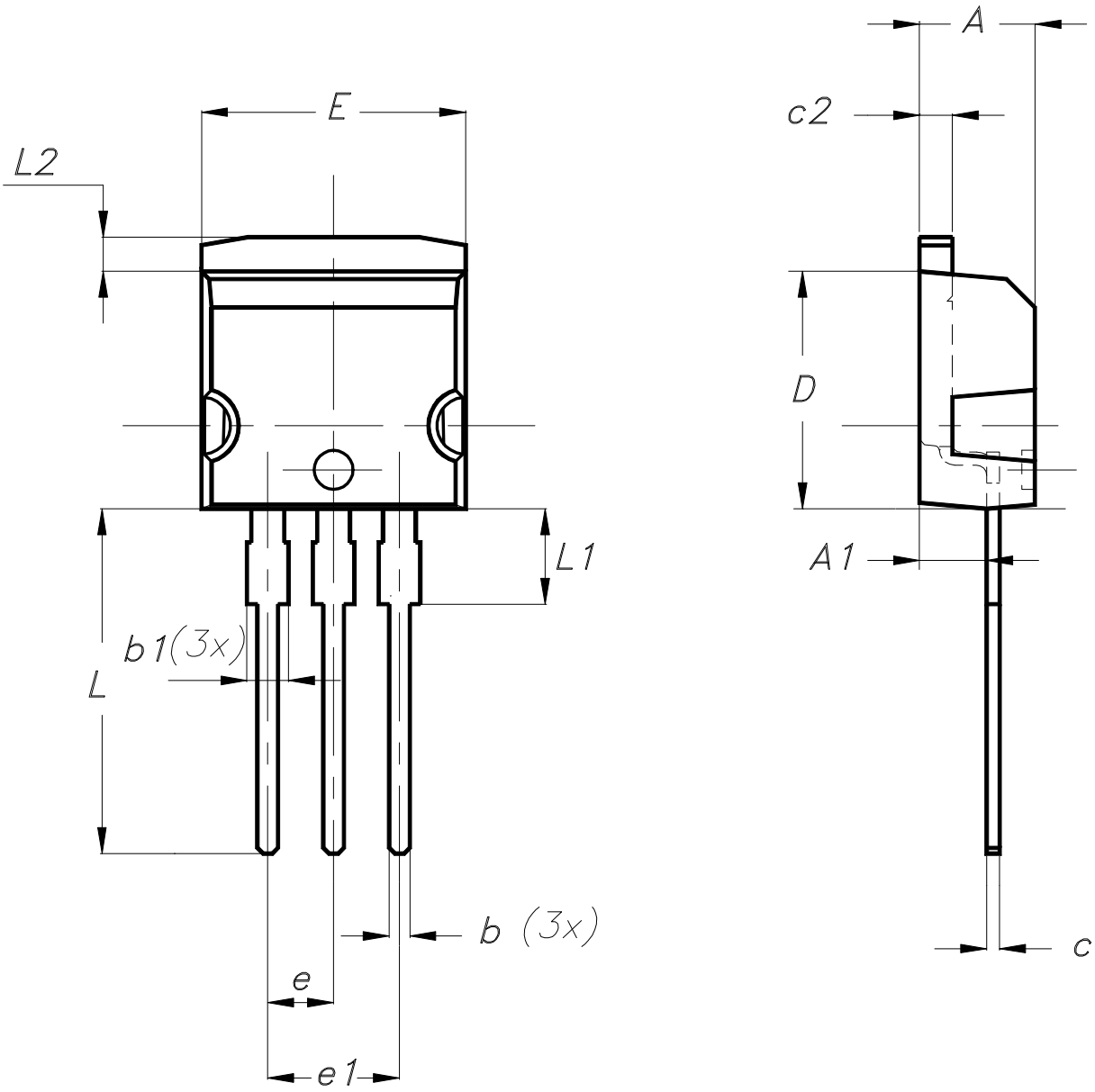
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 22. D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 I²PAK package information

Figure 23. I²PAK package outline



0004982_Rev_10

Table 9. I²PAK package mechanical data

Dim.	mm	
	Min.	Max.
A	4.40	4.60
A1	2.40	2.72
b	0.61	0.88
b1	1.14	1.70
c	0.49	0.70
c2	1.23	1.32
D	8.95	9.35
e	2.40	2.70
e1	4.95	5.15
E	10.00	10.40
L	13.00	14.00
L1	3.50	3.93
L2	1.27	1.40

4.3 TO-220 type A package information

Figure 24. **TO-220 type A package outline**

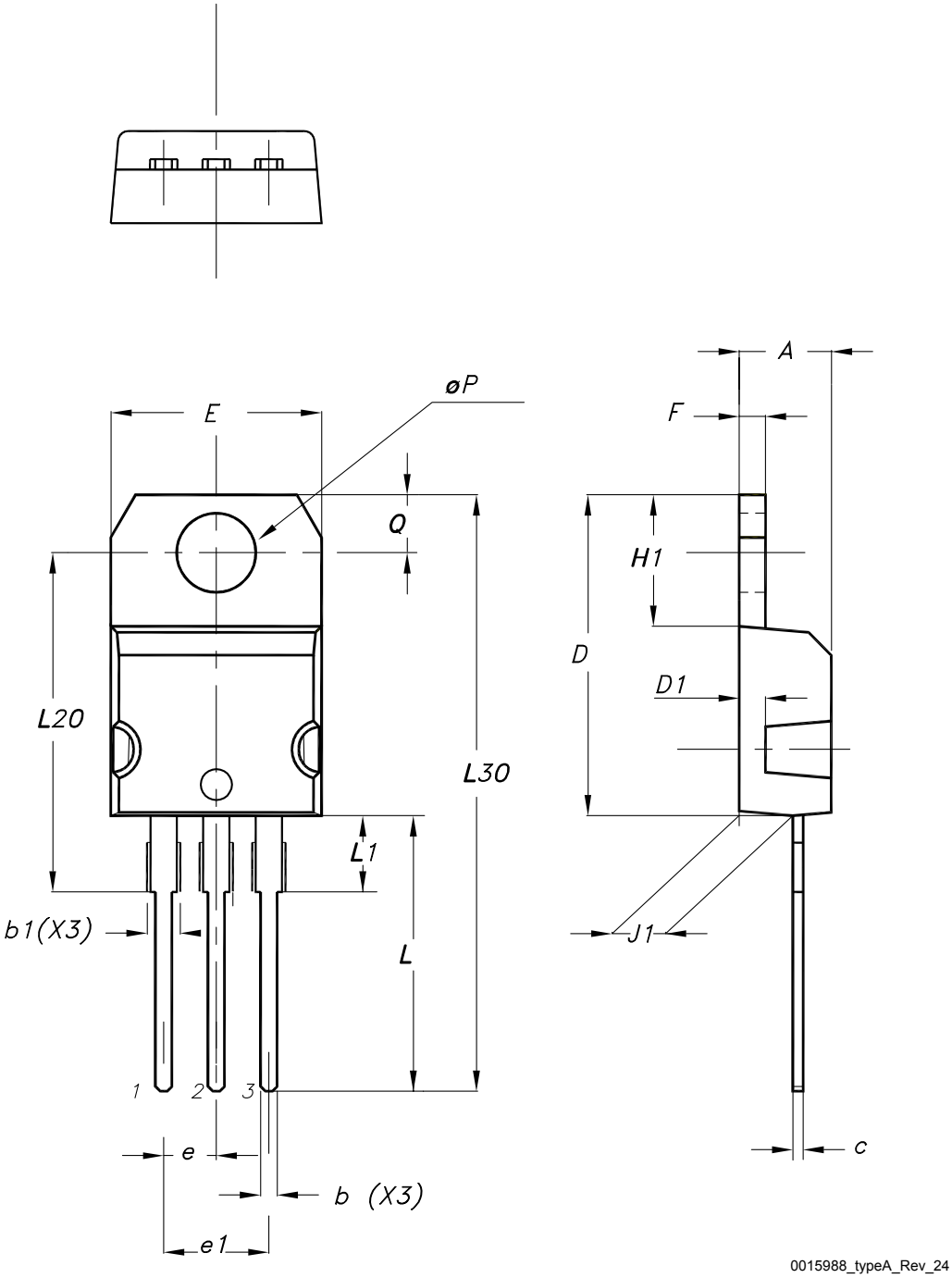
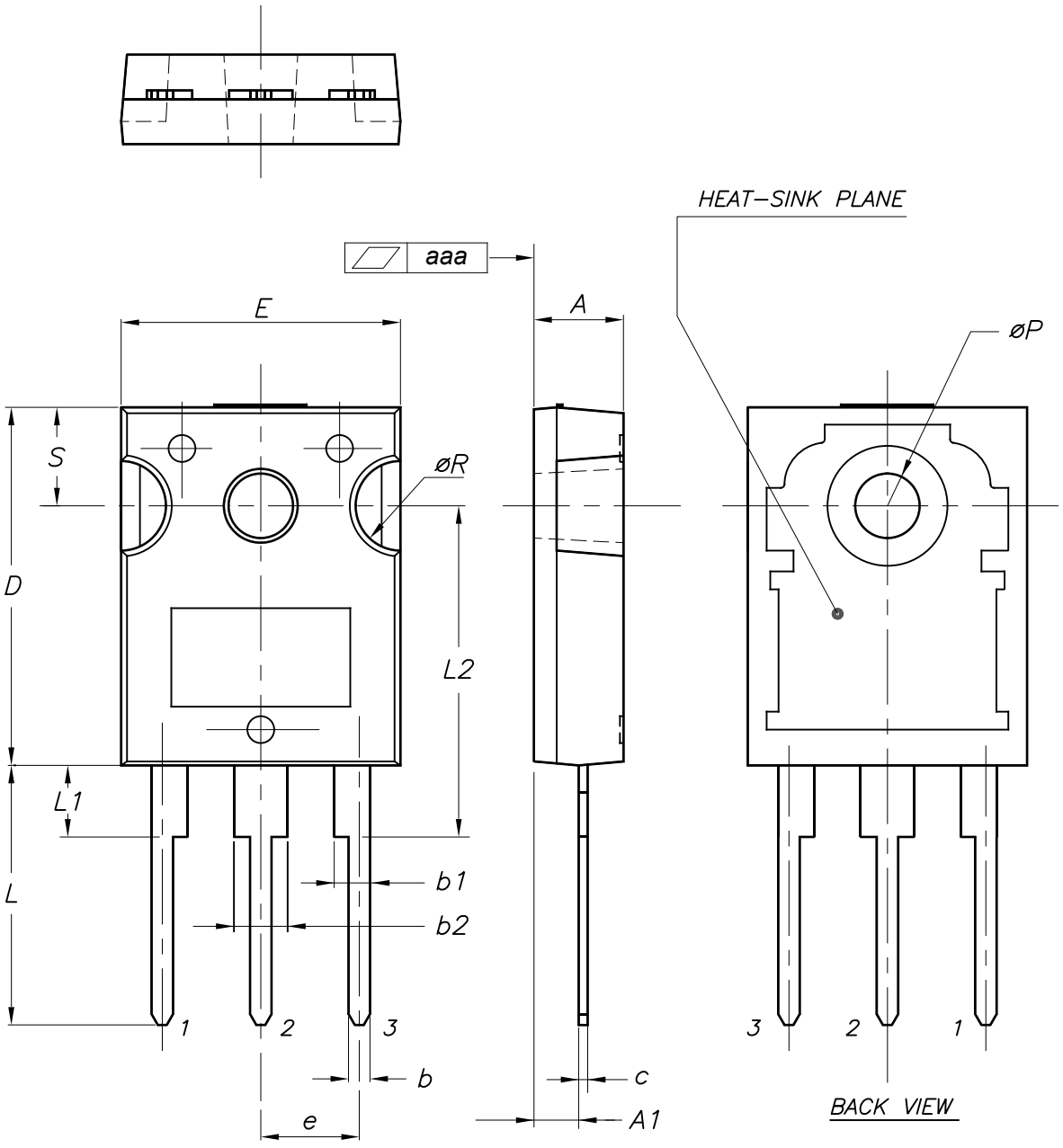


Table 10. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.4 TO-247 package information

Figure 25. **TO-247 package outline**



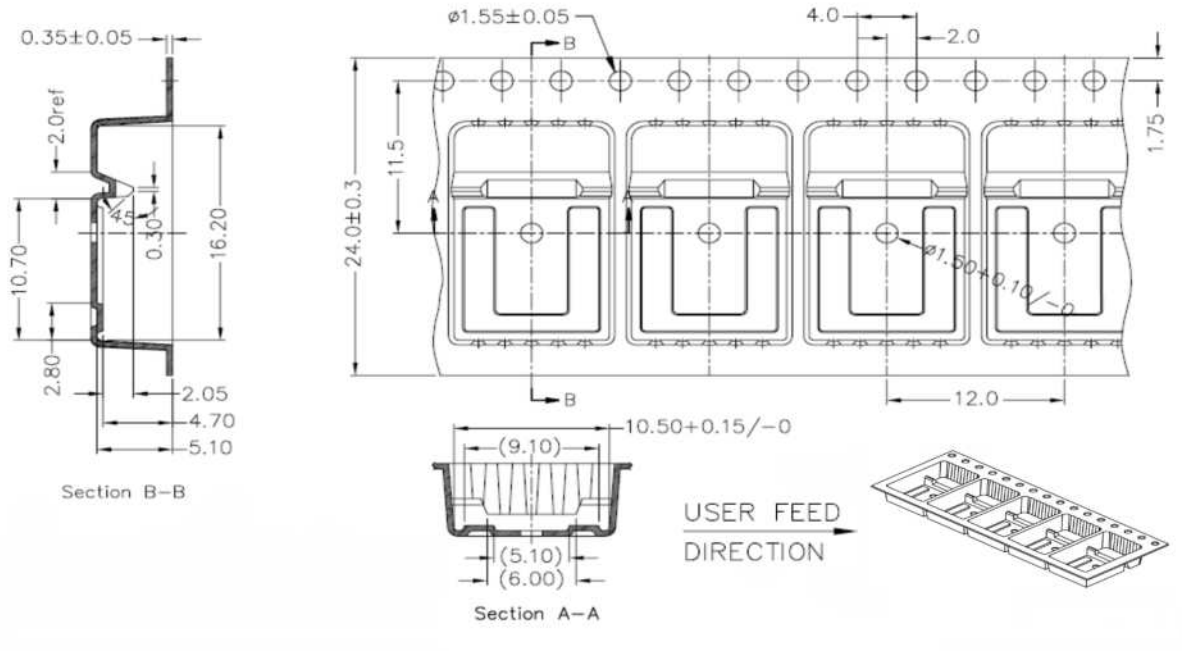
0075325_10

Table 11. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10

4.5 D²PAK packing information

Figure 26. **D²PAK tape drawing (dimensions are in mm)**



DM01095771_2

5 Ordering information

Table 12. **Order codes**

Order codes	Marking	Package	Packing
STB24N60M2	24N60M2	D²PAK	Tape and reel
STI24N60M2		I²PAK	Tube
STP24N60M2		TO-220	
STW24N60M2		TO-247	

Revision history

Table 13. **Document revision history**

Date	Revision	Changes
10-Dec-2012	1	First release.
20-Dec-2012	2	Added MOSFET dv/dt ruggedness in *Table 2: Absolute maximum ratings*.
14-Jan-2013	3	Modified: *Figure 16*, *17*, and *18*.
28-May-2013	4	Minor text changes. Updated: *Table 7*. Updated: *Table 11* and *Figure 25*.
28-Feb-2014	5	Minor text changes. Modified: title of *Figure 15*. Modified: Figure *16*, *17*, *18* and *19*.
12-Aug-2025	6	Updated Section 4: Package information. Minor text changes.

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