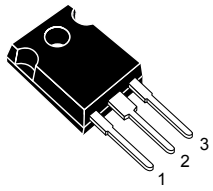
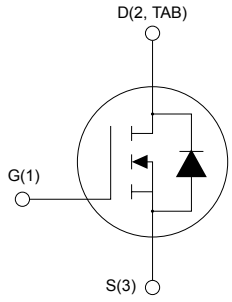
STW45N65M5

Datasheet

N-channel 650 V, 68 mΩ typ., 35 A MDmesh M5 Power MOSFET in a TO-247 package



TO-247



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STW45N65M5	650 V	78 mΩ	35 A

- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Extremely low $R_{DS(on)}$
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Product status link
STW45N65M5

Product summary	
Order code	STW45N65M5
Marking	45N65M5
Package	TO-247
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	35	A
	Drain current (continuous) at T_C = 100 °C	22	
I_{DM}(1)	Drain current (pulsed)	140	A
P_{TOT}	Total power dissipation at T_C = 25 °C	210	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range	150	

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 35 A, di/dt ≤ 400 A/µs; V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
3. *V_{DD} ≤ 520 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.6	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	50	

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	9	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	810	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)	-	-	100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V	-	-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 17.5 A	-	68	78	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	3470	-	pF
C_{oss}	Output capacitance		-	82	-	pF
C_{rss}	Reverse transfer capacitance		-	7	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	280	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	79	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	2	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 17.5 A, V_{GS} = 0 to 10 V (see the Figure 15. Test circuit for gate charge behavior)	-	82	-	nC
Q_{gs}	Gate-source charge		-	18.5	-	nC
Q_{gd}	Gate-drain charge		-	35	-	nC

1. *$C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*
2. *$C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 23 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	79.5	-	ns
$t_{r(v)}$	Voltage rise time		-	11	-	ns
$t_{f(i)}$	Current fall time		-	9.3	-	ns
$t_{c(off)}$	Crossing time		-	16	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	35	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	140	A
V_{SD}(2)	Forward on voltage	I_{SD} = 35 A, V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 35 A, di/dt = 100 A/µs,	-	392	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	7.4	-	µC
I_{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	38	-	A
t_{rr}	Reverse recovery time	I_{SD} = 35 A, di/dt = 100 A/µs,	-	468	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_J = 150 °C	-	9.7	-	µC
I_{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	42	-	A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics curves

Figure 1. Safe operating area

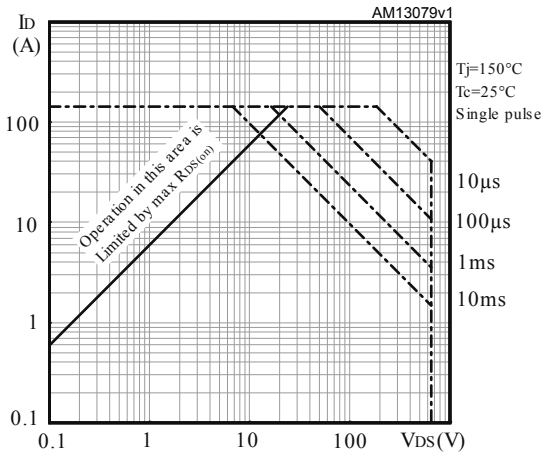


Figure 2. Normalized transient thermal impedance

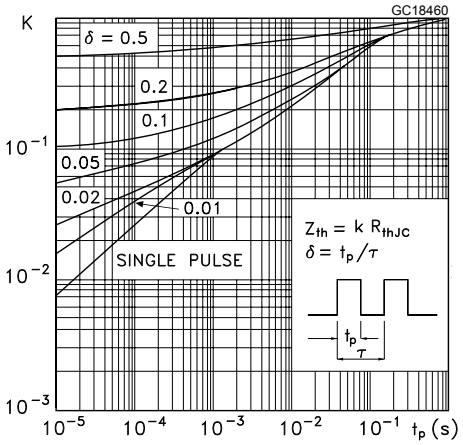


Figure 3. Typical output characteristics

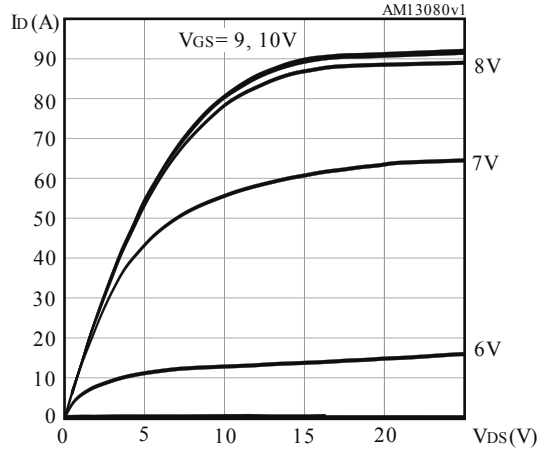


Figure 4. Typical transfer characteristics

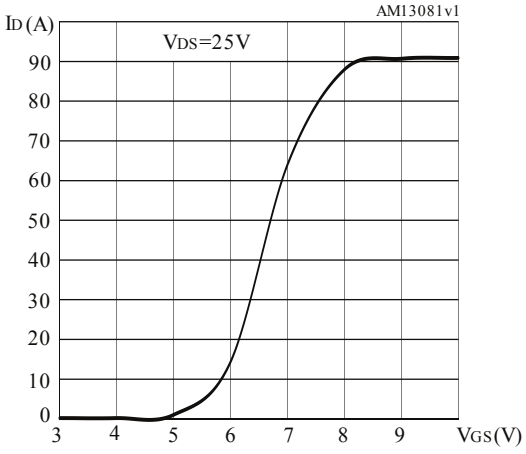


Figure 5. Typical gate charge characteristics

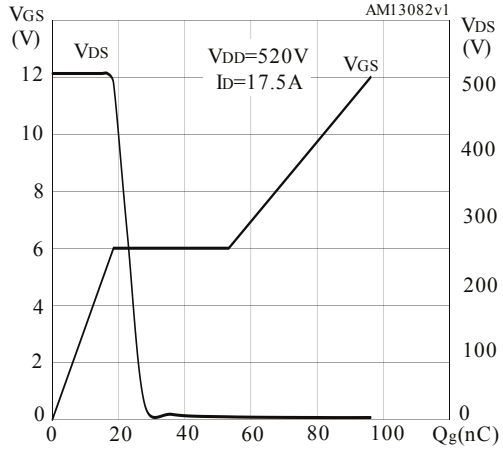


Figure 6. Typical drain-source on-resistance

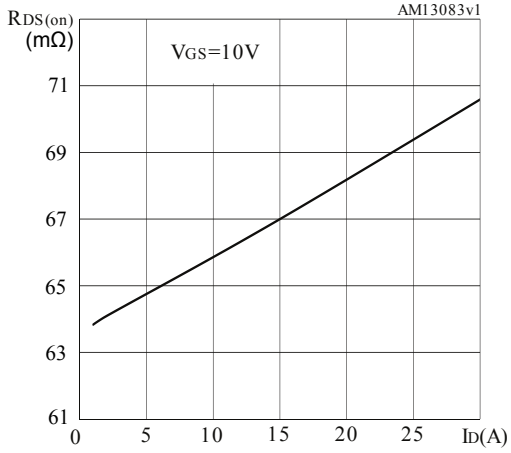


Figure 7. Typical capacitance characteristics

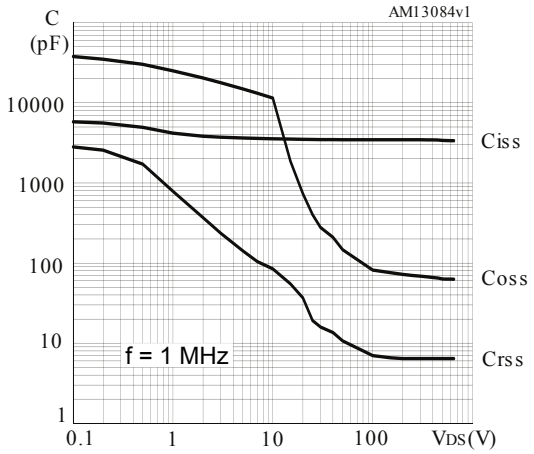


Figure 8. Typical output capacitance stored energy

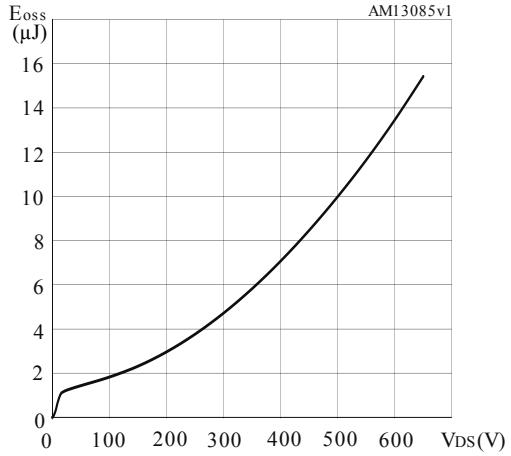


Figure 9. Normalized gate threshold vs temperature

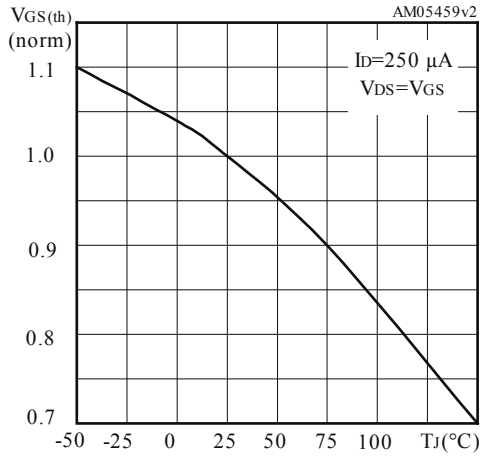


Figure 10. Normalized on-resistance vs temperature

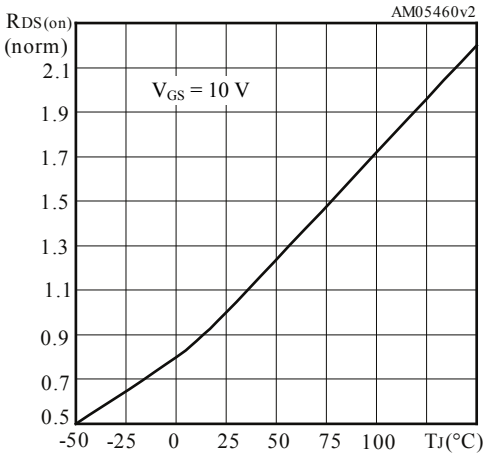


Figure 11. Typical reverse diode forward characteristics

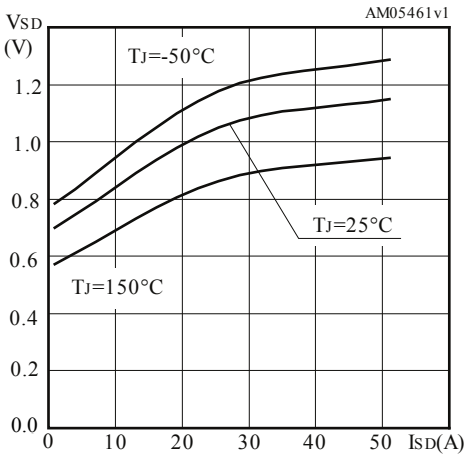


Figure 12. Normalized breakdown voltage vs temperature

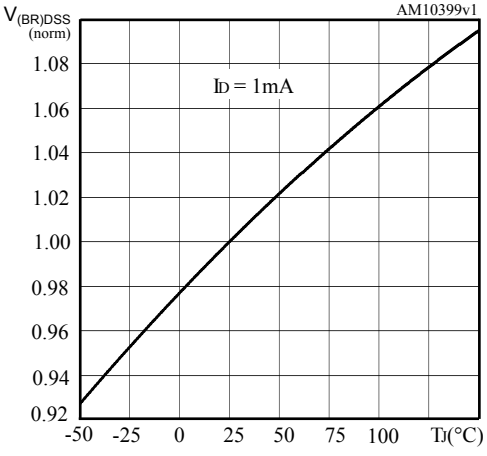
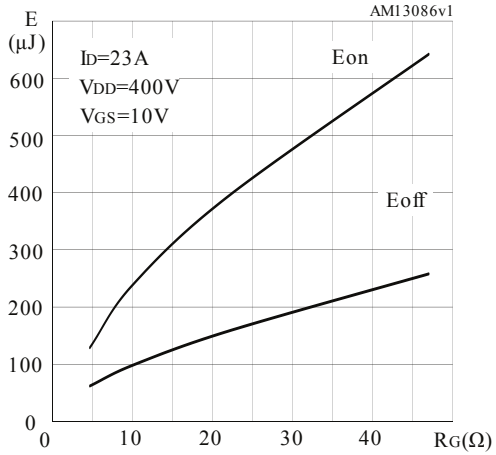


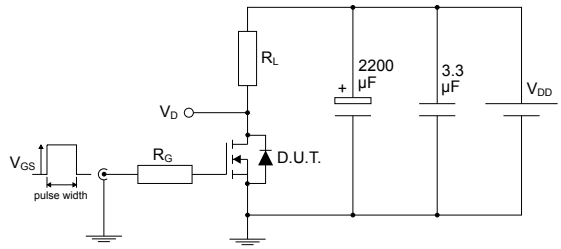
Figure 13. Typical switching energy vs gate resistance



Note: E_{on} including reverse recovery of a SiC diode.

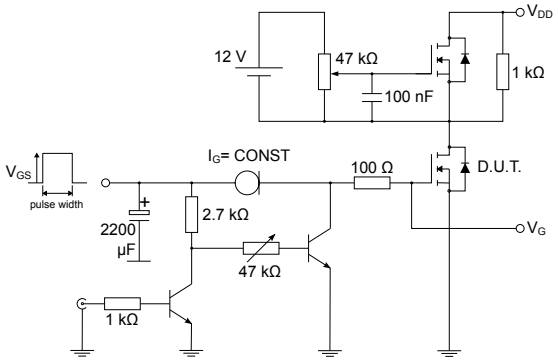
3 Test circuits

Figure 14. Test circuit for resistive load switching times



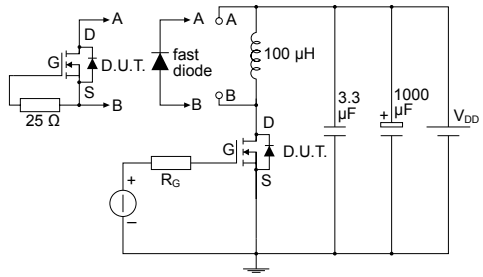
AM01468v1

Figure 15. Test circuit for gate charge behavior



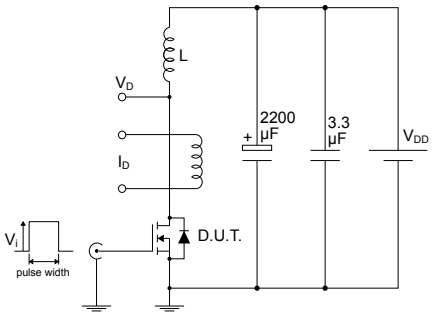
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Figure 16. Test circuit for inductive load switching and diode recovery times



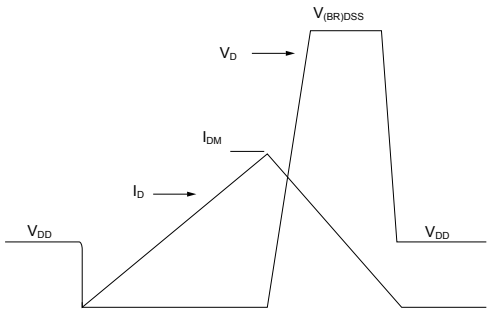
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Figure 17. Unclamped inductive load test circuit



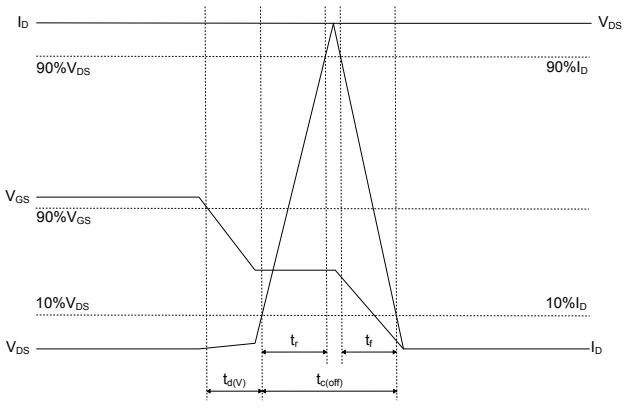
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Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



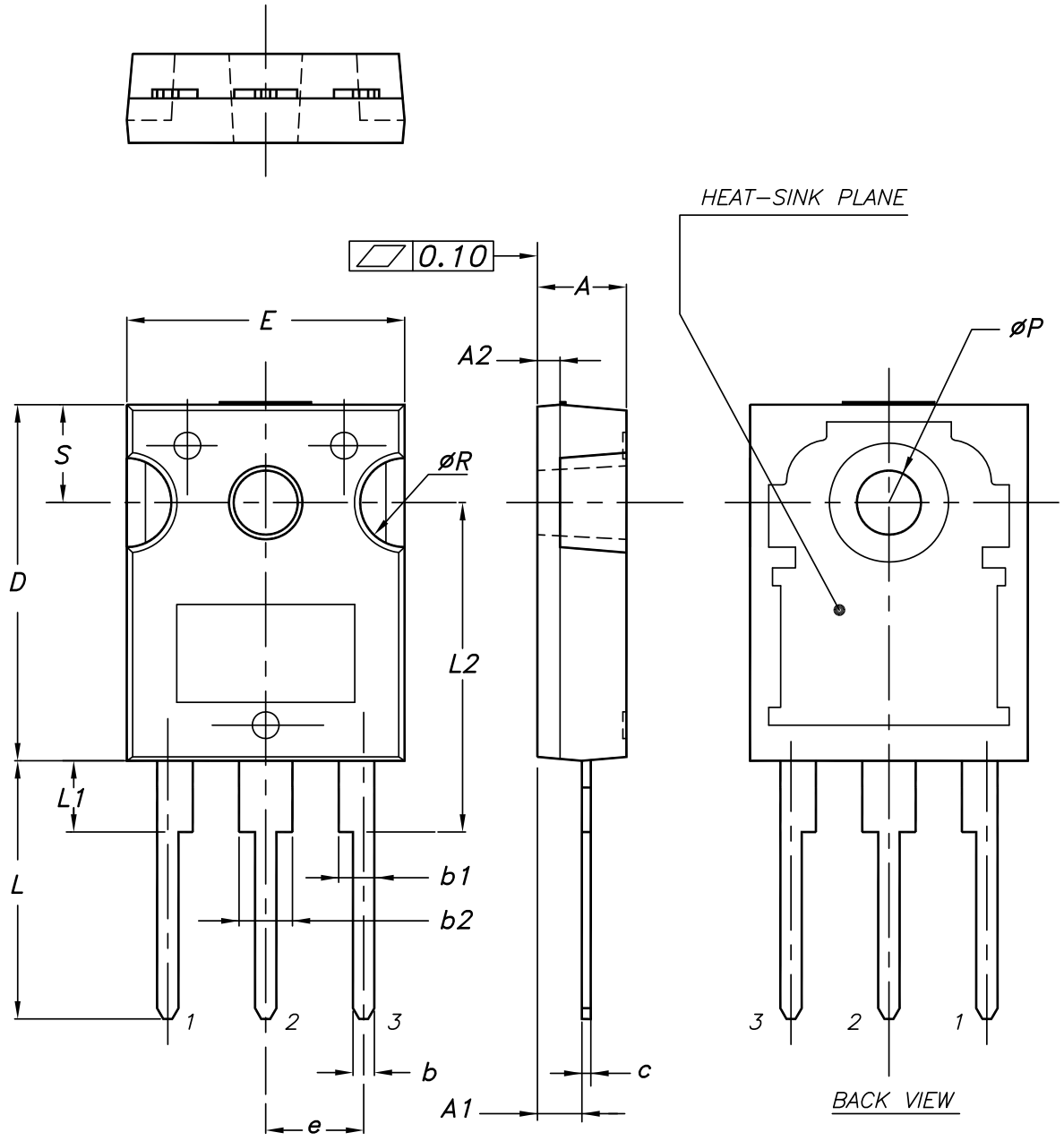
AM05540v2

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 20. **TO-247 package outline**



0075325_11

Table 8. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
A2		1.27	
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
11-Dec-2012	1	First release.
09-May-2014	2	Added: TO-3PF package. Added: dv/dt (MOSFET dv/dt ruggedness) parameter and V_{ISO}. Modified: *Figure 6* and *7*. Minor text changes.
28-Nov-2025	3	Removed order code STFW45N65M5 and STWA45N65M5. Updated Section 4: Package information. Minor text changes.

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