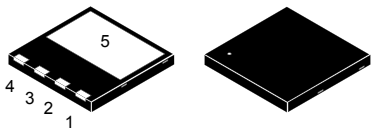
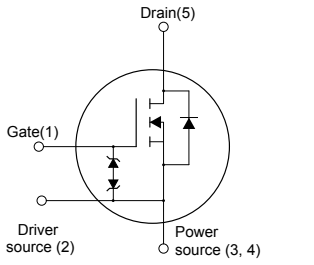
N-channel 600 V, 0.115 Ω typ., 22 A MDmesh M2 Power MOSFET in a PowerFLAT 8x8 HV package



PowerFLAT 8x8 HV



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$max	I_D
STL33N60M2	650 V	0.135 Ω	22 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters, resonant converters

Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Product status link
STL33N60M2

Product summary	
Order code	STL33N60M2
Marking	33N60M2
Package	PowerFLAT™ 8x8 HV
Packing	Tape & reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	22	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	13.8	A
I_{DM} (2)	Drain current (pulsed)	88	A
P_{TOT}	Total power dissipation at T_C = 25 °C	150	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	450	mJ
dv/dt (3)	Peak diode recovery voltage slope	15	V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range	150	°C

1. *The value is limited by package.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 22 A, di/dt ≤ 400 A/µs, $V_{DS(\ peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V.*
4. *V_{DS} ≤ 480 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.83	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	45	°C/W

1. *When mounted on FR-4 board of 1 inch², 2oz Cu.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C =125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 11 A		0.115	0.135	Ω

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1781	-	pF
C_{oss}	Output capacitance		-	85	-	pF
C_{rss}	Reverse transfer capacitance		-	2.5	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	135	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	5.2	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 26 A V_{GS} = 0 to 10 V (see Figure 15. Gate charge test circuit)	-	45.5	-	nC
Q_{gs}	Gate-source charge		-	9.9	-	nC
Q_{gd}	Gate-drain charge		-	18.5	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% V_{DSS}.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 13 A R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Switching times test circuit for resistive load and Figure 19. Switching time waveform)	-	16	-	ns
t_r	Rise time		-	9.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	109	-	ns
t_f	Fall time		-	9	-	ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		22	A
I_{SDM} (1)	Source-drain current (pulsed)		-		88	A
V_{SD} (2)	Forward on voltage	I_{SD} = 22 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 26 A, di/dt = 100 A/µs V_{DD} = 60 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	375		ns
Q_{rr}	Reverse recovery charge		-	5.6		µC
I_{RRM}	Reverse recovery current		-	30		A
t_{rr}	Reverse recovery time	I_{SD} = 26 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	478		ns
Q_{rr}	Reverse recovery charge		-	7.7		µC
I_{RRM}	Reverse recovery current		-	32.5		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

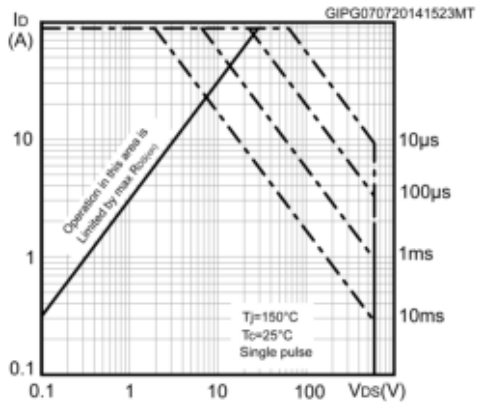


Figure 2. Thermal impedance

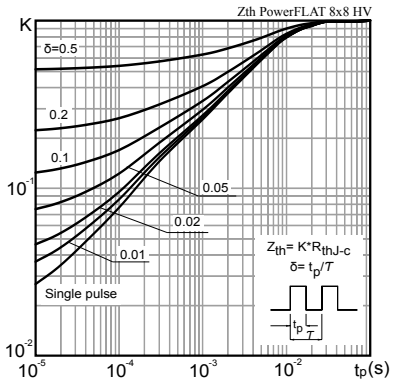


Figure 3. Output characteristics

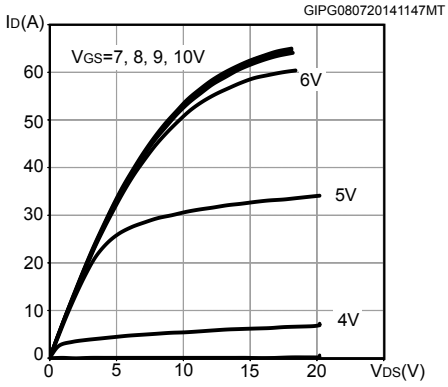


Figure 4. Transfer characteristics

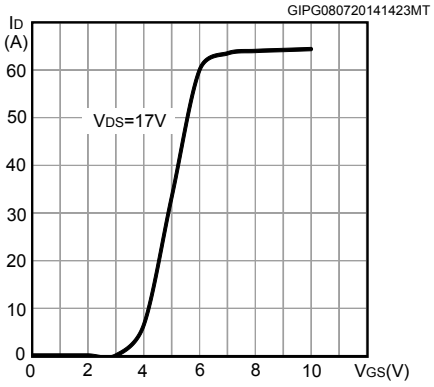


Figure 5. Gate charge vs gate-source voltage

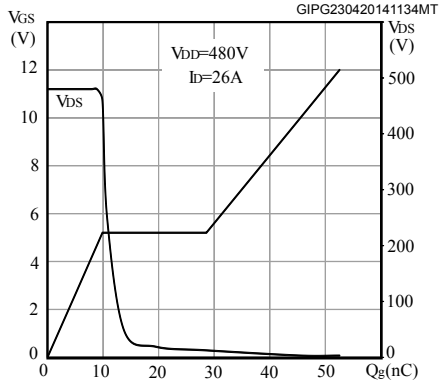


Figure 6. Static drain-source on-resistance

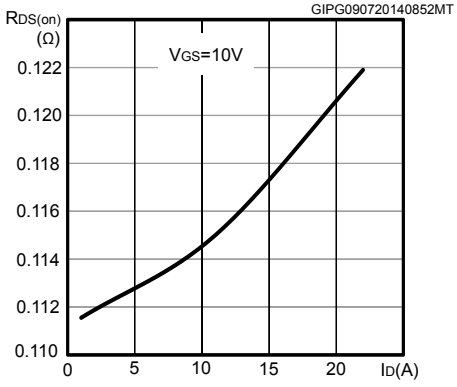


Figure 7. Capacitance variations

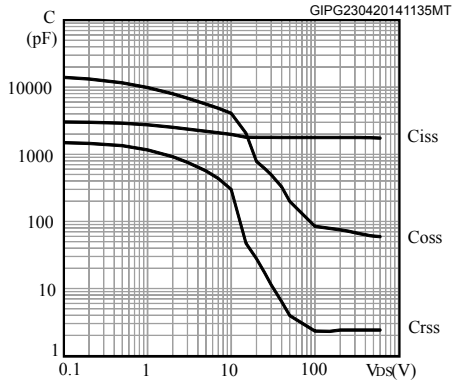


Figure 8. Normalized gate threshold voltage vs temperature

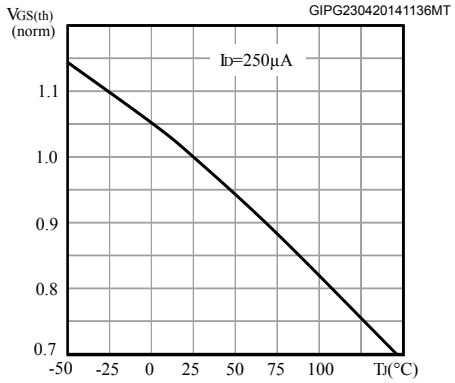


Figure 9. Normalized on-resistance vs temperature

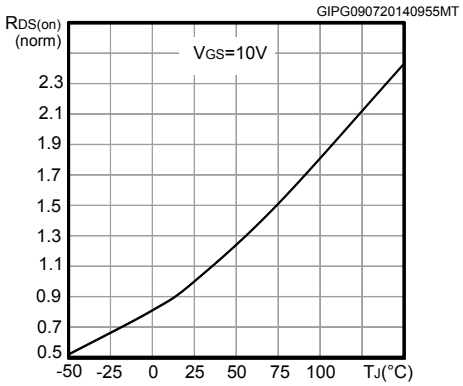


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

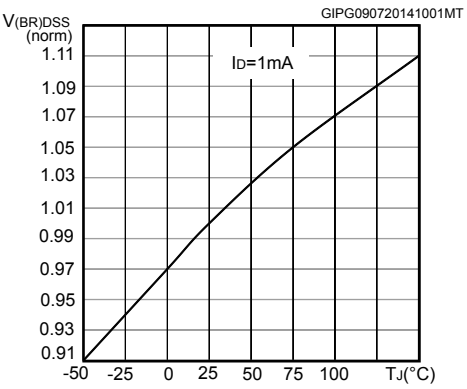


Figure 11. Source-drain diode forward characteristics

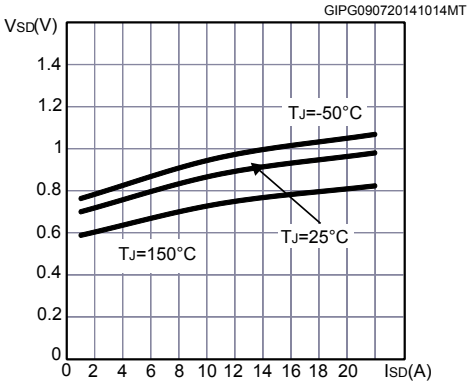


Figure 12. Output capacitance stored energy

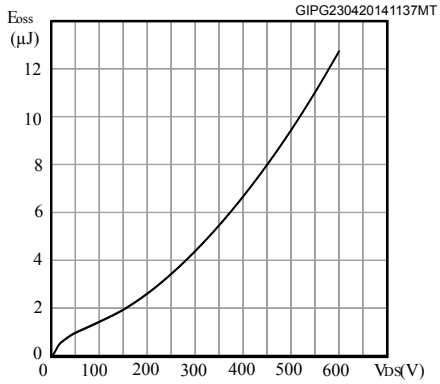
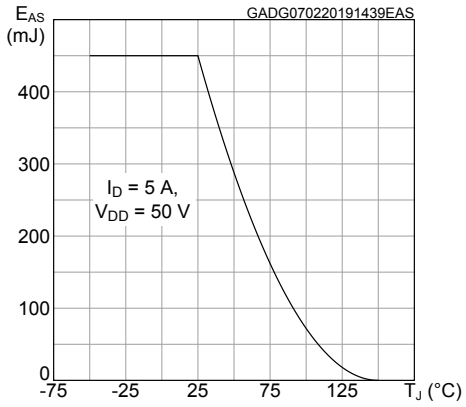


Figure 13. Maximum avalanche energy vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

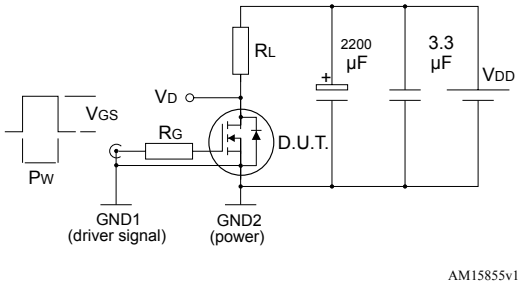


Figure 15. Gate charge test circuit

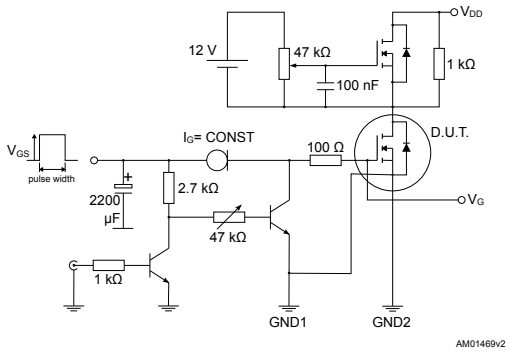


Figure 16. Test circuit for inductive load switching and diode recovery times

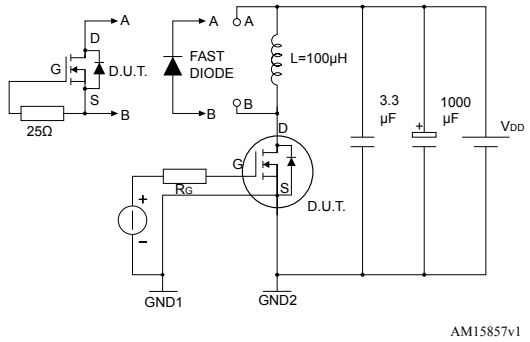


Figure 17. Unclamped inductive load test circuit

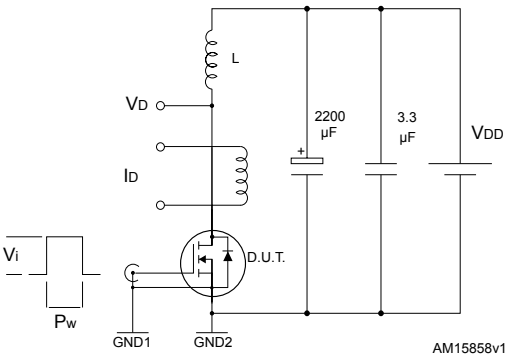


Figure 18. Unclamped inductive waveform

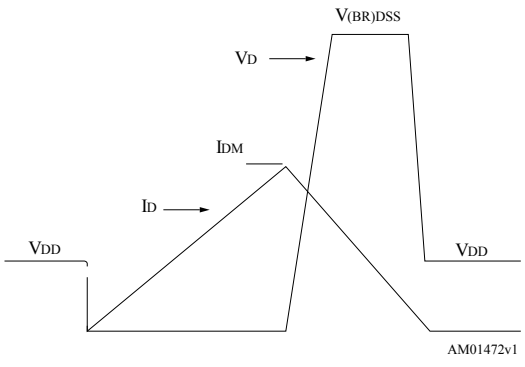
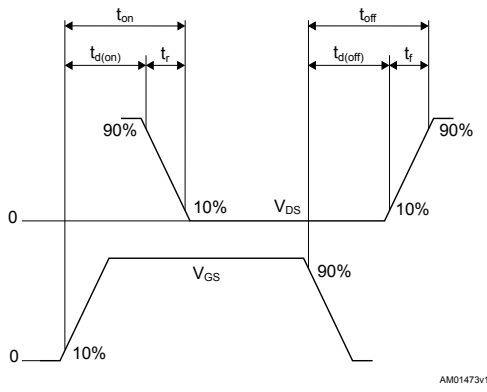


Figure 19. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 8x8 HV package information

Figure 20. PowerFLAT 8x8 HV package outline

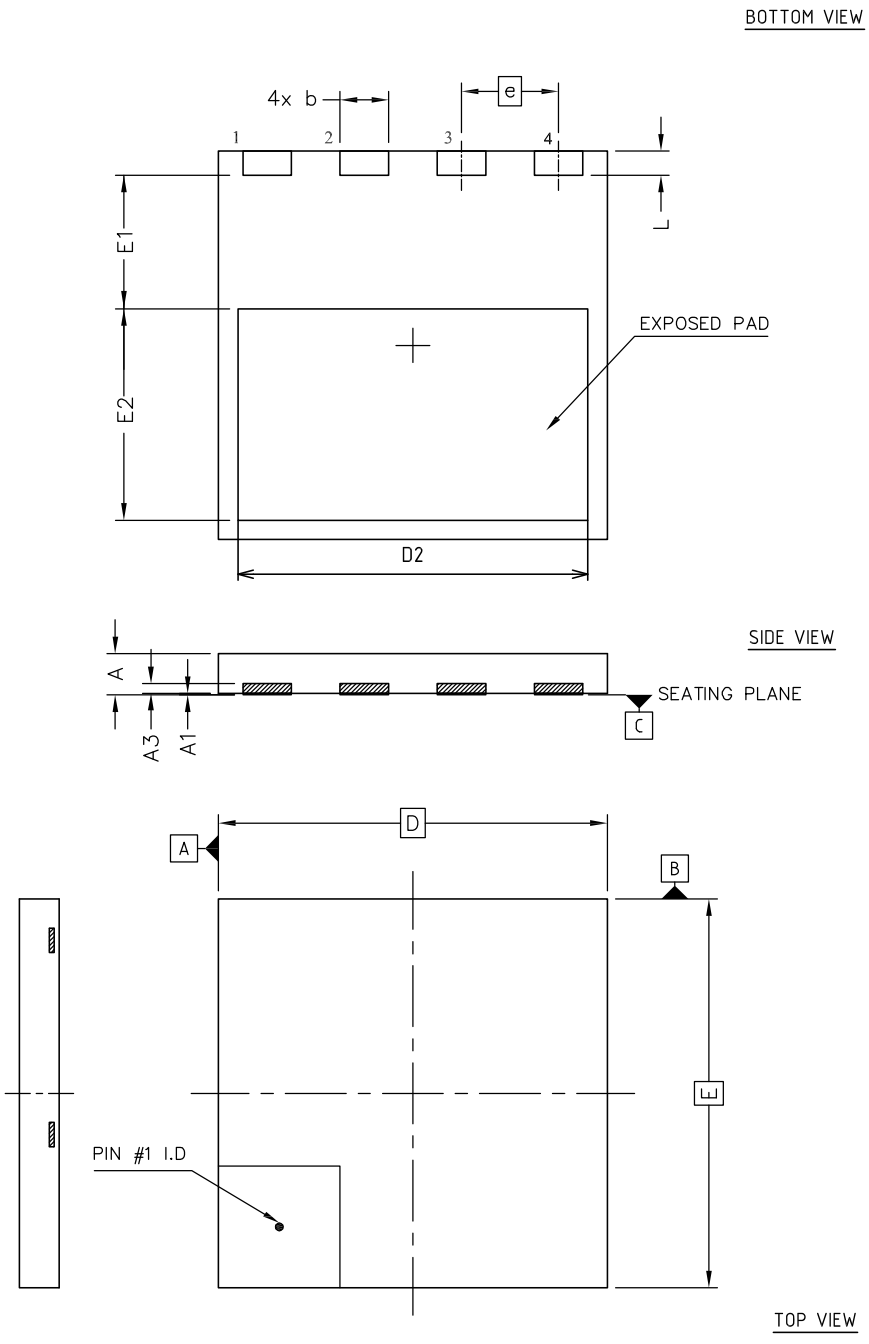
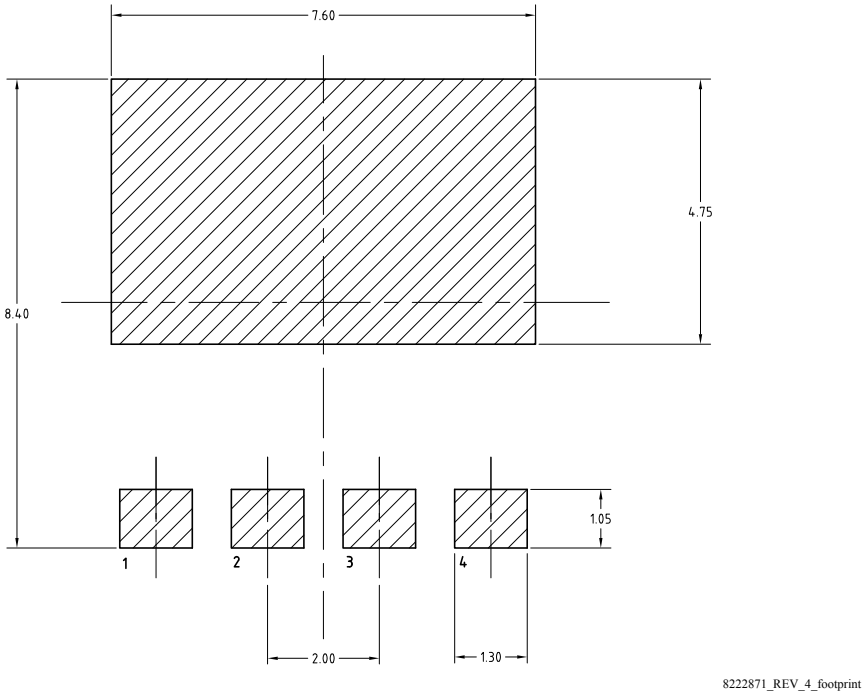


Table 7. PowerFLAT 8x8 HV mechanical data

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00 BSC	
L	0.40	0.50	0.60

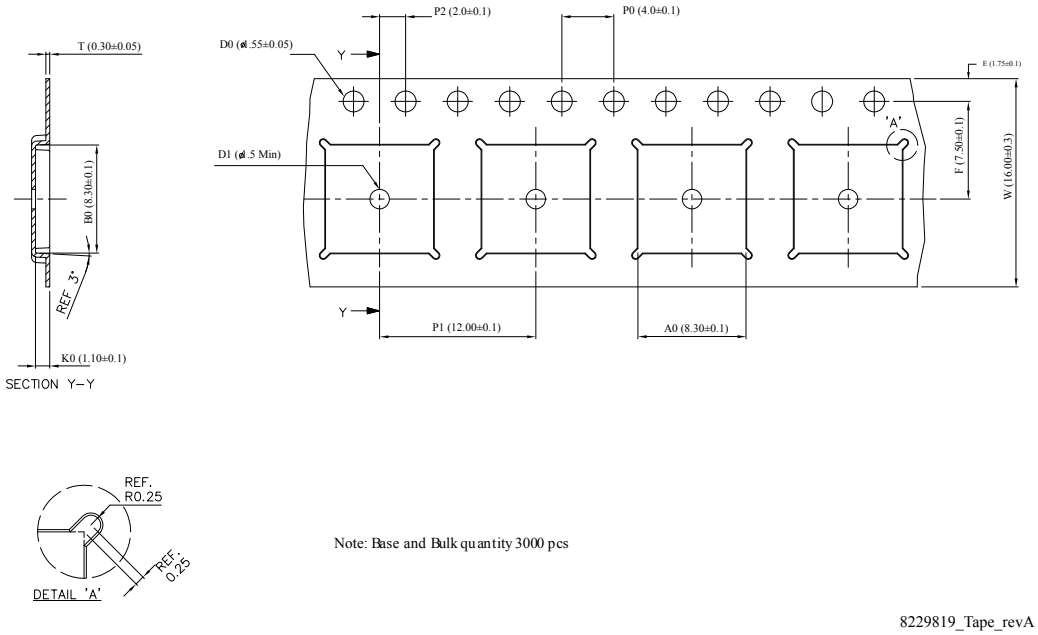
Figure 21. PowerFLAT 8x8 HV footprint



Note: All dimensions are in millimeters.

4.2 PowerFLAT 8x8 HV packing information

Figure 22. PowerFLAT 8x8 HV tape



Note: All dimensions are in millimeters.

Figure 23. PowerFLAT 8x8 HV package orientation in carrier tape

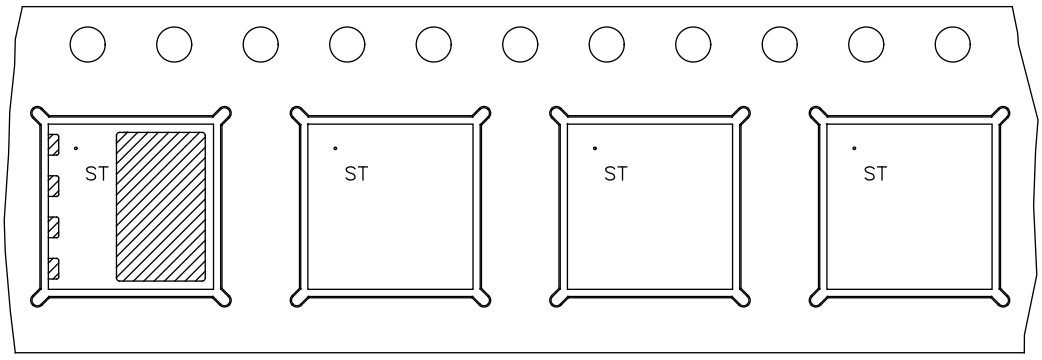
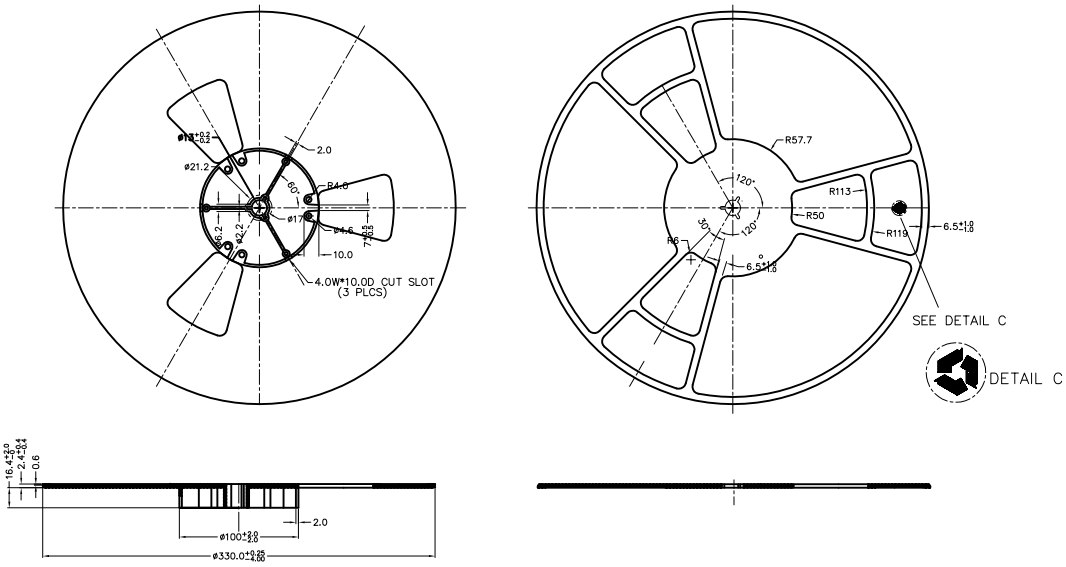


Figure 24. **PowerFLAT 8x8 HV reel**



8229819_Reel_revA

Note: All dimensions are in millimeters.

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
26-Jun-2013	1	First release.
23-Jul-2014	2	Updated the title, the features and the description in cover page. Document status promoted from preliminary data to production data. Updated Figure 1: "Internal schematic diagram", Section 1: "Electrical ratings", Section 2: "Electrical characteristics". Added Section 2.1: "Electrical characteristics (curves)" Updated Section 3: "Test circuits", Section 4.1: "PowerFLAT™ 8x8 HV package mechanical data"..
20-Nov-2015	3	Updated: cover image and *Figure 1: "Internal schematic diagram"* Table 2: "Absolute maximum ratings", Table 3: "Thermal data" and *Table 6: "Switching times"* Updated: *Figure 3: "Thermal impedance"* Updated: *Section 5: "Test circuits"* Updated: Section 6.1: "PowerFLAT™ 8x8 HV package mechanical data" Minor text changes
11-Jun-2019	4	Update Section 1 Electrical ratings. Added Figure 13. Maximum avalanche energy vs temperature. Minor text changes.

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3 **Test circuits** 8
4 **Package mechanical data** 9
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4.2 PowerFLAT 8x8 HV packing information 10
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