STM32L151x6/8/B-A
STM32L152x6/8/B-A

Ultra-low-power 32-bit MCU ARM®-based Cortex®-M3, 128KB Flash, 32KB SRAM, 4KB EEPROM, LCD, USB, ADC, DAC

Datasheet - production data

Features

- Ultra-low-power platform
  - 1.65 V to 3.6 V power supply
  - **-40°C to 105°C** temperature range
  - 0.28 µA Standby mode (3 wakeup pins)
  - **1.11 µA Standby mode + RTC**
  - 0.44 µA Stop mode (16 wakeup lines)
  - 1.38 µA Stop mode + RTC
  - 10.9 µA Low-power Run mode
  - 185 µA/MHz Run mode
  - 10 nA ultra-low I/O leakage
  - < 8 µs wakeup time
- Core: ARM® Cortex®-M3 32-bit CPU
  - From 32 kHz up to 32 MHz max
  - 1.25 DMIPS/MHz (Dhrystone 2.1)
  - Memory protection unit
- Reset and supply management
  - Ultra-safe, low-power BOR (brownout reset) with 5 selectable thresholds
  - Ultra-low-power POR/PDR
  - Programmable voltage detector (PVD)
- Clock sources
  - 1 to 24 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - High Speed Internal 16 MHz factory-trimmed RC (+/- 1%)
  - Internal low-power 37 kHz RC
  - Internal multispeed low-power 65 kHz to 4.2 MHz
  - PLL for CPU clock and USB (48 MHz)
- Pre-programmed bootloader
  - USART supported
- Development support
  - Serial wire debug supported
  - JTAG and trace supported
- Up to 83 fast I/Os (73 I/Os 5V tolerant), all mappable on 16 external interrupt vectors
- Memories
  - Up to 128 Kbytes Flash memory with ECC
  - Up to 32 Kbytes RAM
  - Up to 4 Kbytes of true EEPROM with ECC
  - 80-byte backup register


LQFP100 14 × 14 mm
LQFP64 10 × 10 mm
LQFP48 7 × 7 mm


UFBGA100 7 × 7 mm
TFBGA64 5 × 5 mm


UFQFPN48
7 × 7 mm

- LCD Driver (except STM32L151x6/8/B-A devices) for up to 8x40 segments
  - Support contrast adjustment
  - Support blinking mode
  - Step-up converter on board
- Rich analog peripherals (down to 1.8 V)
  - 12-bit ADC 1 Msps up to 24 channels
  - 12-bit DAC 2 channels with output buffers
  - 2x ultra-low-power-comparators (window mode and wake up capability)
- DMA controller 7x channels
- 8x peripheral communication interfaces
  - 1x USB 2.0 (internal 48 MHz PLL)
  - 3x USART (ISO 7816, IrDA)
  - 2x SPI 16 Mbits/s
  - 2x I2C (SMBus/PMBus)
- 10x timers: 6x 16-bit with up to 4 IC/OC/PWM channels, 2x 16-bit basic timers, 2x watchdog timers (independent and window)
- Up to 20 capacitive sensing channels supporting touchkey, linear and rotary touch sensors
- CRC calculation unit, 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32L151CB-A, STM32L151C8-A, STM32L151C6-A, STM32L151RB-A, STM32L151R8-A, STM32L151R6-A, STM32L151VB-A, STM32L151V8-A	STM32L151CBxxA, STM32L151C8xxA, STM32L151C6xxA, STM32L151RBxxA, STM32L151R8xxA, STM32L151R6xxA, STM32L151VBxxA, STM32L151V8xxA
STM32L152CB-A, STM32L152C8-A, STM32L152C6-A, STM32L152RB-A, STM32L152R8-A, STM32L152R6-A, STM32L152VB-A, STM32L152V8-A	STM32L152CBxxA, STM32L152C8xxA, STM32L152C6xxA, STM32L152RBxxA, STM32L152R8xxA, STM32L152R6xxA, STM32L152VBxxA, STM32L152V8xxA

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151x6/8/B-A and STM32L152x6/8/B-A ultra-low-power ARM® Cortex®-M3 based microcontrollers product line.

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A microcontroller family includes devices in 3 different package types: from 48 to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, Wired and wireless sensors, Video intercom
- Utility metering

This STM32L151x6/8/B-A and STM32L152x6/8/B-A datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038). The document "Getting started with STM32L1xxxx hardware development" AN3216 gives a hardware implementation overview.

Both documents are available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the ARM website.

Figure 1 shows the general block diagram of the device family.

Caution: This datasheet does not apply to:

– STM32L15xx6/8/B

covered by a separate datasheet.

2 Description

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a frequency of 32 MHz (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 128 Kbytes and RAM up to 32 Kbytes) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

All the devices offer a 12-bit ADC, 2 DACs and 2 ultra-low-power comparators, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151x6/8/B-A and STM32L152x6/8/B-A devices contain standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs and a USB. The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices offer up to 20 capacitive sensing channels to simply add touch sensing functionality to any application.

They also include a real-time clock with sub-second counting and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151x6/8/B-A devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +85 °C and -40 to +105°C temperature ranges. A comprehensive set of power-saving modes allows the design of low-power applications.





2.1 Device overview

Table 2. Ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A device features and peripheral counts

Peripheral		STM32L15xCxxxA			STM32L15xRxxxA			STM32L15xVxxxA	
Flash (Kbytes)		32	64	128	32	64	128	64	128
Data EEPROM (Kbytes)		4							
RAM (Kbytes)		16	32	32	16	32	32	32	32
Timers	General-purpose	6							
	Basic	2							
Communication interfaces	SPI	2							
	I^2C	2							
	USART	3							
	USB	1							
GPIOs		37			51/50(1)			83	
12-bit synchronized ADC Number of channels		1 14 channels			1 20/19 channels(1)			1 24 channels	
12-bit DAC Number of channels		2 2							
LCD (STM32L152xxxxA Only) COM x SEG		4x16			4x32/4x31(1) 8x28/8x27(1)			4x44 8x40	
Comparator		2							
Capacitive sensing channels		13			20				
Max. CPU frequency		32 MHz							
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option							
Operating temperatures		Ambient operating temperatures: –40 to +85 °C / –40 to + 105 °C Junction temperature: -40 to +110°C							
Packages		LQFP48, UFQFPN48			LQFP64, TFBGA64			LQFP100, UFBGA100	

1. For TFBGA64 package (instead of PC3 pin there is V_{REF+} pin).

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of cores and features. From a proprietary 8-bit core up to the Cortex-M3, including the Cortex-M0+, the STM8Lx and STM32Lx series offer the best range of choices to meet your requirements in terms of ultra-low-power features. The STM32 Ultra-low-power series is an ideal fit for applications like gas/water meters, keyboard/mouse, or wearable devices for fitness and healthcare. Numerous built-in features like LCD drivers, dual-bank memory, low-power Run mode, op-amp, AES-128bit, DAC, crystal-less USB and many others, allow to build highly cost-optimized applications by reducing the BOM.

Note: STMicroelectronics as a reliable and long-term manufacturer ensures as much as possible the pin-to-pin compatibility between any STM8Lx and STM32Lx devices and between any of the STM32Lx and STM32Fx series. Thanks to this unprecedented scalability, your existing applications can be upgraded to respond to the latest market features and efficiency demand.

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-Low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx and STM32L1xxxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xxx and STM32L1xxxx families use a common architecture:

- Common power supply range from 1.65 V to 3.6 V, (1.65 V at power down only for STM8L15xxx devices)
- Architecture optimized to reach ultra-low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultra-safe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

2.2.4 Features

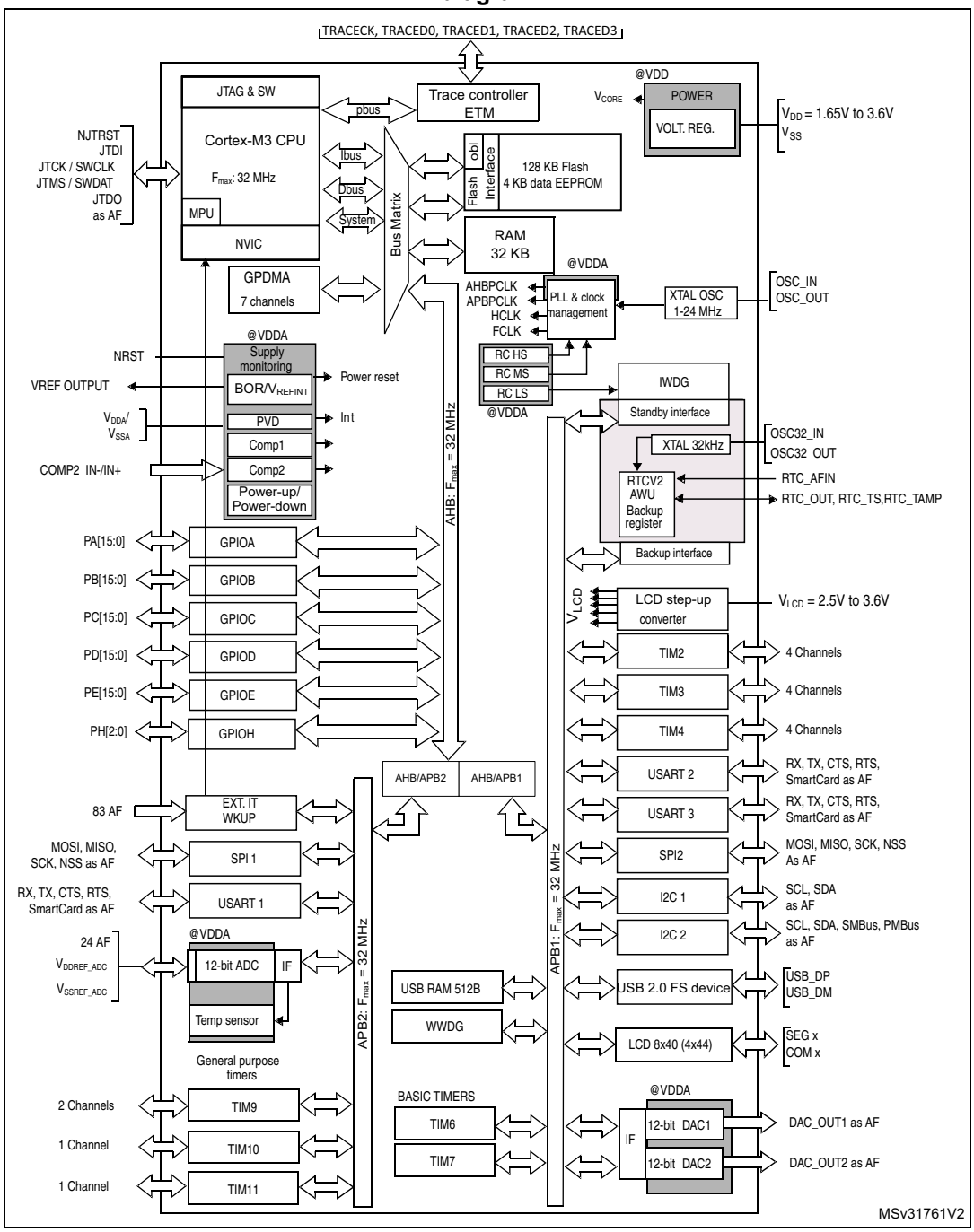
ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 512 Kbytes

3 Functional overview

Figure 1 shows the block diagram.

Figure 1. Ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A block diagram



1. AF = alternate function on I/O port pin.

3.1 Low-power modes

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices support dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply:

- In Range 1 (V_{DD} range limited to 1.71-3.6 V), the CPU runs at up to 32 MHz (refer to *Table 18* for consumption).
- In Range 2 (full V_{DD} range), the CPU runs at up to 16 MHz (refer to *Table 18* for consumption)
- In Range 3 (full V_{DD} range), the CPU runs at up to 4 MHz (generated only with the multispeed internal RC oscillator clock source). Refer to *Table 18* for consumption.

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

  Sleep mode power consumption: refer to *Table 20*.

- **Low-power Run** mode

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the MSI range 0 or MSI range 1 clock range (maximum 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In the low-power Run mode, the clock frequency and the number of enabled peripherals are both limited.

  Low-power Run mode consumption: refer to *Table 21*.

- **Low-power Sleep** mode

  This mode is achieved by entering the Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In the low-power Sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.
  When wakeup is triggered by an event or an interrupt, the system reverts to the run mode with the regulator on.

  Low-power Sleep mode consumption: refer to *Table 22*.

- **Stop** mode with RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSI RC and HSE crystal oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on), it can be the RTC alarm(s), the USB wakeup, the RTC tamper events, the RTC timestamp event or the RTC wakeup.

- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI

line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

Stop mode consumption: refer to *Table 23*.

- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI, RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

  Standby mode consumption: refer to *Table 24*.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering the Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range(1)		
	DAC and ADC operation	USB	Dynamic voltage scaling range
V_{DD} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3
V_{DD}= 1.71 to 1.8 V (2)	Not functional	Not functional	Range 1, Range 2 or Range 3
V_{DD} = 1.8 to 2.0 V(2)	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3
V_{DD} = 2.0 to 2.4 V	Conversion time up to 500 Ksps	Functional(3)	Range 1, Range 2 or Range 3
V_{DD} = 2.4 to 3.6 V	Conversion time up to 1 Msps	Functional(3)	Range 1, Range 2 or Range 3

1. The GPIO speed also depends from VDD voltage and the user has to refer to *Table 45: I/O AC characteristics* for more information about I/O speed.

2. CPU frequency changes from initial to final must respect "F_{CPU} initial < 4*F_{CPU} final" to limit V_{CORE} drop due to current consumption peak when frequency increases. It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.
3. Should be USB-compliant from I/O voltage standpoint, the minimum V_{DD} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1 MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

Table 5. Working mode-dependent functionalities (from Run/active down to standby)

Ips	Run/Active	Sleep	Low-power Run	Low-power Sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	-	Y	-	-	-	-	-
Flash	Y	Y	Y	Y	-	-	-	-
RAM	Y	Y	Y	Y	Y	-	-	-
Backup Registers	Y	Y	Y	Y	Y	-	Y	-
EEPROM	Y	Y	Y	Y	Y	-	-	-
Brown-out reset (BOR)	Y	Y	Y	Y	Y	Y	Y	-
DMA	Y	Y	Y	Y	-	-	-	-
Programmable Voltage Detector (PVD)	Y	Y	Y	Y	Y	Y	Y	-
Power On Reset (POR)	Y	Y	Y	Y	Y	Y	Y	-
Power Down Rest (PDR)	Y	Y	Y	Y	Y	-	Y	-
High Speed Internal (HSI)	Y	Y	-	-	-	-	-	-
High Speed External (HSE)	Y	Y	-	-	-	-	-	-
Low Speed Internal (LSI)	Y	Y	Y	Y	Y	-	Y	-
Low Speed External (LSE)	Y	Y	Y	Y	Y	-	Y	-
Multi-Speed Internal (MSI)	Y	Y	Y	Y	-	-	-	-
Inter-Connect Controller	Y	Y	Y	Y	-	-	-	-
RTC	Y	Y	Y	Y	Y	Y	Y	-
RTC Tamper	Y	Y	Y	Y	Y	Y	Y	Y
Auto Wakeup (AWU)	Y	Y	Y	Y	Y	Y	Y	Y
LCD	Y	Y	Y	Y	Y	-	-	-
USB	Y	Y	-	-	-	Y	-	-
USART	Y	Y	Y	Y	Y	(1)	-	-
SPI	Y	Y	Y	Y	-	-	-	-
I2C	Y	Y	-	-	-	(1)	-	-
ADC	Y	Y	-	-	-	-	-	-

Table 5. Working mode-dependent functionalities (from Run/active down to standby) (continued)

Ips	Run/Active	Sleep	Low-power Run	Low-power Sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
DAC	Y	Y	Y	Y	Y	-	-	-
Temperature sensor	Y	Y	Y	Y	Y	-	-	-
Comparators	Y	Y	Y	Y	Y	Y	-	-
16-bit Timers	Y	Y	Y	Y	-	-	-	-
IWDG	Y	Y	Y	Y	Y	Y	Y	Y
WWDG	Y	Y	Y	Y	-	-	-	-
Touch sensing	Y	-	-	-	-	-	-	-
Systick Timer	Y	Y	Y	Y	-	-	-	-
GPIOs	Y	Y	Y	Y	Y	Y	-	3 pins
Wakeup time to Run mode	0 µs	0.4 µs	3 µs	46 µs	< 8 µs		58 µs	
Consumption V_{DD}=1.8V to 3.6V (Typ)	Down to 185 µA/MHz (from Flash)	Down to 36.9 µA/MHz (from Flash)	Down to 10.9 µA	Down to 5.5 µA	0.43 µA (No RTC) V_{DD}=1.8 V		0.27 µA (No RTC) V_{DD}=1.8 V	
					1.13 µA (with RTC) V_{DD}=1.8 V		0.87 µA (with RTC) V_{DD}=1.8 V	
					0.44 µA (No RTC) V_{DD}=3.0 V		0.28 µA (No RTC) V_{DD}=3.0 V	
					1.38 µA (with RTC) V_{DD}=3.0 V		1.11 µA (with RTC) V_{DD}=3.0 V	

1. The startup on communication line wakes the CPU which was made possible by an EXTI, this induces a delay before entering run mode.

3.2 ARM® Cortex®-M3 core with MPU

The ARM® Cortex®-M3 processor is the industry leading processor for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L151x6/8/B-A and STM32L152x6/8/B-A devices are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices embed a nested vectored interrupt controller able to handle up to 45 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System Memory
- Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. See the application note “STM32 microcontroller system memory boot mode” (AN2606) for details.

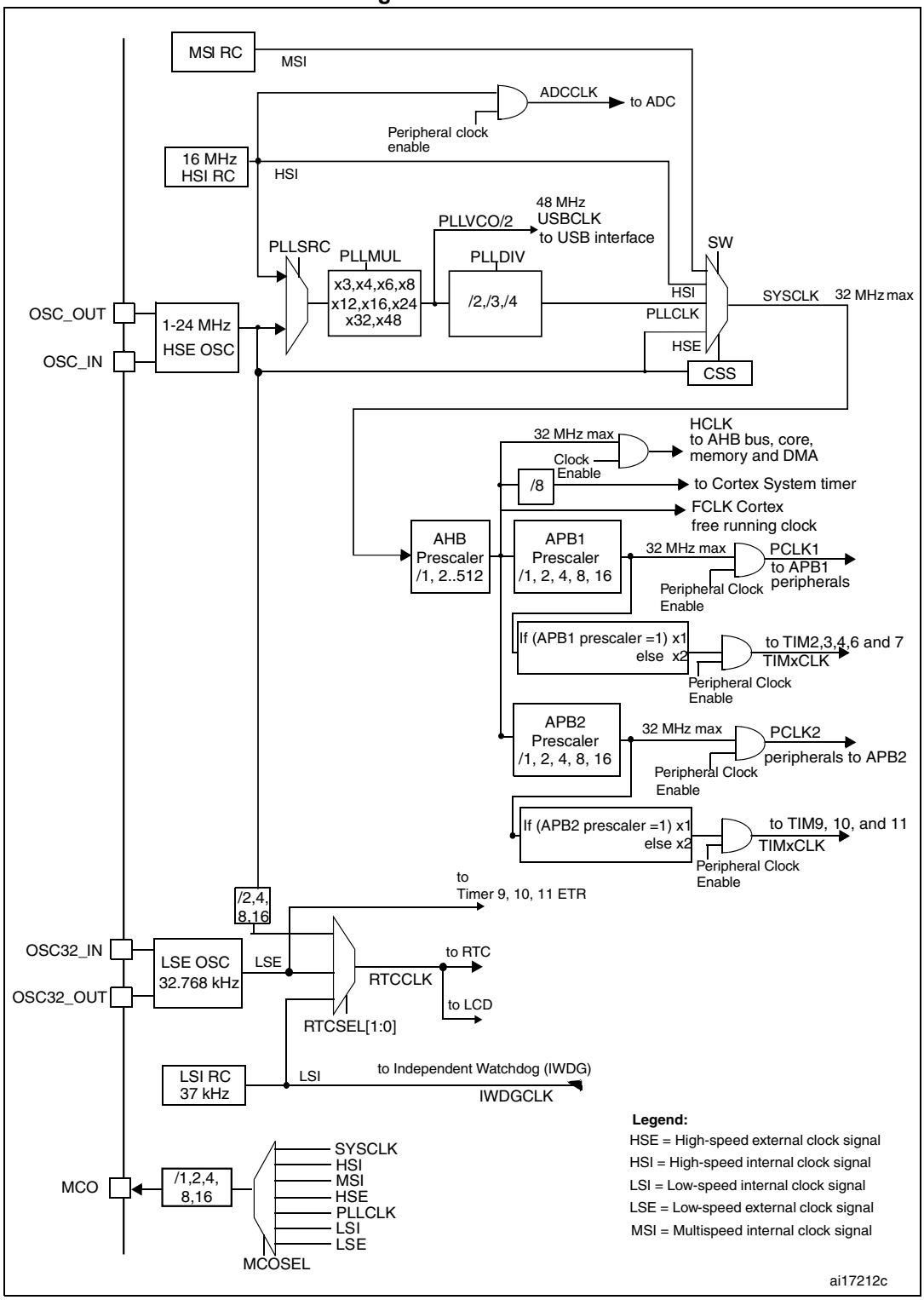
3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Master clock source**: three different clock sources can be used to drive the master clock:
  - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz) with a consumption proportional to speed, down to 750 nA typical. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- **Auxiliary clock source**: two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2.1 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

Figure 2. Clock tree



3.5 Low-power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the sub-second, second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made automatically. The RTC provides two programmable alarms and programmable periodic interrupts with wakeup from Stop and Standby modes.

The programmable wakeup time ranges from 120 µs to 36 hours.

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation. The RTC can also be automatically corrected with a 50/60Hz stable power line.

The RTC calendar can be updated on the fly down to sub second precision, which enables network system synchronization. A time stamp can record an external event occurrence, and generates an interrupt.

There are twenty 32-bit backup registers provided to store 80 bytes of user application data. They are cleared in case of tamper detection. Three pins can be used to detect tamper events. A change on one of these pins can reset backup register and generate an interrupt. To prevent false tamper event, like ESD event, these three tamper inputs can be digitally filtered.

3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high current capable. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 83 GPIOs can be connected to the 16 external interrupt lines. The 7 other lines are connected to RTC, PVD, USB or Comparator events.

3.7 Memories

The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices have the following features:

- Up to 32 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 32, 64 or 128 Kbytes of embedded Flash program memory
  - 4 Kbytes of data EEPROM
  - Options bytes

  The options bytes are used to write-protect or read-out-protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

  The user area of the Flash memory can be protected against Dbus read access by the PCROP feature (see RM0038 for details).

3.8 DMA (direct memory access)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers and ADC.

3.9 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode
- V_{LCD} rail decoupling capability

Table 6. V_{LCD} rail decoupling

	Bias			Pin	
	1/2	1/3	1/4		
$V_{LCDrail1}$	1/2 V_{LCD}	2/3 V_{LCD}	1/2 V_{LCD}	PB2	
$V_{LCDrail2}$	NA	1/3 V_{LCD}	1/4 V_{LCD}	PB12	PE11
$V_{LCDrail3}$	NA	NA	3/4 V_{LCD}	PB0	PE12

3.10 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L151x6/8/B-A and STM32L152x6/8/B-A devices with up to 24 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low-power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

3.10.1 Temperature sensor

The temperature sensor T_{SENSE} generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode, see *Table 59: Temperature sensor calibration values*.

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, VREF+, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode see *Table 17: Embedded internal reference voltage*.

3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- external triggers for conversion
- input reference voltage V_{REF+}

Eight DAC trigger inputs are used in the STM32L151x6/8/B-A and STM32L152x6/8/B-A devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.12 Ultra-low-power comparators and reference voltage

The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- one comparator with fixed threshold
- one comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage (V_{REFINT}) or V_{REFINT} submultiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.13 Routing interface

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage V_{REFINT}.

3.14 Touch sensing

The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 20 capacitive sensing channels distributed over 10 analog I/O groups. Both software and timer capacitive sensing acquisition modes are supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, ...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. The capacitive sensing acquisition only requires few external components to operate. This acquisition is managed directly by the GPIOs, timers and analog I/O groups (see *Section 3.13: Routing interface*).

Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.

3.15 Timers and watchdogs

The ultra-low-power STM32L151x6/8/B-A and STM32L152x6/8/B-A devices include six general-purpose timers, two basic timers and two watchdog timers.

Table 7 compares the features of the general-purpose and basic timers.

Table 7. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.15.1 General-purpose timers (TIM2, TIM3, TIM4, TIM9, TIM10 and TIM11)

There are six synchronizable general-purpose timers embedded in the STM32L151x6/8/B-A and STM32L152x6/8/B-A devices (see *Table 7* for differences).

TIM2, TIM3, TIM4

These timers are based on a 16-bit auto-reload up/down-counter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM10, TIM11 and TIM9

TIM10 and TIM11 are based on a 16-bit auto-reload upcounter. TIM9 is based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4 full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.15.2 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.15.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit down-counter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches 0.

3.15.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down-counter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.15.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit down-counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.16 Communication interfaces

3.16.1 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

3.16.2 Universal synchronous/asynchronous receiver transmitter (USART)

All USART interfaces are able to communicate at speeds of up to 4 Mbit/s. They provide hardware management of the CTS and RTS signals and are ISO 7816 compliant. They support IrDA SIR ENDEC and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

3.16.3 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

3.16.4 Universal serial bus (USB)

The STM32L151x6/8/B-A and STM32L152x6/8/B-A devices embed a USB device peripheral compatible with the USB full speed 12 Mbit/s. The USB interface implements a full speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3.17 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.18 Development support

Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG JTMS and JTCK pins are shared with SWDAT and SWCLK, respectively, and a specific sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

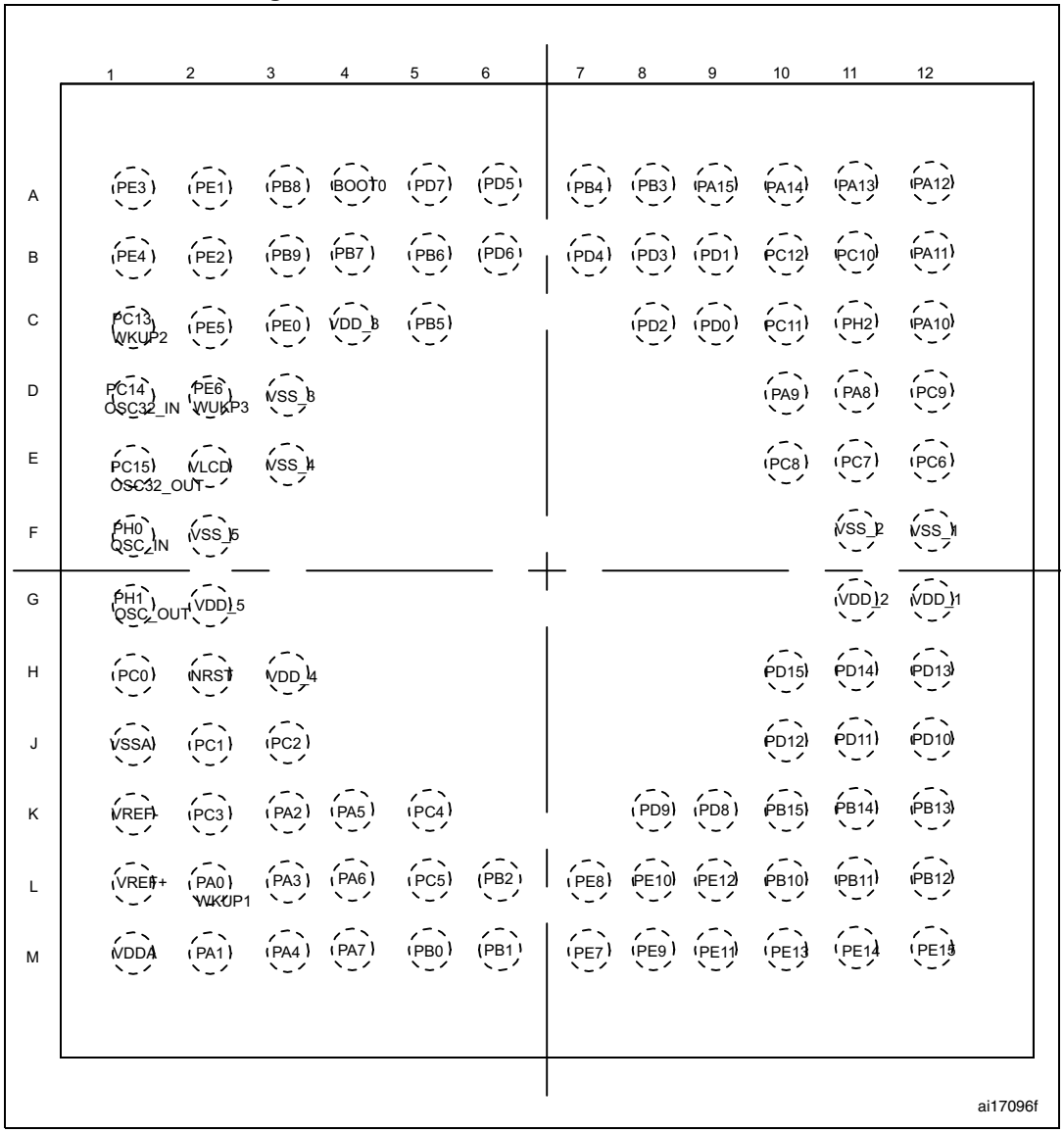
The JTAG port can be permanently disabled with a JTAG fuse.

Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L151x6/8/B-A and STM32L152x6/8/B-A device through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

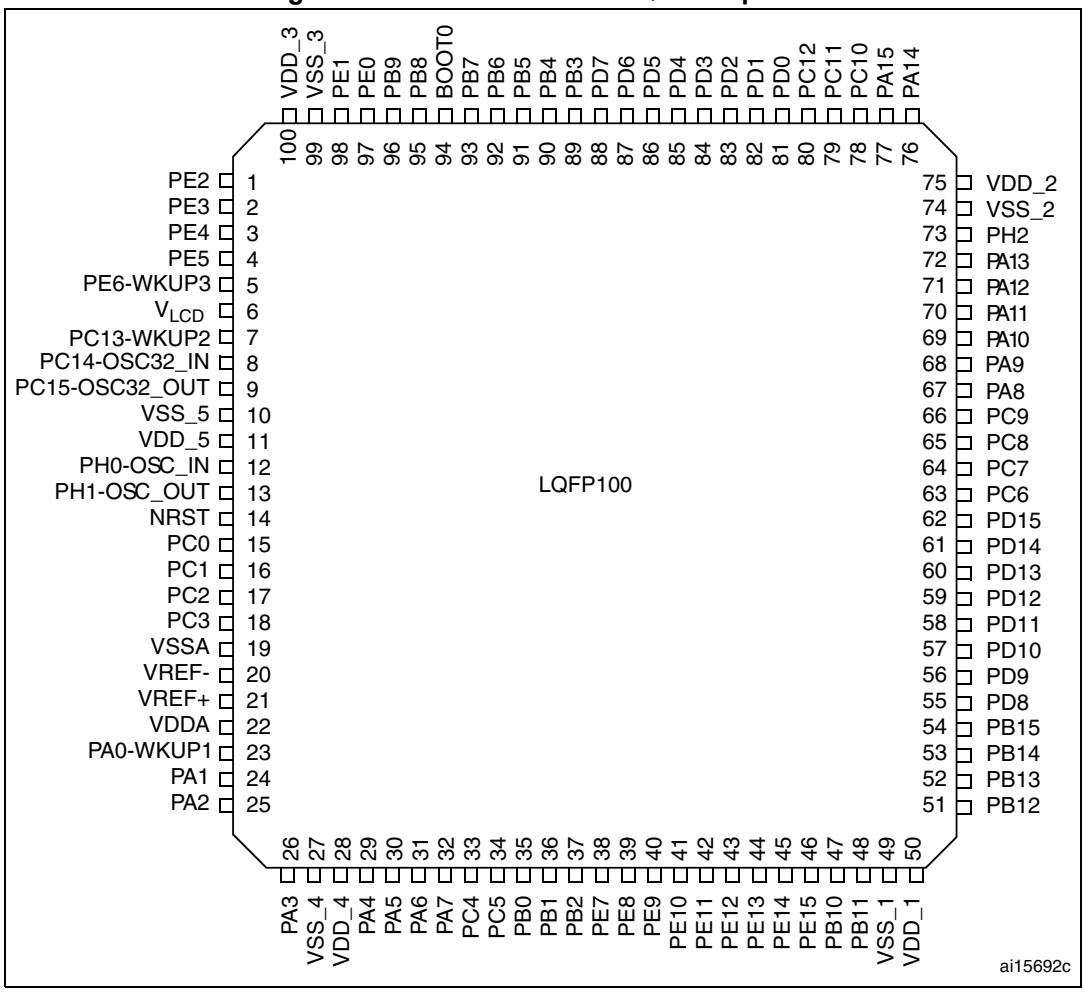
4 Pin descriptions

Figure 3. STM32L15xVxxxA UFBGA100 ballout



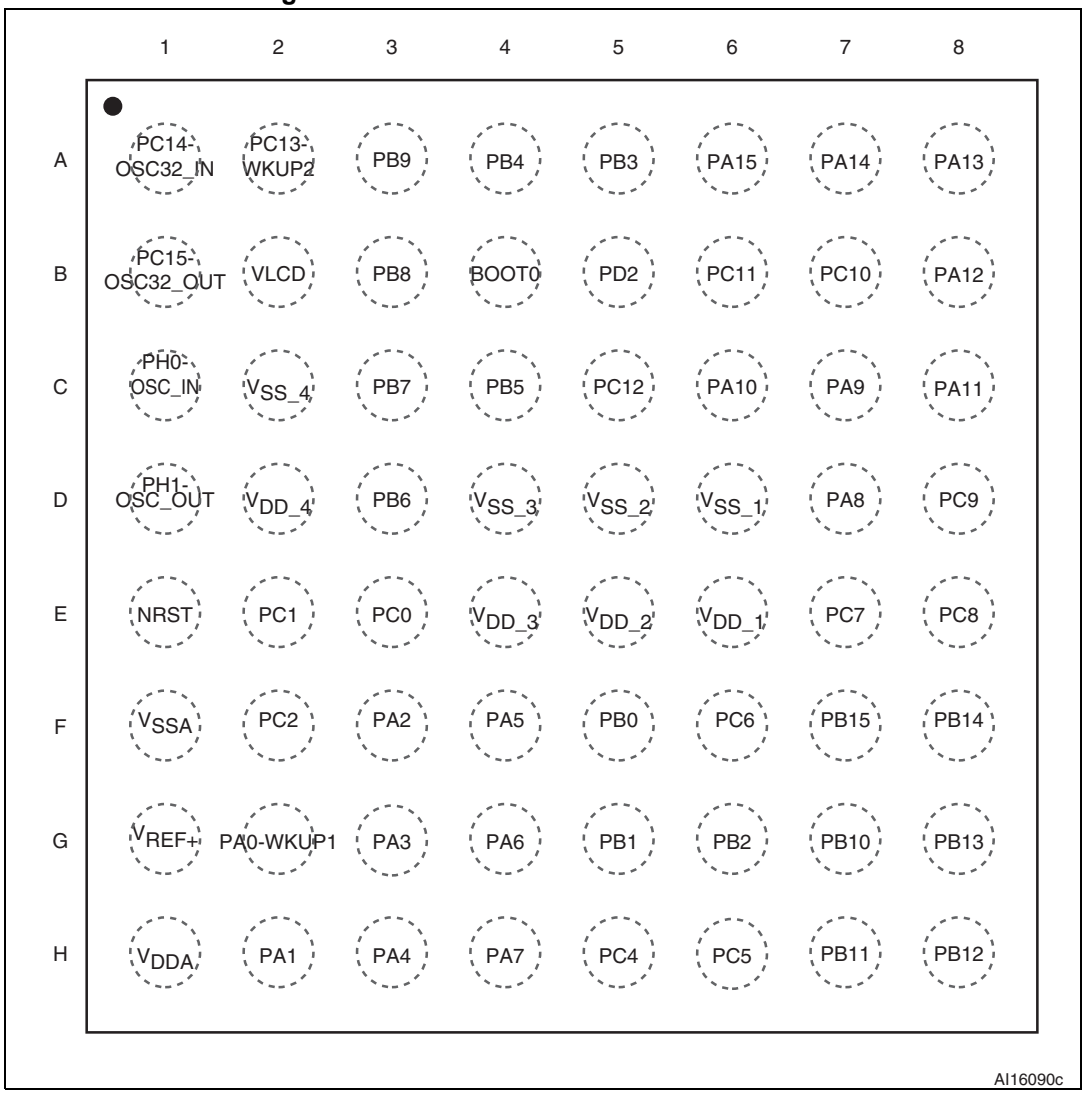
1. This figure shows the package top view.

Figure 4. STM32L15xVxxxA LQFP100 pinout



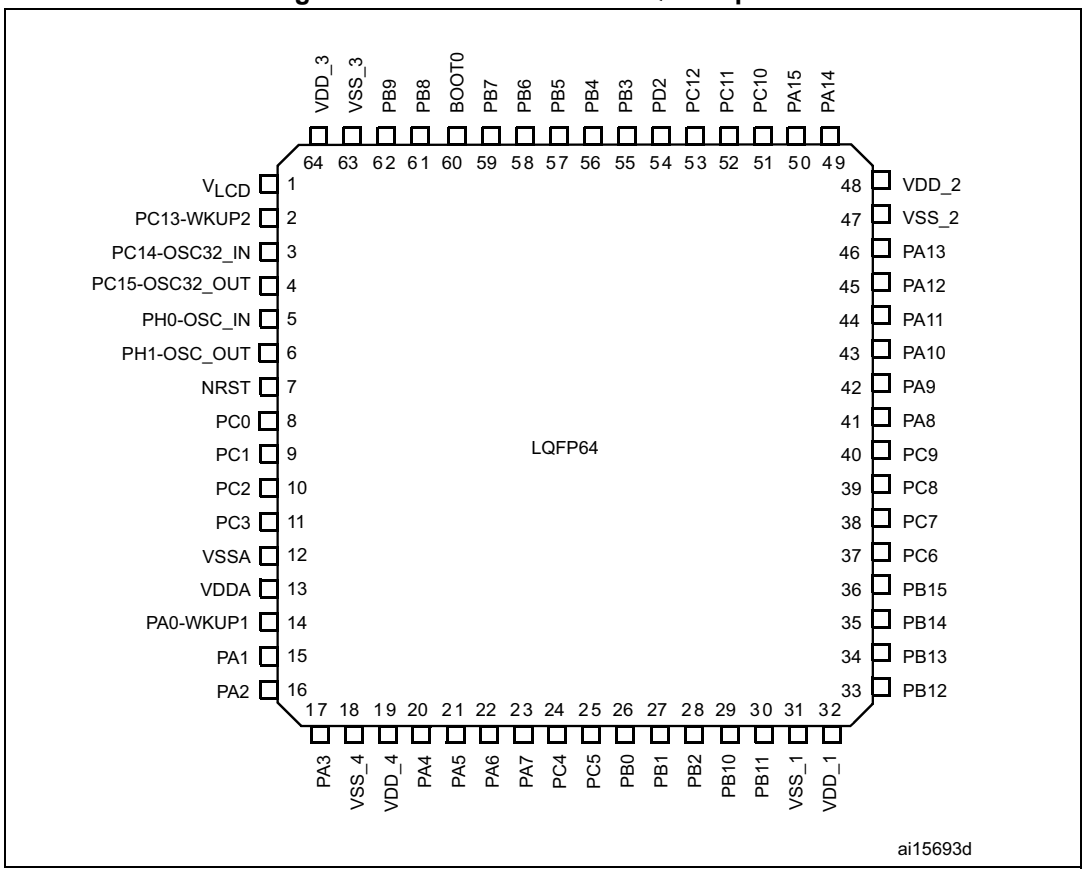
1. This figure shows the package top view.

Figure 5. STM32L15xRxxxA TFBGA64 ballout



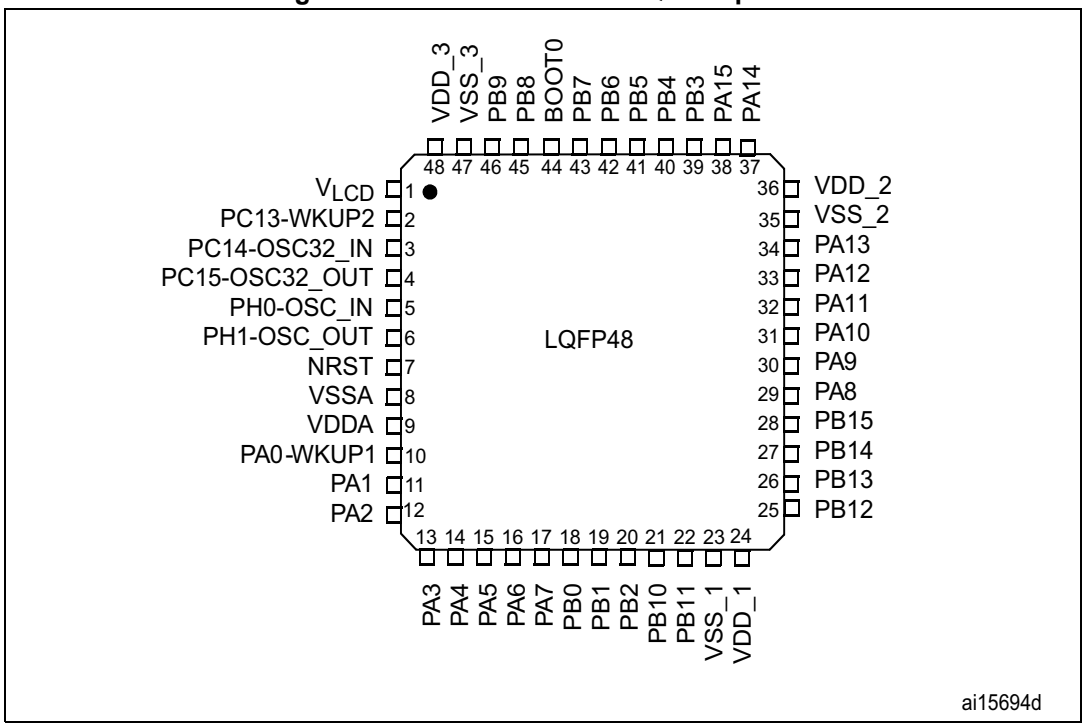
1. This figure shows the package top view.

Figure 6. STM32L15xRxxxA LQFP64 pinout



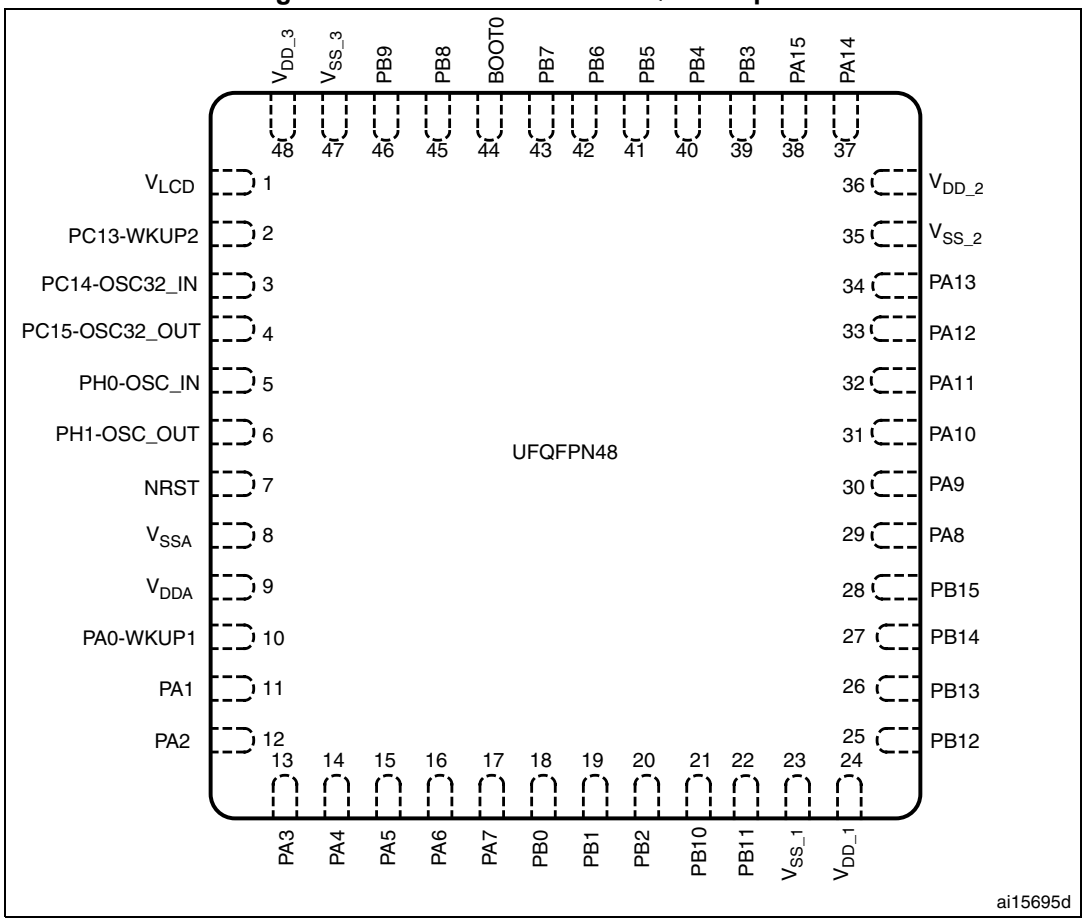
1. This figure shows the package top view.

Figure 7. STM32L15xCxxxA LQFP48 pinout



1. This figure shows the package top view.

Figure 8. STM32L15xCxxxA UFQFPN48 pinout



1. This figure shows the package top view.

Table 8. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions

Pins					Pin name	Pin type(1)	I/O structure	Main function(2) (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
1	-	-	B2	-	PE2	I/O	FT	PE2	TRACECLK/ LCD_SEG38/TIM3_ETR	-
2	-	-	A1	-	PE3	I/O	FT	PE3	TRACED0/ LCD_SEG39/TIM3_CH1	-
3	-	-	B1	-	PE4	I/O	FT	PE4	TRACED1/TIM3_CH2	-
4	-	-	C2	-	PE5	I/O	FT	PE5	TRACED2/TIM9_CH1	-
5	-	-	D2	-	PE6-WKUP3	I/O	FT	PE6	TRACED3/TIM9_CH2	WKUP3 /RTC_TAMP3
6	1	B2	E2	1	V_{LCD}(3)	S		V_{LCD}	-	-
7	2	A2	C1	2	PC13-WKUP2	I/O	FT	PC13	-	RTC_TAMP1/ RTC_TS/ RTC_OUT/ WKUP2
8	3	A1	D1	3	PC14-OSC32_IN(4)	I/O	TC	PC14	-	OSC32_IN
9	4	B1	E1	4	PC15-OSC32_OUT (4)	I/O	TC	PC15	-	OSC32_OUT
10	-	-	F2	-	V_{SS_5}	S	-	V_{SS_5}	-	-
11	-	-	G2	-	V_{DD_5}	S	-	V_{DD_5}	-	-
12	5	C1	F1	5	PH0-OSC_IN(5)	I/O	TC	PH0	-	OSC_IN
13	6	D1	G1	6	PH1-OSC_OUT	I/O	TC	PH1	-	OSC_OUT
14	7	E1	H2	7	NRST	I/O	RST	NRST	-	-
15	8	E3	H1	-	PC0	I/O	FT	PC0	LCD_SEG18	ADC_IN10/ COMP1_INP
16	9	E2	J2	-	PC1	I/O	FT	PC1	LCD_SEG19	ADC_IN11/ COMP1_INP
17	10	F2	J3	-	PC2	I/O	FT	PC2	LCD_SEG20	ADC_IN12/ COMP1_INP
18	11	-(6)	K2	-	PC3	I/O	TC	PC3	LCD_SEG21	ADC_IN13/ COMP1_INP
19	12	F1	J1	8	V_{SSA}	S	-	V_{SSA}	-	-

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type(1)	I/O structure	Main function(2) (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
20	-	-	K1	-	V_{REF-}	S	-	V_{REF-}	-	-
21	-	G1 (6)	L1	-	V_{REF+}	S	-	V_{REF+}	-	-
22	13	H1	M1	9	V_{DDA}	S	-	V_{DDA}	-	-
23	14	G2	L2	10	PA0-WKUP1	I/O	FT	PA0	USART2_CTS/ TIM2_CH1_ETR	WKUP1/ ADC_IN0/ COMP1_INP /RTC_TAMP2
24	15	H2	M2	11	PA1	I/O	FT	PA1	USART2_RTS/ TIM2_CH2/LCD_SEG0	ADC_IN1/ COMP1_INP
25	16	F3	K3	12	PA2	I/O	FT	PA2	USART2_TX/ TIM2_CH3/ TIM9_CH1/ LCD_SEG1	ADC_IN2/ COMP1_INP
26	17	G3	L3	13	PA3	I/O	TC	PA3	USART2_RX/ TIM2_CH4/ TIM9_CH2/ LCD_SEG2	ADC_IN3/ COMP1_INP
27	18	C2	E3	-	V_{SS_4}	S	-	V_{SS_4}	-	-
28	19	D2	H3	-	V_{DD_4}	S	-	V_{DD_4}	-	-
29	20	H3	M3	14	PA4	I/O	TC	PA4	SPI1_NSS/ USART2_CK	ADC_IN4/ DAC_OUT1/ COMP1_INP
30	21	F4	K4	15	PA5	I/O	TC	PA5	SPI1_SCK/ TIM2_CH1_ETR	ADC_IN5/ DAC_OUT2/ COMP1_INP
31	22	G4	L4	16	PA6	I/O	FT	PA6	SPI1_MISO/TIM3_CH1/ LCD_SEG3/TIM10_CH1	ADC_IN6/ COMP1_INP
32	23	H4	M4	17	PA7	I/O	FT	PA7	SPI1_MOSI/TIM3_CH2/ LCD_SEG4/TIM11_CH1	ADC_IN7/ COMP1_INP
33	24	H5	K5	-	PC4	I/O	FT	PC4	LCD_SEG22	ADC_IN14/ COMP1_INP
34	25	H6	L5	-	PC5	I/O	FT	PC5	LCD_SEG23	ADC_IN15/ COMP1_INP

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type(1)	I/O structure	Main function(2) (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
35	26	F5	M5	18	PB0	I/O	TC	PB0	TIM3_CH3/ LCD_SEG5	ADC_IN8/ COMP1_INP/ VREF_OUT /VLCDRAIL3
36	27	G5	M6	19	PB1	I/O	FT	PB1	TIM3_CH4/ LCD_SEG6	ADC_IN9/ COMP1_INP/ VREF_OUT
37	28	G6	L6	20	PB2	I/O	FT	PB2/ BOOT1	BOOT1	VLCDRAIL1
38	-	-	M7	-	PE7	I/O	TC	PE7	-	ADC_IN22/ COMP1_INP
39	-	-	L7	-	PE8	I/O	TC	PE8	-	ADC_IN23/ COMP1_INP
40	-	-	M8	-	PE9	I/O	TC	PE9	TIM2_CH1_ETR	ADC_IN24/ COMP1_INP
41	-	-	L8	-	PE10	I/O	TC	PE10	TIM2_CH2	ADC_IN25/ COMP1_INP
42	-	-	M9	-	PE11	I/O	FT	PE11	TIM2_CH3	VLCDRAIL2
43	-	-	L9	-	PE12	I/O	FT	PE12	TIM2_CH4/ SPI1_NSS	VLCDRAIL3
44	-	-	M10	-	PE13	I/O	FT	PE13	SPI1_SCK	-
45	-	-	M11	-	PE14	I/O	FT	PE14	SPI1_MISO	-
46	-	-	M12	-	PE15	I/O	FT	PE15	SPI1_MOSI	-
47	29	G7	L10	21	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX /TIM2_CH3/ LCD_SEG10	-
48	30	H7	L11	22	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX /TIM2_CH4/ LCD_SEG11	-
49	31	D6	F12	23	V_{SS_1}	S	-	V_{SS_1}	-	-
50	32	E6	G12	24	V_{DD_1}	S	-	V_{DD_1}	-	-

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type(1)	I/O structure	Main function(2) (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
51	33	H8	L12	25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/ USART3_CK/ LCD_SEG12/ TIM10_CH1	ADC_IN18/ COMP1_INP /VLCDRAIL2
52	34	G8	K12	26	PB13	I/O	FT	PB13	SPI2_SCK/ USART3_CTS/ LCD_SEG13/TIM9_CH1	ADC_IN19/ COMP1_INP
53	35	F8	K11	27	PB14	I/O	FT	PB14	SPI2_MISO/ USART3_RTS/ LCD_SEG14/TIM9_CH2	ADC_IN20/ COMP1_INP
54	36	F7	K10	28	PB15	I/O	FT	PB15	SPI2_MOSI/ LCD_SEG15/ TIM11_CH1	ADC_IN21/ COMP1_INP/ RTC_REFIN
55	-	-	K9	-	PD8	I/O	FT	PD8	USART3_TX/ LCD_SEG28	-
56	-	-	K8	-	PD9	I/O	FT	PD9	USART3_RX/ LCD_SEG29	-
57	-	-	J12	-	PD10	I/O	FT	PD10	USART3_CK/ LCD_SEG30	-
58	-	-	J11	-	PD11	I/O	FT	PD11	USART3_CTS/ LCD_SEG31	-
59	-	-	J10	-	PD12	I/O	FT	PD12	TIM4_CH1/ USART3_RTS/ LCD_SEG32	-
60	-	-	H12	-	PD13	I/O	FT	PD13	TIM4_CH2/LCD_SEG33	-
61	-	-	H11	-	PD14	I/O	FT	PD14	TIM4_CH3/LCD_SEG34	-
62	-	-	H10	-	PD15	I/O	FT	PD15	TIM4_CH4/LCD_SEG35	-
63	37	F6	E12	-	PC6	I/O	FT	PC6	TIM3_CH1/LCD_SEG24	-
64	38	E7	E11	-	PC7	I/O	FT	PC7	TIM3_CH2/LCD_SEG25	-
65	39	E8	E10	-	PC8	I/O	FT	PC8	TIM3_CH3/LCD_SEG26	-
66	40	D8	D12	-	PC9	I/O	FT	PC9	TIM3_CH4/LCD_SEG27	-

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type[1]	I/O structure	Main function[2] (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
67	41	D7	D11	29	PA8	I/O	FT	PA8	USART1_CK/MCO/ LCD_COM0	-
68	42	C7	D10	30	PA9	I/O	FT	PA9	USART1_TX/ LCD_COM1	-
69	43	C6	C12	31	PA10	I/O	FT	PA10	USART1_RX/ LCD_COM2	-
70	44	C8	B12	32	PA11	I/O	FT	PA11	USART1_CTS/ SPI1_MISO	USB_DM
71	45	B8	A12	33	PA12	I/O	FT	PA12	USART1_RTS/ SPI1_MOSI	USB_DP
72	46	A8	A11	34	PA13	I/O	FT	JTMS-SWDIO	JTMS-SWDIO	-
73	-	-	C11	-	PH2	I/O	FT	PH2	-	-
74	47	D5	F11	35	V_{SS_2}	S	-	V_{SS_2}	-	-
75	48	E5	G11	36	V_{DD_2}	S	-	V_{DD_2}	-	-
76	49	A7	A10	37	PA14	I/O	FT	JTCK-SWCLK	JCTK-SWCLK	-
77	50	A6	A9	38	PA15	I/O	FT	JTDI	TIM2_CH1_ETR/PA15/ SPI1_NSS/ LCD_SEG17	-
78	51	B7	B11	-	PC10	I/O	FT	PC10	USART3_TX/ LCD_SEG28/ LCD_SEG40/ LCD_COM4	-
79	52	B6	C10	-	PC11	I/O	FT	PC11	USART3_RX/ LCD_SEG29/ LCD_SEG41/ LCD_COM5	-
80	53	C5	B10	-	PC12	I/O	FT	PC12	USART3_CK/ LCD_SEG30/ LCD_SEG42/ LCD_COM6	-
81	-	-	C9	-	PD0	I/O	FT	PD0	SPI2_NSS/TIM9_CH1	-

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type(1)	I/O structure	Main function(2) (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
82	-	-	B9	-	PD1	I/O	FT	PD1	SPI2_SCK	-
83	54	B5	C8	-	PD2	I/O	FT	PD2	TIM3_ETR/LCD_SEG31 /LCD_SEG43/ LCD_COM7	-
84	-	-	B8	-	PD3	I/O	FT	PD3	USART2_CTS/ SPI2_MISO	-
85	-	-	B7	-	PD4	I/O	FT	PD4	USART2_RTS/ SPI2_MOSI	-
86	-	-	A6	-	PD5	I/O	FT	PD5	USART2_TX	-
87	-	-	B6	-	PD6	I/O	FT	PD6	USART2_RX	-
88	-	-	A5	-	PD7	I/O	FT	PD7	USART2_CK/ TIM9_CH2	-
89	55	A5	A8	39	PB3	I/O	FT	JTDO	TIM2_CH2/PB3/ SPI1_SCK/ LCD_SEG7/JTDO	COMP2_INM
90	56	A4	A7	40	PB4	I/O	FT	NJTRST	TIM3_CH1/PB4/ SPI1_MISO/LCD_SEG8 /NJTRST	COMP2_INP
91	57	C4	C5	41	PB5	I/O	FT	PB5	I2C1_SMBA/TIM3_CH2/ SPI1_MOSI/LCD_SEG9	COMP2_INP
92	58	D3	B5	42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1/ USART1_TX	-
93	59	C3	B4	43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2/ USART1_RX	PVD_IN
94	60	B4	A4	44	BOOT0	I	B	BOOT0	-	-
95	61	B3	A3	45	PB8	I/O	FT	PB8	TIM4_CH3/I2C1_SCL/ LCD_SEG16/ TIM10_CH1	-
96	62	A3	B3	46	PB9	I/O	FT	PB9	TIM4_CH4/I2C1_SDA/ LCD_COM3/ TIM11_CH1	-
97	-	-	C3	-	PE0	I/O	FT	PE0	TIM4_ETR/LCD_SEG36 / TIM10_CH1	-

Table 9. STM32L151x6/8/B-A and STM32L152x6/8/B-A pin definitions (continued)

Pins					Pin name	Pin type[1]	I/O structure	Main function[2] (after reset)	Pins functions	
LQFP100	LQFP64	TFBGA64	UFBGA100	LQFP48 or UFQFPN48					Alternate functions	Additional functions
98	-	-	A2	-	PE1	I/O	FT	PE1	LCD_SEG37/ TIM11_CH1	-
99	63	D4	D3	47	V_{SS_3}	S	-	V_{SS_3}	-	-
100	64	E4	C4	48	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 11*.
3. Applicable to STM32L152xxxxA devices only. In STM32L151xxxxA devices, this pin should be connected to V_{DD}.
4. The PC14 and PC15 I/Os are only configured as OSC32_IN/OSC32_OUT when the LSE oscillator is on (by setting the LSEON bit in the RCC_CSR register). The LSE oscillator pins OSC32_IN/OSC32_OUT can be used as general-purpose PC14/PC15 I/Os, respectively, when the LSE oscillator is off (after reset, the LSE oscillator is off). The LSE has priority over the GPIO function. For more details, refer to Using the OSC32_IN/OSC32_OUT pins as GPIO PC14/PC15 port pins section in the STM32L1xxxx reference manual (RM0038).
5. The PH0 and PH1 I/Os are only configured as OSC_IN/OSC_OUT when the HSE oscillator is on (by setting the HSEON bit in the RCC_CR register). The HSE oscillator pins OSC_IN/OSC_OUT can be used as general-purpose PH0/PH1 I/Os, respectively, when the HSE oscillator is off (after reset, the HSE oscillator is off). The HSE has priority over the GPIO function.
6. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.

Table 10. Alternate function input/output

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
BOOT0	BOOT0	-	-	-	-	-	-	-	-	-	-	-	-	-	-
NRST	NRST	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PA0-WKUP1	-	TIM2_CH1_ETR	-	-	-	-	-	USART2_CTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA1	-	TIM2_CH2	-	-	-	-	-	USART2_RTS	-	-	[SEG0]	-	-	TIMx_IC2	EVENTOUT
PA2	-	TIM2_CH3	-	TIM9_CH1	-	-	-	USART2_TX	-	-	[SEG1]	-	-	TIMx_IC3	EVENTOUT
PA3	-	TIM2_CH4	-	TIM9_CH2	-	-	-	USART2_RX	-	-	[SEG2]	-	-	TIMx_IC4	EVENTOUT
PA4	-	-	-	-	-	SPI1_NSS	-	USART2_CK	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA5	-	TIM2_CH1_ETR	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA6	-	-	TIM3_CH1	TIM10_CH1	-	SPI1_MISO	-	-	-	-	[SEG3]	-	-	TIMx_IC3	EVENTOUT
PA7	-	-	TIM3_CH2	TIM11_CH1	-	SPI1_MOSI	-	-	-	-	[SEG4]	-	-	TIMx_IC4	EVENTOUT
PA8	MCO	-	-	-	-	-	-	USART1_CK	-	-	[COM0]	-	-	TIMx_IC1	EVENTOUT
PA9	-	-	-	-	-	-	-	USART1_TX	-	-	[COM1]	-	-	TIMx_IC2	EVENTOUT
PA10	-	-	-	-	-	-	-	USART1_RX	-	-	[COM2]	-	-	TIMx_IC3	EVENTOUT
PA11	-	-	-	-	-	SPI1_MISO	-	USART1_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PA12	-	-	-	-	-	SPI1_MOSI	-	USART1_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PA15	JTDI	TIM2_CH1_ETR	-	-	-	SPI1_NSS	-	-	-	-	SEG17	-	-	TIMx_IC4	EVENTOUT
PB0	-	-	TIM3_CH3	-	-	-	-	-	-	-	[SEG5]	-	-	-	EVENTOUT
PB1	-	-	TIM3_CH4	-	-	-	-	-	-	-	[SEG6]	-	-	-	EVENTOUT
PB2	BOOT1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PB3	JTDO	TIM2_CH2	-	-	-	SPI1_SCK	-	-	-	-	[SEG7]	-	-	-	EVENTOUT

Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	-	-	-	-	[SEG8]	-	-	-	EVENTOUT
PB5	-	-	TIM3_CH2	-	I2C1_ SMBA	SPI1_MOSI	-	-	-	-	[SEG9]	-	-	-	EVENTOUT
PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	-	-	-	-	-	EVENTOUT
PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	-	-	EVENTOUT
PB8	-	-	TIM4_CH3	TIM10_CH1*	I2C1_SCL	-	-	-	-	-	SEG16	-	-	-	EVENTOUT
PB9	-	-	TIM4_CH4	TIM11_CH1*	I2C1_SDA	-	-	-	-	-	[COM3]	-	-	-	EVENTOUT
PB10	-	TIM2_CH3	-	-	I2C2_SCL	-	-	USART3_TX	-	-	SEG10	-	-	-	EVENTOUT
PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	SEG11	-	-	-	EVENTOUT
PB12	-	-	-	TIM10_CH1	I2C2_ SMBA	SPI2_NSS	-	USART3_CK	-	-	SEG12	-	-	-	EVENTOUT
PB13	-	-	-	TIM9_CH1	-	SPI2_SCK	-	USART3_CTS	-	-	SEG13	-	-	-	EVENTOUT
PB14	-	-	-	TIM9_CH2	-	SPI2_MISO	-	USART3_RTS	-	-	SEG14	-	-	-	EVENTOUT
PB15	-	-	-	TIM11_CH1	-	SPI2_MOSI	-	-	-	-	SEG15	-	-	-	EVENTOUT
PC0	-	-	-	-	-	-	-	-	-	-	SEG18	-	-	TIMx_IC1	EVENTOUT
PC1	-	-	-	-	-	-	-	-	-	-	SEG19	-	-	TIMx_IC2	EVENTOUT
PC2	-	-	-	-	-	-	-	-	-	-	SEG20	-	-	TIMx_IC3	EVENTOUT
PC3	-	-	-	-	-	-	-	-	-	-	SEG21	-	-	TIMx_IC4	EVENTOUT
PC4	-	-	-	-	-	-	-	-	-	-	SEG22	-	-	TIMx_IC1	EVENTOUT
PC5	-	-	-	-	-	-	-	-	-	-	SEG23	-	-	TIMx_IC2	EVENTOUT
PC6	-	-	TIM3_CH1	-	-	-	-	-	-	-	SEG24	-	-	TIMx_IC3	EVENTOUT
PC7	-	-	TIM3_CH2	-	-	-	-	-	-	-	SEG25	-	-	TIMx_IC4	EVENTOUT
PC8	-	-	TIM3_CH3	-	-	-	-	-	-	-	SEG26	-	-	TIMx_IC1	EVENTOUT
PC9	-	-	TIM3_CH4	-	-	-	-	-	-	-	SEG27	-	-	TIMx_IC2	EVENTOUT

Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PC10	-	-	-	-	-	-	-	USART3_TX	-	-	COM4 / SEG28 / SEG40	-	-	TIMx_IC3	EVENTOUT
PC11	-	-	-	-	-	-	-	USART3_RX	-	-	COM5 / SEG29 / SEG41	-	-	TIMx_IC4	EVENTOUT
PC12	-	-	-	-	-	-	-	USART3_CK	-	-	COM6 / SEG30 / SEG42	-	-	TIMx_IC1	EVENTOUT
PC13-WKUP2	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PC14-OSC32_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PC15-OSC32_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD0	-	-	-	TIM9_CH1	-	SPI2_NSS	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD1	-	-	-	-	-	SPI2_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD2	-	-	TIM3_ETR	-	-	-	-	-	-	-	COM7 / SEG31 / SEG43	-	-	TIMx_IC3	EVENTOUT
PD3	-	-	-	-	-	SPI2_MISO	-	USART2_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD4	-	-	-	-	-	SPI2_MOSI	-	USART2_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD7	-	-	-	TIM9_CH2	-	-	-	USART2_CK	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	-	-	TIMx_IC2	EVENTOUT

Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD11	-	-	-	-	-	-	-	USART3_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE0	-	-	TIM4_ETR	TIM10_CH1	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE1	-	-		TIM11_CH1	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE4	TRACED1	-	TIM3_CH2	-	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE5	TRACED2	-	-	TIM9_CH1*	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE6	TRACED3	-	-	TIM9_CH2*	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE7	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE8	-	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE9	-	TIM2_CH1_ETR	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE10	-	TIM2_CH2	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE11	-	TIM2_CH3	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PE12	-	TIM2_CH4	-	-	-	SPI1_NSS	-	-	-	-	-	-	-	TIMx_IC1	EVENTOUT
PE13	-	-	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PE14	-	-	-	-	-	SPI1_MISO	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PE15	-	-	-	-	-	SPI1_MOSI	-	-	-	-	-	-	-	TIMx_IC4	EVENTOUT
PH0-OSC_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

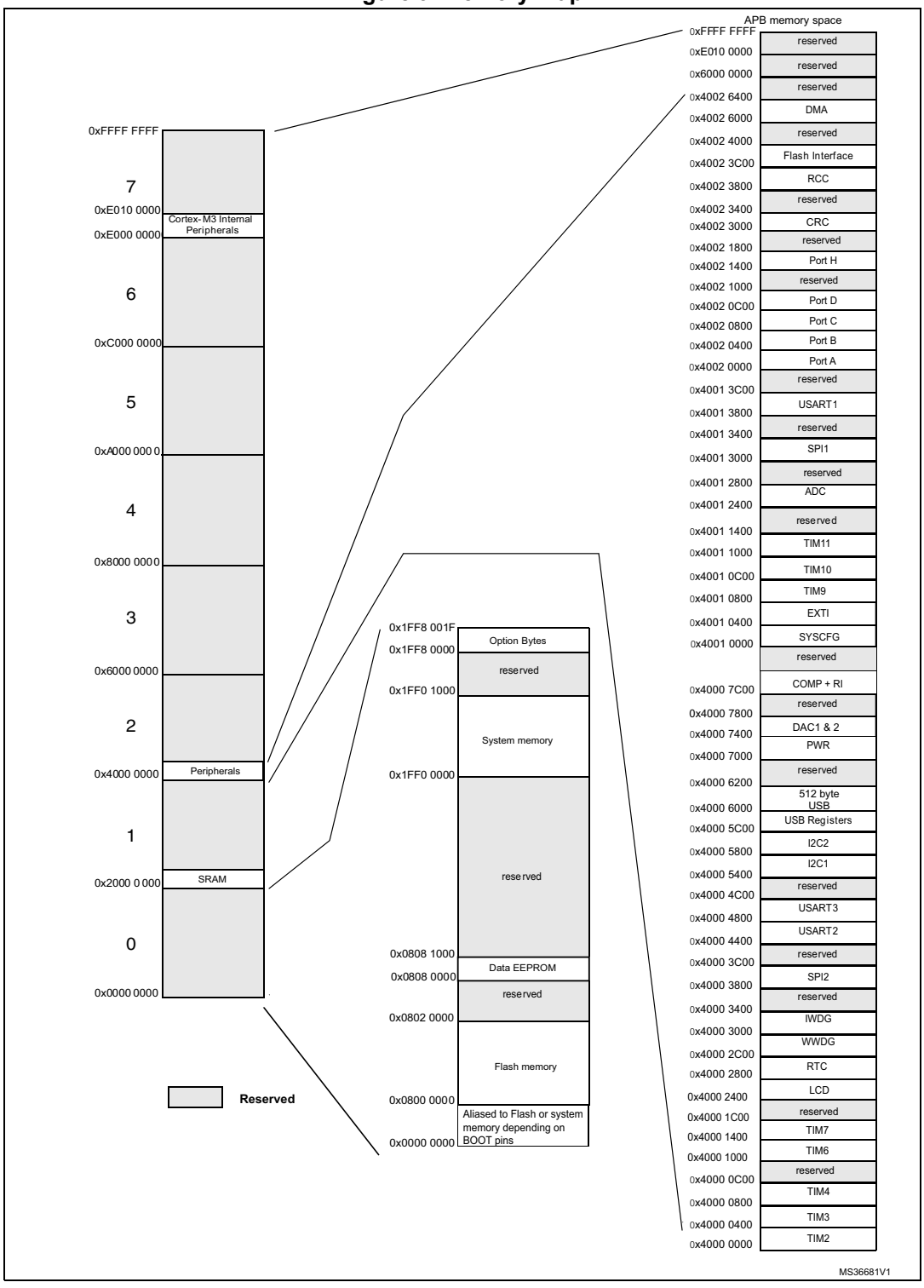
Table 10. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
PH1-OSC_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PH2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

5 Memory mapping

The memory map is shown in the following figure.

Figure 9. Memory map



6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

Please refer to device ErrataSheet for possible latest changes of electrical characteristics.

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.0 V (for the 1.65 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

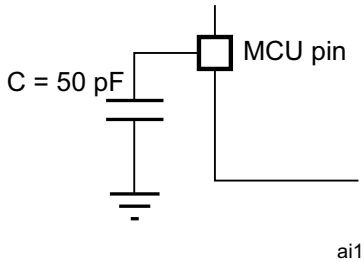
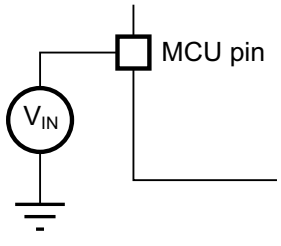
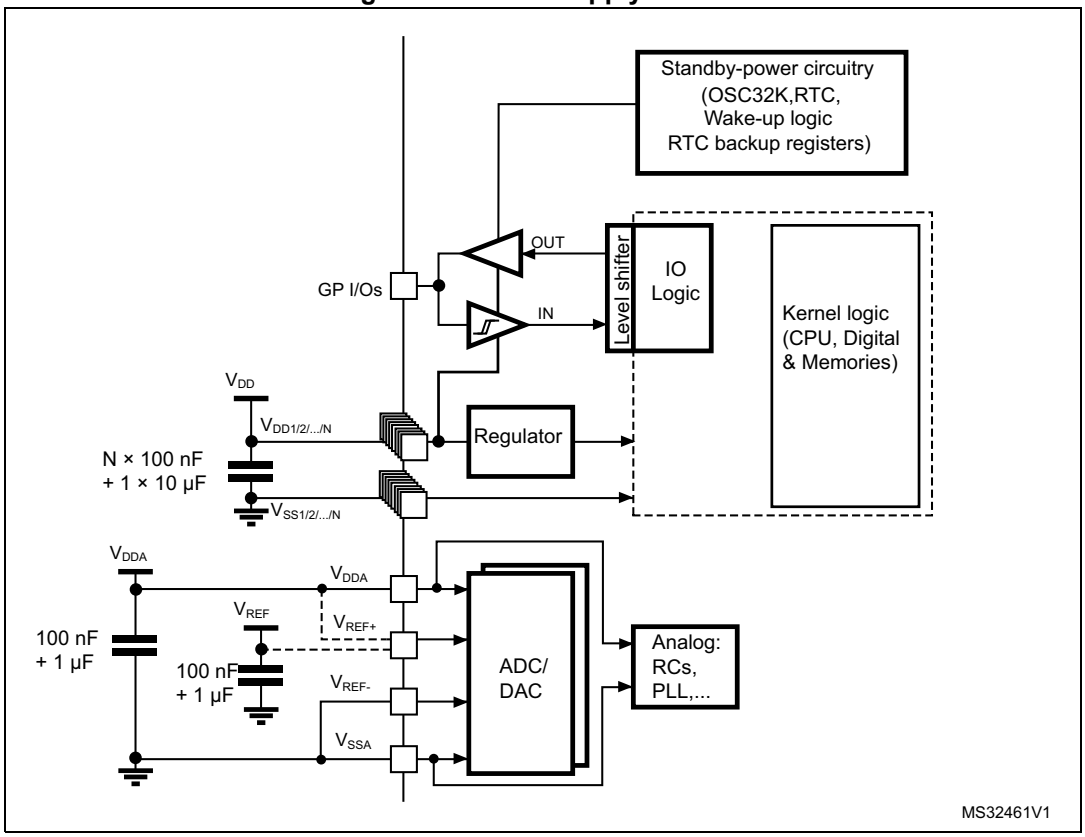


Figure 11. Pin input voltage



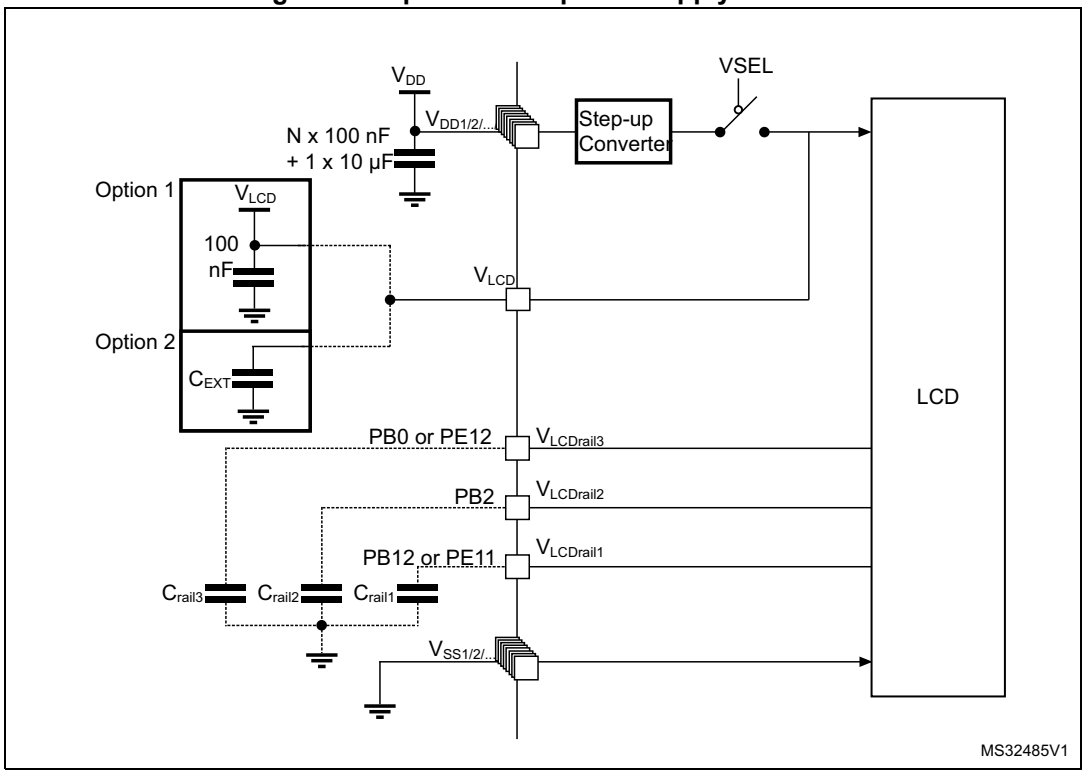
6.1.6 Power supply scheme

Figure 12. Power supply scheme



6.1.7 Optional LCD power supply scheme

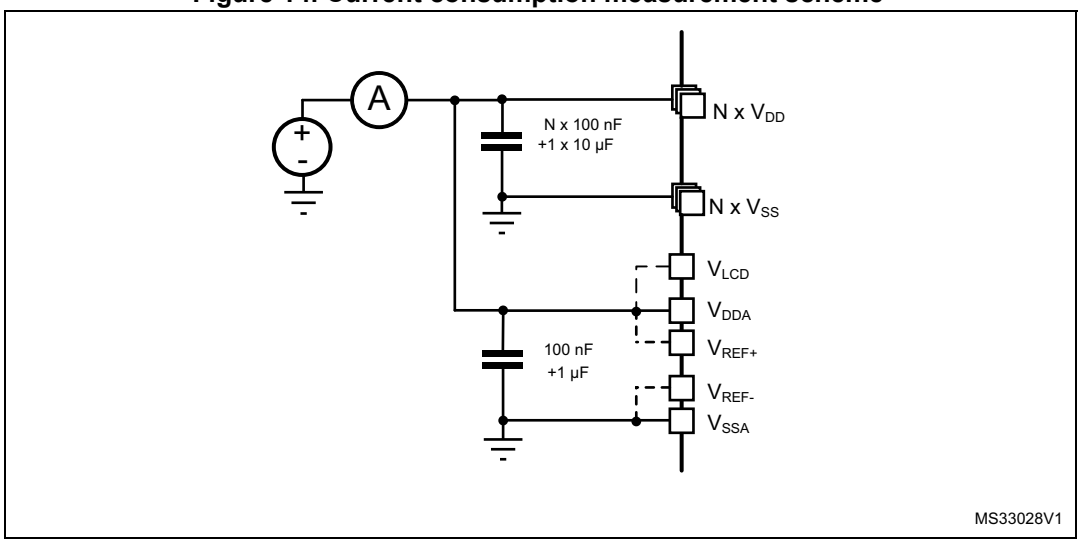
Figure 13. Optional LCD power supply scheme



1. Option 1: LCD power supply is provided by a dedicated VLCD supply source, VSEL switch is open.
2. Option 2: LCD power supply is provided by the internal step-up converter, VSEL switch is closed, an external capacitance is needed for correct behavior of this converter.

6.1.8 Current consumption measurement

Figure 14. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 11: Voltage characteristics*, *Table 12: Current characteristics*, and *Table 13: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 11. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five-volt tolerant pin	V_{SS} –0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all different ground pins(3)	-	50	
V_{REF+} –V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA}	-	0.4	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 12* for maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 12. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source)(1)	100	mA
ΣI_{VSS}(2)	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	100	
$I_{VDD(PIN)}$	Maximum current into each V_{DD_x} power pin (source)(1)	70	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS_x} ground pin (sink)(1)	-70	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	- 25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	60	
	Total output current sourced by sum of all IOs and control pins(2)	-60	
$I_{INJ(PIN)}$ (3)	Injected current on five-volt tolerant I/O(4) RST and B pins	-5/+0	
	Injected current on any other pin(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.17*.
4. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11* for maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 11: Voltage characteristics* for the maximum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C
T_{LEAD}	Maximum lead temperature during soldering	see note (1)	°C

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (ROHS directive 2011/65/EU, July 2011).

6.3 Operating conditions

6.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	32	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	32	
f_{PCLK2}	Internal APB2 clock frequency	-	0	32	
V_{DD}	Standard operating voltage	BOR detector disabled	1.65	3.6	V
		BOR detector enabled, at power on	1.8	3.6	
		BOR detector disabled, after power on	1.65	3.6	
V_{DDA} (1)	Analog operating voltage (ADC and DAC not used)	Must be the same voltage as V_{DD} (2)	1.65	3.6	V
	Analog operating voltage (ADC or DAC used)		1.8	3.6	
V_{IN}	I/O input voltage	FT pins: 2.0 V ≤V_{DD}	–0.3	5.5 (3)	V
		FT pins: V_{DD} < 2.0 V	–0.3	5.25 (3)	
		BOOT0	0	5.5	
		Any other pin	–0.3	V_{DD}+0.3	

Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D	Power dissipation at TA = 85 °C for suffix 6 or TA = 105 °C for suffix 7(4)	UFBGA100 package	-	339	mW
		LQFP100 package	-	435	
		TFBGA64 package	-	308	
		LQFP64 package	-	444	
		LQFP48 package	-	364	
		UFQFPN48 package	-	606	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation(5)	–40	85	°C
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	
T_J	Junction temperature range	6 suffix version	–40	105	°C
	Junction temperature range	7 suffix version	–40	110	

1. When the ADC is used, refer to *Table 55: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 13: Thermal characteristics on page 56*).
5. In low-power dissipation state, T_A can be extended to -40°C to 105°C temperature range as long as T_J does not exceed T_J max (see *Table 13: Thermal characteristics on page 56*).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in the following table.

Table 15. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	

Table 15. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	V
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.60	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	V
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization.
2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in the following table are based on characterization results, unless otherwise specified.

Table 16. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C ±5 °C, V_{DDA}= 3 V ±10 mV	0x1FF8 0078-0x1FF8 0079

Table 17. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$(1)	Internal reference voltage	– 40 °C < T_J < +110 °C	1.202	1.224	1.242	V
I_{REFINT}	Internal reference current consumption	-	-	1.4	2.3	µA
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REF} value (2)	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}(3)	Temperature coefficient	–40 °C < T_J < +110 °C	-	25	100	ppm/°C
A_{Coeff}(3)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(3)(4)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S_vrefint}$(3)	ADC sampling time when reading the internal reference voltage	-	4	-	-	µs
T_{ADC_BUF}(3)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(3)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(3)	VREF_OUT output current(5)	-	-	-	1	µA
C_{VREF_OUT}(3)	VREF_OUT output load	-	-	-	50	pF
I_{LPBUF}(3)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(3)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(3)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(3)	3/4 reference voltage	-	74	75	76	

1. Guaranteed by test in production.
2. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
3. Guaranteed by characterization results.
4. Shortest sampling time can be determined in the application by multiple interactions.
5. To guarantee less than 1% VREF_OUT deviation.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code, unless otherwise specified.

The current consumption values are derived from the tests performed under ambient temperature T_A=25°C and V_{DD} supply voltage conditions summarized in *Table 14: General operating conditions*, unless otherwise specified.

The MCU is placed under the following conditions:

- All I/O pins are configured in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time, 64-bit access and prefetch is adjusted depending on f_{HCLK} frequency and voltage range to provide the best CPU performance.
- When the peripherals are enabled $f_{APB1} = f_{APB2} = f_{AHB}$.
- When PLL is ON, the PLL inputs are equal to HSI = 16 MHz (if internal clock is used) or HSE = 16 MHz (if HSE bypass mode is used).
- The HSE user clock applied to OSC_IN input follows the characteristics specified in *Table 27: High-speed external user clock characteristics*.
- For maximum current consumption $V_{DD} = V_{DDA}$ = 3.6 V is applied to all supply pins.
- For typical current consumption $V_{DD} = V_{DDA}$ = 3.0 V is applied to all supply pins if not specified otherwise.

Table 18. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	215	285	µA
				2 MHz	400	490	
				4 MHz	725	1000	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.915	1.3	mA
				8 MHz	1.75	2.15	
				16 MHz	3.4	4	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	2.1	2.9	
				16 MHz	4.2	5.2	
				32 MHz	8.25	9.6	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	3.5	4.4	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	8.2	10.2	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	0.041	0.085	
		MSI clock, 524 kHz		524 kHz	0.125	0.180	
		MSI clock, 4.2 MHz		4.2 MHz	0.775	0.935	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 19. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	185	255	µA
				2 MHz	345	435	
				4 MHz	645	930	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.755	1.5	mA
				8 MHz	1.5	2.2	
				16 MHz	3.0	3.6	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	1.8	2.9	
				16 MHz	3.6	4.3	
				32 MHz	7.15	8.5	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	2.95	3.7	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	7.15	8.7	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	39	115	µA
		MSI clock, 524 kHz		524 kHz	110	205	
		MSI clock, 4.2 MHz		4.2 MHz	690	870	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 20. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	50	155	µA
				2 MHz	78.5	235	
				4 MHz	140	370(3)	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	165	375	
				8 MHz	310	530	
				16 MHz	590	1000	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	350	615	
				16 MHz	680	1200	
				32 MHz	1600	2350	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	640	970	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1600	2350	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	19	60	
		MSI clock, 524 kHz		524 kHz	33	90	
		MSI clock, 4.2 MHz		4.2 MHz	145	210	
	Supply current in Sleep mode, Flash ON	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	60.5	145	µA
				2 MHz	89.5	225	
				4 MHz	150	360	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	180	370	
				8 MHz	320	490	
				16 MHz	605	895	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	380	565	
				16 MHz	695	1070	
				32 MHz	1600	2200	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	650	970	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1600	2320	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2V VOS[1:0] = 11	65 kHz	29.5	65	
		MSI clock, 524 kHz		524 kHz	44	80	
		MSI clock, 4.2 MHz		4.2 MHz	155	220	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)
3. Guaranteed by test in production.

Table 21. Current consumption in Low-power run mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (LP Run)	Supply current in Low-power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	10.9	12	µA
				T_A = 85 °C	16.5	23	
				T_A = 105 °C	26	47	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	15	16	
				T_A = 85 °C	22	29	
				T_A = 105 °C	32	51	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	29	37	
				T_A = 55 °C	32.5	40	
				T_A = 85 °C	35.5	54	
				T_A = 105 °C	45	65	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	23	24	
				T_A = 85 °C	31	34	
				T_A = 105 °C	42.5	56	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	29	31	
				T_A = 85 °C	38	41	
				T_A = 105 °C	49	63	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	46	55	
				T_A = 55 °C	48	59	
				T_A = 85 °C	53.5	72	
				T_A = 105 °C	64.8	84	
I_{DD} Max (LP Run)(2)	Max allowed current in Low-power run mode	V_{DD} from 1.65 V to 3.6 V	-	-	-	200	

1. Guaranteed by characterization results, unless otherwise specified.
2. This limitation is related to the consumption of the CPU core and the peripherals that are powered by the regulator. Consumption of the I/Os is not included in this limitation.

Table 22. Current consumption in Low-power sleep mode

Symbol	Parameter	Conditions			Typ	Max (1)	Unit
I_{DD} (LP Sleep)	Supply current in Low-power sleep mode	All peripherals OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz Flash OFF	T_A = -40 °C to 25 °C	5.5	-	µA
			MSI clock, 65 kHz f_{HCLK} = 32 kHz Flash ON	T_A = -40 °C to 25 °C	15	16	
				T_A = 85 °C	20	23	
				T_A = 105 °C	24	26	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz, Flash ON	T_A = -40 °C to 25 °C	15	16	
				T_A = 85 °C	20.5	23	
				T_A = 105 °C	25.4	27	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz, Flash ON	T_A = -40 °C to 25 °C	18	20	
				T_A = 55 °C	21	22	
				T_A = 85 °C	23	27	
				T_A = 105 °C	28	31	
		TIM9 and USART1 enabled, Flash ON, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	15	16	
				T_A = 85 °C	20	22	
				T_A = 105 °C	24	26	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	15	16	
				T_A = 85 °C	20.5	23	
				T_A = 105 °C	25.4	27	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	18	20	
				T_A = 55 °C	21	22	
				T_A = 85 °C	23	27	
				T_A = 105 °C	28	30	
I_{DD} Max (LP Sleep)	Max allowed current in Low-power Sleep mode	V_{DD} from 1.65 V to 3.6 V	-	-	-	200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 23. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions			Typ(1)	Max (1)(2)	Unit
I_{DD} (Stop with RTC)	Supply current in Stop mode with RTC enabled	RTC clocked by LSI, regulator in LP mode, HSI and HSE OFF (no independent watchdog)	LCD OFF	T_A = -40°C to 25°C V_{DD} = 1.8 V	1.13	-	µA
				T_A = -40°C to 25°C	1.38	4	
				T_A = 55°C	1.70	6	
				T_A= 85°C	3.30	10	
				T_A = 105°C	7.80	23	
			LCD ON (static duty)(3)	T_A = -40°C to 25°C	1.50	6	
				T_A = 55°C	1.80	7	
				T_A= 85°C	3.45	12	
				T_A = 105°C	8.02	27	
			LCD ON (1/8 duty)(4)	T_A = -40°C to 25°C	3.80	10	
				T_A = 55°C	4.30	11	
				T_A= 85°C	6.10	16	
				T_A = 105°C	10.8	44	
		RTC clocked by LSE external clock (32.768 kHz), regulator in LP mode, HSI and HSE OFF (no independent watchdog)	LCD OFF	T_A = -40°C to 25°C	1.50	-	
				T_A = 55°C	1.90	-	
				T_A= 85°C	3.65	-	
				T_A = 105°C	8.25	-	
			LCD ON (static duty)(3)	T_A = -40°C to 25°C	1.60	-	
				T_A = 55°C	2.05	-	
				T_A= 85°C	3.75	-	
				T_A = 105°C	8.40	-	
			LCD ON (1/8 duty)(4)	T_A = -40°C to 25°C	3.90	-	
				T_A = 55°C	4.55	-	
				T_A= 85°C	6.35	-	
				T_A = 105°C	11.10	-	
		RTC clocked by LSE (no independent watchdog)(5)	LCD OFF	T_A = -40°C to 25°C V_{DD} = 1.8 V	1.23	-	
				T_A = -40°C to 25°C V_{DD} = 3.0 V	1.50	-	
				T_A = -40°C to 25°C V_{DD} = 3.6 V	1.75	-	

Table 23. Typical and maximum current consumptions in Stop mode (continued)

Symbol	Parameter	Conditions		Typ(1)	Max (1)(2)	Unit
$I_{DD\ (Stop)}$	Supply current in Stop mode (RTC disabled)	Regulator in LP mode, HSI and HSE OFF, independent watchdog and LSI enabled	T_A = -40°C to 25°C	1.80	2.2	µA
		Regulator in LP mode, LSI, HSI and HSE OFF (no independent watchdog)	T_A = -40°C to 25°C	0.434	1	
			T_A = 55°C	0.735	3	
			T_A= 85°C	2.350	9	
			T_A = 105°C	6.84	22(6)	
$I_{DD\ (WU\ from\ Stop)}$	RMS (root mean square) supply current during wakeup time when exiting from Stop mode	MSI = 4.2 MHz	V_{DD} = 3.0 V T_A = -40°C to 25°C	2	-	mA
		MSI = 1.05 MHz		1.45	-	
		MSI = 65 kHz(7)		1.45	-	

1. The typical values are given for V_{DD} = 3.0 V and max values are given for V_{DD} = 3.6 V, unless otherwise specified.
2. Guaranteed by characterization results, unless otherwise specified.
3. LCD enabled with external VLCD, static duty, division ratio = 256, all pixels active, no LCD connected.
4. LCD enabled with external VLCD, 1/8 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
5. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.
6. Guaranteed by test in production.
7. When MSI = 64 kHz, the RMS current is measured over the first 15 µs following the wakeup event. For the remaining time of the wakeup period, the current is similar to the Run mode current.

Table 24. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions		Typ(1)	Max (1)(2)	Unit
I_{DD} (Standby with RTC)	Supply current in Standby mode with RTC enabled	RTC clocked by LSI (no independent watchdog)	T_A = -40 °C to 25 °C V_{DD} = 1.8 V	0.865	-	µA
			T_A = -40 °C to 25 °C	1.11	1.9	
			T_A = 55 °C	1.15	2.2	
			T_A= 85 °C	1.35	4	
			T_A = 105 °C	1.93	8.3(3)	
		RTC clocked by LSE (no independent watchdog)(4)	T_A = -40 °C to 25 °C V_{DD} = 1.8 V	0.97	-	
			T_A = -40 °C to 25 °C	1.28	-	
			T_A = 55 °C	1.4	-	
			T_A= 85 °C	1.7	-	
			T_A = 105 °C	2.34	-	
I_{DD} (Standby)	Supply current in Standby mode with RTC disabled	Independent watchdog and LSI enabled	T_A = -40 °C to 25 °C	1.0	1.7	
		Independent watchdog and LSI OFF	T_A = -40 °C to 25 °C	0.277	0.6	
			T_A = 55 °C	0.31	0.9	
			T_A = 85 °C	0.52	2.75	
			T_A = 105 °C	1.09	7(3)	
I_{DD} (WU from Standby)	RMS supply current during wakeup time when exiting from Standby mode	-	V_{DD} = 3.0 V T_A = -40 °C to 25 °C	1	-	mA

1. The typical values are given for V_{DD} = 3.0 V and max values are given for V_{DD} = 3.6 V, unless otherwise specified.
2. Guaranteed by characterization results, unless otherwise specified.
3. Guaranteed by test in production.
4. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8pF loading capacitors.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on

Table 25. Peripheral current consumption(1)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}= 1.8 V VOS[1:0] = 01	Range 2, V_{CORE}= 1.5 V VOS[1:0] = 10	Range 3, V_{CORE}= 1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB1	TIM2	11.3	9.0	7.3	9.0	µA/MHz (f_{HCLK})
	TIM3	11.4	9.1	7.1	9.1	
	TIM4	11.3	9.0	7.3	9.0	
	TIM6	3.9	3.1	2.5	3.1	
	TIM7	4.2	3.3	2.6	3.3	
	LCD	4.7	3.6	2.9	3.6	
	WWDG	3.7	2.9	2.4	2.9	
	SPI2	5.9	4.8	3.9	4.8	
	USART2	8.1	6.6	5.1	6.6	
	USART3	7.9	6.4	5.0	6.4	
	I2C1	7.8	6.1	4.9	6.1	
	I2C2	7.2	5.7	4.6	5.7	
	USB	12.7	10.3	8.1	10.3	
	PWR	3.1	2.4	2.0	2.4	
	DAC	6.6	5.3	4.3	5.3	
	COMP	5.3	4.3	3.4	4.3	
APB2	SYSCFG & RI	2.2	1.9	1.6	1.9	µA/MHz (f_{HCLK})
	TIM9	9.1	7.3	5.9	7.3	
	TIM10	6.0	4.9	3.9	4.9	
	TIM11	5.8	4.6	3.8	4.6	
	ADC(2)	8.7	7.0	5.6	7.0	
	SPI1	4.4	3.4	2.8	3.4	
	USART1	8.1	6.5	5.2	6.5	
AHB	GPIOA	4.4	3.5	2.9	3.5	
	GPIOB	4.4	3.5	2.9	3.5	
	GPIOC	3.7	3.0	2.5	3.0	
	GPIOD	3.6	2.8	2.4	2.8	
	GPIOE	4.7	3.8	3.1	3.8	
	GPIOH	3.7	2.9	2.4	2.9	
	CRC	0.6	0.4	0.4	0.4	
	FLASH	12.2	10.2	7.8	-(3)	
	DMA1	12.4	10.1	8.2	10.1	
All enabled		160	135	103	124.8	

Table 25. Peripheral current consumption(1) (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}= 1.8 V VOS[1:0] = 01	Range 2, V_{CORE}= 1.5 V VOS[1:0] = 10	Range 3, V_{CORE}= 1.2 V VOS[1:0] = 11	Low-power sleep and run	
$I_{DD\ (RTC)}$		0.4				µA
$I_{DD\ (LCD)}$		3.1				
$I_{DD\ (ADC)}$(4)		1450				
$I_{DD\ (DAC)}$(5)		340				
$I_{DD\ (COMP1)}$		0.16				
$I_{DD\ (COMP2)}$	Slow mode	2				
	Fast mode	5				
$I_{DD\ (PVD / BOR)}$(6)		2.6				
$I_{DD\ (IWDG)}$		0.25				

1. Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (Range 1), f_{HCLK} = 16 MHz (Range 2), f_{HCLK} = 4 MHz (Range 3), f_{HCLK} = 64kHz (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling.
2. HSI oscillator is OFF for this measure.
3. In low-power sleep and run mode, the Flash memory must always be in power-down mode.
4. Data based on a differential I_{DD} measurement between ADC in reset configuration and continuous ADC conversion (HSI consumption not included).
5. Data based on a differential I_{DD} measurement between DAC in reset configuration and continuous DAC conversion of V_{DD}/2. DAC is in buffered mode, output is left floating.
6. Including supply current of internal reference voltage.

6.3.5 Wakeup time from Low-power mode

The wakeup times given in the following table are measured with the MSI RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is the MSI oscillator in the range configured before entering Stop mode
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	f_{HCLK} = 32 MHz	0.4	-	µs
$t_{WUSLEEP_LP}$	Wakeup from Low-power sleep mode f_{HCLK} = 262 kHz	f_{HCLK} = 262 kHz Flash enabled	46	-	
		f_{HCLK} = 262 kHz Flash switched OFF	46	-	
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz	8.2	-	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage Range 1 and 2	7.7	8.9	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage Range 3	8.2	13.1	
		$f_{HCLK} = f_{MSI}$ = 2.1 MHz	10.2	13.4	
		$f_{HCLK} = f_{MSI}$ = 1.05 MHz	16	20	
		$f_{HCLK} = f_{MSI}$ = 524 kHz	31	37	
		$f_{HCLK} = f_{MSI}$ = 262 kHz	57	66	
		$f_{HCLK} = f_{MSI}$ = 131 kHz	112	123	
		f_{HCLK} = MSI = 65 kHz	221	236	
$t_{WUSTDBY}$	Wakeup from Standby mode FWU bit = 1	f_{HCLK} = MSI = 2.1 MHz	58	104	
	Wakeup from Standby mode FWU bit = 0	f_{HCLK} = MSI = 2.1 MHz	2.6	3.25	ms

1. Guaranteed by characterization results, unless otherwise specified

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

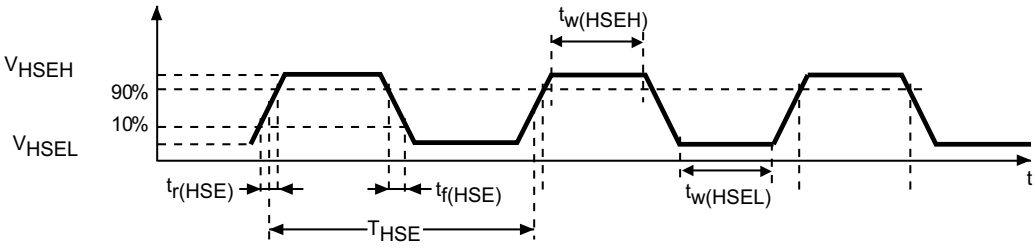
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 15*.

Table 27. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0			
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance	-	-	2.6	-	pF

1. Guaranteed by design.

Figure 15. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

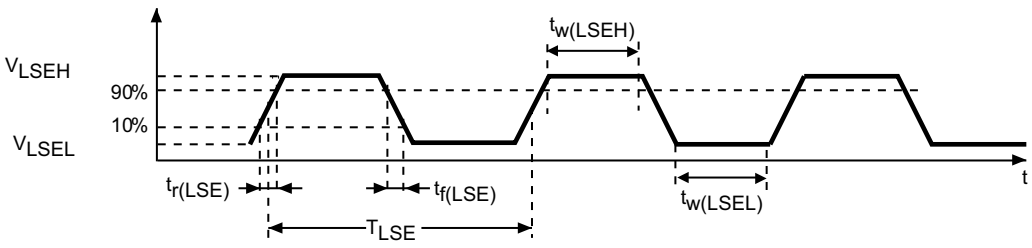
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 14*.

Table 28. Low-speed external user clock characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	$0.7V_{DD}$	-	V_{DD}	-
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	$0.3V_{DD}$	-
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	0.6	-	pF

1. Guaranteed by design.

Figure 16. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 29*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 29. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		24	MHz
R_F	Feedback resistor	-		200	-	kΩ

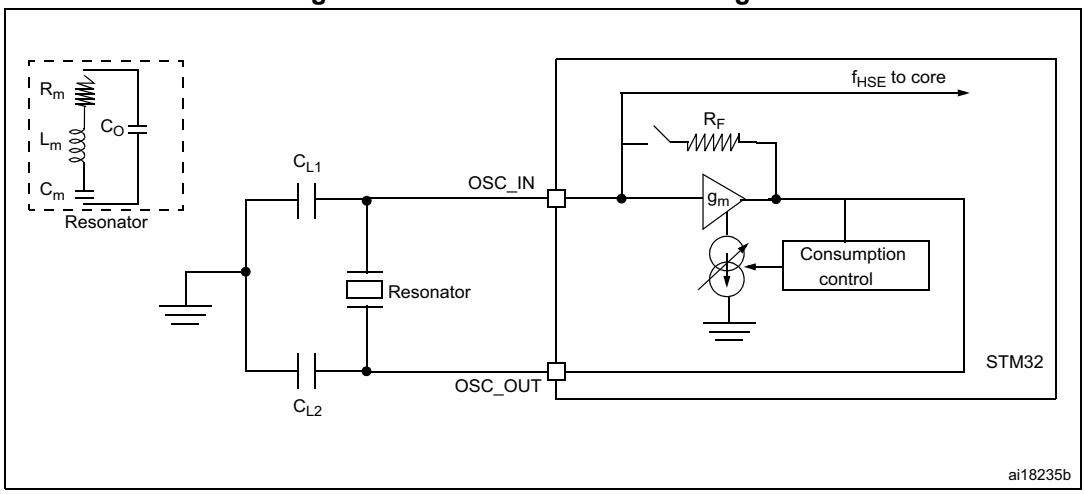
Table 29. HSE oscillator characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	20	-	pF
I_{HSE}	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA /V
$t_{SU(HSE)}$ (4)	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 17. HSE oscillator circuit diagram



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 14*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 30. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

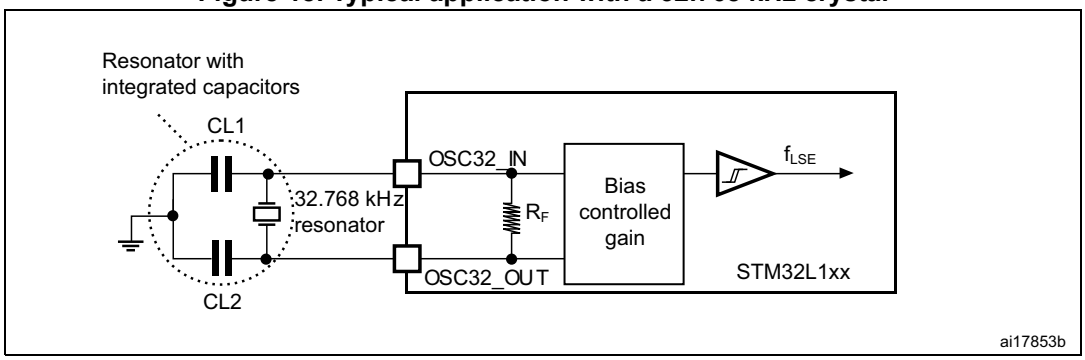
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_F	Feedback resistor	-	-	1.2	-	MΩ
$C^{(2)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 kΩ	-	8	-	pF
I_{LSE}	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}	-	-	1.1	µA
$I_{DD\ (LSE)}$	LSE oscillator current consumption	V_{DD} = 1.8 V	-	450	-	nA
		V_{DD} = 3.0 V	-	600	-	
		V_{DD} = 3.6V	-	750	-	
g_m	Oscillator transconductance	-	3	-	-	µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	s

1. Guaranteed by characterization results.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For CL1 and CL2, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 18). CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.
Load capacitance CL has the following formula: CL = CL1 x CL2 / (CL1 + CL2) + Cstray where Cstray is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of CL1 and CL2 (15 pF) it is strongly recommended to use a resonator with a load capacitance CL ≤ 7 pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if the user chooses a resonator with a load capacitance of CL = 6 pF and Cstray = 2 pF, then CL1 = CL2 = 8 pF.

Figure 18. Typical application with a 32.768 kHz crystal



6.3.7 Internal clock source characteristics

The parameters given in the following table are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

High-speed internal (HSI) RC oscillator

Table 31. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI user-trimmed resolution	Trimming code is not a multiple of 16	-	±0.4	0.7	%
		Trimming code is a multiple of 16	-	-	±1.5	%
$ACC_{HSI}^{(2)}$	Accuracy of the factory-calibrated HSI oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1(3)	-	1(3)	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = -40 to 105 °C	-4	-	3	%
$t_{SU(HSI)}^{(2)}$	HSI oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI)}^{(2)}$	HSI oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Low-speed internal (LSI) RC oscillator

Table 32. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(1)}$	LSI frequency	26	38	56	kHz
$D_{LSI}^{(2)}$	LSI oscillator frequency drift 0°C ≤T_A ≤85°C	-10	-	4	%
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

Multi-speed internal (MSI) RC oscillator

Table 33. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at V_{DD}= 3.3 V and T_A = 25 °C	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	
		MSI range 4	1.05	-	MHz
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤T_A ≤105 °C	-	±3	-	%
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤V_{DD} ≤3.6 V, T_A = 25 °C	-	-	2.5	%/V
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	

Table 33. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$t_{STAB(MSI)}$(2)	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage Range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results.

6.3.8 PLL characteristics

The parameters given in *Table 34* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 34. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	2	-	24	MHz
	PLL input clock duty cycle	45	-	55	%
f_{PLL_OUT}	PLL output clock	2	-	32	MHz
t_{LOCK}	PLL lock time PLL input = 16 MHz PLL VCO = 96 MHz	-	115	160	µs
Jitter	Cycle-to-cycle jitter	-	-	± 600	ps
I_{DDA}(PLL)	Current consumption on V_{DDA}	-	220	450	µA
I_{DD}(PLL)	Current consumption on V_{DD}	-	120	150	

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

6.3.9 Memory characteristics

The characteristics are given at T_A = -40 to 105 °C unless otherwise specified.

RAM memory

Table 35. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode(1)	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 36. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming / erasing time for byte / word / double word / half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during whole program/erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	300	-	µA
	Maximum current (peak) during program/erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 37. Flash memory, data EEPROM endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
NCYC(2)	Cycling (erase / write) Program memory	T_A = -40°C to 105 °C	10	-	-	kcycles
	Cycling (erase / write) EEPROM data memory		300	-	-	
t_{RET}(2)	Data retention (program memory) after 10 kcycles at T_A = 85 °C	TRET = +85 °C	30	-	-	years
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 85 °C		30	-	-	
	Data retention (program memory) after 10 kcycles at T_A = 105 °C	TRET = +105 °C	10	-	-	
	Data retention (EEPROM data memory) after 300 kcycles at T_A = 105 °C		10	-	-	

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during the device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 38*. They are based on the EMS levels and classes defined in application note AN1709.

Table 38. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 39. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. frequency range			Unit
				4 MHz voltage Range 3	16 MHz voltage Range 2	32 MHz voltage Range 1	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	-16	-7	-3	dBµV
			30 to 130 MHz	-12	2	12	
			130 MHz to 1GHz	-11	0	8	
			SAE EMI Level	1	1.5	2	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114, ANSI/ESD STM5.3.1 standard.

Table 40. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	All	C4	500	V

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 41. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence, oscillator frequency deviation, LCD levels).

The test results are given in *Table 42*.

Table 42. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all 5 V tolerant (FT) pins	-5	NA(1)	mA
	Injected current on BOOT0	-0	NA(1)	
	Injected current on any other pin	-5	+5	

1. Injection is not possible.

Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 43. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TC and FT I/O	-	-	0.3 V_{DD}(1)(2)	V
		BOOT0	-		0.14 V_{DD}(2)	
V_{IH}	Input high level voltage	TC I/O	0.45 V_{DD}+0.38(2)	-	-	
		FT I/O	0.39 V_{DD}+0.59(2)	-	-	
		BOOT0	0.15 V_{DD}+0.56(2)	-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis(2)	TC and FT I/O	-	10% V_{DD}(3)	-	
		BOOT0	-	0.01	-	
I_{lkg}	Input leakage current(4)	$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with LCD	-	-	±50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches and LCD	-	-	±50	
		$V_{SS} \le V_{IN} \le V_{DD}$ I/Os with USB	-	-	±250	
		$V_{SS} \le V_{IN} \le V_{DD}$ TC and FT I/O	-	-	±50	
		FT I/O $V_{DD} \le V_{IN} \le 5V$	-	-	±10	uA
R_{PU}	Weak pull-up equivalent resistor(5)(1)	$V_{IN} = V_{SS}$	25	45	65	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	25	45	65	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by test in production.
2. Guaranteed by design.
3. With a minimum of 200 mV.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with the non-standard V_{OL}/V_{OH} specifications given in *Table 44*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 12*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 12*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

Table 44. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)(2)}$	Output low level voltage for an I/O pin	I_{IO} = 8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
$V_{OH}^{(3)(2)}$	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	I_{IO} = 4 mA 1.65 V < V_{DD} < 2.7 V	-	0.45	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin		V_{DD}-0.45	-	
$V_{OL}^{(1)(4)}$	Output low level voltage for an I/O pin	I_{IO} = 15 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
$V_{OH}^{(3)(4)}$	Output high level voltage for an I/O pin		V_{DD}-1.3	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. Guaranteed by test in production.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 19* and *Table 45*, respectively.

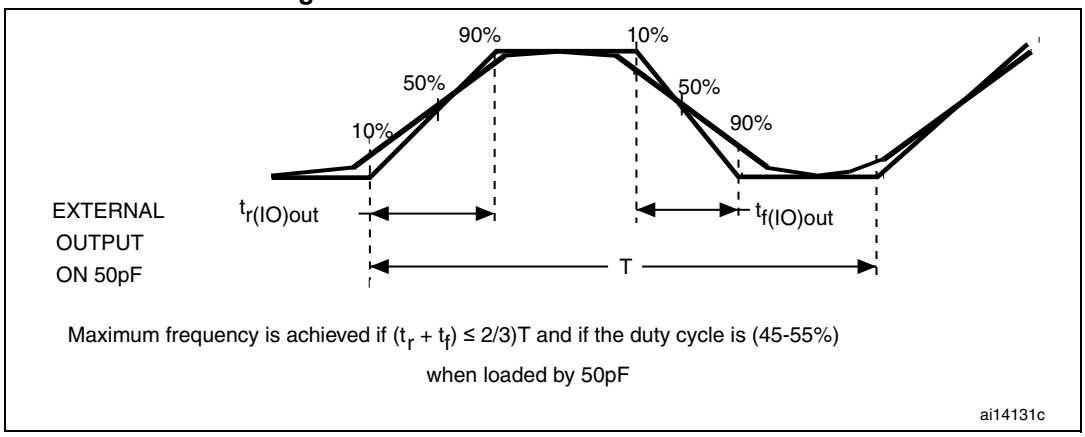
Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 45. I/O AC characteristics(1)

OSPEEDRx [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max(2)	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	400	kHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	400	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	625	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	625	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	2	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	1	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	125	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	250	
10	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	10	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	2	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	25	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	125	
11	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	8	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	30	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	8	-	

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. The maximum frequency is defined in *Figure 19*.

Figure 19. I/O AC characteristics definition



6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, RPU (see *Table 46*).

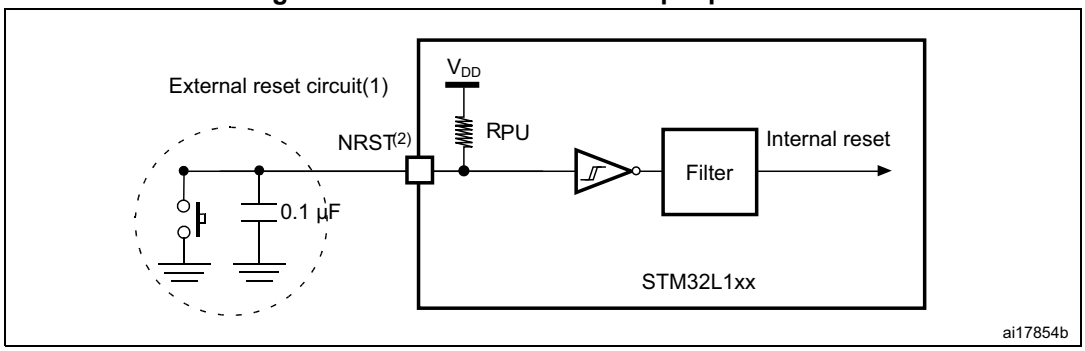
Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 46. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-	-	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	0.39 V_{DD}+0.59	-		
$V_{OL(NRST)}$(1)	NRST output low level voltage	I_{OL} = 2 mA 2.7 V < V_{DD} < 3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA 1.65 V < V_{DD} < 2.7 V	-	-		
$V_{hys(NRST)}$(1)	NRST Schmitt trigger voltage hysteresis	-	-	10%V_{DD}(2)		mV
R_{PU}	Weak pull-up equivalent resistor(3)	V_{IN} = V_{SS}	25	45	65	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	-	350	-	-	ns

1. Guaranteed by design.
2. 200 mV minimum value.
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

Figure 20. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets. 0.1 uF capacitor must be placed as close as possible to the chip.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 46*. Otherwise the reset will not be taken into account by the device.

6.3.15 TIM timer characteristics

The parameters given in *Table 47* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 47. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	16	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

6.3.16 Communication interfaces

I^2C interface characteristics

The STM32L151x6/8/B-A and STM32L152x6/8/B-A product line I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: SDA and SCL are not “true” open-drain I/O pins. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

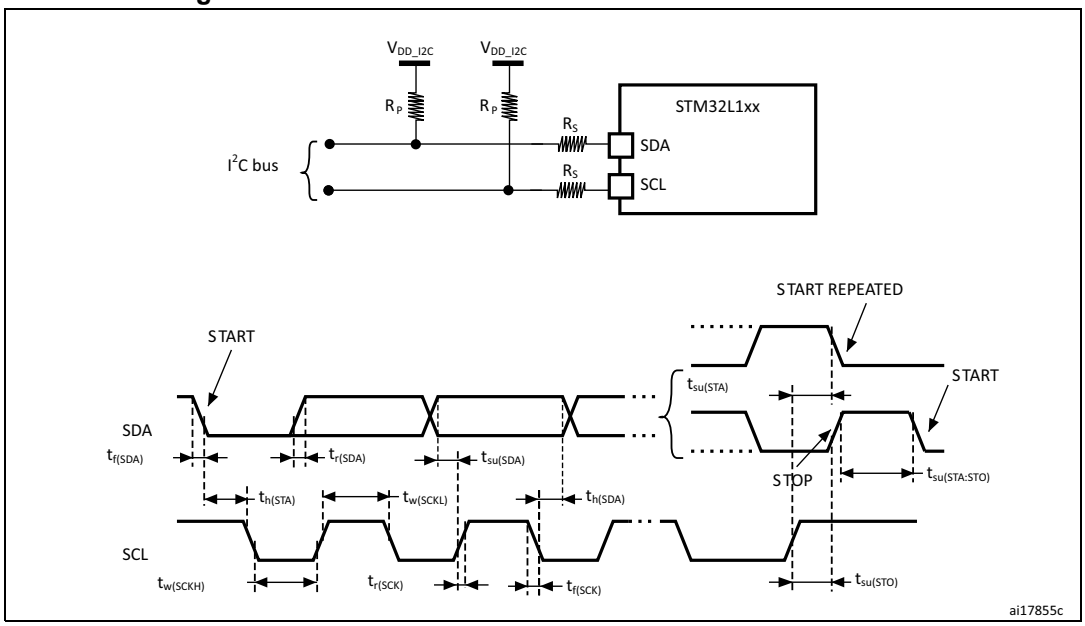
The I^2C characteristics are described in *Table 48*. Refer also to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 48. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)(2)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	0	50(4)	0	50(4)	ns

1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. The minimum width of the spikes filtered by the analog filter is above $t_{SP(max)}$.

Figure 21. I²C bus AC waveforms and measurement circuit



1. R_S = series protection resistors
2. R_P = pull-up resistors
3. V_{DD_I2C} = I2C bus supply
4. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 49. SCL frequency (f_{PCLK1}= 32 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801B
300	0x8024
200	0x8035
100	0x00A0
50	0x0140
20	0x0320

1. R_P = External pull-up resistance, f_{SCL} = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14*.

Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 50. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max(2)	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	16	
		Slave transmitter	-	12(3)	
$t_{r(SCK)}$(2) $t_{f(SCK)}$(2)	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{HCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{HCLK}$	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode	$t_{SCK}/2-5$	$t_{SCK}/2+3$	
$t_{su(MI)}$(2)	Data input setup time	Master mode	5	-	
$t_{su(SI)}$(2)		Slave mode	6	-	
$t_{h(MI)}$(2)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$(2)		Slave mode	5	-	
$t_{a(SO)}$(4)	Data output access time	Slave mode	0	$3t_{HCLK}$	
$t_{v(SO)}$(2)	Data output valid time	Slave mode	-	33	
$t_{v(MO)}$(2)	Data output valid time	Master mode	-	6.5	
$t_{h(SO)}$(2)	Data output hold time	Slave mode	17	-	
$t_{h(MO)}$(2)		Master mode	0.5	-	

1. The characteristics above are given for voltage Range 1.
2. Guaranteed by characterization results.
3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.
4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

Figure 22. SPI timing diagram - slave mode and CPHA = 0

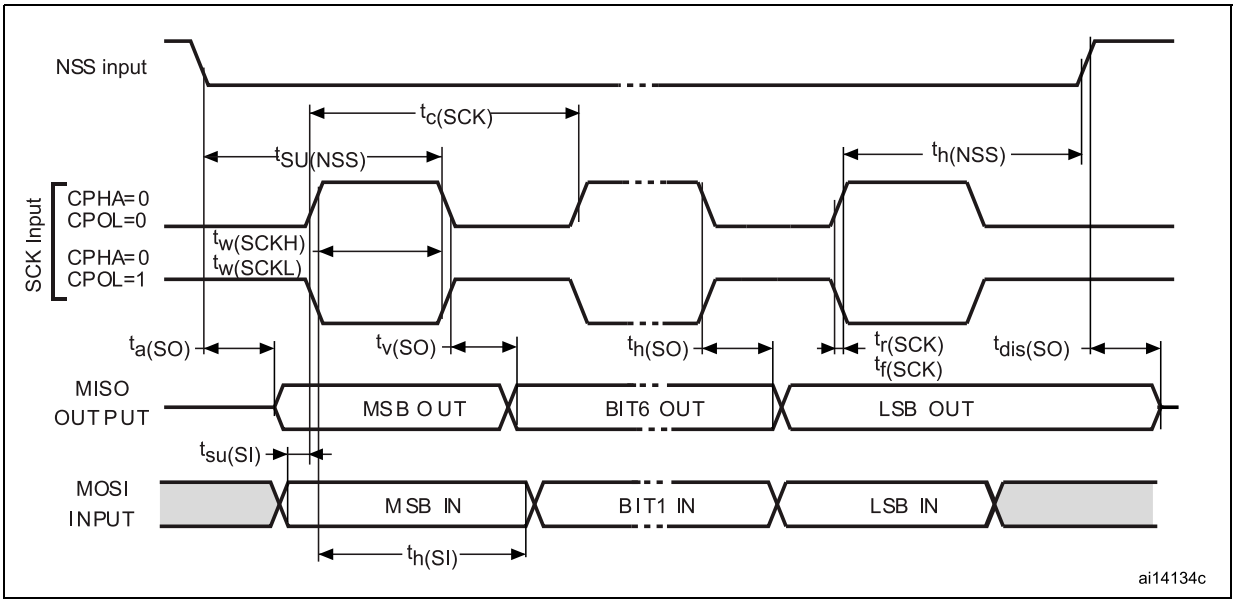
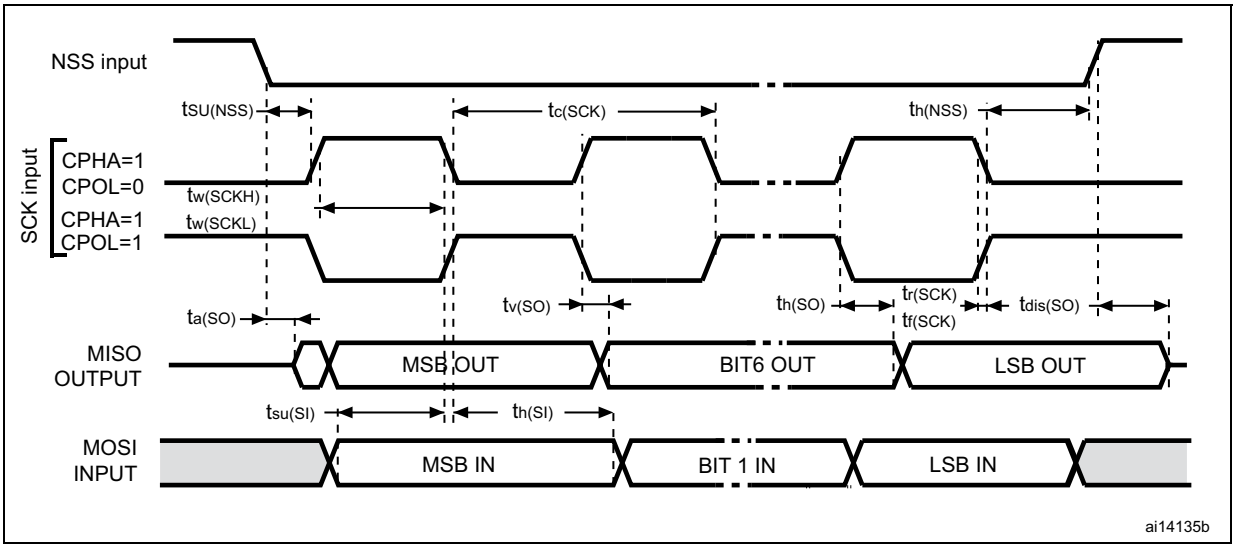
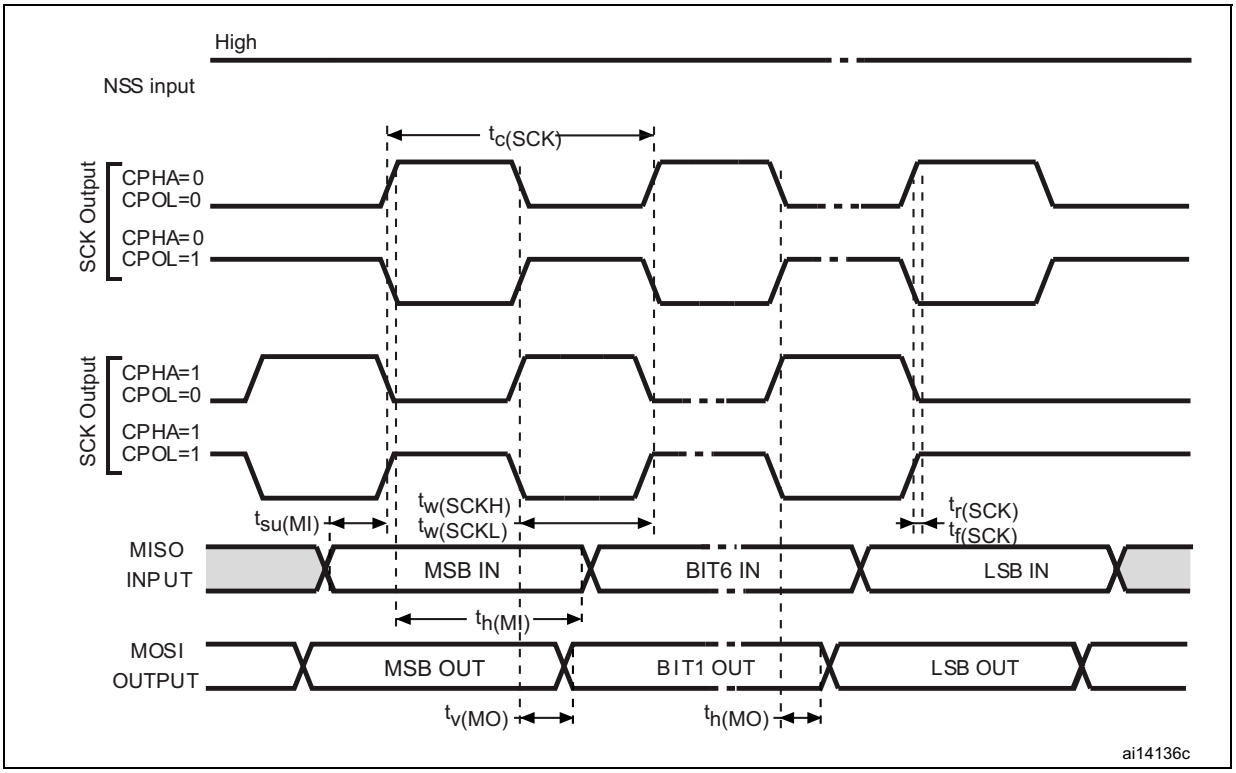


Figure 23. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 24. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 51. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 52. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0	3.6	V
V_{DI}(3)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(3)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}(4)	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}(4)	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. Guaranteed by characterization results.
4. Guaranteed by test in production.
5. R_L is the load connected on the USB drivers.

Figure 25. USB timings: definition of data signal rise and fall time

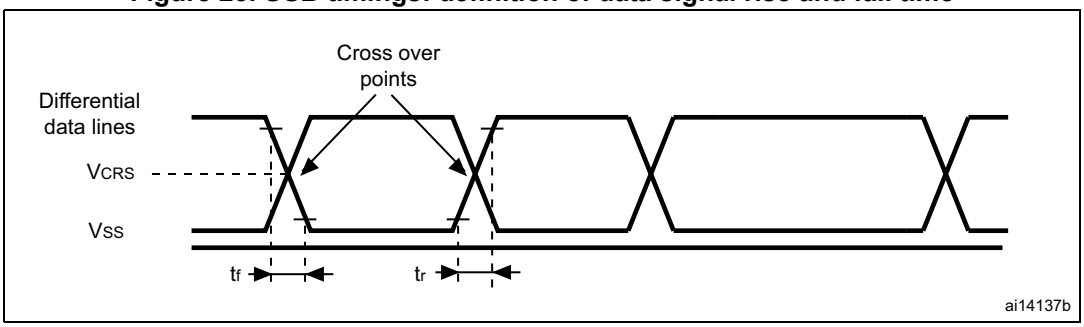


Table 53. USB: full speed electrical characteristics

Driver characteristics(1)					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall Time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification section 7 (version 2.0).

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 55* are guaranteed by design.

Table 54. ADC clock frequency

Symbol	Parameter	Conditions			Min	Max	Unit
f_{ADC}	ADC clock frequency	Voltage Range 1 & 2	2.4 V ≤V_{DDA} ≤3.6 V	V_{REF+} = V_{DDA}	0.480	16	MHz
				V_{REF+} < V_{DDA} V_{REF+} > 2.4 V		8	
				V_{REF+} < V_{DDA} V_{REF+} ≤2.4 V		4	
			1.8 V ≤V_{DDA} ≤2.4 V	V_{REF+} = V_{DDA}		8	
				V_{REF+} < V_{DDA}		4	
		Voltage Range 3				4	

Table 55. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	2.4 V ≤V_{DDA} ≤3.6 V V_{REF+} must be below or equal to V_{DDA}	1.8(1)	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	-	V_{SSA}	-	V
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF}(2)	Current on the V_{REF} input pin	Peak	-	400	700	µA
		Average	-		450	µA
V_{AIN}	Conversion voltage range(3)	-	0(4)	-	V_{REF+}	V
f_S	12-bit sampling rate	Direct channels	-	-	1	Msps
		Multiplexed channels	-	-	0.76	
	10-bit sampling rate	Direct channels	-	-	1.07	Msps
		Multiplexed channels	-	-	0.8	
	8-bit sampling rate	Direct channels	-	-	1.23	Msps
		Multiplexed channels	-	-	0.89	
	6-bit sampling rate	Direct channels	-	-	1.45	Msps
		Multiplexed channels	-	-	1	

Table 55. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Sampling time(5)	Direct channels 2.4 V ≤V_{DDA} ≤3.6 V	0.25	-	-	µs
		Multiplexed channels 2.4 V ≤V_{DDA} ≤3.6 V	0.56	-	-	
		Direct channels 1.8 V ≤V_{DDA} ≤2.4 V	0.56	-	-	
		Multiplexed channels 1.8 V ≤V_{DDA} ≤2.4 V	1	-	-	
		-	4	-	384	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 16 MHz	1	-	24.75	µs
		-	4 to 384 (sampling phase) +12 (successive approximation)			$1/f_{ADC}$
C_{ADC}	Internal sample and hold capacitor	Direct channels	-	16	-	pF
		Multiplexed channels	-		-	
f_{TRIG}	External trigger frequency Regular sequencer	12-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv	$1/f_{ADC}$
f_{TRIG}	External trigger frequency Injected sequencer	12-bit conversions	-	-	Tconv+2	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
R_{AIN}	Signal source impedance(5)	-	-	-	50	kΩ
t_{lat}	Injection trigger conversion latency	f_{ADC} = 16 MHz	219	-	281	ns
		-	3.5	-	4.5	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 16 MHz	156	-	219	ns
		-	2.5	-	3.5	$1/f_{ADC}$
t_{STAB}	Power-up time	-	-	-	3.5	µs

1. The V_{REF+} input can be grounded if neither the ADC nor the DAC are used (this allows to shut down an external voltage reference).
2. The current consumption through V_{REF} is composed of two parameters:

   - one constant (max 300 µA)

   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.

   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pin descriptions* for further details.
4. V_{SSA} or V_{REF-} must be tied to ground.
5. See *Table 57: Maximum source impedance RAIN max* for R_{AIN} limitations

Table 56. ADC accuracy(1)(2)

Symbol	Parameter	Test conditions	Min(3)	Typ	Max(3)	Unit
ET	Total unadjusted error	$2.4\ V \le V_{DDA} \le 3.6\ V$ $2.4\ V \le V_{REF+} \le 3.6\ V$ $f_{ADC} = 8\ MHz$, $R_{AIN} = 50\ \Omega$ $T_A = -40$ to $105\ °C$	-	2.5	4	LSB
EO	Offset error		-	1	2	
EG	Gain error		-	1.5	3.5	
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-	2	3	
ENOB	Effective number of bits	$2.4\ V \le V_{DDA} \le 3.6\ V$ $V_{DDA} = V_{REF+}$ $f_{ADC} = 16\ MHz$, $R_{AIN} = 50\ \Omega$ $T_A = -40$ to $105\ °C$ F_{input} =10 kHz	9.5	10	-	bits
SINAD	Signal-to-noise and distortion ratio		59	62	-	dB
SNR	Signal-to-noise ratio		60	62	-	
THD	Total harmonic distortion		-	-72	-69	
ENOB	Effective number of bits	$1.8\ V \le V_{DDA} \le 2.4\ V$ $V_{DDA} = V_{REF+}$ $f_{ADC} = 8\ MHz$ or $4\ MHz$, $R_{AIN} = 50\ \Omega$ $T_A = -40$ to $105\ °C$ F_{input} =10 kHz	9.5	10	-	bits
SINAD	Signal-to-noise and distortion ratio		59	62	-	dB
SNR	Signal-to-noise ratio		60	62	-	
THD	Total harmonic distortion		-	-72	-69	
ET	Total unadjusted error	$2.4\ V \le V_{DDA} \le 3.6\ V$ $1.8\ V \le V_{REF+} \le 2.4\ V$ $f_{ADC} = 4\ MHz$, $R_{AIN} = 50\ \Omega$ $T_A = -40$ to $105\ °C$	-	4	6.5	LSB
EO	Offset error		-	1.5	3.5	
EG	Gain error		-	3.5	6	
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-	2.5	3.5	
ET	Total unadjusted error	$1.8\ V \le V_{DDA} \le 2.4\ V$ $1.8\ V \le V_{REF+} \le 2.4\ V$ $f_{ADC} = 4\ MHz$, $R_{AIN} = 50\ \Omega$ $T_A = -40$ to $105\ °C$	-	2	3	LSB
EO	Offset error		-	1	1.5	
EG	Gain error		-	1.5	2.5	
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-	2	3	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.12* does not affect the ADC accuracy.
3. Guaranteed by characterization results.

Figure 26. ADC accuracy characteristics

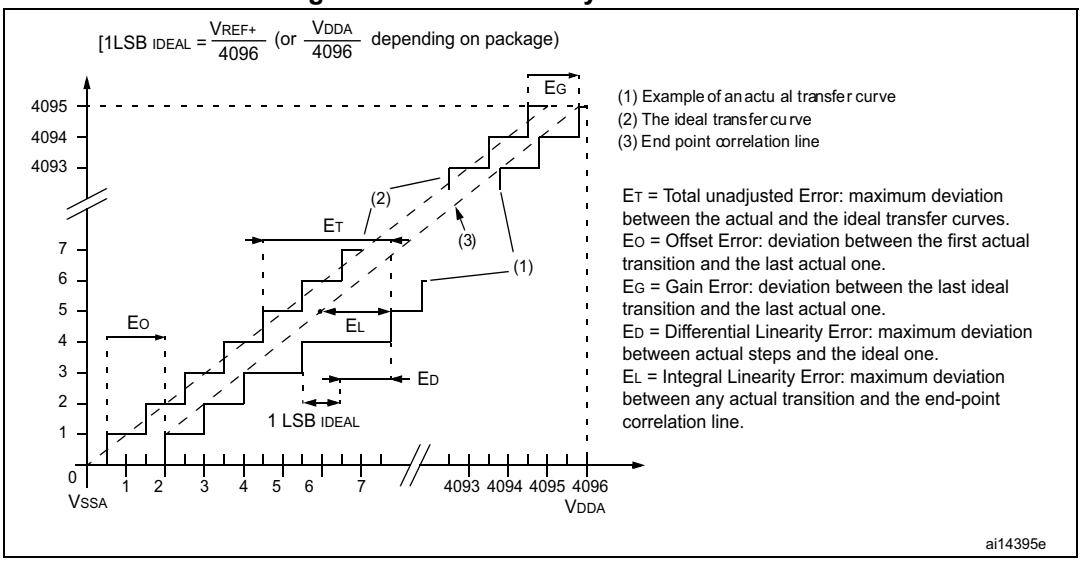
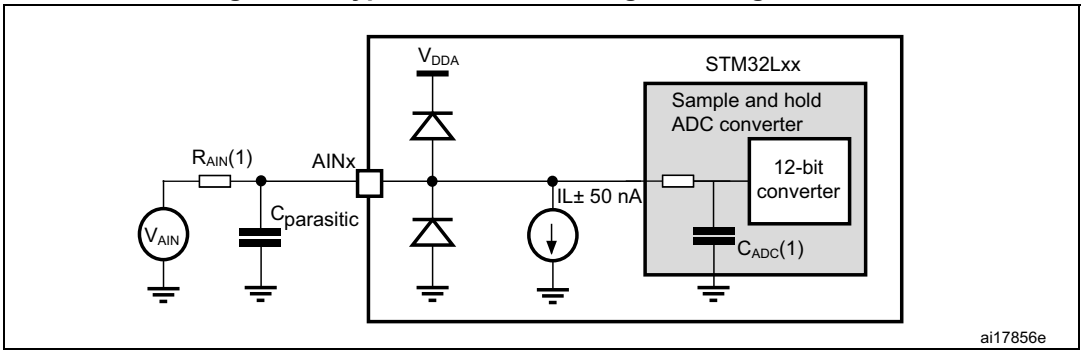


Figure 27. Typical connection diagram using the ADC



1. Refer to *Table 57: Maximum source impedance RAIN max* for the value of R_{AIN} and *Table 55: ADC characteristics* for the value of CADC
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

Figure 28. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

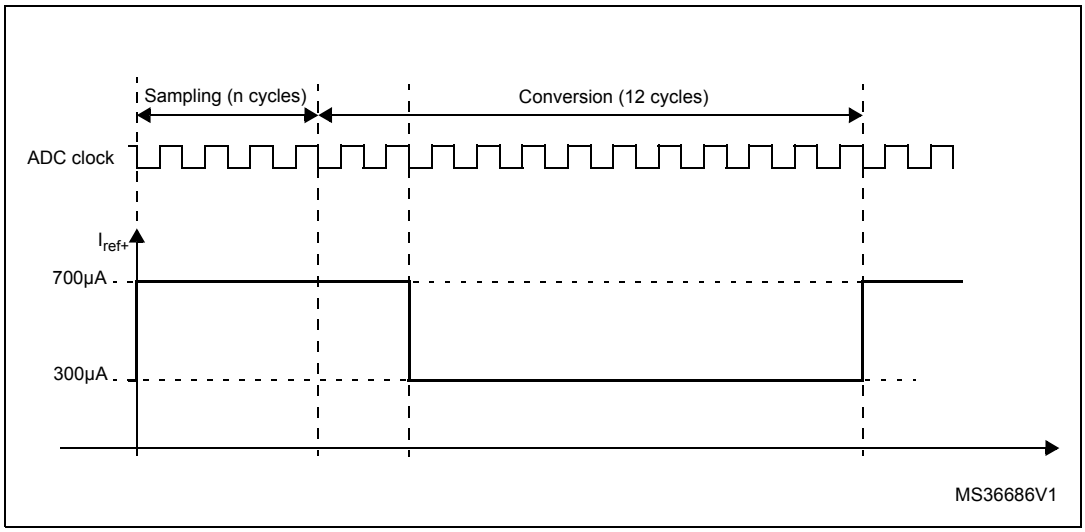


Table 57. Maximum source impedance R_{AIN} max(1)

Ts (µs)	R_{AIN} max (kOhm)				Ts (cycles) f_{ADC}= 16 MHz(2)
	Multiplexed channels		Direct channels		
	2.4 V < V_{DDA}< 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA}< 3.3 V	1.8 V < V_{DDA} < 2.4 V	
0.25	Not allowed	Not allowed	0.7	Not allowed	4
0.5625	0.8	Not allowed	2.0	1.0	9
1	2.0	0.8	4.0	3.0	16
1.5	3.0	1.8	6.0	4.5	24
3	6.8	4.0	15.0	10.0	48
6	15.0	10.0	30.0	20.0	96
12	32.0	25.0	50.0	40.0	192
24	50.0	50.0	50.0	50.0	384

1. Guaranteed by design.
2. Number of samples calculated for **f_{ADC} = 16 MHz. F**or **f_{ADC} = 8 and 4 MHz the number of sampling cycles can be reduced with respect to the minimum sampling time Ts (us).**

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 12*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

6.3.18 DAC electrical specifications

Data guaranteed by design, unless otherwise specified.

Table 58. DAC characteristics

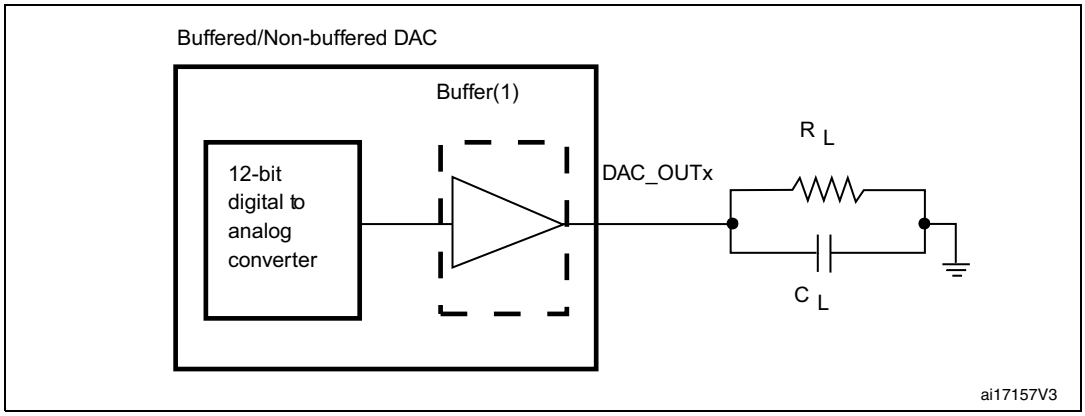
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.8	-	3.6	V
V_{REF+}	Reference supply voltage	V_{REF+} must always be below V_{DDA}		1.8	-	3.6	V
V_{REF-}	Lower reference voltage	-		V_{SSA}			V
$I_{DDVREF+}$(1)	Current consumption on V_{REF+} supply V_{REF+} = 3.3 V	No load, middle code (0x800)		-	130	220	µA
		No load, worst code (0x000)		-	220	350	µA
I_{DDA}(1)	Current consumption on V_{DDA} supply V_{DDA} = 3.3 V	No load, middle code (0x800)		-	210	320	µA
		No load, worst code (0xF1C)		-	320	520	µA
R_L	Resistive load	DAC output buffer ON	Connected to V_{SSA}	5	-	-	kΩ
			Connected to V_{DDA}	25	-	-	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
R_O	Output impedance	DAC output buffer OFF		12	16	20	kΩ
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF		0.5	-	V_{REF+}– 1LSB	mV
DNL(1)	Differential non linearity(2)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		-	1.5	3	LSB
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF		-	1.5	3	
INL(1)	Integral non linearity(3)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		-	2	4	
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF		-	2	4	
Offset(1)	Offset error at code 0x800 (4)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON		-	±10	±25	
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF		-	±5	±8	
Offset1(1)	Offset error at code 0x001(5)	No R_L, $C_L \leq 50$ pF DAC output buffer OFF		-	±1.5	±5	

Table 58. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dOffset/dT(1)	Offset error temperature coefficient (code 0x800)	V_{DDA} = 3.3V,V_{REF+} = 3.0V T_A = 0 to 50 °C DAC output buffer OFF	-20	-10	0	µV/°C
		V_{DDA} = 3.3V, V_{REF+} = 3.0V T_A = 0 to 50 °C DAC output buffer ON	0	20	50	
Gain(1)	Gain error(6)	$C_L \leq$50 pF, $R_L \geq$ 5 kΩ DAC output buffer ON	-	+0.1 / -0.2%	+0.2 / -0.5%	%
		No R_L, $C_L \leq$50 pF DAC output buffer OFF	-	+0 / -0.2%	+0 / -0.4%	
dGain/dT(1)	Gain error temperature coefficient	V_{DDA} = 3.3V, V_{REF+} = 3.0V T_A = 0 to 50 °C DAC output buffer OFF	-10	-2	0	µV/°C
		V_{DDA} = 3.3V, V_{REF+} = 3.0V T_A = 0 to 50 °C DAC output buffer ON	-40	-8	0	
TUE(1)	Total unadjusted error	$C_L \leq$50 pF, $R_L \geq$ 5 kΩ DAC output buffer ON	-	12	30	LSB
		No R_L, $C_L \leq$50 pF DAC output buffer OFF	-	8	12	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \leq$50 pF, $R_L \geq$ 5 kΩ	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \leq$50 pF, $R_L \geq$ 5 kΩ	-	-	1	Msps
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)(7)	$C_L \leq$50 pF, $R_L \geq$ 5 kΩ	-	9	15	µs
PSRR+	V_{DDA} supply rejection ratio (static DC measurement)	$C_L \leq$50 pF, $R_L \geq$ 5 kΩ	-	-60	-35	dB

1. Guaranteed by characterization results.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x800) and the ideal value = V_{REF+}/2.
5. Difference between the value measured at Code (0x001) and the ideal value.
6. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is ON.
7. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Figure 29. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.19 Temperature sensor characteristics

Table 59. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C±5, V_{DDA}= 3 V ±10mV	0x1FF8 007A-0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 110 ±5°C V_{DDA}= 3 V ±10mV	0x1FF8 007E-0x1FF8 007F

Table 60. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	1.48	1.61	1.75	mV/°C
V_{110}	Voltage at 110°C ±5°C(2)	612	626.8	641.5	mV
$I_{DDA(TEMP)}$(3)	Current consumption	-	3.4	6	µA
t_{START}(3)	Startup time	-	-	10	µs
T_{S_temp}(3)	ADC sampling time when reading the temperature	4	-	-	

1. Guaranteed by characterization results.
2. Measured at V_{DD} = 3 V ±10 mV. V110 ADC conversion result is stored in the byte.
3. Guaranteed by design.

6.3.20 Comparator

Table 61. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

Table 62. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay(2) in slow mode	1.65 V ≤V_{DDA} ≤2.7 V	-	1.8	3.5	
		2.7 V ≤V_{DDA} ≤3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay(2) in fast mode	1.65 V ≤V_{DDA} ≤2.7 V	-	0.8	2	
		2.7 V ≤V_{DDA} ≤3.6 V	-	1.2	4	
V_{offset}	Comparator offset error	-	-	±4	±20	mV
dThreshold/ dt	Threshold voltage temperature coefficient	V_{DDA} = 3.3V T_A = 0 to 50 °C V- = V_{REFINT}, 3/4 V_{REFINT}, 1/2 V_{REFINT}, 1/4 V_{REFINT}	-	15	100	ppm /°C
I_{COMP2}	Current consumption(3)	Fast mode	-	3.5	5	µA
		Slow mode	-	0.5	2	

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

6.3.21 LCD controller (STM32L152x6/8/B-A devices only)

The STM32L152xx-A devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 63. LCD controller characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.73	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.86	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.98	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.26	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.55	-	
C_{ext}	V_{LCD} external capacitance	0.1	-	2	µF
I_{LCD}(1)	Supply current at V_{DD} = 2.2 V	-	3.3	-	µA
	Supply current at V_{DD} = 3.0 V	-	3.1	-	
R_{Htot}(2)	Low drive resistive network overall value	5.28	6.6	7.92	MΩ
R_L(2)	High drive resistive network total value	192	240	288	kΩ
V_{44}	Segment/Common highest level voltage	-	-	V_{LCD}	V
V_{34}	Segment/Common 3/4 level voltage	-	3/4 V_{LCD}	-	V
V_{23}	Segment/Common 2/3 level voltage	-	2/3 V_{LCD}	-	
V_{12}	Segment/Common 1/2 level voltage	-	1/2 V_{LCD}	-	
V_{13}	Segment/Common 1/3 level voltage	-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage	-	1/4 V_{LCD}	-	
V_0	Segment/Common lowest level voltage	0	-	-	
ΔVxx(2)	Segment/Common level voltage error T_A = -40 to 105 °C	-	-	±50	mV

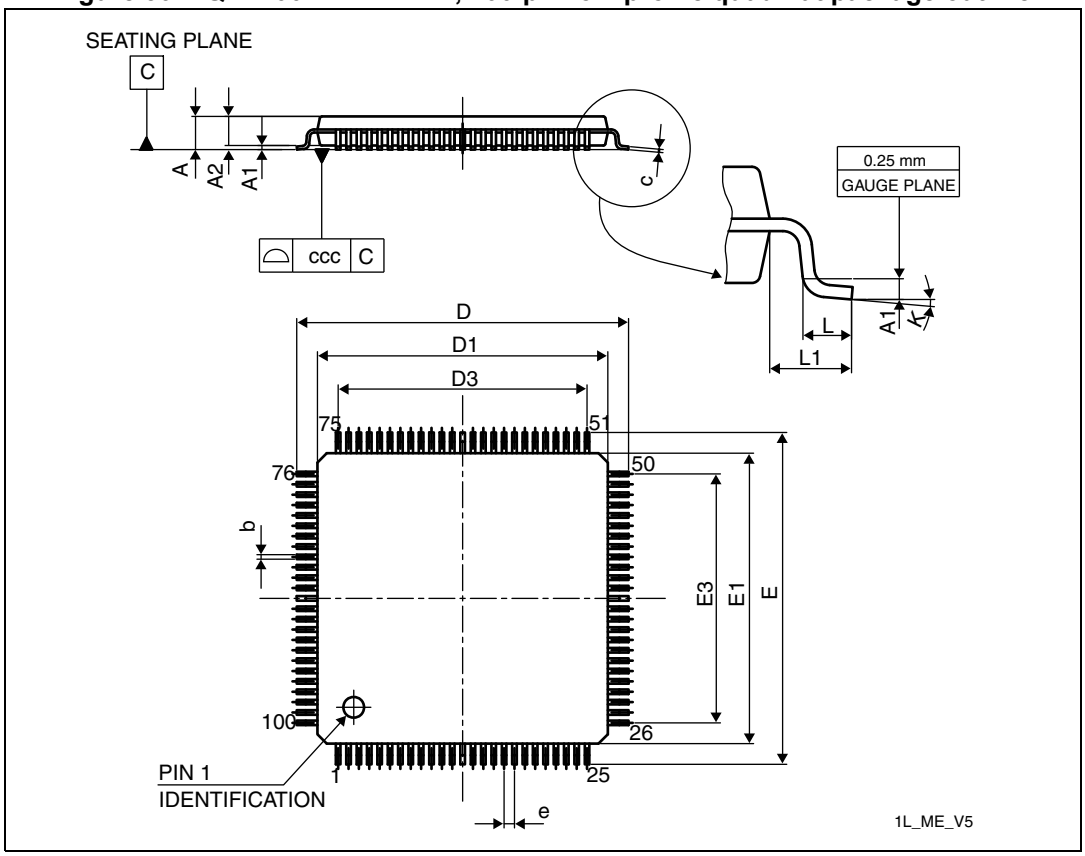
1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected
2. Guaranteed by characterization results.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP100 14 x 14 mm, 100-pin low-profile quad flat package information

Figure 30. LQFP100 14 x 14 mm, 100-pin low-profile quad flat package outline



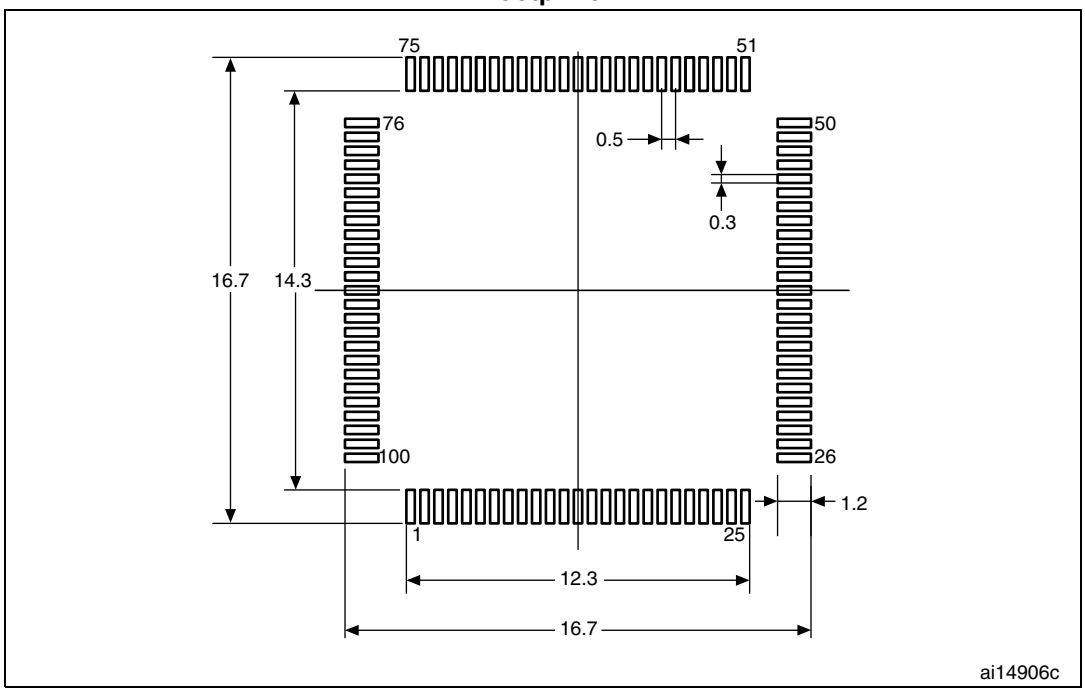
1. Drawing is not to scale.

Table 64. LQPF100 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 31. LQPF100 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint



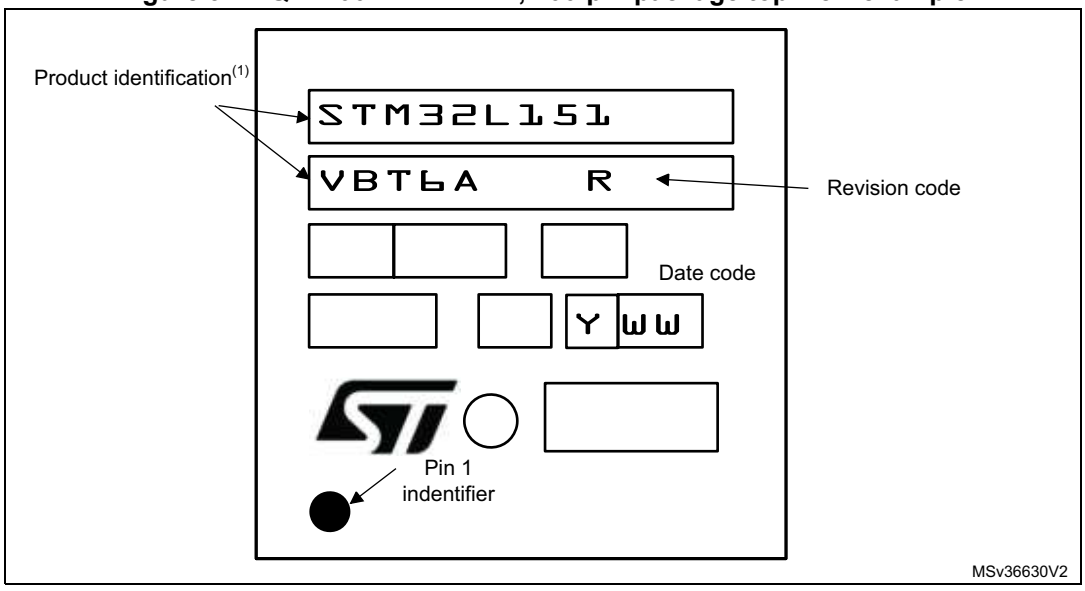
1. Dimensions are in millimeters.

LQFP100 device Marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 32. LQFP100 14 x 14 mm, 100-pin package top view example

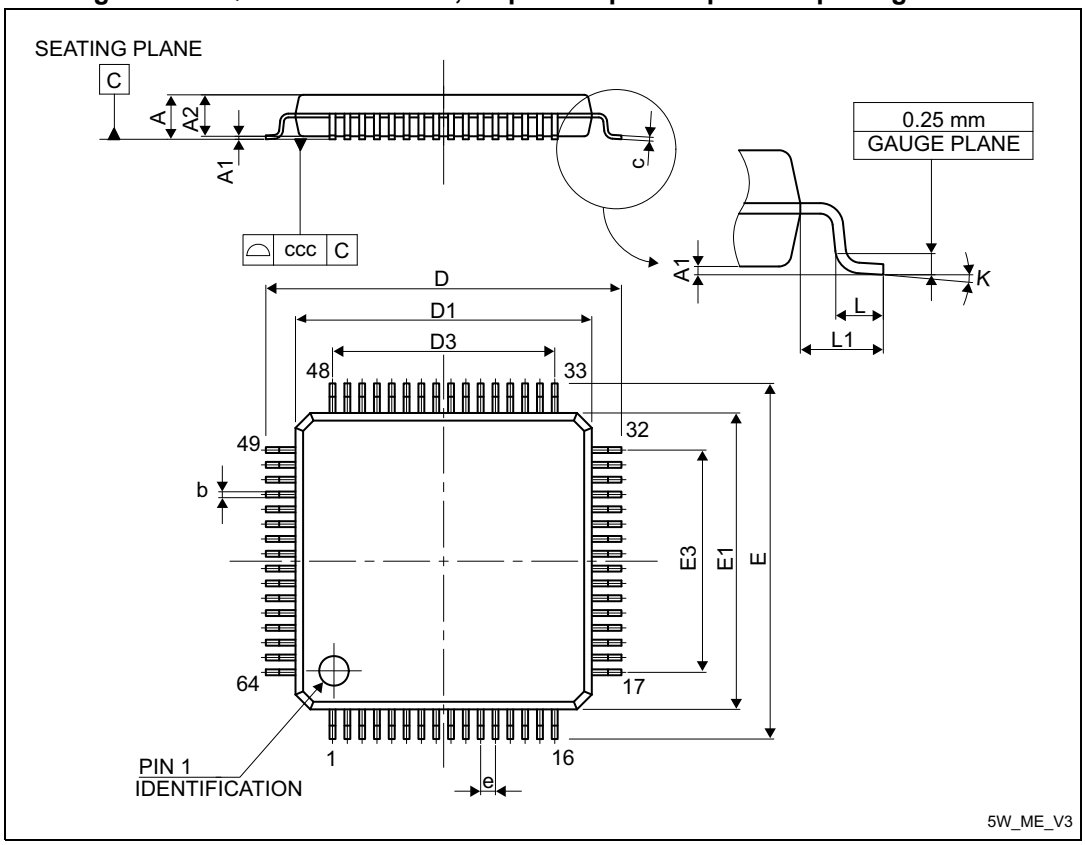


1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified

and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.2 LQFP64 10 x 10 mm, 64-pin low-profile quad flat package information

Figure 33. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 65. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

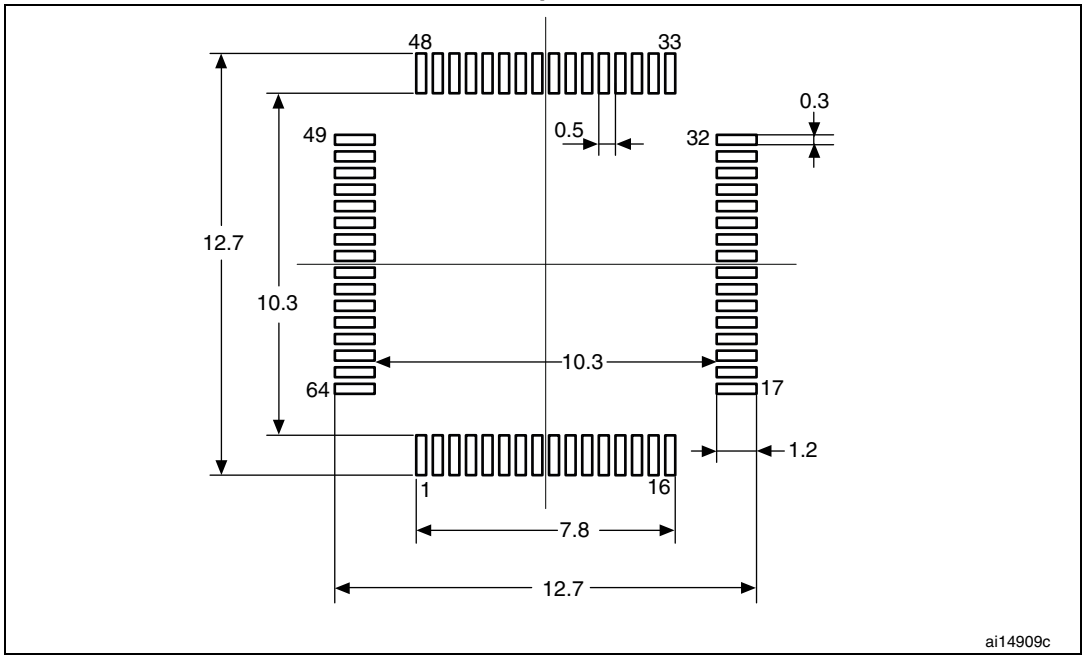
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-

Table 65. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 34. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package recommended footprint



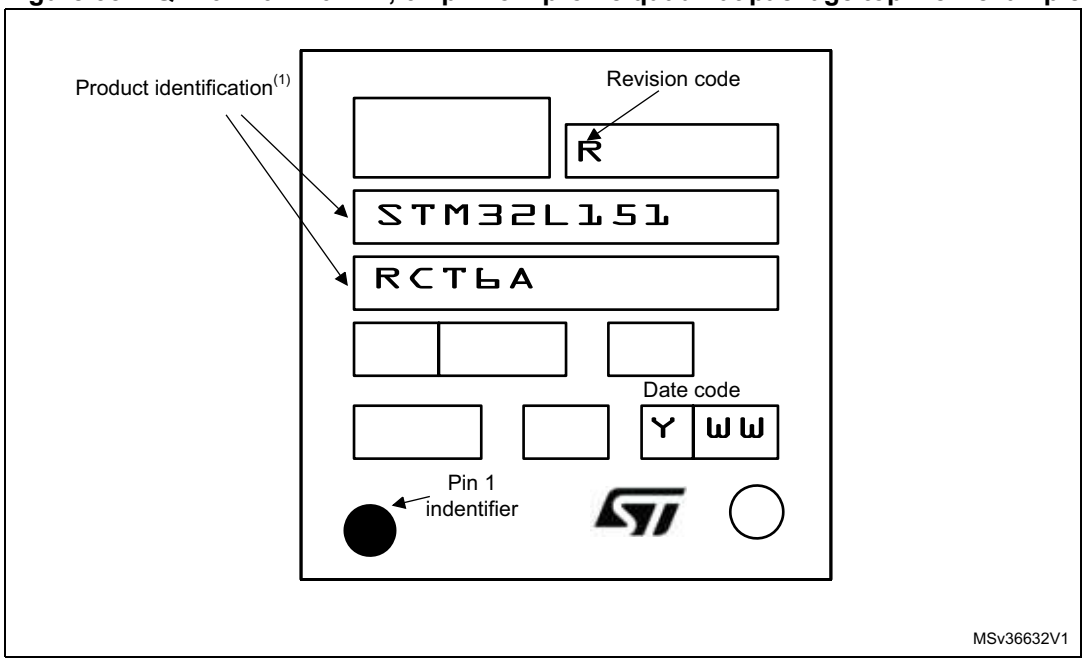
1. Dimensions are in millimeters.

LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

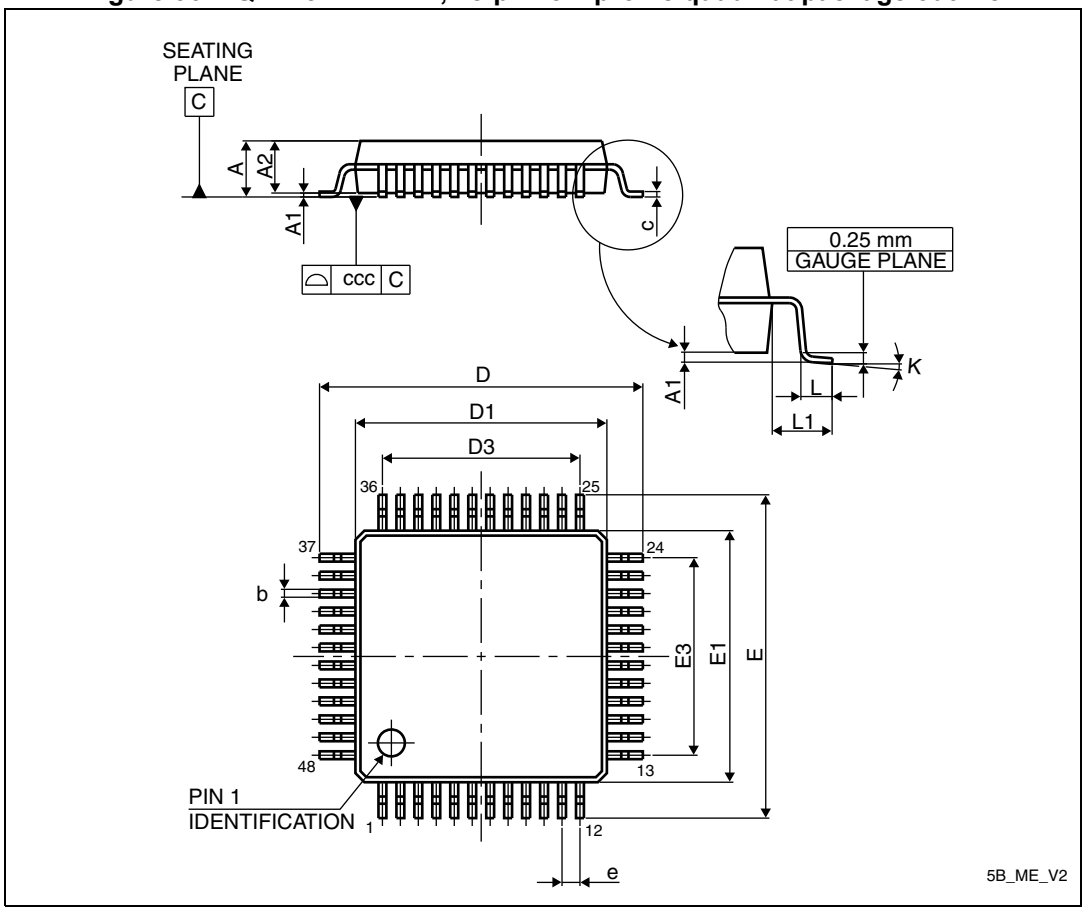
Figure 35. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example



1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.3 LQFP48 7 x 7 mm, 48-pin low-profile quad flat package information

Figure 36. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package outline



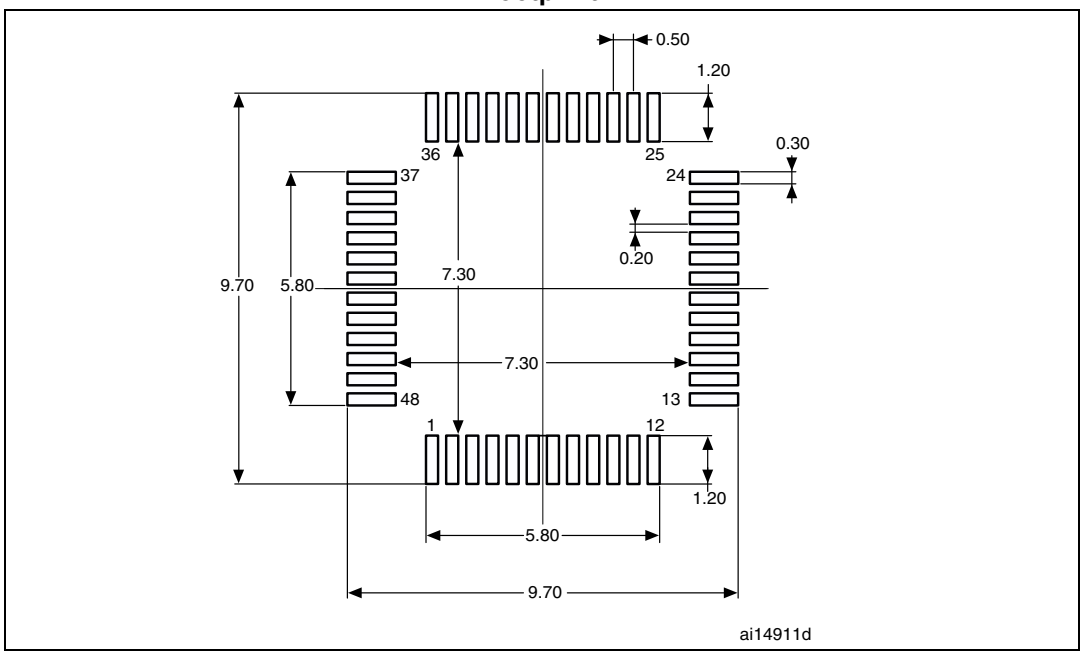
1. Drawing is not to scale.

Table 66. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package recommended footprint



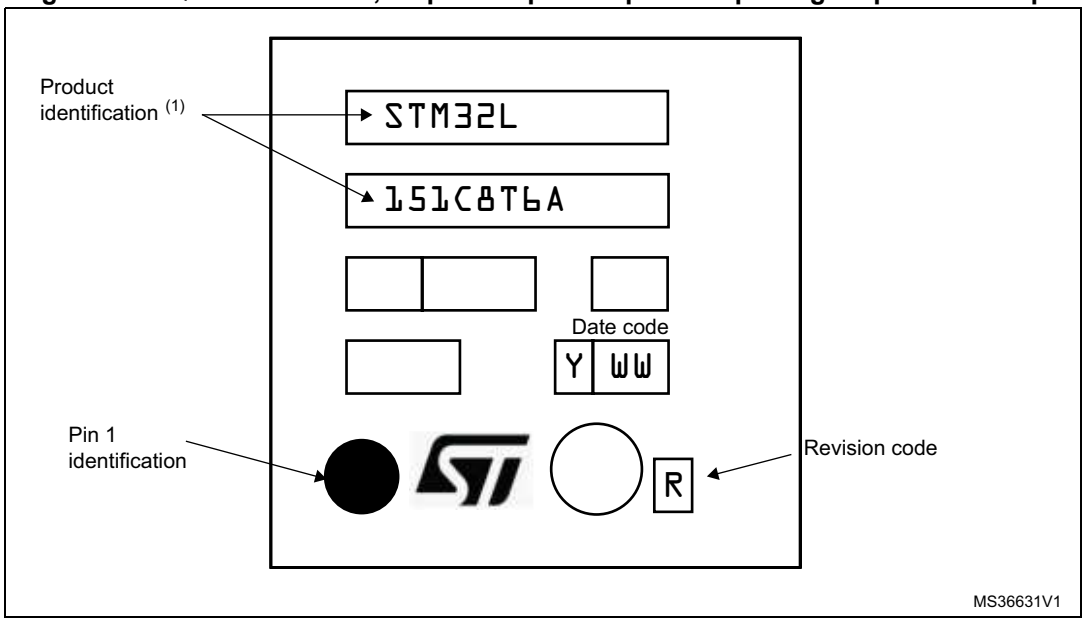
1. Dimensions are in millimeters.

LQFP48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 38. LQFP48 7 x 7 mm, 48-pin low-profile quad flat package top view example

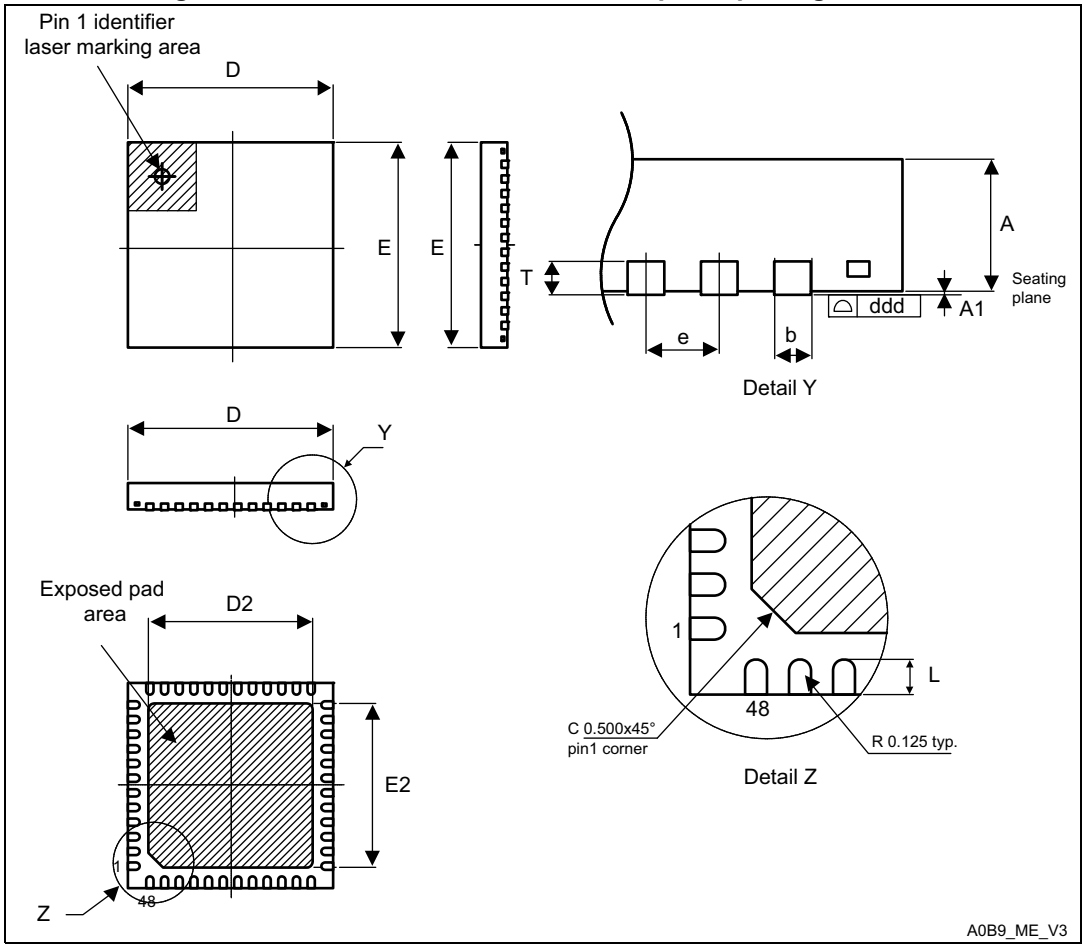


1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified

and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.4 UFQFPN48 7 x 7 mm, 0.5 mm pitch, package information

Figure 39. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline



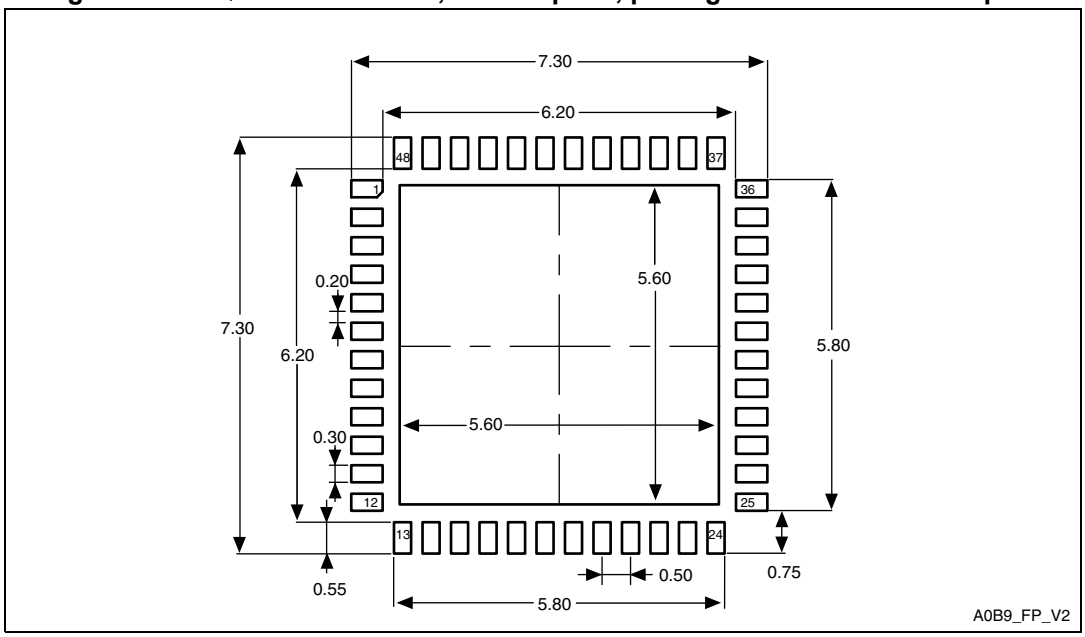
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 67. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 40. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package recommended footprint



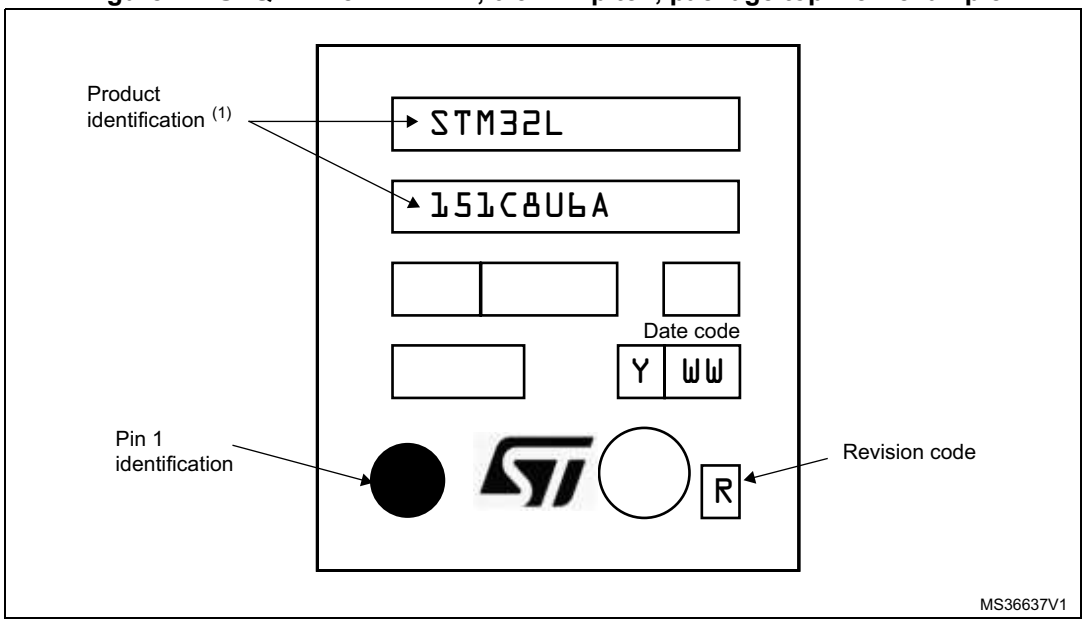
1. Dimensions are in millimeters.

UFQFPN48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

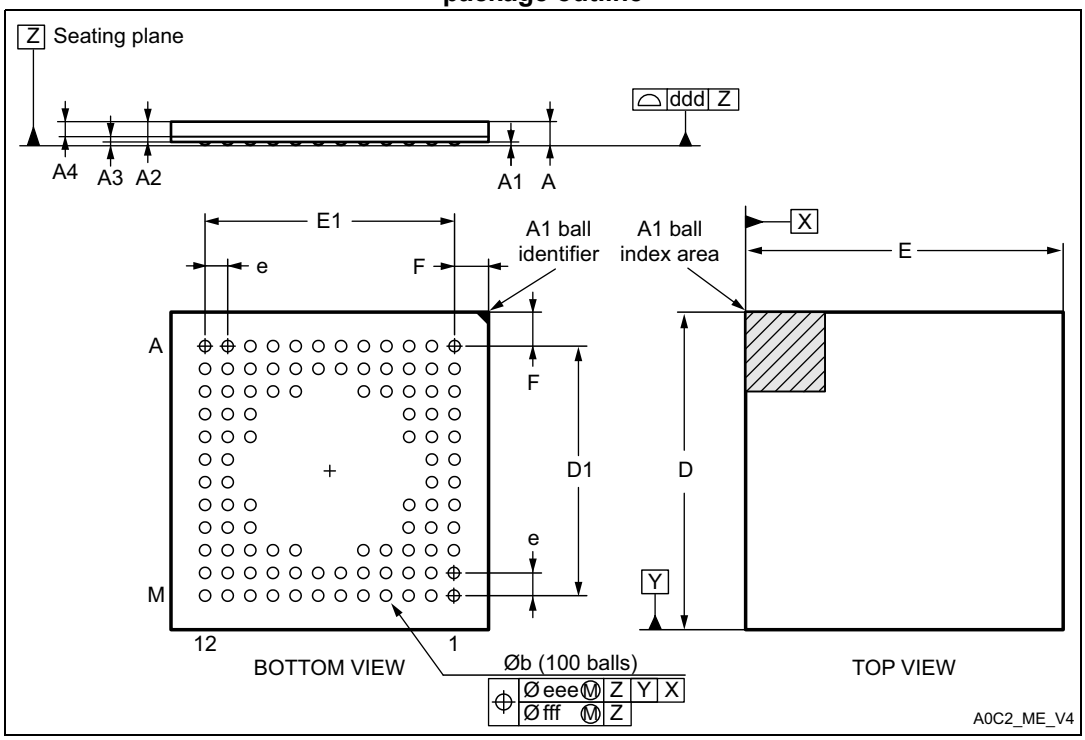
Figure 41. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package top view example



1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.5 UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package information

Figure 42. UFBGA100, 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 68. UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.6	-	-	0.0236
A1	0.05	0.08	0.11	0.002	0.0031	0.0043
A2	0.4	0.45	0.5	0.0157	0.0177	0.0197
A3	0.08	0.13	0.18	0.0031	0.0051	0.0071
A4	0.27	0.32	0.37	0.0106	0.0126	0.0146
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
D	6.95	7	7.05	0.2736	0.2756	0.2776
D1	5.45	5.5	5.55	0.2146	0.2165	0.2185
E	6.95	7	7.05	0.2736	0.2756	0.2776
E1	5.45	5.5	5.55	0.2146	0.2165	0.2185
e	-	0.5	-	-	0.0197	-

Table 68. UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
F	0.7	0.75	0.8	0.0276	0.0295	0.0315
ddd	-	-	0.1	-	-	0.0039
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 43. UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package recommended footprint

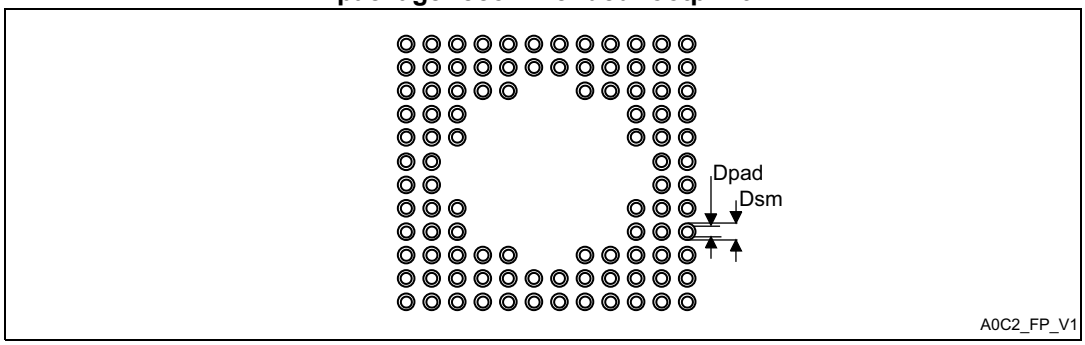


Table 69. UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules

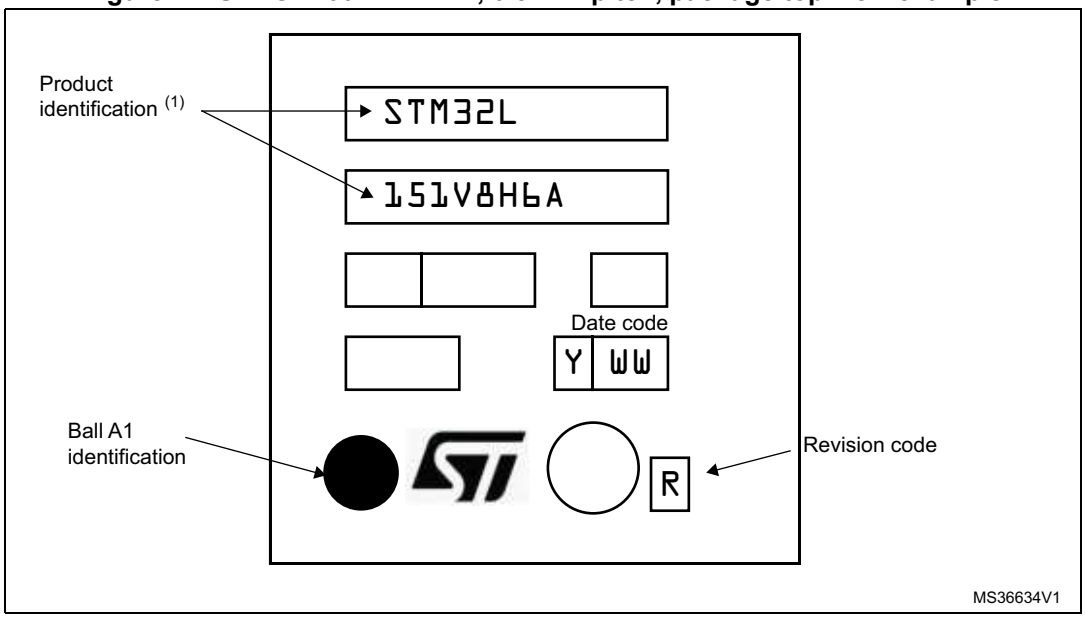
Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

UFBGA100 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

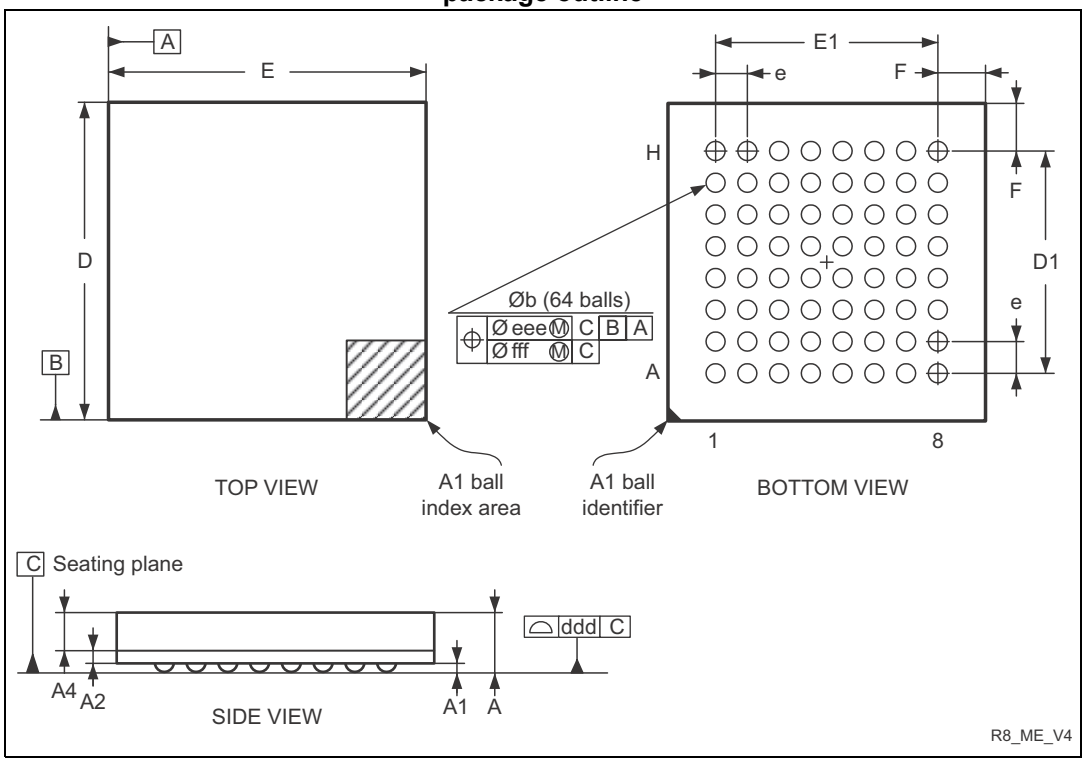
Figure 44. UFBGA100 7 x 7 mm, 0.5 mm pitch, package top view example



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7.6 TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information

Figure 45. TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 70. TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.600	-	-	0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	-	3.500	-	-	0.1378	-
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	-	3.500	-	-	0.1378	-
e	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-

Table 70. TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.15	-	-	0.0059
fff	-	-	0.05	-	-	0.002

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 46. TFBGA64, 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package recommended footprint

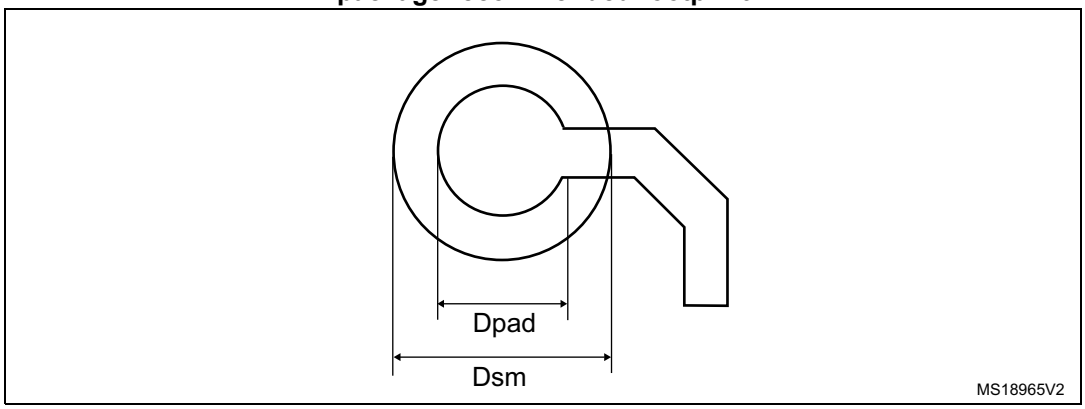


Table 71. TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules

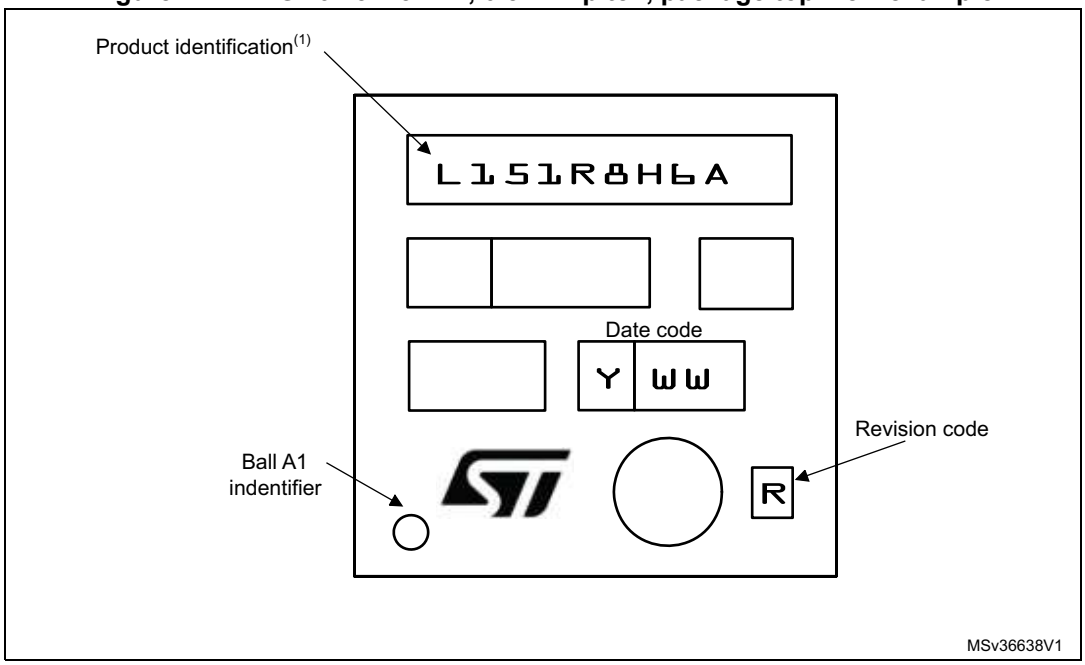
Dimension	Recommended values
Pitch	0.5
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

TFBGA64 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 47. TFBGA64 5 x 5 mm, 0.5 mm pitch, package top view example



1. Parts marked as ES or E or accompanied by an engineering sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 72. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** UFBGA100 - 7 x 7 mm	59	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient TFBGA64 - 5 x 5 mm	65	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm / 0.5 mm pitch	33	

Figure 48. Thermal resistance suffix 6

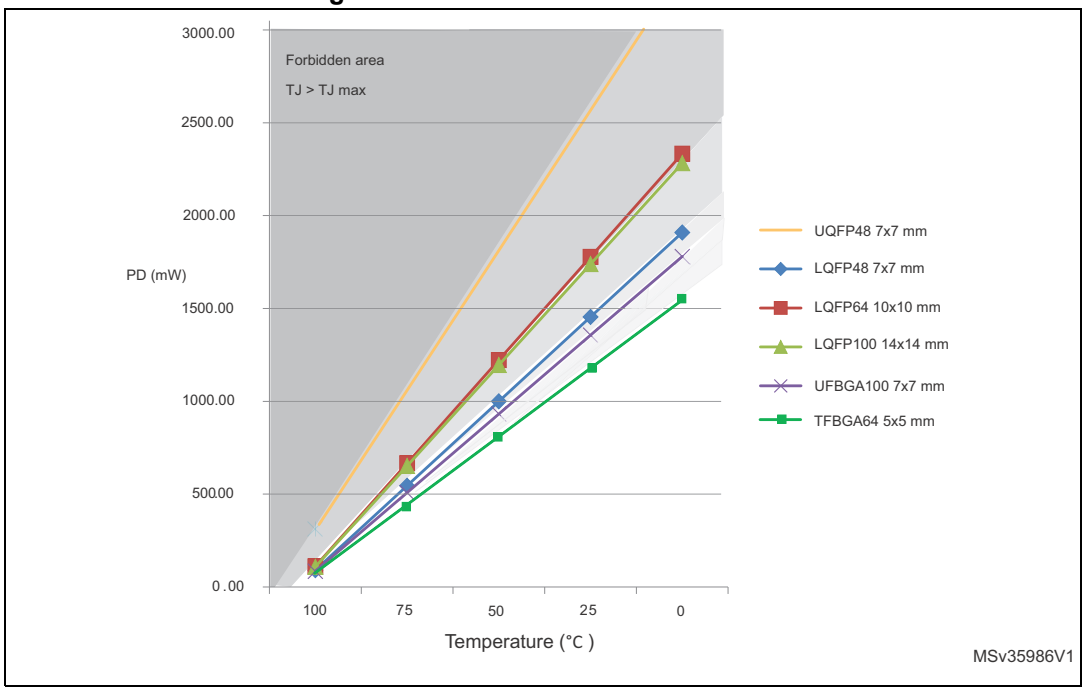
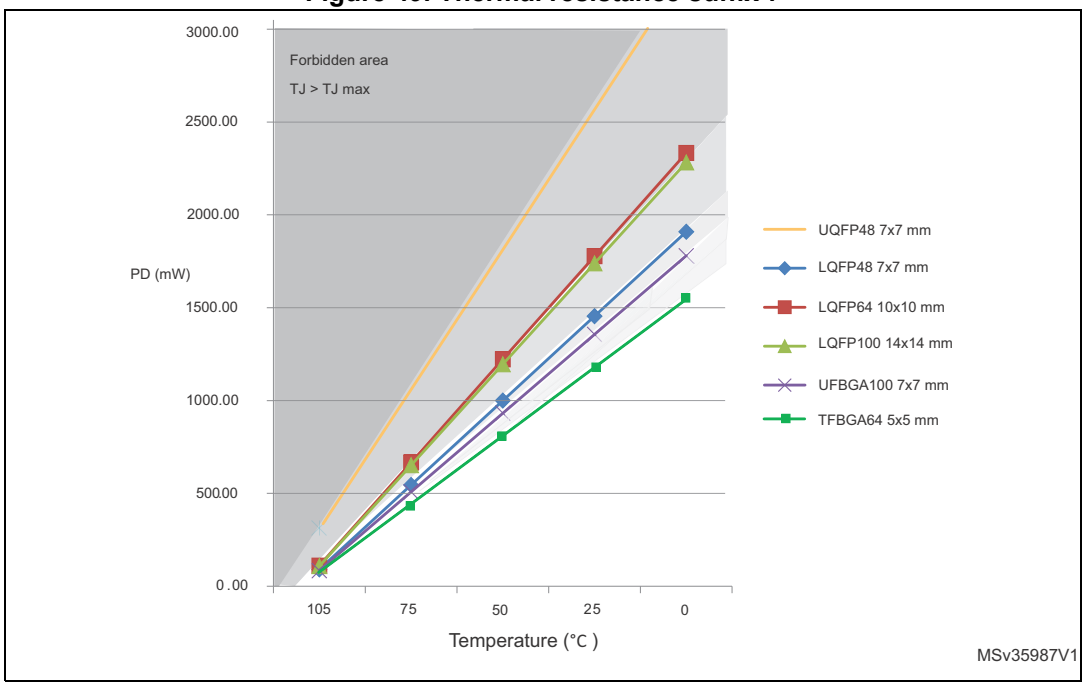


Figure 49. Thermal resistance suffix 7



7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

8 Ordering information

Table 73. Ordering information scheme

Example: STM32 L 152 R B T 6 A D TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low-power

Device subfamily

151: Devices without LCD

152: Devices with LCD

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Flash memory size

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

Package

H = BGA

T = LQFP

U = UFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

A = device generation A

No character = VDD range: 1.8 to 3.6 V and BOR enabled

D = VDD range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

9 Revision history

Table 74. Document revision history

Date	Revision	Changes
04-Feb-2014	1	Initial release.
12-Mar-2014	2	Updated *Section 3.5: Low-power real-time clock and backup registers*, *Section 6.1.2: Typical values* and *Section 6.3.4: Supply current characteristics*. Updated *General PCB design guidelines*. Updated *Table 5: Working mode-dependent functionalities (from Run/active down to standby)*, *Table 14: General operating conditions*, *Table 21: Current consumption in Low-power run mode*, *Table 22: Current consumption in Low-power sleep mode*, *Table 23: Typical and maximum current consumptions in Stop mode*, *Table 24: Typical and maximum current consumptions in Standby mode*, *Table 25: Peripheral current consumption*, *Table 42: I/O current injection susceptibility*, *Table 43: I/O static characteristics* and *Table 46: NRST pin characteristics*. Updated *Figure 14: Current consumption measurement scheme*.
04-Feb-2015	3	Updated DMIPS features in cover page and *Section 2: Description*. Updated max temperature at 105°C instead of 85°C in the whole datasheet. Updated current consumption in *Table 20: Current consumption in Sleep mode*. Updated *Table 25: Peripheral current consumption* with new measured values. Updated *Table 57: Maximum source impedance RAIN max* adding note 2. Updated *Section 7: Package information* with new package device marking. Updated *Figure 9: Memory map*.

Table 74. Document revision history (continued)

Date	Revision	Changes
25-Apr-2016	4	Updated *Section 7: Package information* structure: Paragraph titles and paragraph heading level. Updated *Section 7: Package information* for all package device markings, adding text for device orientation versus pin 1/ ball A1 identifier. Updated *Figure 32: LQFP100 14 x 14 mm, 100-pin package top view example* removing gate mark. Updated *Table 65: LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data*. Updated *Section 7.5: UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package information* adding *Table 69: UFBGA100 7 x 7 mm, 0.5 mm pitch, recommended PCB design rules* and *Figure 43: UFBGA100 7 x 7 mm, 0.5 mm pitch, ultra thin fine-pitch ball grid array package recommended footprint*. Updated *Section 7.6: TFBGA64 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package information* adding *Table 71: TFBGA64 5 x 5 mm, 0.5 mm pitch, recommended PCB design rules* and changing *Figure 46: TFBGA64, 5 x 5 mm, 0.5 mm pitch, thin fine-pitch ball grid array package recommended footprint*. Updated *Table 17: Embedded internal reference voltage* temperature coefficient at 100ppm/°C and table note 3: “guaranteed by design” changed by “guaranteed by characterization results”. Updated *Table 62: Comparator 2 characteristics* new maximum threshold voltage temperature coefficient at 100ppm/°C. Updated *Table 40: ESD absolute maximum ratings* CDM class. Updated all the notes, removing ‘not tested in production’. Updated *Table 11: Voltage characteristics* adding note about V_{REF-} pin. Updated *Table 3: Functionalities depending on the operating power supply range* LSI and LSE functionalities putting “Y” in Standby mode. Removed note 1 below *Figure 2: Clock tree*. Updated *Table 58: DAC characteristics* resistive load.

Table 74. Document revision history (continued)

Date	Revision	Changes
25-Aug-2017	5	Updated *Table 43: I/O static characteristics* pull-up and pull-down values. Updated *Table 46: NRST pin characteristics* pull-up values. Updated *Section 7: Package information* adding information about other optional marking or inset/upset marks. Updated note 1 below all the package device marking figures. Updated *Nested vectored interrupt controller (NVIC)* in *Section 3.2: ARM® Cortex®-M3 core with MPU* about process state automatically saved. Updated *Table 3: Functionalities depending on the operating power supply range* removing I/O operation column and adding note about GPIO speed. Updated *Table 42: I/O current injection susceptibility* note by 'injection is not possible'. Updated *Figure 20: Recommended NRST pin protection* note about the 0.1uF capacitor. Updated *Section 3.1: Low-power modes* Low-power run mode (MSI) RC oscillator clock. Updated *Table 5: Working mode-dependent functionalities (from Run/active down to standby)* disabling I2C functionality in Low-power Run and Low-power Sleep modes.

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