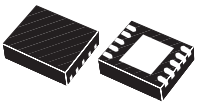
STEF05D

Electronic fuse for 5 V line

Datasheet - production data



DFN10 (3 x 3 mm)

Features

- Continuous current typ: 3.6 A
- N-channel on-resistance typ: 40 mΩ
- Enable/fault functions
- Output clamp voltage typ: 6.65 V
- Undervoltage lockout
- Short-circuit limit
- Overload current limit
- Controlled output voltage ramp
- Thermal latch typ: 165 °C
- Uses tiny capacitors
- Operating junction temp. - 40 °C to 125 °C
- Available in DFN10 (3 x 3 mm).

Applications

- Hard disk drives
- Solid state drives (SSD)
- Hard disk and SSD arrays
- Set-top boxes
- DVD and Blu-ray disc drivers

Description

The STEF05D is an integrated electronic fuse optimized for monitoring output current and input voltage. Connected in series to a 5 V rail, it is capable of protecting the electronic circuitry on its output from overcurrent and overvoltage. The device has a controlled delay and turn-on time. When an overload condition occurs, the STEF05D limits the output current to a predefined safe value. If the anomalous overload condition. persists, it goes into an open state, disconnecting the load from the power supply. If a continuous short-circuit is present on the board, when power is re-applied the E-fuse initially limits the output current to a safe value, and then again goes into an open state.

The device is equipped with a thermal protection circuit. The intervention of the thermal protection is signal led to the board monitoring circuits through a signal on the Fault pin.

Unlike mechanical fuses, which must be physically replaced after a single event, the E-fuse does not degrade in its performance after short-circuit/thermal protection interventions and it is reset either by recycling the supply voltage or using the Enable pin.

The companion chip for 12 V power rails is also available with part number STEF12.

Table 1. Device summary

Order code	Package	Packaging
STEF05DPUR	DFN10 (3 x 3 mm)	Tape and reel

This is information on a product in full production. www.st.com

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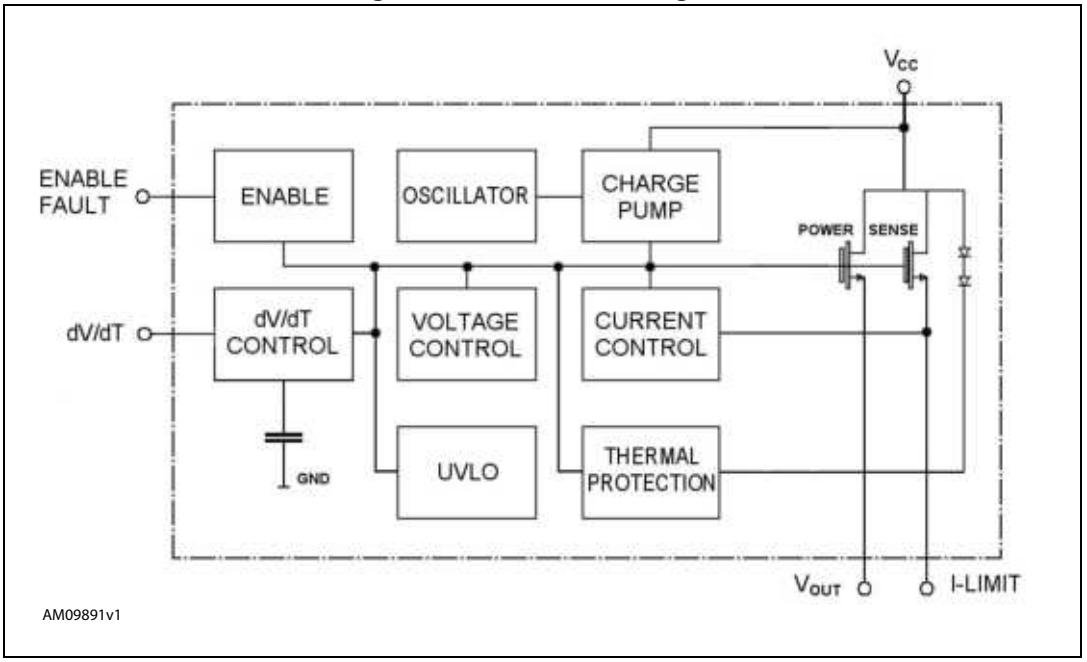
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1 Block diagram

Figure 1. Device block diagram



2 Pin configuration

Figure 2. Pin configuration (top view)

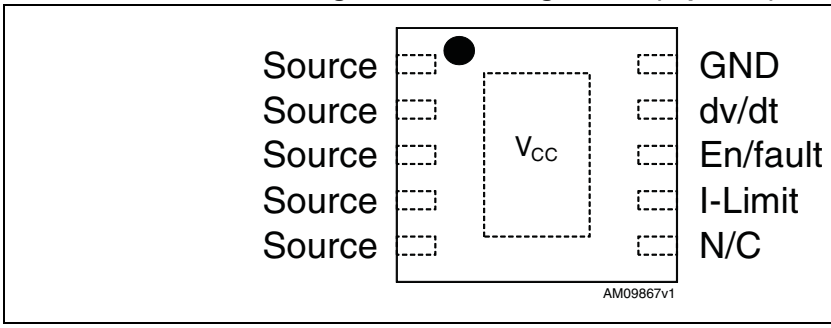


Table 2. Pin description

Pin N°	Symbol	Note
1 to 5	V_{OUT}/Source	Connected to the Source of the internal power MOSFET and to the output terminal of the fuse
6	NC	Not connected
7	I-Limit	A resistor between this pin and the Source pin sets the overload and short-circuit current limit levels.
8	En/Fault	The enable/fault pin is a tri-state, bi-directional interface. During normal operation the pin must be left floating, or it can be used to disable the output of the device by pulling it to Ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin will go to an intermediate state to signal a monitor circuit that the device is in thermal shutdown. It can be connected to another device of this family to cause a simultaneous shutdown during thermal events.
9	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn-on. The internal capacitor allows a ramp-up time of around 1ms. An external capacitor can be added to this pin to increase the ramp time. If an additional capacitor is not required, this pin should be left open.
10	GND	Ground Pin
11	V_{CC}	Exposed pad. Positive input voltage must be connected to V_{CC}.

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Positive power supply voltage (steady state)	-0.3 to 10	V
	Positive power supply voltage (max 100 ms)	-0.3 to 15	
V_{OUT}/source	(max 100 ms)	-0.3 to Vcc+0.3	V
I-Limit	(max 100 ms)	-0.3 to 15	V
En/Fault		-0.3 to 7	V
dv/dt		-0.3 to 7	V
T_{OP}	Operating junction temperature range(1)	-40 to 125	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{LEAD}	Lead temperature (Soldering) 10 sec	260	°C

1. The thermal limit is set above the maximum thermal rating. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	52.7	°C/W
R_{thJC}	Thermal resistance junction-case	17.4	°C/W

Table 5. ESD performances

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD Protection	HBM	2	KV
		MM	150	V
		CDM	500	V

4 Electrical characteristics

V_{CC} = 5 V, V_{EN} = 3.3 V, C_I = 10 µF, C_O = 47 µF, T_J = 25 °C, unless otherwise specified

Table 6. Electrical characteristics for STEF05D

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Under/Overvoltage Protection						
V_{Clamp}	Output clamping voltage	V_{CC} = 10 V	5.95	6.65	7.7	V
V_{UVLO}	Undervoltage lockout	Turn-on, voltage going up	3.2	3.6	4.3	V
V_{Hyst}	UVLO Hysteresis			0.40		V
Power MOSFET						
t_{dly}	Delay time	Enabling of chip to I_D = 100 mA with a 1 A resistive load		200		µs
R_{DSon}	ON resistance(1)	T_J = 25 °C		40	60	mΩ
		T_J = 125 °C (2)			70	
V_{OFF}	Off state output voltage	V_{CC} = 10 V, V_{GS} = 0, R_{Limit} = infinite		50	200	mV
I_D	Continuous current	0.5 inch² pad (2), T_A = 25 °C		3.6		A
		Minimum copper, T_A = 80 °C		1.7		
Current Limit						
I_{Short}	Short-circuit current limit	R_{Limit} = 11 Ω	3.1	4.1	5.1	A
I_{Lim}	Overload current limit	R_{Limit} = 11 Ω		4		A
dv/dt Circuit						
dv/dt	Output voltage ramp time	Enable to V_{OUT}=4.7V, No $C_{dv/dt}$		0.8		ms
Enable/Fault						
V_{IL}	Low level input voltage(2)	Output Disabled	0.35	0.58	0.81	V
$V_{I(INT)}$	Intermediate level input voltage(2)	Thermal Fault, Output Disabled	0.82	1.4	1.95	V
V_{IH}	High level input voltage	Output Enabled	1.96	2.64	3.3	V
$V_{I(MAX)}$	High state maximum voltage		3.4	4.3	5.4	V
I_{IL}	Low level input current (sink)	V_{Enable} = 0 V		-10	-30	µA
I_I	High level leakage current for external switch	V_{Enable} = 3.3 V			1	µA
	Maximum fan-out for fault signal	Total numbers of chips that can be connected to this pin for simultaneous shutdown			3	Units

Table 6. Electrical characteristics for STEF05D

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Total Device						
I_{Bias}	Bias current	Device operational		0.5	2	mA
		Thermal Shutdown		1		
V_{min}	Minimum operating voltage				3.1	V
Thermal Latch						
TSD	Shutdown temperature(2)			165		°C

1. Pulse test: Pulse width = 300 µs, Duty cycle = 2%
2. Limits in temperature are guaranteed by design, but not tested in production

5 Typical application

Figure 3. Application circuit

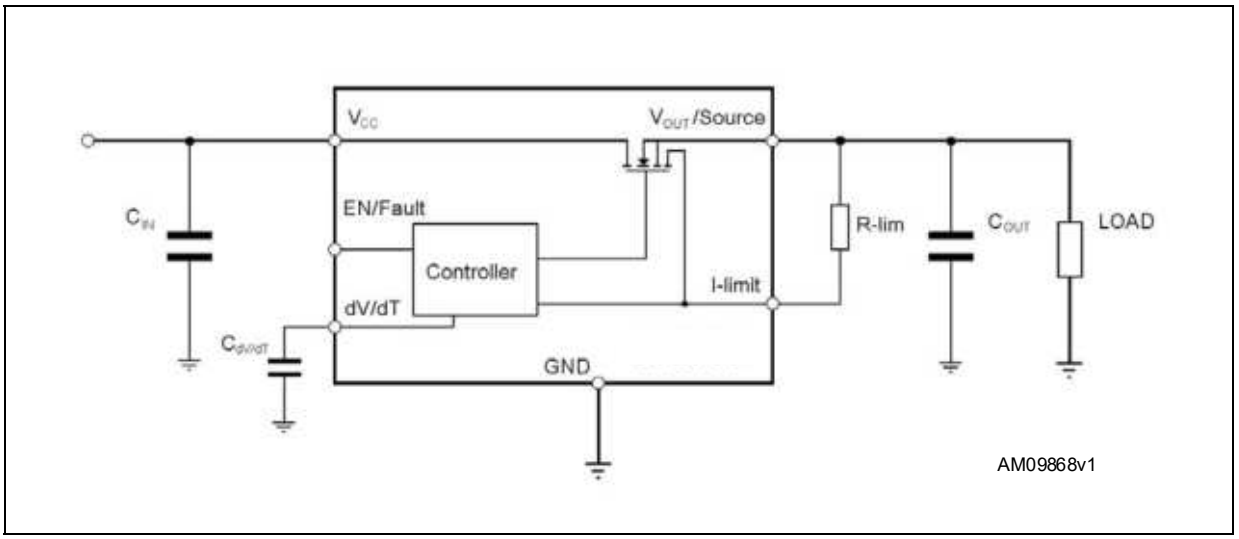
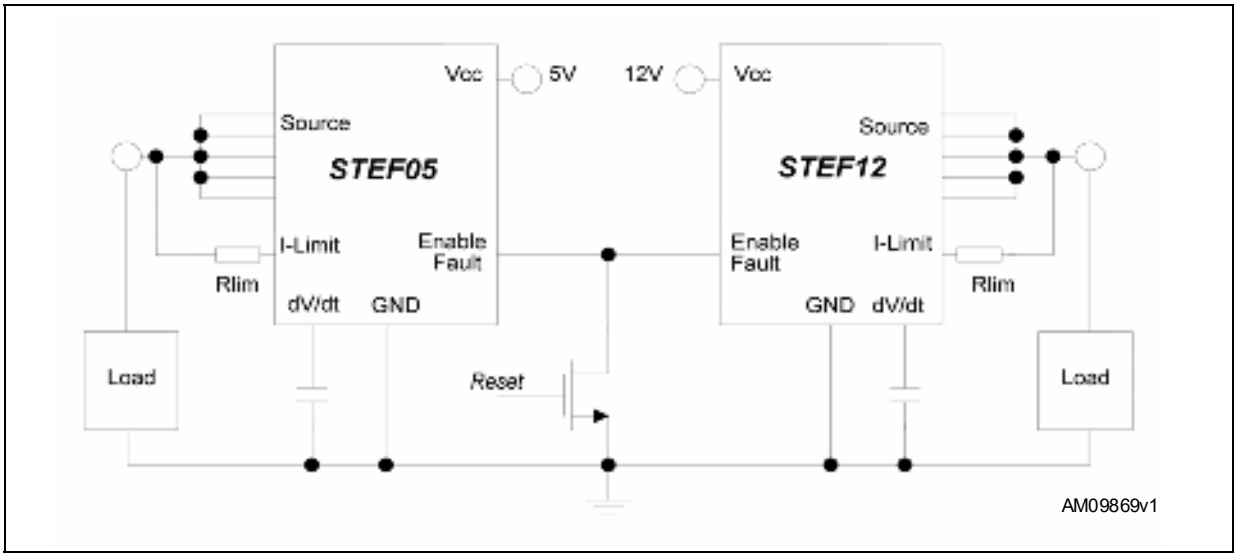


Figure 4. Typical HDD application circuit



5.1 Operating modes

5.1.1 Turn-on

When the input voltage is applied, the Enable/Fault pin goes up to the high state, enabling the internal control circuitry.

After an initial delay time of typically 200 µs, the output voltage is supplied with a slope defined by the internal dv/dt circuitry. If no additional capacitor is connected to dv/dt pin, the total time from the Enable signal going high and the output voltage reaching the nominal value is around 1 ms (refer to *Figure 5 and Figure 7*).

5.1.2 Normal operating condition

The STEF05D E-fuse behaves like a mechanical fuse, buffering the circuitry on its output with the same voltage shown at its input, with a small voltage fall due to the N-channel MOSFET R_{DSOn}.

5.1.3 Output voltage clamp

This internal protection circuit clamps the output voltage to a maximum safe value, typically 6.65V, if the input voltage exceeds this threshold.

5.1.4 Current limiting

When an overload event occurs, the current limiting circuit reduces the conductivity of the power MOSFET, in order to clamp the output current at the value selected externally by means of the limiting resistor R_{Limit} (*Figure 3*).

5.1.5 Thermal shutdown

If the device temperature exceeds the thermal latch threshold, typically 165°C, the thermal shutdown circuitry turns the power MOSFET off, thus disconnecting the load. The EN/Fault pin of the device will automatically be set at an intermediate voltage, in order to signal the overtemperature event.

From this condition the E-fuse can be reset either by cycling the supply voltage or by pulling down the EN pin below the V_{il} threshold, and then releasing it.

5.2 R_{Limit} calculation

As shown in *Figure 3*, the device uses an internal N-channel sense FET with a fixed ratio, to monitor the output current and limit it at the level set by the user.

The R_{Limit} value for achieving the requested current limitation can be estimated by using the following theoretical formula, together with the graph in *Figure 13*:

Equation 1

$$R_{Limit} = \frac{42}{Ishort}$$

5.3 $C_{dv/dt}$ calculation

Connecting a capacitor between the $C_{dv/dt}$ pin and GND will allow the modification of the output voltage ramp time.

Given the desired time interval Δt during which the output voltage goes from zero to his maximum value, the capacitance to be added on $C_{dv/dt}$ pin can be calculated using the following theoretical formula:

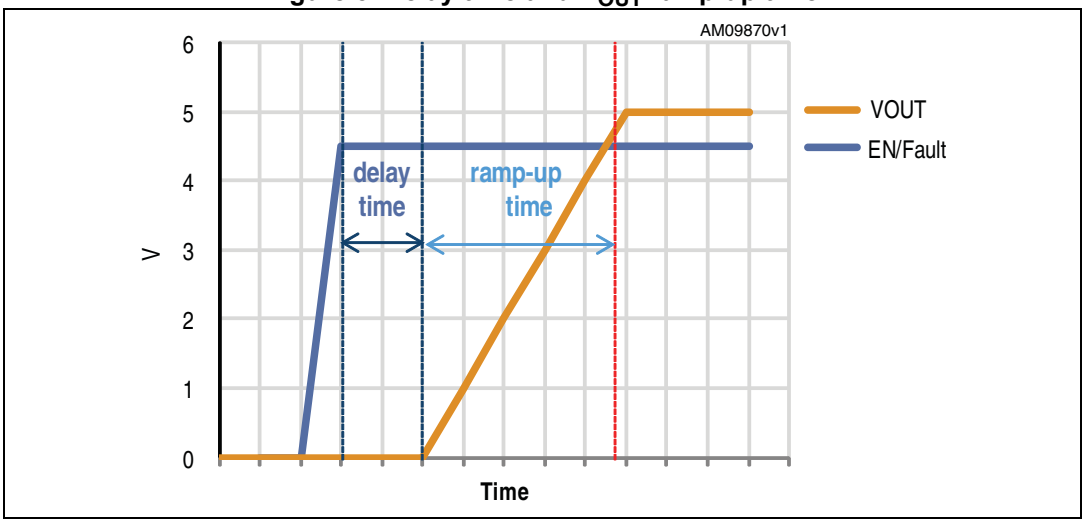
Equation 2

$$C_{dvdt} = 36 \times 10^{-9} \Delta t - 30x10^{-12}$$

Where $C_{dv/dt}$ is expressed in Farad, and the time Δt in seconds.

Figure 5 shows a graphical explanation of delay time and ramp-up time.

Figure 5. Delay time and V_{OUT} ramp-up time



5.4 Enable/fault pin

The Enable/Fault pin has the dual function of controlling the output of the device and, at the same time, of providing information about the device status to the application.

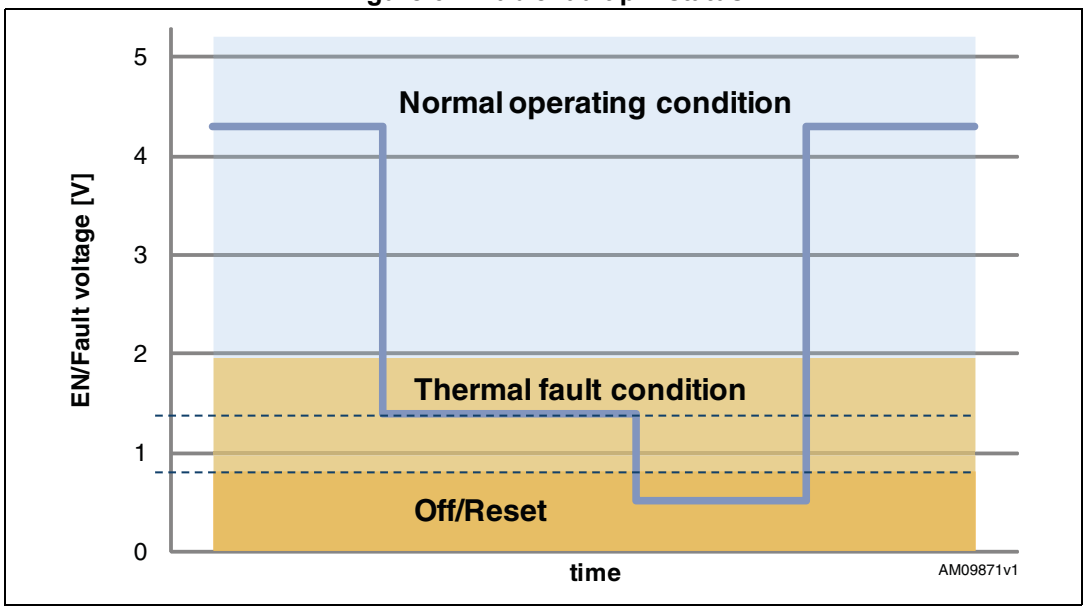
When it is used, it should be connected to an external open-drain or open-collector device. In this case, when it is pulled at low logic level, it turns the output of the E-Fuse off.

If this pin is left floating, since it has internal pull-up circuitry, the output of the E-Fuse is kept ON in normal operating conditions.

In case of thermal fault, the pin is pulled to an intermediate state (*Figure 6*). This signal can be provided to a monitor circuit, informing it that a thermal shutdown has occurred, or it can be directly connected to the Enable/Fault pins of other STEFxx devices on the same application in order to achieve a simultaneous enable/disable feature.

When a thermal fault occurs, the device can be reset either by cycling the supply voltage or by pulling down the Enable pin below the V_{il} threshold and then releasing it.

Figure 6. Enable/fault pin status



6 Typical performance characteristics

The following plots are referred to the typical application circuit and, unless otherwise noted, at T_A = 25°C.

Figure 7. V_{OUT} ramp-up vs. EN/fault

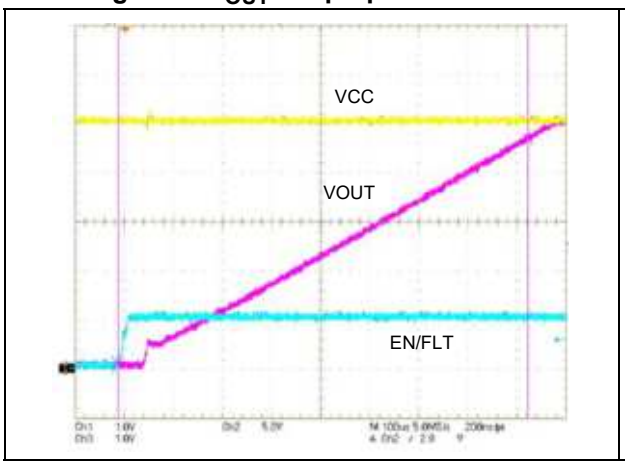


Figure 8. Startup vs. V_{CC}

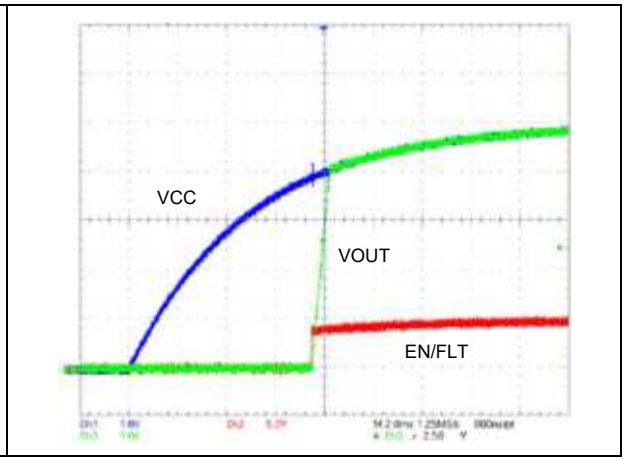


Figure 9. Startup @ short-circuit

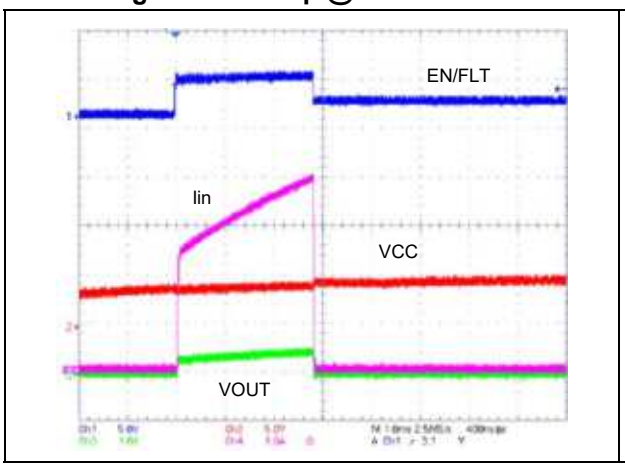


Figure 10. Startup @ heavy load

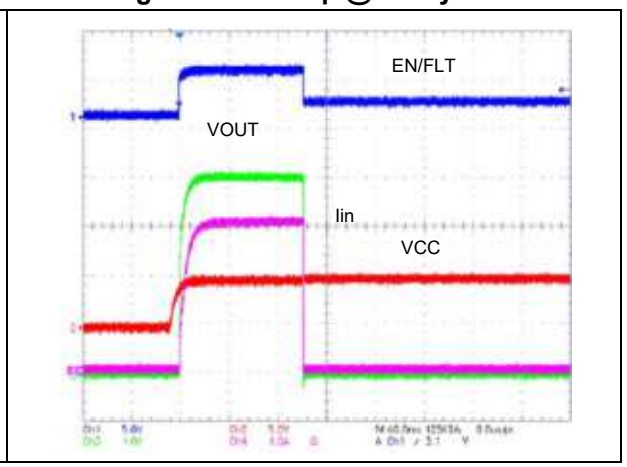


Figure 11. Startup vs. EN/fault

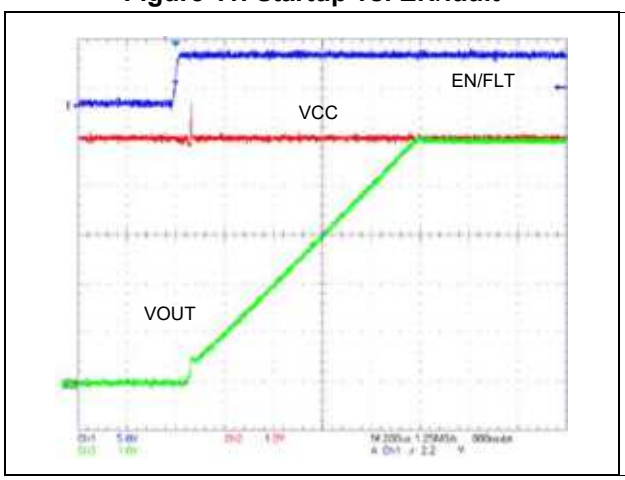


Figure 12. Clamp voltage

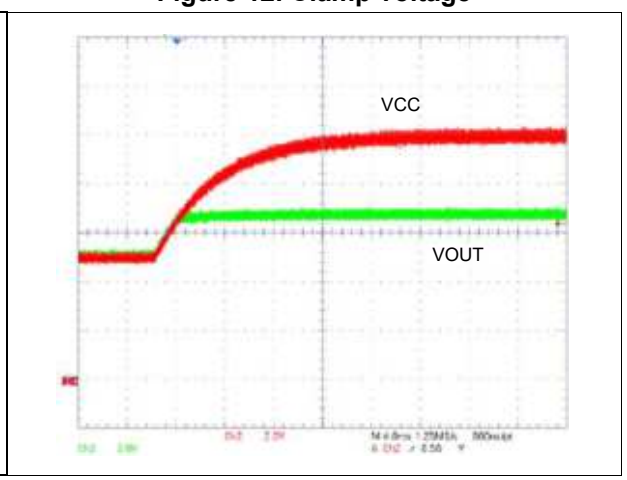


Figure 13. Current limit and short circuit current vs. R_{limit}

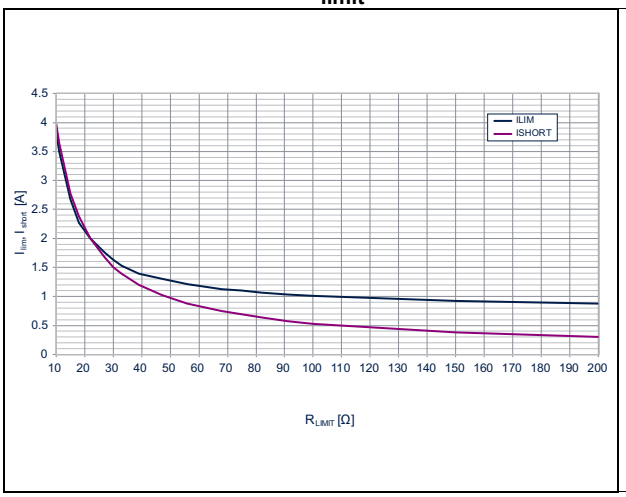
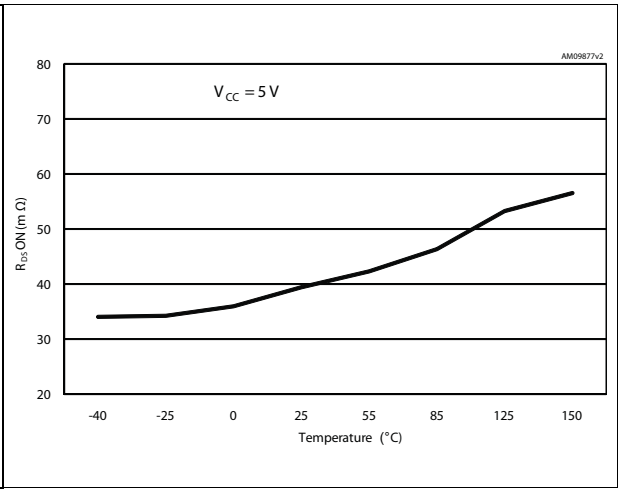


Figure 14. R_{DSON} vs. temperature



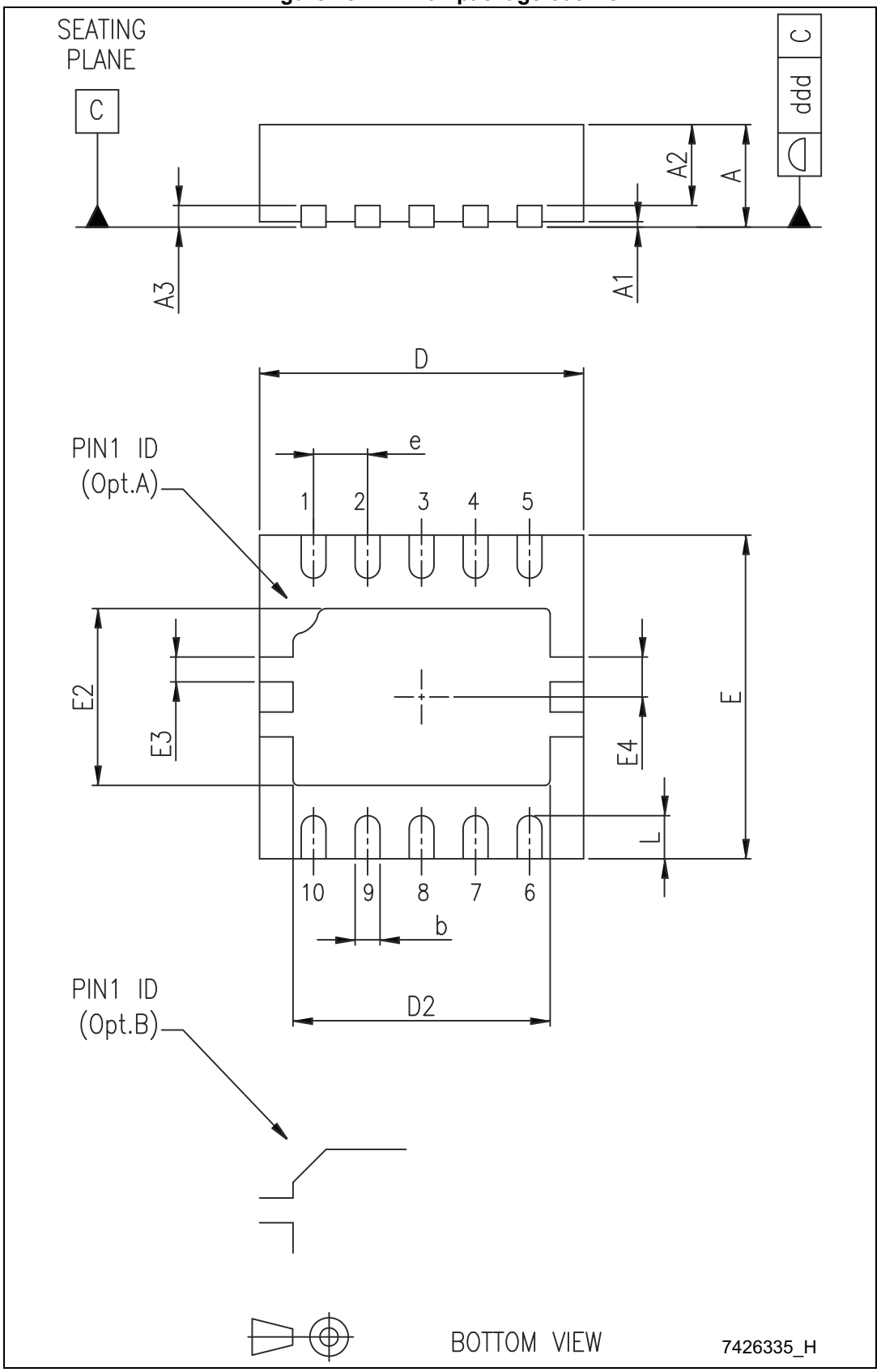
7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 7. DFN10L (3 x 3 mm.) mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A2	0.55	0.65	0.80
A3		0.20	
b	0.18	0.25	0.30
D	2.85	3.00	3.15
D2	2.20		2.70
E	2.85	3.00	3.15
E2	1.40		1.75
E3	0.230		
E4	0.365		
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

Figure 15. DFN10L package outline



Tape and reel QFNxx/DFNxx (3x3 mm) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	

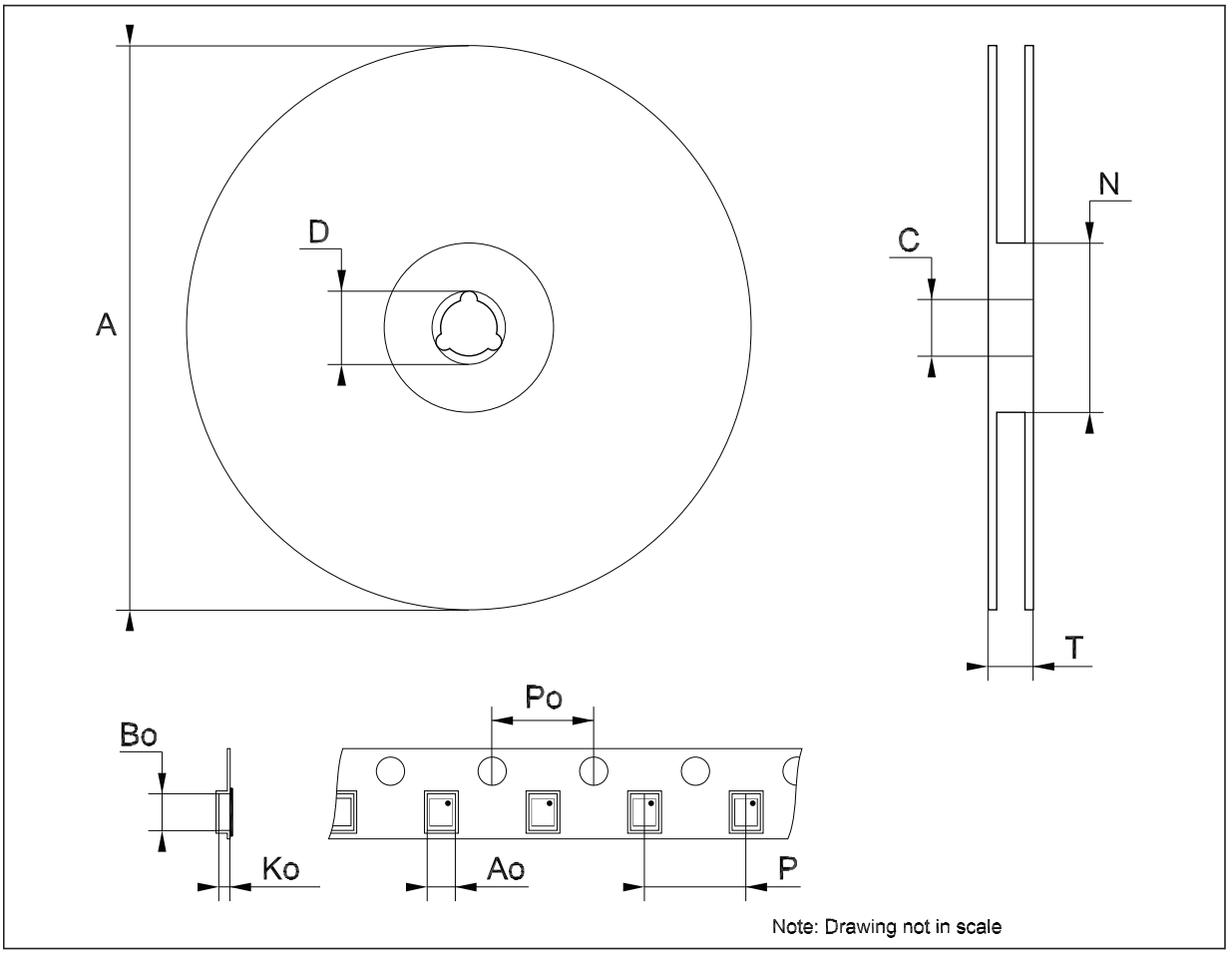
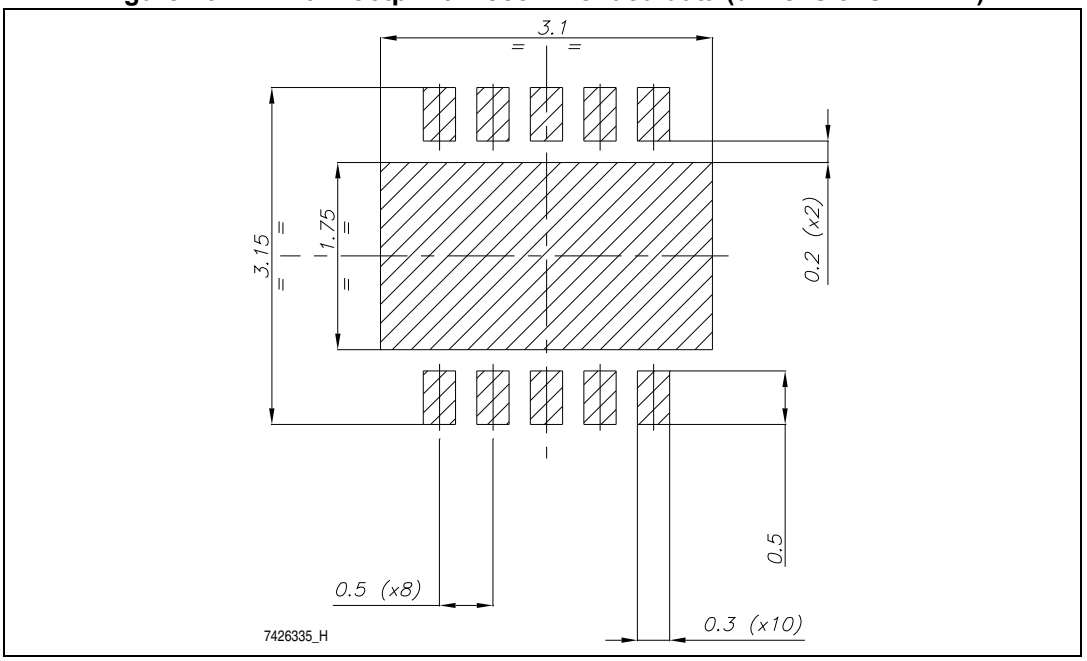


Figure 16. DFN10L footprint - recommended data (dimensions in mm.)



8 Revision history

Table 8. Document revision history

Date	Revision	Changes
19-Mar-2013	1	Initial release.
22-May-2020	2	Datasheet promoted from preliminary data to production data. Updated *Figure 13*.

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