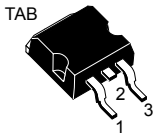
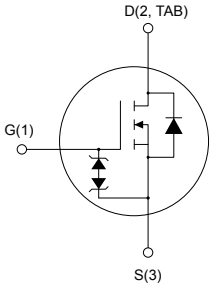
STB9NK80Z

Datasheet

Automotive-grade N-channel 800 V, 1.5 Ω typ., 5.2 A SuperMESH Power MOSFET in a D²PAK package



D²PAK



AM01476v1_tab

STPOWER

Product status link
STB9NK80Z

Product summary	
Order code	STB9NK80Z
Marking	B9NK80Z
Package	D²PAK
Packing	Tape and reel

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB9NK80Z	800 V	1.8 Ω	5.2 A

- AEC-Q101 qualified
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	800	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	5.2	A
I_D	Drain current (continuous) at T_C = 100 °C	3.3	A
I_{DM} (1)	Drain current (pulsed)	20.8	A
P_{TOT}	Total power dissipation at T_C = 25 °C	125	W
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	4	kV
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 5.2 A, di/dt ≤ 200 A/µs, V_{DD} ≤ $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1	°C/W
R_{thJA}	Thermal resistance junction-to-ambient	62.5	

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} (1)	Avalanche current, repetitive or not-repetitive	5.2	A
E_{AS} (2)	Single pulse avalanche energy	210	mJ

1. *Pulse width limited by T_J max.*
2. *Starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V			1	µA
		V_{GS} = 0 V, V_{DS} = 800 V, T_C = 125 °C (1)			50	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.6 A		1.5	1.8	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 2.6 A		5		S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1138	-	pF
C_{oss}	Output capacitance			122		
C_{rss}	Reverse transfer capacitance			25		
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 V to 640 V	-	50	-	pF
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 2.6 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	40	-	nC
Q_{gs}	Gate-source charge			7		
Q_{gd}	Gate-drain charge			21		

1. *Pulsed: pulse duration=300µs, duty cycle 1.5%.*
2. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS}increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 2.6 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	20	-	ns
t_r	Rise time			12		
$t_{d(off)}$	Turn-off delay time			45		
t_f	Fall time			22		
$t_{r(Voff)}$	Off-voltage rise time	V_{DD} = 640 V, I_D = 5.2 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)		12		
t_f	Fall time			10		
t_c	Cross-over time			20		

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5.2	A
I_{SDM} (1)	Source-drain current (pulsed)		-		20.8	
V_{SD} (2)	Forward on voltage	I_{SD} = 5.2 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 5.2 A, di/dt = 100 A/µs	-	530		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 50 V, T_J = 150 °C	-	3.31		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	12.5		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

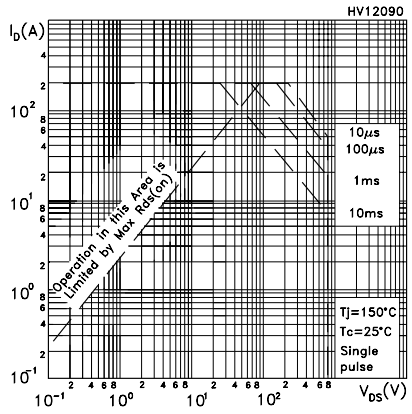


Figure 2. Thermal impedance

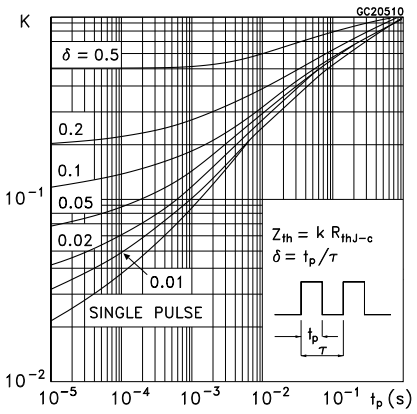


Figure 3. Output characteristics

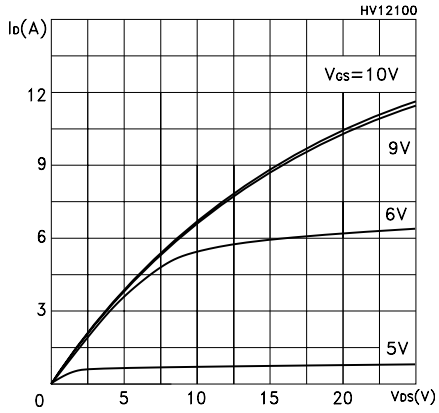


Figure 4. Transfer characteristics

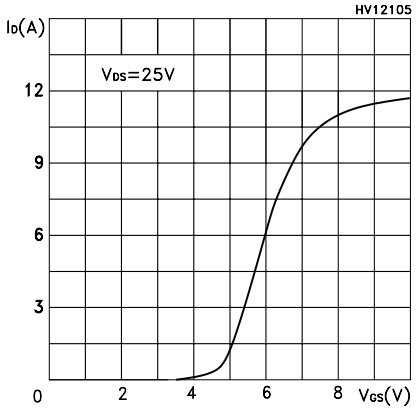


Figure 5. Transconductance

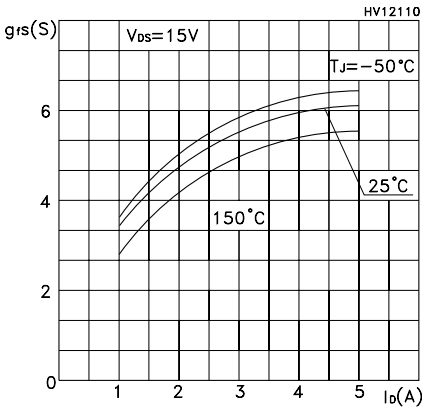


Figure 6. Static drain-source on- resistance

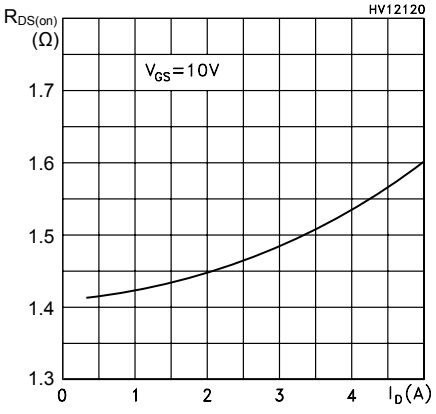


Figure 7. Gate charge vs gate-source voltage

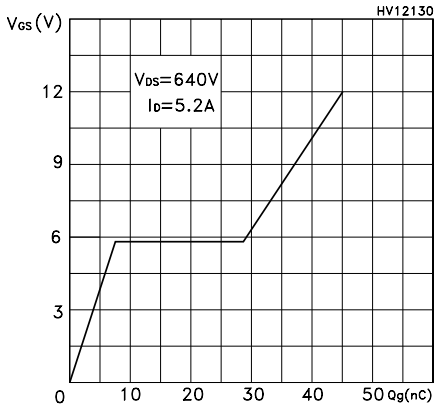


Figure 8. Capacitance variations

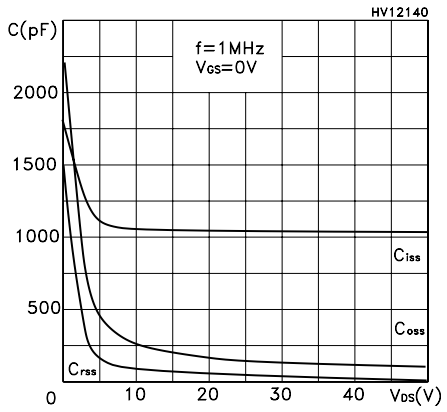


Figure 9. Normalized gate threshold voltage vs temperature

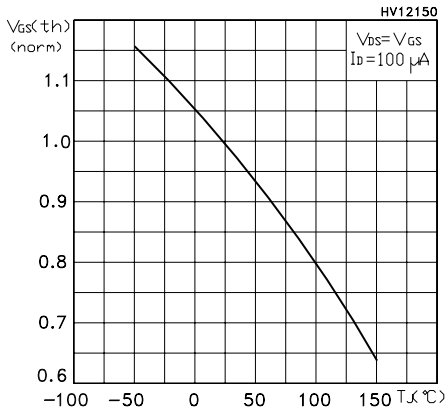


Figure 10. Normalized on-resistance vs temperature

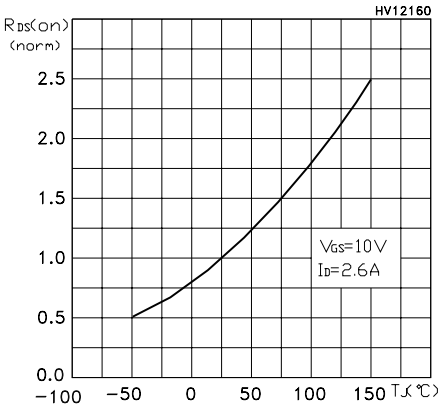


Figure 11. Source-drain diode forward characteristics

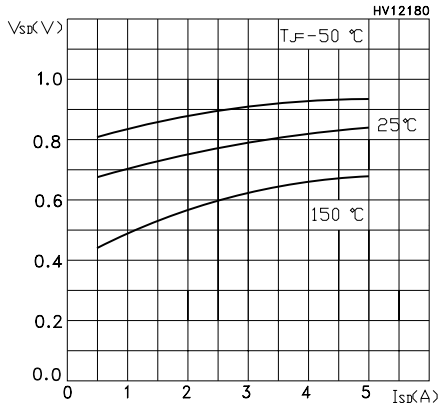


Figure 12. Normalized breakdown voltage vs temperature

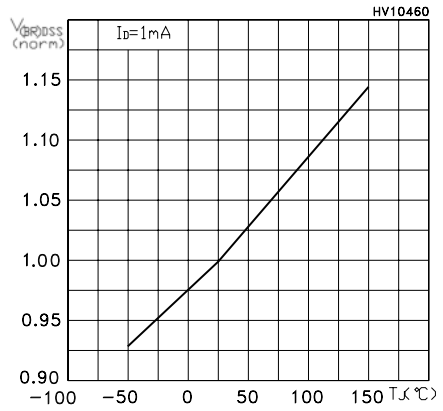
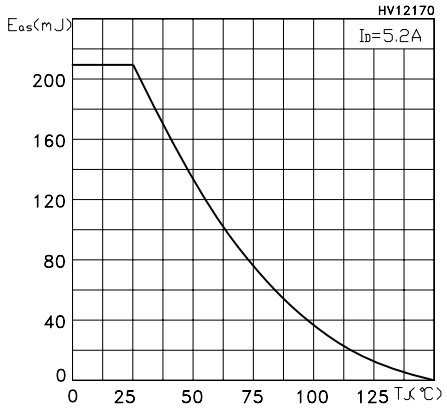
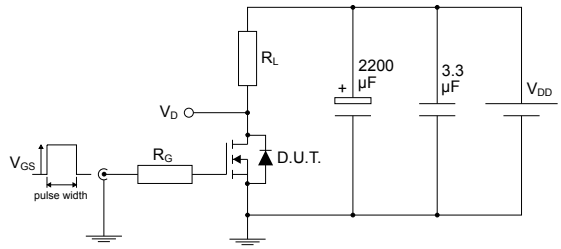


Figure 13. **Maximum avalanche energy vs temperature**



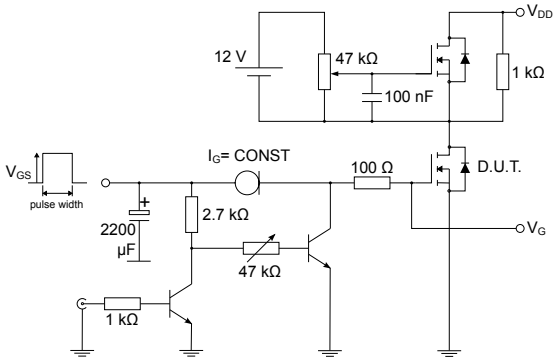
3 Test circuits

Figure 14. Test circuit for resistive load switching times



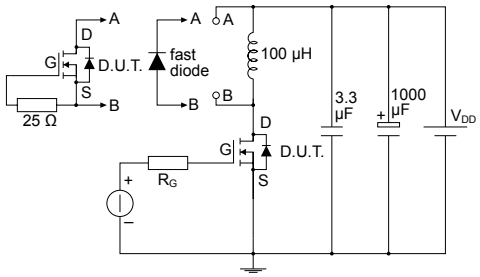
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Figure 15. Test circuit for gate charge behavior



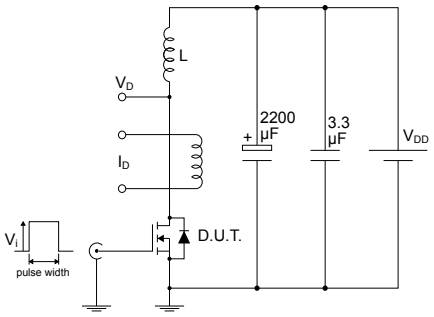
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Figure 16. Test circuit for inductive load switching and diode recovery times



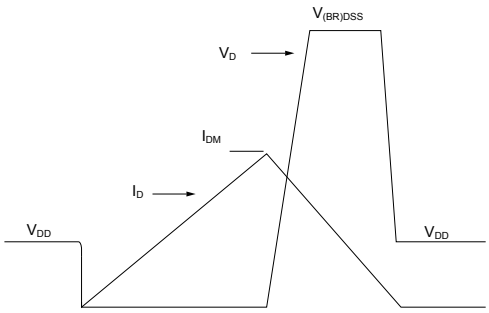
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Figure 17. Unclamped inductive load test circuit



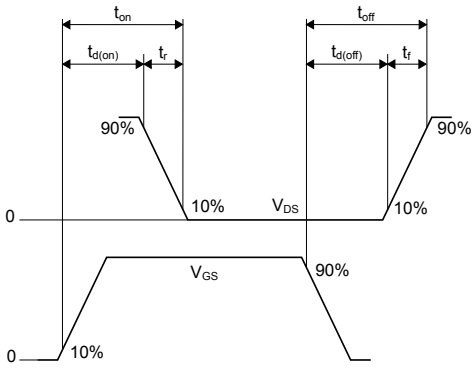
AM01471v1

Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 20. **D²PAK (TO-263) type A package outline**

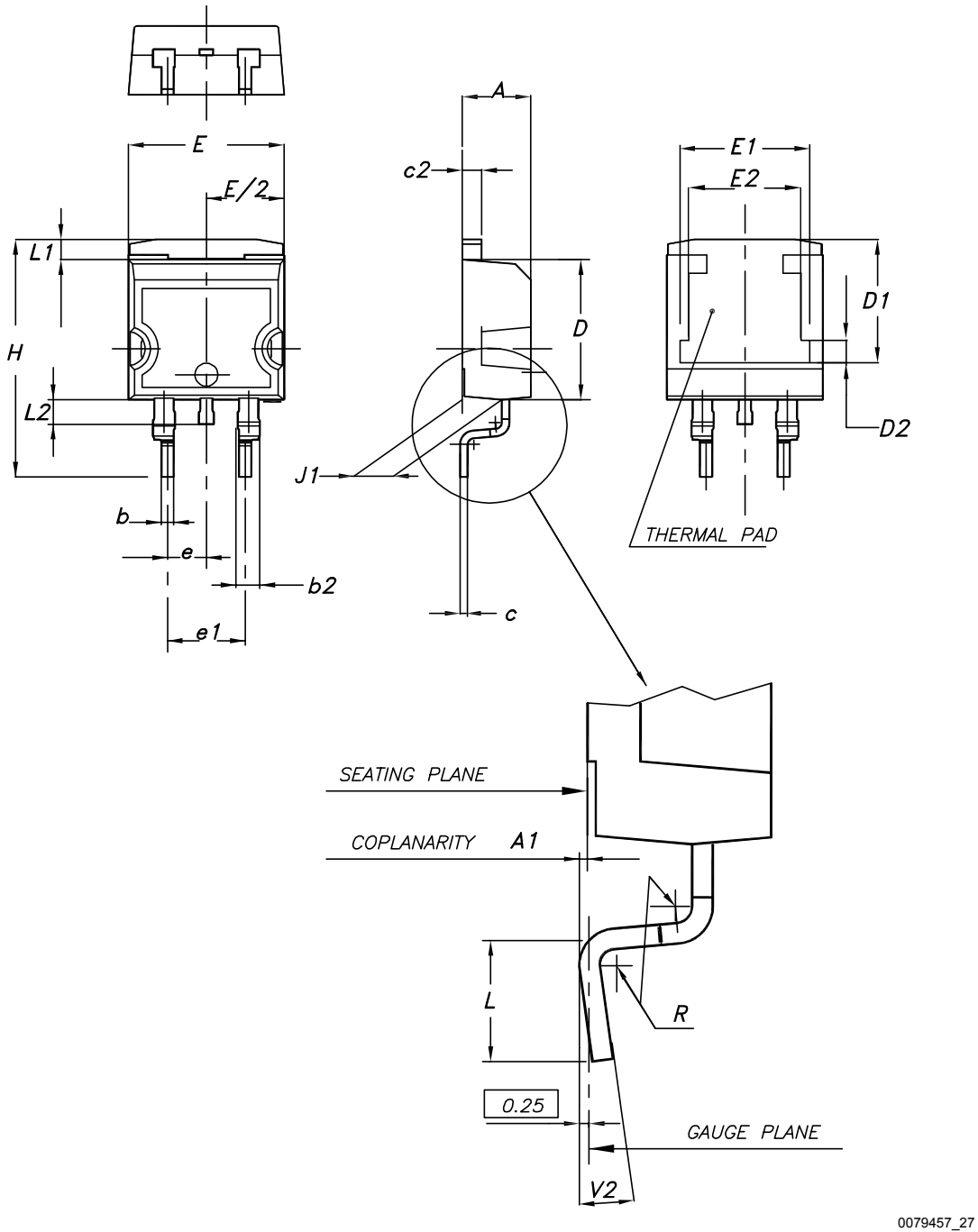
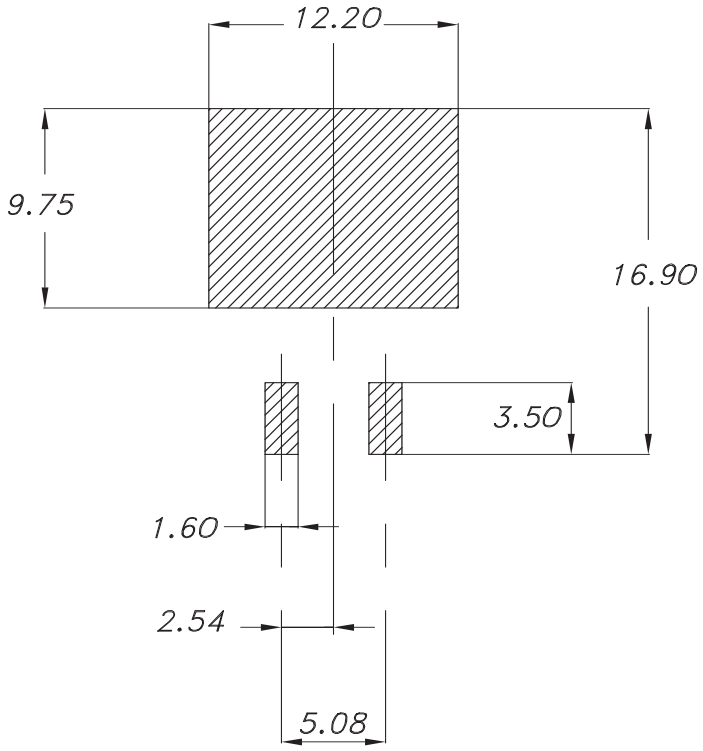


Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

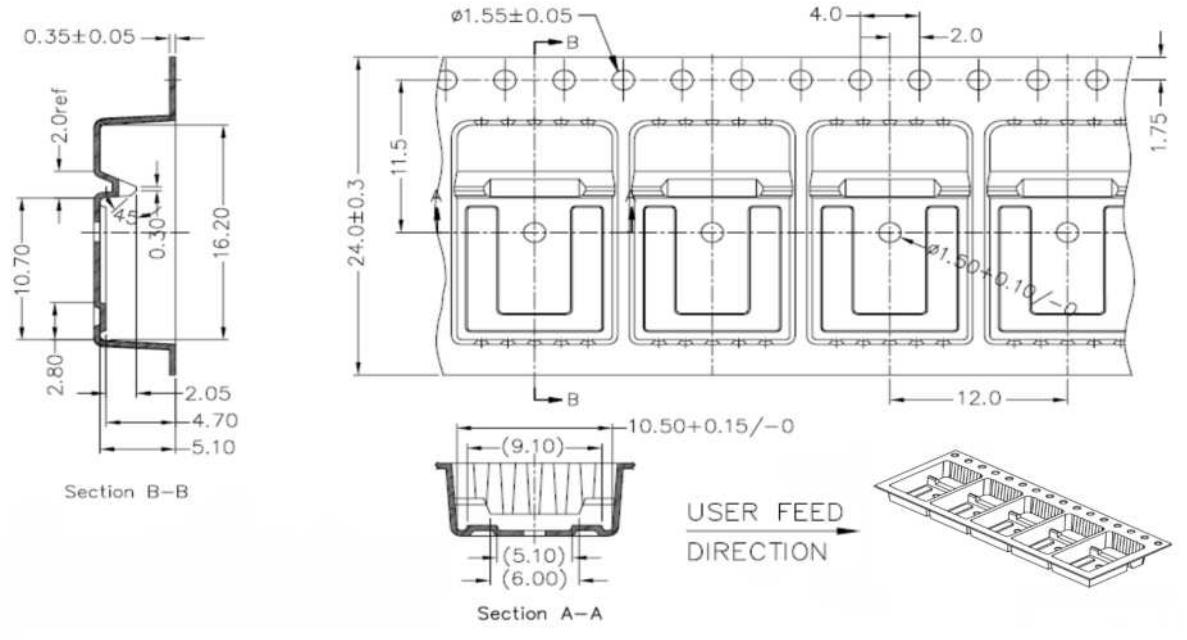
Figure 21. D²PAK (TO-263) recommended footprint (dimensions are in mm)



0079457_Rev27_footprint

4.2 D²PAK packing information

Figure 22. D²PAK tape drawing (dimensions are in mm)



DM01095771_3

Revision history

Table 9. **Document revision history**

Date	Version	Changes
05-Jun-2013	1	First issue.
12-Jul-2013	2	Document status promoted from preliminary to production data.
21-Oct-2019	3	Modified *Table 5. Dynamic* and *Section 4.1 D²PAK (TO-263) type A package information*. Minor text changes.
22-Aug-2025	4	Updated *Section 4: Package information.* Minor text changes.
25-Jun-2026	5	Updated Section 4: Package information.

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