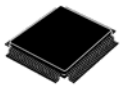
SPC570S40E1, SPC570S40E3, SPC570S50E1, SPC570S50E3

32-bit Power Architecture® microcontroller for automotive ASILD applications

Datasheet - production data



eTQFP100 (14 x 14 x 1.0 mm)



eTQFP64 (10 x 10 x 1.0 mm)

Features



- AEC-Q100 qualified
- High performance e200z0h dual core
  - 32-bit Power Architecture technology CPU
  - Core frequency as high as 80 MHz
  - Single issue 4-stage pipeline in-order execution core
  - Variable Length Encoding (VLE)
- Up to 544 KB (512 KB code + 32 KB data, suitable for EEPROM emulation) on-chip flash memory: supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- Up to 48 KB on-chip general-purpose SRAM
- Multi-channel direct memory access controller (eDMA paired in lockstep) with 16 channels
- Comprehensive new generation ASILD safety concept
  - Safety of bus masters (core+INTC, DMA) by delayed lockstep approach
  - Safety of storage (Flash, SRAM) by mainly ECC
  - Safety of the data path to storage and periphery by mainly End-to-End EDC (E2E EDC)
  - Clock and power, generation and distribution, supervised by dedicated monitors
  - Fault Collection and Control Unit (FCCU) for collection and reaction to failure notifications
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
  - Boot time MBIST and LBIST for latent faults
  - Check of safety mechanisms availability and error reaction path functionality by dedicated mechanisms
  - Safety of the periphery by application-level measures supported by replicated peripheral bridges and by LBIST
  - Further measures on dedicated peripherals (e.g. ADC supervisor)
  - Junction temperature sensor
  - 8-region system memory protection unit (SMPU) with process ID support (tasks isolation)
  - Enhanced SW watchdog
  - Cyclic redundancy check (CRC) unit
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Nexus Class 3 debug and trace interface
- Communication interfaces
  - 2 LINFlexD modules, 3 deserial serial peripheral interface (DSPI) modules, and Up to 2 FlexCAN interfaces with 32 message buffers each
- On-chip CAN/UART Bootstrap loader with Boot Assisted Flash (BAF). Physical Interface (PHY) can be
  - UART and CAN
- 2 enhanced 12-bit SAR analog converters
  - 1.5 µs conversion time (12 MHz)
  - 16 physical channels (fully shared between the 2 SARADC units)
  - Supervisor ADC concept
  - Programmable Cross Triggering Unit (CTU)
- Single 3.3 V or 5 V voltage supply
- 4 general purpose eTimer units (6 channels each)
- Junction temperature range -40 °C to 150 °C (165 °C grade optional)

This is information on a product in full production. www.st.com

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1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

1.2 Description

The SPC570Sx is a family of next generation microcontrollers built on the Power Architecture embedded category.

The SPC570Sx family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of Chassis and Safety electronics applications within the vehicle. The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 80 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 1. SPC570Sx device feature summary (Family Superset Configuration)

Feature		Description
Process		55 nm
Main processor	Core	e200z0h
	Number of main cores	1
	Number of checker cores	1
	VLE	Yes
	Main processor frequency	80 MHz(1)
Interrupt controllers (including interrupt controller checker)		1
Software watchdog timer		1
System timers		1 AUTOSAR® STM 1 PIT with four 32-bit channels
DMA (including DMA checker)		1
DMA channels		16
SMPU		Yes (8 regions)(2)
System SRAM		Up to 48 KB
Code flash memory		Up to 512 KB

Table 1. SPC570Sx device feature summary (Family Superset Configuration) (continued)

Feature		Description
Data flash memory (suitable for EEPROM emulation)		32 KB
UTEST flash memory		8 KB
Boot assist flash (BAF)		8 KB
CRC		1
LINFlexD		Up to 2
FlexCAN		Up to 2
DSPI		3
eTimer		4 x 6 channels
ADC (SAR)		2(3)
CTU (Cross Triggering Unit)		1
Temperature sensor		1
Self-test control unit (memory and logic BIST)		1
FCCU		1
MEMU		1
PLL		Dual PLL with FM
Nexus		3(4)
Sequence processing unit (SPU)		1
External power supplies		5 V(5) 3.3 V(5)
Junction temperature		–40 to 150 °C
		165 °C grade optional (6)
Packages	Device SPC570SxxE3	eTQFP100
	Device SPC570SxxE1	eTQFP64

1. Includes user programmable CPU core and one safety core. The two e200z0h processors in the lockstep pair run at 80 MHz. The e200z0h is compatible with the Power Architecture embedded specification.
2. SMPU with process ID support extension
3. One ADC can be used as supervisor ADC
4. Including trace for the crossbar masters (data & instruction trace on core and data trace on eDMA). 4 MDO pin Nexus trace port.
5. All I/Os can be supplied at 3.3 V or 5 V (mutually exclusive)
6. Refer to technical note "SPC570S family - High Temperature "D" Grade (DocID031416 - TN1262)" for associated specification limitation.

Table 2. SPC570S40Ex, SPC570S50Ex device configuration differences

	SPC570S40 (full option configuration)	SPC570S50 (full option configuration)
Flash	256 KB(1)	512 KB
RAM	32 KB(2)	48 KB
CAN	1(3)	2
Others	aligned to the *SPC570Sx device feature summary (Family Superset Configuration)* described in *Table 1*	

1. Flash blocks excluded on SPC570S40:
   128K Block 0 [0x0100_0000 … 0x0101_FFFF]
   128K Block 1 [0x0102_0000 … 0x0103_FFFF]
2. SRAM area excluded on SPC570S40
   [0x4000_8000…0x4000_BFFF]
3. FlexCAN1 excluded on SPC570S40

1.3 Feature overview

On-chip modules within the SPC570Sx include the following features:

- 2 main CPUs, single-issue, 32-bit CPU core complexes (e200z0h), running in lockstep
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
- Up to 544 KB (512 KB code + 32 KB data, suitable for EEPROM emulation) on-chip flash memory: supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- Up to 48 KB on-chip general-purpose SRAM
- Multi-channel direct memory access controller (eDMA paired in lockstep)
  - 16 channels per eDMA
- Interrupt controller (INTC) with dedicated interrupt source channels, including software interrupts and 32 priority levels
- Dual phase-locked loops with stable clock domain for peripherals and frequency modulation domain for computational shell
- Crossbar switch architecture for concurrent access to peripherals, flash memory, or SRAM from multiple bus masters with end-to-end ECC
- System integration unit lite (SIUL2)
- Boot Assist Flash (BAF) supports factory programming using serial bootload through ‘UART Serial Boot Mode Protocol’. Physical Interface (PHY) can be
  - UART / LIN
  - CAN
- Enhanced analog-to-digital converter system
  - 2 separate 12-bit SAR analog converters
  - 1.5 µs conversion time (at 12 MHz)
  - 16 physical channels
- Temperature sensor
  - Range –40 to +150 °C
  - Sensitivity approximately 5.14 mV/°C
- STCU2
  - Support for Logic BIST and Memory BIST at power on
  - ASIL D
- 3 deserial serial peripheral interface (DSPI) modules
- 2 LIN and UART communication interface (LINFlexD) modules
  - LINFlexD_0 (master/slave)
  - LINFlexD_1 (master)
- Up to 2 FlexCAN modules
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with partial support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- On-chip voltage regulator controller manages the supply voltage down to 1.2 V for core logic

2 Block diagram

Figure 1 shows the top-level block diagram.

Figure 1. Block diagram

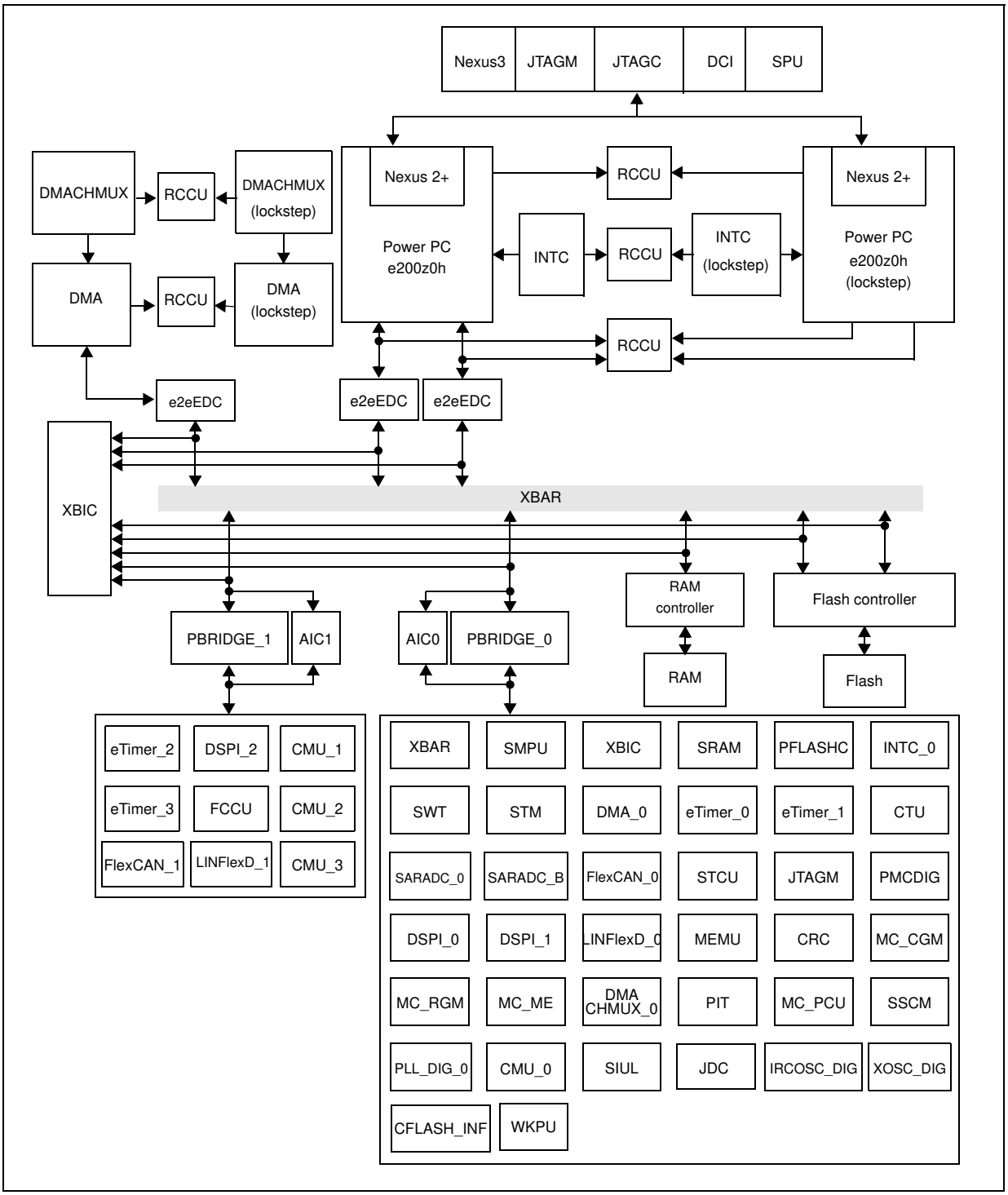


Table 3 summarizes the functions of all blocks present in the SPC570Sx series of microcontrollers. Please note that the presence and number of blocks vary by device and package.

Table 3. SPC570Sx series block summary

Block	Function
e200z0 CPU	Allows single clock instruction execution
Analog-to-digital converter (ADC)	Multi-channel, 12-bit analog-to-digital converter
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via 16 programmable channels.
DMACHMUX	Allows to route a defined number of DMA peripheral sources to the DMA channels
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
PLL0	Output independent of core clock frequency
Frequency-modulated phase-locked loop (PLL1)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
AIPS	System bus to peripheral bus interface
RAM controller	Acts as an interface between the system bus and the integrated system RAM
System RAM	Supports read/write accesses mapped to the SRAM memory from any master
Flash memory controller	Acts as an interface between the system bus and the Flash memory module
Flash memory	Up to 512 KB of programmable, non-volatile Flash memory for code and 32 KB for data
IRCOSC	Controls the internal 16 MHz RC oscillator system
XOSC	Controls the on-chip oscillator (XOSC) and provides the register interface for the programmable features
JTAG Master	Provides software the option to write data for driving JTAG
JTAG Data Communication Module	Provides the capability to move register data between the IPS and JTAG domains
PASS	Programs a set of Flash memory access protections, based on user programmable passwords
Sequence Processing Unit	Provides an on-device trigger functions similar to those found on a logic analyzer
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load

Table 3. SPC570Sx series block summary (continued)

Block	Function
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
MC_PMC	Contains registers that enable/disable the various voltage monitors
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device
eTimer	Has six 16-bit general purpose counter, where each counter can be used as input capture or output compare function
FCCU	Collects fault event notification from the rest of the system and translates them into internal and/or external system reactions
RCCU	Compares input signals and issues an alarm in the case of a mismatch
MEMU	Collects and reports error events associated with ECC (Error Correction Code) logic used on SRAM, DMA RAM and Flash memory
XBIC	Verifies the integrity of the attribute information for crossbar transfers and signals the Fault Collection and Control Unit (FCCU) when an error is detected
STCU2	Handles the BIST procedure
CRC	Controls the computation of CRC, off-loading this work from the CPU
RegProt	Protects several registers against accidental writing, locking their value till the next reset phase
Temperature sensor	Monitors the device temperature
Debug Control Interface	Provides debug features for the MCU
Nexus Port Controller	Monitor a variety of signals including addresses, data, control signals, status signals, etc.
Nexus Multimaster Trace Client	Monitors the system bus and provides real-time trace information to debug or development tools
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
System integration unit (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code

Table 3. SPC570Sx series block summary (continued)

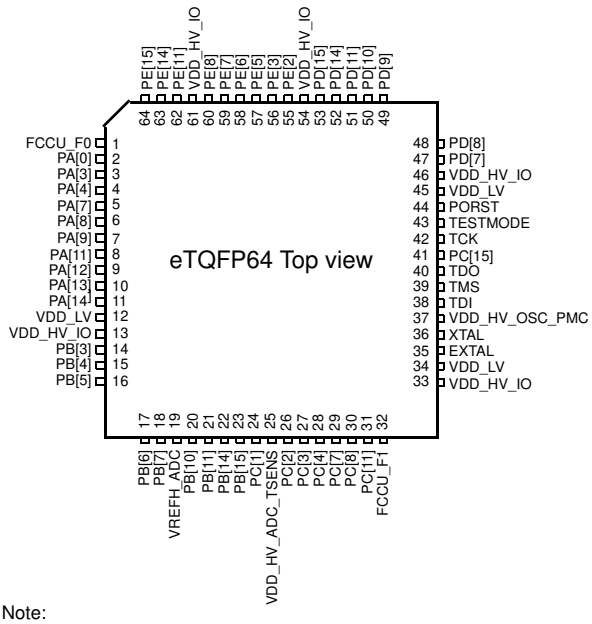
Block	Function
Wakeup unit (WKPU)	The wakeup unit supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.
Crossbar (XBAR) switch	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

3 Package pinouts and signal descriptions

3.1 Package pinouts

The available eTQFP pinouts are provided in the following figures. For pin signal descriptions, please refer to the device reference manual.

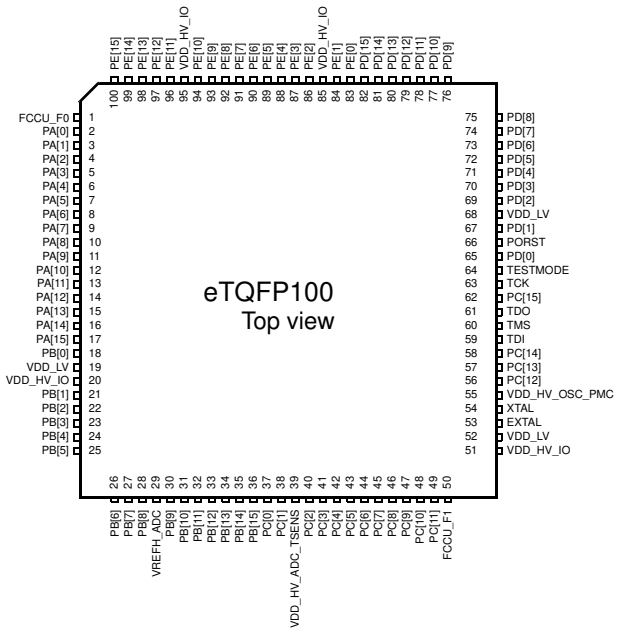
Figure 2. eTQFP 64-pin configuration[a]



Note:
Availability of port pin alternate functions depends on product selection.

a. All eTQFP64 information is indicative and must be confirmed during silicon validation.

Figure 3. eTQFP 100-pin configuration



Note:
Availability of port pin alternate functions depends on product selection.

3.2 Pin descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC570Sx devices.

For information on the signal descriptions and related information about the functionality and configuration of the SPC570Sx devices, refer to the "Signal description" chapter in the devices' reference manual.

3.3 Package pads/pins

Table 4 shows the eTQFP64 and eTQFP100 pinouts. The default reset state for all the pins associated with a programmable alternate function is GPIO.

Note: Nexus pins can be enabled via JTAG during the reset phase

Table 4. eTQFP64 and eTQFP100 pinout

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
—	FCCU_F0	1	1	IO	FCCU_F0(1)			
PA[0]	PAD[0]	2	2	IO	DSPI 0 - CS 0	Ext. INT 0	DSPI 1 - CS 1	Timer 0 - ch. 0
PA[1]	PAD[1]	—	3	IO	DSPI 1 - CS 1	Timer 0 - ch. 0	Nexus EVTI	Timer 1 - ch. 0
PA[2]	PAD[2]	—	4	IO	DSPI 2 - CS 1	DSPI 0 - CS 4	Nexus EVTO	Timer 1 - ch. 1
PA[3]	PAD[3]	3	5	IO	DSPI 0 - CLK	Ext. INT 1	Timer 0 - ch. 0	DSPI 1 - CLK
PA[4]	PAD[4]	4	6	IO	DSPI 0 - Serial Data	NMI	Timer 0 - ch. 1	DSPI 1 - Serial Data
PA[5]	PAD[5]	—	7	IO	LINFlex 1 - TX	Timer 0 - ch. 1	Nexus MCK 0	Timer 1 - ch. 2
PA[6]	PAD[6]	—	8	IO	LINFlex 1 - RX	Timer 0 - ch. 2	Nexus MDO 0	Timer 1 - ch. 3
PA[7]	PAD[7]	5	9	IO	DSPI 0 - Serial Data	—	Timer 0 - ch. 2	DSPI 1 - Serial Data
PA[8]	PAD[8]	6	10	IO	DSPI 0 - CS 1	DSPI 2 - CS 0	LINFlex 1 - TX	Timer 0 - ch. 1
PA[9]	PAD[9]	7	11	IO	DSPI 0 - CS 2	DSPI 0 - CS 7	LINFlex 1 - RX	Timer 0 - ch. 2
PA[10]	PAD[10]	—	12	IO	—	DSPI 1 - CS 1	Nexus MDO 1	Ext. INT 3

Table 4. eTQFP64 and eTQFP100 pinout (continued)

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
PA[11]	PAD[11]	8	13	IO	DSPI 0 - CS 3	DSPI 0 - CS 5	Timer 0 - ch. 3	Ext. INT 4
PA[12]	PAD[12]	9	14	IO	LINFlex 0 - RX	FlexCAN 1 - RX	LINFlex 1 - RX	Timer 0 - ch. 3
PA[13]	PAD[13]	10	15	IO	LINFlex 0 - TX	FlexCAN 1 - TX	LINFlex 1 - TX	Timer 0 - ch. 4
PA[14]	PAD[14]	11	16	IO	Timer 0 - ch. 4	DSPI 1 - CS 1	Ext. INT 3	Timer 0 - ch. 5
PA[15]	PAD[15]	—	17	IO	FlexCAN 1 - RX	Timer 1 - ch. 0	Nexus MDO 2	Timer 1 - ch. 4
PB[0]	PAD[16]	—	18	IO	FlexCAN 1 - TX	Timer 1 - ch. 1	Nexus MDO 3	Timer 1 - ch. 5
—	VDD_LV	12	19	PW	—			
—	VDD_HV_IO	13	20	PWB20	—			
PB[1]	PAD[17]	—	21	IO	Timer 1 - ch. 5	DSPI 0 - CS 6	Nexus MSEO 0	DSPI 1 - CS 0
PB[2]	PAD[18]	—	22	IN/ANA	Timer 0 - ch. 4	ADC ch. 15	Ext. INT 3	FlexCAN 0 - RX
PB[3]	PAD[19]	14	23	IN/ANA	Timer 0 - ch. 0	ADC ch. 9	Timer 1 - ch. 0	DSPI 0 - Serial Data
PB[4]	PAD[20]	15	24	IN/ANA	Timer 0 - ch. 1	ADC ch. 8	Timer 1 - ch. 1	DSPI 1 - Serial Data
PB[5]	PAD[21]	16	25	IN/ANA	Timer 0 - ch. 2	ADC ch. 7	Timer 1 - ch. 2	DSPI 2 - Serial Data
PB[6]	PAD[22]	17	26	IN/ANA	Timer 0 - ch. 3	ADC ch. 6	Timer 1 - ch. 3	—
PB[7]	PAD[23]	18	27	IN/ANA	Ext. INT 0	ADC ch. 5	Timer 0 - ch. 4	Timer 1 - ch. 4
PB[8]	PAD[24]	—	28	IN/ANA	Timer 0 - ch. 5	ADC ch.14	Ext. INT 4	FlexCAN 1 - RX
—	VREFH_ADC	19	29	REF	—			
PB[9]	PAD[25]	—	30	IN/ANA	Timer 2 - ch. 3	ADC ch. 13	Ext. INT 5	LINFlex 0 - RX
PB[10]	PAD[26]	20	31	IN/ANA	Ext. INT 1	ADC ch. 4	Timer 0 - ch. 5	Timer 1 - ch. 5
PB[11]	PAD[27]	21	32	IN/ANA	Ext. INT 2	ADC ch. 3	Timer 1 - ch. 4	Timer 0 - ch. 4

Table 4. eTQFP64 and eTQFP100 pinout (continued)

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
PB[12]	PAD[28]	—	33	IN/ANA	Timer 2 - ch. 4	ADC ch. 12	Timer 1 - ch. 5	LINFlex 1 - RX
PB[13]	PAD[29]	—	34	IN/ANA	Timer 2 - ch. 5	ADC ch. 11	Timer 3 - ch. 0	NMI
PB[14]	PAD[30]	22	35	IN/ANA	Timer 2 - ch. 0	ADC ch. 2	Timer 3 - ch. 1	Timer 2 - ch. 1
PB[15]	PAD[31]	23	36	IN/ANA	Timer 2 - ch. 1	ADC ch. 1	Timer 3 - ch. 2	Timer 2 - ch. 2
PC[0]	PAD[32]	—	37	IN/ANA	Timer 1 - ch. 0	ADC ch. 10	Timer 3 - ch. 3	Ext. INT 0
PC[1]	PAD[33]	24	38	IN/ANA	Timer 2 - ch. 2	ADC ch. 0	Timer 3 - ch. 4	Timer 2 - ch. 4
—	VDD_HV_ADC_TSENS	25	39	PW	—			
PC[2]	PAD[34]	26	40	IO	Timer 0 - ch. 5	DSPI 2 - CS 1	FlexCAN 1 - RX	FlexCAN 0 - RX
PC[3]	PAD[35]	27	41	IO	Timer 1 - ch. 0	DSPI 2 - CS 2	FlexCAN 1 - TX	FlexCAN 0 - TX
PC[4]	PAD[36]	28	42	IO	Timer 1 - ch. 1	DSPI 1 - CS 0	Ext. INT 1	FlexCAN 1 - RX
PC[5]	PAD[37]	—	43	IO	DSPI 1 - CS 0	Timer 1 - ch. 2	Nexus RDY	FlexCAN 1 - TX
PC[6]	PAD[38]	—	44	IO	DSPI 1 - Serial Data	Timer 1 - ch. 3	DSPI 2 - CS 4	DSPI 0 - Serial Data
PC[7]	PAD[39]	29	45	IO	Timer 1 - ch. 2	DSPI 1 - Serial Data	DSPI 2 - CS 5	DSPI 0 - CS 0
PC[8]	PAD[40]	30	46	IO	Timer 1 - ch. 3	DSPI 1 - Serial Data	DSPI 2 - CS 6	DSPI 0 - CS 1
PC[9]	PAD[41]	—	47	IO	DSPI 1 - Serial Data	Timer 1 - ch. 4	DSPI 2 - CS 7	DSPI 0 - Serial Data
PC[10]	PAD[42]	—	48	IO	DSPI 1 - CLK	Timer 1 - ch. 5	—	DSPI 0 - CLK
PC[11]	PAD[43]	31	49	IO	Timer 1 - ch. 4	DSPI 1 - CLK	—	DSPI 0 - CS 2
—	FCCU_F1	32	50	IO	FCCU_F1			
—	VDD_HV_IO	33	51	PWB51	—			
—	VDD_LV	34	52	PW	—			
—	EXTAL	35	53	ANA	—			

Table 4. eTQFP64 and eTQFP100 pinout (continued)

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
—	XTAL	36	54	ANA	—			
—	VDD_HV_OSC_PMC	37	55	PW	—			
PC[12]	PAD[44]	—	56	IO	Timer 0 - ch. 0	DSPI 1 - CS 3	—	LINFlex 0 - RX
PC[13]	PAD[45]	—	57	IO	Timer 0 - ch. 1	DSPI 1 - CS 4	—	LINFlex 0 - TX
PC[14]	PAD[46]	—	58	IO	Timer 0 - ch. 2	DSPI 1 - CS 5	—	DSPI 0 - CS 3
—	TDI	38	59	IO	—			
—	TMS	39	60	IO	—			
—	TDO	40	61	IO	—			
PC[15]	PAD[47]	41	62	IO	NMI	DSPI 1 - CS 2	Ext. INT 4	Timer 2 - ch. 0
—	TCK	42	63	IO	—			
—	TESTMODE	43	64	IO	—			
PD[0]	PAD[48]	—	65	IO	DSPI 1 - CS 6	Ext. INT 0	—	Timer 2 - ch. 1
—	PORST	44	66	IO	—			
PD[1]	PAD[49]	—	67	IO	Timer 0 - ch. 3	DSPI 1 - CS 7	—	DSPI 0 - CS 4
—	VDD_LV	45	68	PW	—			
PD[2]	PAD[50]	—	69	IO	Timer 2 - ch. 0	DSPI 2 - CS 1	DSPI 1 - CS 6	Timer 3 - ch. 0
PD[3]	PAD[51]	—	70	IO	Timer 2 - ch. 1	DSPI 2 - CS 2	DSPI 1 - CS 4	Timer 3 - ch. 1
PD[4]	PAD[52]	—	71	IO	Timer 2 - ch. 2	DSPI 2 - CS 3	DSPI 1 - CS 7	Timer 3 - ch. 2
—	VDD_HV_IO	46	—	PWB51	—			
PD[5]	PAD[53]	—	72	IO	DSPI 2 - CS 0	Timer 2 - ch. 1	DSPI 1 - CS 6	Timer 3 - ch. 3
PD[6]	PAD[54]	—	73	IO	DSPI 2 - Serial Data	Timer 2 - ch. 2	DSPI 1 - CS 5	DSPI 0 - CS 5
PD[7]	PAD[55]	47	74	IO	Timer 3 - ch. 0	CTU trg_inp	DSPI 1 - CS 2	LINFlex 1 - RX
PD[8]	PAD[56]	48	75	IO	Timer 3 - ch. 1	CTU trg_outp	DSPI 1 - CS 6	LINFlex 1 - TX

Table 4. eTQFP64 and eTQFP100 pinout (continued)

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
PD[9]	PAD[57]	49	76	IO	FlexCAN 0 - RX	DSPI 2 - CS 1	FlexCAN 1 - RX	Timer 2 - ch. 2
PD[10]	PAD[58]	50	77	IO	FlexCAN 0 - TX	—	FlexCAN 1 - TX	Timer 2 - ch. 3
PD[11]	PAD[59]	51	78	IO	Timer 3 - ch. 2	DSPI 2 - CLK	DSPI 1 - CS 7	—
PD[12]	PAD[60]	—	79	IO	DSPI 2 - Serial Data	Timer 2 - ch. 3	DSPI 2 - CS 2	—
PD[13]	PAD[61]	—	80	IO	DSPI 2 - CLK	Timer 2 - ch. 4	DSPI 2 - CS 3	—
PD[14]	PAD[62]	52	81	IO	Timer 2 - ch. 3	DSPI 2 - Serial Data	Timer 3 - ch. 3	—
PD[15]	PAD[63]	53	82	IO	Timer 2 - ch. 4	DSPI 2 - Serial Data	Timer 3 - ch. 4	—
PE[0]	PAD[64]	—	83	IO	Timer 3 - ch. 3	Ext. INT 2	—	Timer 2 - ch. 4
PE[1]	PAD[65]	—	84	IO	Timer 3 - ch. 4	—	—	Timer 2 - ch. 5
—	VDD_HV_IO	54	85	PWB85	—			
PE[2]	PAD[66]	55	86	IO	Timer 2 - ch. 5	DSPI 2 - CS 0	DSPI 0 - CS 3	—
PE[3]	PAD[67]	56	87	IO	Nexus MSEO(2)	—	DSPI 0 - CS 4	DSPI 2 - CLK
PE[4]	PAD[68]	—	88	IO	Timer 3 - ch. 5	DSPI 2 - CS 2	Timer 2 - ch. 4	—
PE[5]	PAD[69]	57	89	IO	Nexus MDO 3(2)	—	CLOCKOUT	DSPI 2 - Serial Data
PE[6]	PAD[70]	58	90	IO	Nexus MDO 2(2)	—	DSPI 0 - CS 6	DSPI 2 - Serial Data
PE[7]	PAD[71]	59	91	IO	Nexus MDO 1(2)	—	DSPI 0 - CS 7	Timer 3 - ch. 4
PE[8]	PAD[72]	60	92	IO	Nexus MDO 0(2)	DSPI 0 - CS 0	Ext. INT 3	Timer 3 - ch. 5
PE[9]	PAD[73]	—	93	IO	—	Timer 3 - ch. 2	Ext. INT 4	DSPI 2 - CS 1
PE[10]	PAD[74]	—	94	IO	—	Timer 3 - ch. 3	DSPI 0 - CS 5	DSPI 2 - CS 2
—	VDD_HV_IO	61	95	PW	—			

Table 4. eTQFP64 and eTQFP100 pinout (continued)

Port pin	Pad	Pin No.		Type	Alternate functions			
		eTQFP64	eTQFP100		AF1	AF2	AF3	AF4
PE[11]	PAD[75]	62	96	IO	Nexus MCK0(2)	DSPI 0 - CLK	DSPI 0 - CS 1	DSPI 1 - CS 3
PE[12]	PAD[76]	—	97	IO	—	Timer 3 - ch. 4	DSPI 2 - CS 0	DSPI 1 - CS 2
PE[13]	PAD[77]	—	98	IO	—	Timer 3 - ch. 5	DSPI 2 - CS 1	DSPI 1 - CS 1
PE[14]	PAD[78]	63	99	IO	Nexus EVTO (2)	DSPI 0 - Serial Data	DSPI 0 - CS 2	DSPI 2 - CS 3
PE[15]	PAD[79]	64	100	IO	Nexus EVTI(2)	DSPI 0 - Serial Data	DSPI 1 - CS 3	—

1. Cannot be changed
2. Can be enabled via JTAG during the reset phase

4 Electrical characteristics

4.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid applying any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

4.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 5* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 5. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4.3 Absolute maximum ratings

Table 6. Absolute maximum ratings (1)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
Cycle	T	Lifetime power cycles	—	—	1000k	—
V_{SS}	C	Ground voltage	—	—	—	—
V_{DD_LV}	C	1.2 V core supply voltage	—	-0.3	1.5	V
$V_{DD_HV_IO}$	C	I/O supply voltage(2)	—	-0.3	6.0	V
$V_{DD_HV_OSC_PMC}$	C	Power management unit and OSC power supply	—	-0.3	6.0	V
$V_{DD_HV_ADC_TSENS}$	C	ADC & TSENS power supply	—	-0.3	6.0	V
V_{REFH_ADC}	C	ADC reference supply	—	0	$V_{DD_HV_ADC_TSENS}$	V
V_{IN}	C	I/O input voltage range(3)	—	-0.3	6.0	V
			Relative to V_{SS}	-0.3	—	
			Relative to $V_{DD_HV_IO}$	—	0.3	
I_{INJD}	T	Maximum DC injection current for digital pad during overload condition	Per pin, applies to all digital pins	-3	3	mA
I_{INJA}	T	Maximum DC injection current for analog pad during overload condition	Per pin, applies to all analog pins	-3	3	mA
I_{MAXD}	SR	Maximum output DC current when driven	Medium	-7	8	mA
			Strong	-10	10	
			Very strong	-11	11	
I_{MAXSEG}	SR	Maximum current per power segment(4)	—	-90	90	mA
T_{STG}	SR	Storage temperature range and non-operating times	—	-55	175	°C
STORAGE	SR	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range -40 °C to 85 °C	—	20	years
T_{SDR}	SR	Maximum solder temperature(5) Pb-free package	—	—	260	°C
MSL	SR	Moisture sensitivity level(6)	—	—	3	—
X-rays dose	T	Maximum cumulated dose allowable	Range for x-rays source during inspection: 80÷130 KV; 20÷50 µA	—	1	Grey

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability or cause permanent damage to the device. During overload conditions (V_{IN} > $V_{DD_HV_IO}$ or V_{IN} < V_{SS}), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.
2. Allowed 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J = 150 °C remaining time at or below 5.5 V.
3. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3V can be used for nominal calculations.
4. A $V_{DD_HV_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD_HV_IO}$ supply pins.
5. Solder profile per IPC/JEDEC J-STD-020D
6. Moisture sensitivity per JEDEC test method A112

4.4 Electromagnetic compatibility (EMC)

Table 7 describes the EMC characteristics of the device.

Table 7. Radiated emissions testing specification(1),(2)

Coupling structure	Test setup	Function	Functional configuration	BISS radiated emissions limit
Entire IC	(G) TEM	Reference test	C1-S3	18 dBµV
		Reference test with SSCG	C1-S3	18 dBµV
		Memory copy	C4-S2	18 dBµV
		Memory copy with SSCG	C4-S2	18 dBµV

1. Reference “BISS Generic IC EMC Test Specification”, version 1.2, section 9.3, “Emission test configuration for ICs with CPU”.
2. The EMC parameters are classified as “T”, validated on testbench.

4.5 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device.

Table 8. ESD ratings(1),(2)

Parameter	C	Conditions	Value	Unit
ESD for Human Body Model (HBM)(3)	T	All pins	2000	V
ESD for field induced Charged Device Model (CDM)(4)	T	All pins	500	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature. Maximum DC parametrics variation within 10% of maximum specification”
3. This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing
4. This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level

4.6 Operating conditions

Table 9. Device operating conditions(1)

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Frequency							
f_{SYS}	SR	Device operating frequency(2)	-40 °C < T_J < 150 °C	—	—	80	MHz
Temperature							
T_J	SR P	Operating temperature range - junction	—	-40.0	—	150.0	°C
		Operating temperature range - junction	—	—	—	165.0 (3)	°C
T_A (T_L to T_H)	SR P	Ambient operating temperature range	—	-40.0	—	125.0	°C
Voltage							
$V_{DD_HV_IO}$	SR P	I/O supply voltage	LVD290/HVD400 enabled	2.97	—	3.63	V
	C		LVD290 enabled HVD400 disabled (4),(5)	2.97	—	5.5	
$V_{DD_HV_OSC_PMC}$	SR P	PMC and OSC supply voltage	LVD290/HVD400 enabled	2.97	—	3.63	V
	C		LVD290 enabled HVD400 disabled	2.97	—	5.5	
$V_{DD_HV_ADC_TSENS}$	SR D	SAR ADC supply voltage	LVD400 enabled	4.5	—	5.5	V
	C		LVD400 disabled(4),(6)	3.0	—	3.6	
V_{REFH_ADC}	SR P	SAR ADC reference voltage	—	2.0	—	$V_{DD_HV_ADC_TSENS}$	V
V_{REFH_ADC} - $V_{DD_HV_ADC_TSENS}$	SR D	SAR ADC reference differential voltage	—	—	—	25	mV
V_{RAMP}	SR D	Slew rate on power supply pins	—	—	—	0.5	V/µs
V_{IN}	SR C	I/O input voltage range	—	0	—	5.5	V

Table 9. Device operating conditions(1) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
Injection current								
I_{IC}	SR	T	DC injection current (per pin)(7),(8),(9)	Digital pins and analog pins	-3	—	3	mA
I_{MAXSEG}	SR	D	Maximum current per power segment(10)	—	-80	—	80	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the *SPC570Sx Microcontroller Reference Manual* for more information on the clock limitations for the various IP blocks on the device.
3. Refer to technical note "SPC570S family - High Temperature "D" Grade (DocID031416 - TN1262)" for associated specific limitation.
4. Maximum voltage is not permitted for entire product life. See *Absolute maximum ratings*.
5. Reduced output/input capabilities below 4.2 V. See performance derating values in *I/O pad electrical characteristics*.
6. This LVD/HVD disabled supply voltage condition only applies after LVD/HVD are disabled by the application during the reset sequence, and the LVD/HVD are active until that point.
7. Full device lifetime without performance degradation
8. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See *Table 6: Absolute maximum ratings* for maximum input current for reliability requirements.
9. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current will be injected through the clamp diode to the supply rail. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature. For more information, see the device characterization report.
10. A $V_{DD_HV_IO}$ power segment is defined as one or more GPIO pins located between two $V_{DD_HV_IO}$ supply pins.

4.7 Thermal characteristics

4.7.1 Package thermal characteristics

Table 10. Thermal characteristics for eTQFP64

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction to ambient, natural convection(1)	Four layer board - 2s2p board	32.3	°C/W
$R_{\theta JMA}$	CC	D	Junction to ambient in forced air @ 200 ft/min (1 m/s)(1)	Four layer board - 2s2p board	26.5	°C/W
$R_{\theta JB}$	CC	D	Junction to board(2)	—	12.1	°C/W
$R_{\theta JCtop}$	CC	D	Junction to top case(3)	—	19.0	°C/W
$R_{\theta JCbotttom}$	CC	D	Junction to bottom case thermal resistance(4)	—	1.9	°C/W
Ψ_{JT}	CC	D	Junction to package top, natural convection(5)	—	0.6	°C/W

1. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
2. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

3. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1021.1).
4. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
5. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Table 11. Thermal characteristics for eTQFP100(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-ambient, natural convection(2)	Four layer board—2s2p	30.7	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-moving-air, ambient(2)	At 200 ft./min., four layer board—2s2p	24.3	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(3)	Ring cold plate	11.3	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top(4)	Cold plate	16.0	°C/W
$R_{\theta JCbotttom}$	CC	D	Junction-to-case bottom(5)	Cold plate	1.5	°C/W
Ψ_{JT}	CC	D	Junction-to-package top(6)	Natural convection	0.5	°C/W

1. The values are based on simulation; actual data may vary in the given range. The specified characteristics are subject to change per final device design and characterization. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.7.2 Power considerations

An estimation of the chip junction temperature, T_J can be obtained from the equation:

Equation 1: $T_J = T_A + (R_{\theta JA} * P_D)$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The differences between the values determined for the single-layer (1s) board compared to a four-layer board that has

two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

Equation 2: $T_J = T_B + (R_{qJB} * P_D)$

where:

T_B = board temperature for the package perimeter (°C)

R_{qJB} = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Equation 3: $R_{qJA} = R_{qJC} + R_{qCA}$

where:

R_{qJA} = junction-to-ambient thermal resistance (°C/W)

R_{qJC} = junction-to-case thermal resistance (°C/W)

R_{qCA} = case to ambient thermal resistance (°C/W)

R_{qJC} is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, R_{qCA}. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the

printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (YJT) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

Equation 4: $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

Equation 5: $T_J = T_B + (\Psi_{JPB} \times P_D)$

where:

T_B = thermocouple temperature on bottom of the package (°C)

Ψ_{JPB} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

4.8 Current consumption

The following table describes the consumption figures.

Table 12. Current consumption

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
IDD	P	Operating current all supply rails	F_{max}(1)	—	—	110(1)	mA
	T		T_j = 150 °C(1)	—	—	0.75 * f_{CPU}(2) + 50	mA
Stop	P	Stop mode consumption	Device working on RC clock	—	—	40(3)	mA

1. Values are based on typical application code executing from Flash memory, where the DMA is running in continuous mode, the ADC is in continuous conversion, the timers are running to maximum counter values and communication IPs are in loopback or transmitting mode. IOs are unloaded.
The maximum consumption can reach 110 mA during boot time M/LBIST (before reset).
2. f_{CPU} is measured in MHz
3. ADC and XOSC disabled, Includes regulator consumption for VDD_LV generation. Includes static I/O current with no pins toggling.

4.9 I/O pad electrical characteristics

4.9.1 I/O pad types

Table 13 describes the different pad type configurations.

Table 13. I/O pad specification descriptions

Pad type	Description
Weak configuration	Provides a good compromise between transition time and low electromagnetic emission. Pad impedance is centered around 800 Ω
Medium configuration	Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission. Pad impedance is centered around 200 Ω
Strong configuration	Provides fast transition speed; used for fast interface. Pad impedance is centered around 50 Ω
Very strong configuration	Provides maximum speed and controlled symmetric behavior for rise and fall transition. Used for fast interfaces requiring fine control of rising/falling edge jitter. Pad impedance is centered around 40 Ω
Input only pads	These pads are associated to ADC channels and the external 8-40 MHz crystal oscillator (XOSC) providing low input leakage

4.9.2 I/O input DC characteristics

Table 14 provides input DC electrical characteristics as described in *Figure 4*.

Figure 4. I/O input DC electrical characteristics definition

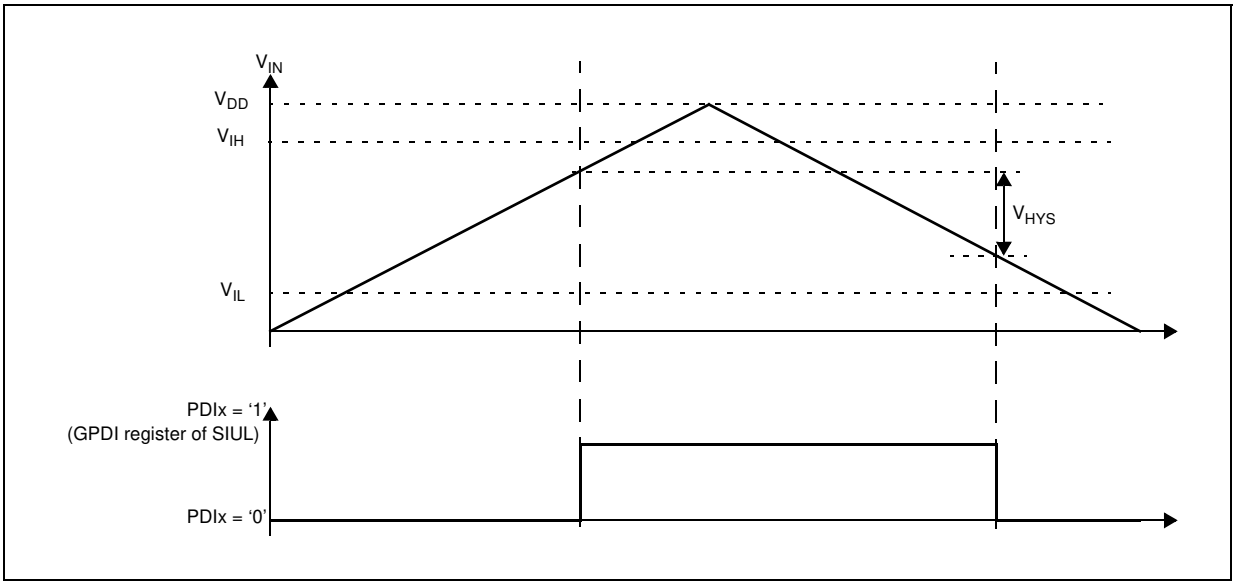


Table 14. I/O input DC electrical characteristics

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
TTL							
V_{IH}	SR	P	Input high level TTL	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	2.0	—	$V_{DD_HV_IO}$ + 0.3	V
V_{IL}	SR	P	Input low level TTL	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	-0.3	—	0.8	
V_{HYST}	—	C	Input hysteresis TTL	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	0.3(1)	—	—	
CMOS							
V_{IHCMOS_H}(2)	SR	P	Input high level CMOS (with hysteresis)	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	0.65 * $V_{DD_HV_IO}$	—	$V_{DD_HV_IO}$ + 0.3	V
V_{IHCMOS}(2)	SR	P	Input high level CMOS (without hysteresis)	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	0.6 * $V_{DD_HV_IO}$	—	$V_{DD_HV_IO}$ + 0.3	V
V_{ILCMOS_H}(2)	SR	P	Input low level CMOS (with hysteresis)	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	-0.3	—	0.35 * $V_{DD_HV_IO}$	V

Table 14. I/O input DC electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ILCMOS}(2)	SR	P	Input low level CMOS (without hysteresis)	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	-0.3	—	0.4 * $V_{DD_HV_IO}$	V
$V_{HYSCMOS}$	—	C	Input hysteresis CMOS	3.0 V < $V_{DD_HV_IO}$ < 3.6 V and 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	0.1 * $V_{DD_HV_IO}$	—	—	V
Automotive								
V_{IH}(3)	SR	P	Input high level Automotive	4.5 V < $V_{DD_HV_IO}$ < 5.5 V	3.8	—	$V_{DD_HV_IO}$ + 0.3	V
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V	0.75 * $V_{DD_HV_IO}$	—	$V_{DD_HV_IO}$ + 0.3	
V_{IL}	SR	P	Input low level Automotive	4.5 V < $V_{DD_HV_IO}$ < 5.5 V	-0.3	—	2.2	V
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V	-0.3	—	0.35 * $V_{DD_HV_IO}$	
V_{HYST}	—	C	Input hysteresis Automotive	4.5 V < $V_{DD_HV_IO}$ < 5.5 V	0.5	—	—	V
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V	0.11 * $V_{DD_HV_IO}$	—	—	
Input Characteristics								
I_{LKG}	CC	P	Digital input leakage	—	—	—	1	µA
C_{IN}	C	D	Digital input capacitance	—	—	—	10	pF

1. Minimum hysteresis at 4.0 V
2. VSIO[VSIO_xx] = 0 in the range 3.0 V < $V_{DD_HV_IO}$ < 4.0 V, VSIO[VSIO_xx] = 1 in the range 4.0 V < $V_{DD_HV_IO}$ < 5.9 V.
3. VSIO[VSIO_xx] = 0 in the range 3.0 V < $V_{DD_HV_IO}$ < 4.0 V, VSIO[VSIO_xx] = 1 in the range 4.0 V < $V_{DD_HV_IO}$ < 5.9 V.

Table 15 provides weak pull figures. Both pull-up and pull-down current specifications are provided.

Table 15. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$\|I_{WPU}\|$	CC	P	Weak pull-up/down current absolute value(1)	V_{IN} = 0.69 * $V_{DD_HV_IO}$ 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	23	—	—	µA
				V_{IN} = 0.49 * $V_{DD_HV_IO}$ 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	—	—	82	
				V_{IN} > V_{IL} = 1.1 V (TTL) 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	—	—	130	
	CC	T		V_{IN} = 0.75 * $V_{DD_HV_IO}$ 3.0 V < $V_{DD_HV_IO}$ < 3.6 V	10	—	—	
				V_{IN} = 0.35 * $V_{DD_HV_IO}$ 3.0 V < $V_{DD_HV_IO}$ < 3.6 V	—	—	70	
				V_{IN} > V_{IL} = 1.1 V (TTL) 3.0 V < $V_{DD_HV_IO}$ < 3.6 V	—	—	75	
$\|I_{WPD}\|$	CC	P	Weak pull-down current absolute value	V_{IN} = 0.69 * $V_{DD_HV_IO}$ 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	—	—	130	µA
				V_{IN} = 0.49 * $V_{DD_HV_IO}$ 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	40	—	—	
				V_{IN} > V_{IL} = 1.1 V (TTL) 4.5 V < $V_{DD_HV_IO}$ < 5.5 V	16	—	—	
	CC	T		V_{IN} = 0.75 * $V_{DD_HV_IO}$ 3.0 V < $V_{DD_HV_IO}$ < 3.6 V	—	—	92	
				V_{IN} = 0.35 * $V_{DD_HV_IO}$ 3.0 V < $V_{DD_HV_IO}$ < 3.6 V	19	—	—	
				V_{IN} > V_{IL} = 1.1 V (TTL) 3.0 V < $V_{DD_HV_IO}$ < 3.6 V	16	—	—	

1. Weak pull-up/down is enabled within t_{WK_PU} = 1 µs after internal/external reset has been asserted. Output voltage will depend on the amount of capacitance connected to the pin.

4.9.3 I/O output DC characteristics

Table 16: Weak configuration I/O output characteristics, provide DC characteristics for bidirectional pads in the following configurations:

- Weak
- Medium
- Strong
- Very Strong

Table 16. Weak configuration I/O output characteristics(1),(2)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
R_{OH_W}	CC	P	PMOS output impedance weak configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OH}< 0.5 mA	—	—	1040	Ω
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OH} < 0.5 mA	—	—	1040	
R_{OL_W}	CC	P	NMOS output impedance weak configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OL} < 0.5 mA	—	—	1040	Ω
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OL} < 0.5 mA	—	—	1040	
f_{max_W}	CC	T	Output frequency weak configuration	C_L = 25 pF	—	—	2	MHz
				C_L = 50 pF	—	—	1	
t_{TR_W}	CC	D	Transition time output pin weak configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V C_L = 25 pF	—	—	150	ns
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V C_L = 50 pF	—	—	300	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V C_L = 25 pF	—	—	100	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V C_L = 50 pF	—	—	200	
t_{SKEW_W}	CC	T	Difference between rise time and fall time	3.0 V < $V_{DD_HV_IO}$ < 3.6 V	—	—	40	%
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V	—	—	28	

1. The above mentioned values are different for M/W (Medium/Weak) pads.
2. Please refer to *Table 20: I/O output characteristics for pads 4, 9, 11, 55, 56*

Table 17. Medium configuration I/O output characteristics(1),(2)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
R_{OH_M}	CC	P	PMOS output impedance medium configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OH}< 2 mA	—	—	270	Ω
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OH} < 2 mA	—	—	270	
R_{OL_M}	CC	P	NMOS output impedance medium configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OL} < 2 mA	—	—	270	Ω
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OL} < 2 mA	—	—	270	
f_{max_M}	CC	T	Output frequency medium configuration	C_L = 25 pF	—	—	12	MHz
				C_L = 50 pF	—	—	6	

Table 17. Medium configuration I/O output characteristics(1),(2) (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
t_{TR_M}	CC	D	Transition time output pin medium configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V C_L = 25 pF	—	—	37	ns
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V C_L = 50 pF	—	—	72	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V C_L = 25 pF	—	—	25	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V C_L = 50 pF	—	—	50	
t_{SKEW_M}	CC	T	Difference between rise time and fall time	3.0 V < $V_{DD_HV_IO}$ < 3.6 V	—	—	40	%
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V	—	—	28	

1. The above mentioned values are different for M/W (Medium/Weak) pads.
2. Please refer to *Table 20: I/O output characteristics for pads 4, 9, 11, 55, 56*

Table 18. Strong configuration I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
R_{OH_S}	CC	P	PMOS output impedance strong configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OH}< 6 mA	—	—	90	Ω
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OH} < 8 mA	—	—	75	
R_{OL_S}	CC	P	NMOS output impedance strong configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OL}< 6 mA	—	—	90	Ω
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OL} < 8 mA	—	—	75	
f_{max_S}	CC	T	Output frequency strong configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V C_L = 25 pF	—	—	25	MHz
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V C_L = 50 pF	—	—	12.5	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V C_L = 25 pF	—	—	50	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V C_L = 50 pF	—	—	25	

Table 18. Strong configuration I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
t_{TR_S}	CC	D	Transition time output pin strong configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V C_L = 25 pF	—	—	11	ns
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V C_L = 50 pF	—	—	22	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V C_L = 25 pF	—	—	8	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V C_L = 50 pF	—	—	13	
t_{SKEW_S}	CC	T	Difference between rise time and fall time	3.0 V < $V_{DD_HV_IO}$ < 3.6 V	—	—	40	%
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V	—	—	28	

Table 19. Very Strong configuration I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
R_{OH_V}	CC	P	PMOS output impedance very strong configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OH} < 7 mA	—	—	85	Ω
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OH} < 8 mA	—	—	65	
R_{OL_V}	CC	P	NMOS output impedance very strong configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OL} < 7 mA	—	—	85	Ω
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V Push pull, I_{OL} < 8 mA	—	—	65	
f_{max_V}	CC	T	Output frequency very strong configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V C_L = 15 pF	—	—	50	MHz
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V C_L = 25 pF	—	—	30	
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V T_d = 0.6 ns, load = 10 pF	—	—	25	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V C_L = 25 pF	—	—	50	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V C_L = 50 pF	—	—	25	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V T_d = 1 ns, load = 10 pF	—	—	25	

Table 19. Very Strong configuration I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
t_{TR_V}	CC	D	Transition time output pin very strong configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V C_L = 15 pF	—	—	4.5	ns
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V C_L = 25 pF	—	—	5	
				3.0 V < $V_{DD_HV_IO}$ < 3.6 V T_d = 0.6 ns, load = 10 pF	—	—	(4.5 * T_r) + T_f < 9	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V C_L = 25 pF	—	—	4	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V C_L = 50 pF	—	—	8	
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V T_d = 1 ns, load = 10 pF	—	—	(4.5 * T_r) + T_f < 9	
$t_{PHL-PLH_V}$	CC	T	Difference between delay of rising and falling edges	3.0 V < $V_{DD_HV_IO}$ < 3.6 V C_L = 15 pF	0	—	1.2	ns
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V C_L = 25 pF	0	—	1.2	

For W/M (Weak/Medium) pads the following values hold true.

Table 20. I/O output characteristics for pads 4, 9, 11, 55, 56

Functionality	Symbol	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Weak	R_{OH_S}	PMOS output impedance weak configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OH} < 0.5 mA	—	—	1600	Ω
	R_{OL_S}	NMOS output impedance weak configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OL} < 0.5 mA	—	—	1896	Ω
	f_{max_S}	Output frequency weak configuration	C_L = 25 pF	—	—	2	MHz
			C_L = 50 pF	—	—	1	
	t_{TR_S}	Transition time output pin weak configuration	C_L = 25 pF	—	—	127	ns
			C_L = 50 pF	—	—	2443	
	t_{SKEW_S}	Difference between rise time and fall time	—	—	—	50	%

Table 20. I/O output characteristics for pads 4, 9, 11, 55, 56 (continued)

Functionality	Symbol	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
Medium	R_{OH_M}	PMOS output impedance medium configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OH} < 0.5 mA	—	—	405	Ω
	R_{OL_M}	NMOS output impedance medium configuration	3.0 V < $V_{DD_HV_IO}$ < 3.6 V Push pull, I_{OL} < 0.5 mA	—	—	495	Ω
	f_{max_M}	Output frequency medium configuration	C_L = 25 pF	—	—	12	MHz
			C_L = 50 pF	—	—	6	
	t_{TR_M}	Transition time output pin medium configuration	C_L = 25 pF	—	—	34	ns
			C_L = 50 pF	—	—	62	
	t_{SKEW_M}	Difference between rise time and fall time	—	—	—	46	%

4.10 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional reset pin ($\overline{\text{PORST}}$).

Note: $\overline{PORST}$ pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 Kohm.

Figure 5. Start-up reset requirements

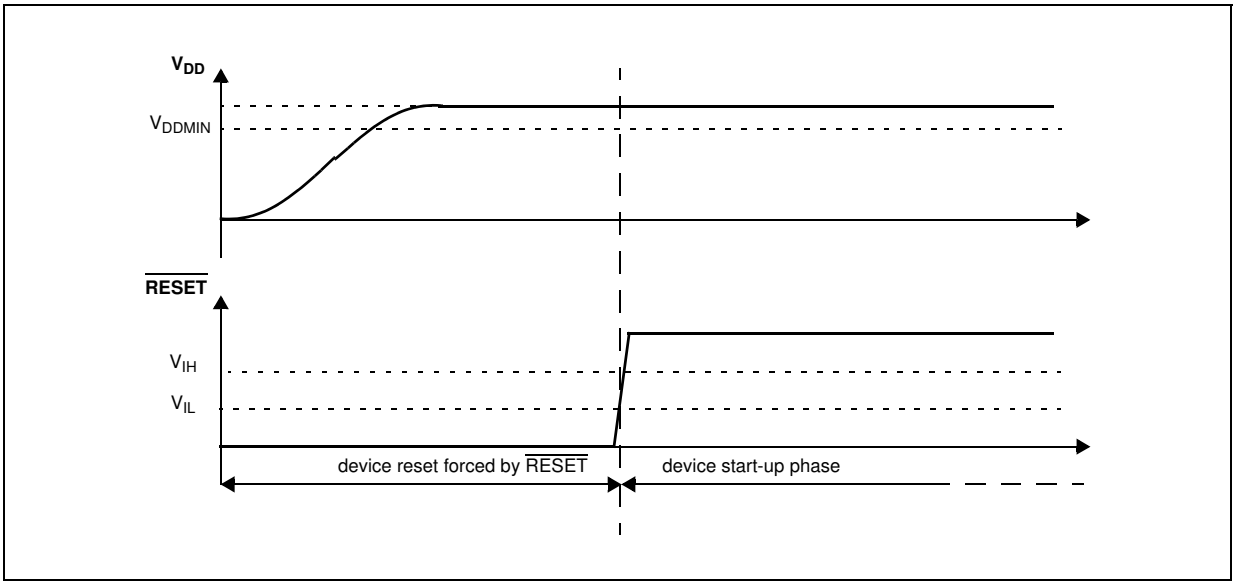


Figure 6 describes device behavior depending on supply signal on $\overline{\text{PORST}}$:

1. $\overline{\text{PORST}}$ does not go low enough: it is filtered by input buffer hysteresis. The device remains in the current state.
2. $\overline{\text{PORST}}$ goes low enough, but not for long enough: it is filtered by a low pass filter. The device remains in the current state.
3. The $\overline{\text{PORST}}$ generates a reset:
   a) $\overline{\text{PORST}}$ low but initially filtered during at least W_{FRST}. Device remains initially in current state.
   b) $\overline{\text{PORST}}$ potentially filtered until W_{NFRST}. Device state is unknown. It may either be reset or remains in current state depending on extra conditions (PVT — process, voltage, temperature).
   c) $\overline{\text{PORST}}$ asserted for longer than W_{NFRST}. The device is under hardware reset.

Figure 6. Noise filtering on reset signal

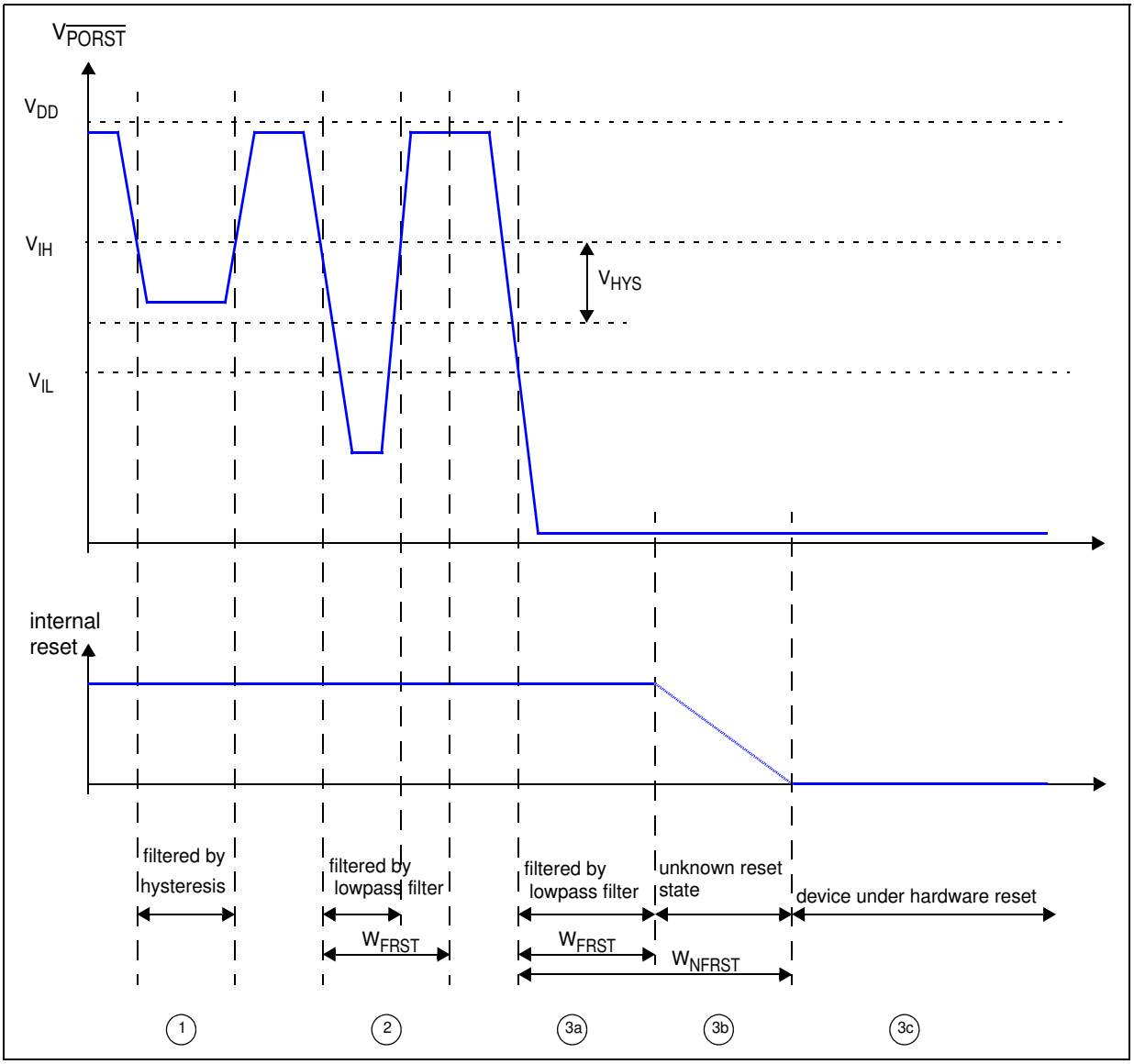


Table 21. Reset electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level TTL (Schmitt trigger)	—	2.0	—	$V_{DD_HV_IO}$ + 0.4	V
V_{IL}	SR	P	Input low level TTL (Schmitt trigger)	3.0 V < $V_{DD_HV_IO}$ < 3.6 V	0.4	—	0.6	V
				4.5 V < $V_{DD_HV_IO}$ < 5.5 V	0.4	—	0.8	
V_{HYS}	CC	C	Input hysteresis TTL (Schmitt trigger)	—	275	—	—	mV
V_{DD_POR}	CC	C	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	CC	P	Strong pull-down current	Device under power-on reset 3.0 V < $V_{DD_HV_IO}$ < 5.5 V, V_{OL} > 1.0 V	0.2	—	—	mA
				Device under power-on reset $V_{DD_HV_IO}$ = 4.0 V, V_{OL} = V_{IL}	12	—	—	mA
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	$\overline{ESR0}$ pin V_{IN} = 0.69 * $V_{DD_HV_IO}$	23	—	—	µA
				$\overline{ESR0}$ pin V_{IN} = 0.49 * $V_{DD_HV_IO}$	—	—	82	
$\lvert I_{WPD} \rvert$	CC	P	Weak pull-down current absolute value	$\overline{PORST}$ pin V_{IN} = 0.69 * $V_{DD_HV_IO}$	—	—	130	µA
				$\overline{PORST}$ pin V_{IN} = 0.49 * $V_{DD_HV_IO}$	40	—	—	
W_{FRST}	SR	P	$\overline{PORST}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	SR	P	$\overline{PORST}$ input not filtered pulse	—	2000	—	—	ns

4.11 Power management electrical characteristics

4.11.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply $V_{DD_HV_IO}$. The regulator itself is supplied by $V_{DD_HV_OSC_PMC}$.

Note: $V_{DD_HV_OSC_PMC}$ is to be shorted with $V_{DD_HV_IO}$ supply at package level.

The following supplies are involved:

- HV—High voltage external for voltage regulator module. This must be provided externally through $V_{DD_HV_OSC_PMC}$ power pin.
- BV—High voltage external power supply for internal ballast module. This must be provided externally through $V_{DD_HV_IO}$ power pins. Voltage values should be aligned with $V_{DD_HV_OSC_PMC}$.
- LV—Low voltage internal power supply for core, PLL and Flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is split into three further domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR—Low voltage supply for the core. It is also used to provide supply for PLL1 through double bonding.
  - LV_FLA—Low voltage supply for code Flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL—Low voltage supply for PLL1. It is shorted to LV_COR through double bonding.

Figure 7. Recommended parasitics on board

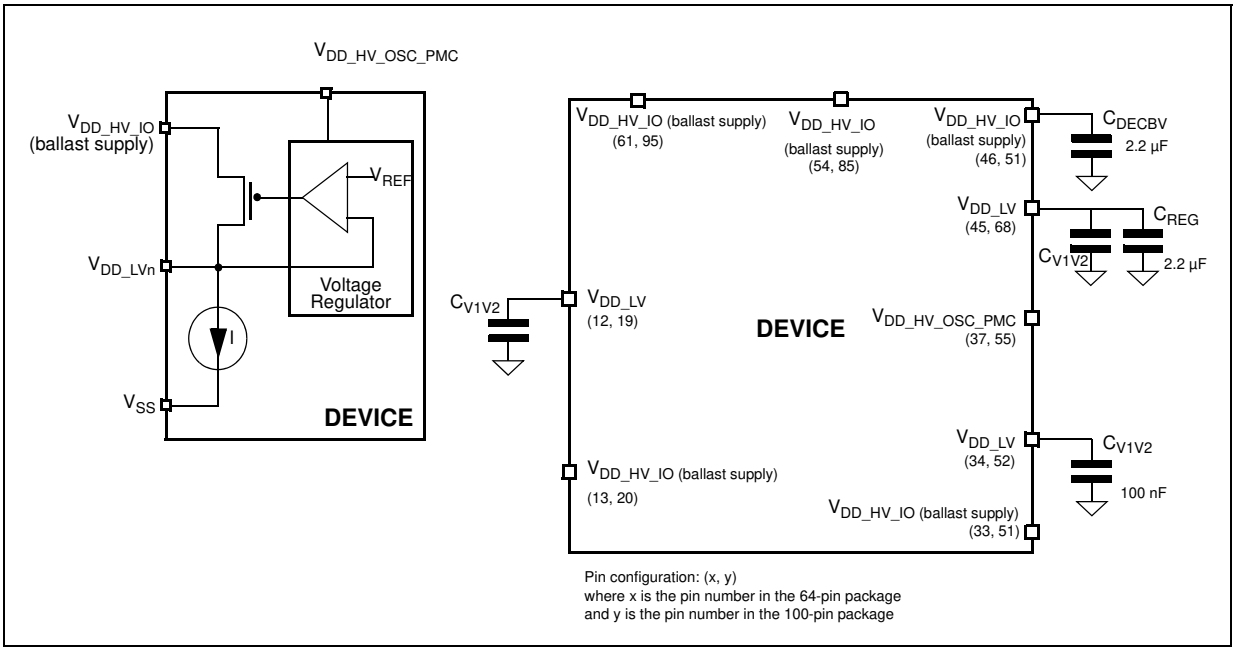


Table 22. Voltage regulator electrical characteristics

Symbol		Parameter	Conditions[1]	Value[2]			Unit
				Min	Typ	Max	
C_{REG}	SR	Main internal voltage regulator stability external capacitance	—	1.1	2.2[3]	2.97	µF
$R_{DECREGn}$	SR	Stability capacitor equivalent serial resistance	Total resistance including board track	1	—	50	mΩ
C_{V1V2}	SR	EMC cap to be placed on every 1.2V pin	V_{DD_LV}/V_{SS} pair	50	100	135	nF
C_{DECBV}	SR	Decoupling capacitance ballast	$V_{DD_HV_IO}/V_{SS_LV}$	1.1	2.2[4]	3	µF

1. V_{DD} = 5.0 V ± 10%, T_A = -40 / 125 °C, unless otherwise specified.
2. All values need to be confirmed during device validation.
3. Recommended X7R or X5R ceramic -43% / +35% variation, 20% tolerance and 12.5% temperature.
4. Recommended X7R or X5R ceramic -43% / +35% variation, 20% tolerance and 12.5% temperature.

Note: All 1.2 V pins should be shorted externally on board with minimum resistance and minimum inductance. It is recommended to use a 1.2 V plane on which all 1.2 V pins are shorted to keep resistance and inductance negligible. Recommended capacitors should be placed very close to the device pins such that parasitic resistance can be reduced. Connection from V_{DD_LV} pin to capacitor top plate should not exceed more than 5 mΩ in resistance and 0.5 nH in inductance. Similarly connection from bottom plate of capacitor to PCB ground should not have more than 5mohm resistance and 0.5 nH inductance.

4.12 PMU monitor specifications

4.12.1 Nomenclature

- **POR** stands for Power On Reset. The POR circuit manages the reset from very low voltage up to its threshold. Cannot be disabled.
- **MVD** stands for Minimum Voltage Detector. It cannot be disabled by the user and generate a destructive Reset.
- **LVD** stands for Low Voltage Detector. It can be disabled by the user.
- **HVD** stands for High Voltage Detector. It can be disabled by the user.
- **UVD** stands for Upper Voltage Detector. It cannot be disabled by the user and generate a destructive reset.

Table 23. Trimmed (PVT) values

Domain monitor	Voltage	Name	Segment	Lower limit	Upper limit
1.2 V	Power On Reset	POR041	Core	0.39 V	0.95 V
	Low	MVD098	Core	1.005 V	1.055 V
			Flash	1.005 V	1.055 V
		LVD108	Core	1.085 V	1.137 V
	High	HVD140	Core	1.340 V	1.400 V
		UVD145	Core	1.379 V	1.441 V
			Flash	1.379 V	1.441 V
3.3 V	Power On Reset	POR200	Core	1.750 V	2.400 V
	Low	MVD270	Core	2.694 V	2.826 V
			Flash	2.694 V	2.826 V
		LVD290	Core	2.881 V	2.999 V
			Flash	2.881 V	2.999 V
			ADC	2.881 V	2.999 V
	High	HVD400	Core	3.660 V	3.840 V
5 V	Low	LVD400	ADC	4.128 V	4.332 V
	High	UVD600	Core	5.684 V	5.920 V

4.12.2 Power up/down sequencing

For proper device functioning please adhere to following power sequence:

$V_{DD_HV_OSC_PMC}$ supply should always be greater than or equal to $V_{DD_HV_IO}$ supply (even during ramping up).

$V_{DD_HV_ADC_TSENS}$ supply should always be greater than or equal to V_{REFH_ADC} supply.

4.13 Platform Flash controller electrical characteristics

Table 24. RWSC settings(1)

Max Flash operating Frequency (MHz)(2)	RWSC
20	0b000
40	0b001
64	0b010
80	0b011

1. RWSC is a field in the Flash memory of PFCR register used to specify the wait states for address pipelining and read/write accesses.
2. Maximum frequencies (FM modulation up to 2% could be enabled additionally).

4.14 Flash memory electrical characteristics

Table 25 shows the program and erase characteristics.

Table 25. Flash memory program and erase specifications

Symbol	Characteristics[1]	Value								Unit
		Typ (2)	C	Initial max			Typical end of life[3]	Lifetime max[4]		C	
				25 °C (5)	All temp (6)	C		≤ 1 K cycles	≤ 100 K cycles		
$t_{dwprogram}$	Double Word (64 bits) program time [Packaged part]	38	C	150	—	—	94	500		C	µs
$t_{pprogram}$	Page (256 bits) program time	78	C	300	—	—	214	1000		C	µs
$t_{pprogrameep}$	Page (256 bits) program time EEPROM (partition 1) [Packaged part]	90	C	330	—	—	250	1000		C	µs
$t_{qprogram}$	Quad Page (1024 bits) program time	274	C	1000	1500	P	802	2000		C	µs
$t_{qprogrameep}$	Quad Page (1024 bits) program time EEPROM (partition 1) [Packaged part]	315	C	1100	1650	P	925	2000		C	µs
$t_{16kpperase}$	16 KB block pre-program and erase time	350	C	1000	1500	P	424	5000	—	C	ms
$t_{32kpperase}$	32 KB block pre-program and erase time	500	C	1000	1500	P	605	5000	—	C	ms
$t_{64kpperase}$	64 KB block pre-program and erase time	800	C	1000	1500	P	968	5000	—	C	ms
$t_{128kpperase}$	128 KB block pre-program and erase time	1000	C	2000	3000	P	1254	15000	—	C	ms
$t_{16kprogram}$	16 KB block program time	42	C	54	80	P	51	1000	—	C	ms
$t_{32kprogram}$	32 KB block program time	85	C	108	160	P	103	2000	—	C	ms
$t_{64kprogram}$	64 KB block program time	169	C	216	320	P	204	4000	—	C	ms
$t_{128kprogram}$	128 KB block program time	339	C	432	640	P	410	17000	—	C	ms
$t_{8kprogrameep}$	Program 8 KB EEPROM (partition 1)	21	C	27	40	P	44	1000		C	ms
$t_{8keraseeep}$	Erase 8KB EEPROM (partition 1)	300	C	1000	1500	P	660	5000		C	ms
t_{tr}	Program rate[7]	2.34	C	3.04	4.56	C	2.60	—		C	s/MB
t_{pr}	Erase rate[7]	7.2	C	14.4	28.8	C	7.92	—		C	s/MB
$t_{ffprogram}$	Full Flash programming time[8]	4	C	16	24	P	5	26	—	C	s
$t_{fferase}$	Full Flash erasing time[8]	12	C	24	30	P	15	40	—	C	s
t_{ESRT}	Erase suspend request rate[9]	500	T	—	—	—	—	—		—	µs

Table 25. Flash memory program and erase specifications (continued)

Symbol	Characteristics[1]	Value									Unit
		Typ [2]	C	Initial max			Typical end of life[3]	Lifetime max[4]		C	
				25 °C [5]	All temp [6]	C		≤ 1 K cycles	≤ 100 K cycles		
t_{PSRT}	Program suspend request rate[9]	30	T	—	—	—	—	—		—	µs
t_{PSUS}	Program suspend latency[10]	—	—	—	—	—	—	15		T	µs
t_{ESUS}	Erase suspend latency[10]	—	—	—	—	—	—	30		T	µs
t_{AIC0S}	Array Integrity Check Partition 0 (0.5 MB, sequential)[11]	7.5	T	—	—	—	—	—	—	—	ms
$t_{AIC128K}$	Array Integrity Check (128 KB, sequential)[11]	1.9	T	—	—	—	—	—	—	—	ms
t_{AIC0P}	Array Integrity Check (0.5 MB, proprietary)[11]	0.75	T	—	—	—	—	—	—	—	s
t_{MR0S}	Margin Read (0.5 MB, sequential)	25	T	—	—	—	—	—	—	—	ms
$t_{MR128KS}$	Margin Read (128 KB, sequential)	6.26	T	—	—	—	—	—	—	—	ms
t_{AABT}	Array Integrity Check Abort Latency	—	—	—	—	—	—	10		—	µs
t_{MABT}	Margin Read Abort Latency	—	—	—	—	—	—	10		—	µs

1. Actual hardware programming times; this does not include software overhead.
2. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
3. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.
4. Lifetime maximum program & erase times apply across the voltages and temperatures and occur after the specified number of program/erase cycles. These maximum values are characterized but not tested or guaranteed.
5. Initial factory condition: < 100 program/erase cycles, 20 °C < T_J < 30 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
6. Initial maximum “All temp” program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, -40 °C < T_J < 150 °C junction temperature, and nominal (± 2%) supply voltages. These values are verified at production testing.
7. Rate computed based on 128K sectors.
8. Only code sectors, not including EEPROM.
9. Time between erase suspend resume and next erase suspend.
10. Timings guaranteed by design.
11. AIC is done using system clock, thus all timing is dependant on system frequency and number of wait states. Timing in the table is calculated at 80 MHz.

All the Flash operations require the presence of the system clock for internal synchronization. About 50 synchronization cycles are needed: this means that the timings of the previous table can be longer if a low frequency system clock is used.

Table 26. Flash memory Life Specification

Symbol	Characteristics[1]	Value				Unit
		Min	C	Typ	C	
N_{CER16K}	16 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER32K}	32 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER64K}	64 KB CODE Flash endurance	10	—	100	—	Kcycles
$N_{CER128K}$	128 KB CODE Flash endurance	1	—	100	—	Kcycles
N_{DER8K}	8 KB EEPROM Flash endurance	100	—		—	Kcycles
t_{DR1k}	Minimum data retention Blocks with 0 - 1,000 P/E cycles	25	—		—	Years
t_{DR10k}	Minimum data retention Blocks with 1,001 - 10,000 P/E cycles	15	—		—	Years
t_{DR100k}	Minimum data retention Blocks with 10,001 - 100,000 P/E cycles	15	—		—	Years

1. Program and erase cycles supported across specified temperature specs.

4.15 PLL0/PLL1 electrical characteristics

The device provides a phase-locked loop (PLL0) as well as a frequency-modulated phase-locked loop (PLL1) module to generate a fast system clock from the main oscillator driver.

Table 27. PLL1 electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	PLL1 reference clock[2]	—	37.5	—	78.125	MHz
Δ_{PLLIN}	SR	—	PLL1 reference clock duty cycle[2]	—	35	—	65	%
f_{PLLOUT}	CC	D	PLL1 output clock frequency	—	4.762	—	625	MHz
f_{VCO}[3]	CC	P	VCO frequency	—	600	—	1250	MHz
t_{LOCK}	CC	P	PLL1 lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	—	110	µs
Δt_{STJIT}	CC	T	PLL1 short term jitter	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} @ 64 MHz	—	—	1.8	ns
I_{PLL}	CC	C	PLL1 consumption	T_A = 25 °C	—	—	6	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.
3. Frequency modulation is considered ±2%.

Table 28. PLL0 electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	PLL0 reference clock[2]	—	8	—	56	MHz
Δ_{PLLIN}	SR	—	PLL0 reference clock duty cycle[2]	—	30	—	70	%
f_{PLLOUT}	CC	D	PLL0 output clock frequency	—	4.762	—	625	MHz
f_{VCO}	CC	P	VCO frequency	—	600	—	1250	MHz
t_{LOCK}	CC	P	PLL0 lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	—	110	µs
Δt_{STJIT}	CC	T	PLL0 short term jitter	f_{sys} maximum	—	—	300	ps
Δt_{LTJIT}	CC	T	PLL0 long term jitter	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} @ 64 MHz	-1	—	1	ns
I_{PLL}	CC	C	PLL0 consumption	T_A = 25 °C	—	—	5.5	mA

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, TA = -40 to 125 °C, unless otherwise specified.
2. PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

4.16 External oscillator (XOSC) electrical characteristics

Table 29. External Oscillator electrical specifications[1]

Symbol		C	Parameter	Conditions		Value		Unit
						Min	Max	
f_{XTAL}	CC	D	Crystal Frequency Range[2]	—		4	8	MHz
				—		>8	20	
				—		>20	40	
t_{cst}	CC	T	[Covers: ADD12.017]Crystal start-up time [3],[4]	T_J = 150 °C		—	5	ms
trec	CC	—	Crystal recovery time[5]	—		—	0.5	ms
V_{IHEXT}	CC	D	EXTAL input high voltage (External Reference)	V_{REF} = 0.28 * $V_{DD_HV_IO}$		V_{REF} + 0.6	—	V
V_{ILEXT}	CC	D	EXTAL input low voltage[6],[7]	V_{REF} = 0.28 * $V_{DD_HV_IO}$		—	V_{REF} - 0.6	V
C_{S_EXTAL}	CC	T	Total on-chip stray capacitance on EXTAL pin[8]	QFP		6.0	8.0	pF
C_{S_XTAL}	CC	T	Total on-chip stray capacitance on XTAL pin[8]	QFP		6.0	8.0	pF
g_m	CC	P	Oscillator Transconductance (5 V)	T_J = -40 °C to 150 °C	$f_{XTAL} \leq 8$ MHz	2.6	11.0	mA/V
		C			$f_{XTAL} \leq 20$ MHz	7.9	26.0	
		C			$f_{XTAL} \leq 40$ MHz	10.4	34.0	

Table 29. External Oscillator electrical specifications(1) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{EXTAL}	CC	D	Oscillation Amplitude on the EXTAL pin after startup(9)	T_J = –40 °C to 150 °C	0.5	1.6	V
V_{HYS}	CC	D	Comparator Hysteresis	T_J = 150 °C	0.1	1.0	V
I_{XTAL}	CC	D	XTAL current(10)	T_J = 150 °C	—	14	mA

1. All oscillator specifications are valid for $V_{DD_HV_IO}$ = 3.0 V – 5.5 V.
2. The range is selectable by UTEST miscellaneous DCF clients XOSC_LF_EN and XOSC_EN_40 MHZ.
3. This value is determined by the crystal manufacturer and board design.
4. Proper PC board layout procedures must be followed to achieve specifications.
5. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
6. This parameter is guaranteed by design rather than 100% tested.
7. Applies to an external clock input and not to crystal mode.
8. See crystal manufacturer's specification for recommended load capacitor (C_L) values.The external oscillator requires external load capacitors when operating from 8 MHz to 16 MHz. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating at 20 MHz/40 MHz, the integrated load capacitor value is selected via S/W to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.
9. Amplitude on the EXTAL pin after startup is determined by the ALC block, i.e., the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid over-driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
10. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator. The current after oscillation is typically in the 2-3 mA range and is dependent on the load and series resistance of the crystal. Test circuit is shown in *Figure 9*. The ALC block is the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid overdriving the crystal.

Figure 8. Crystal/Resonator Connections

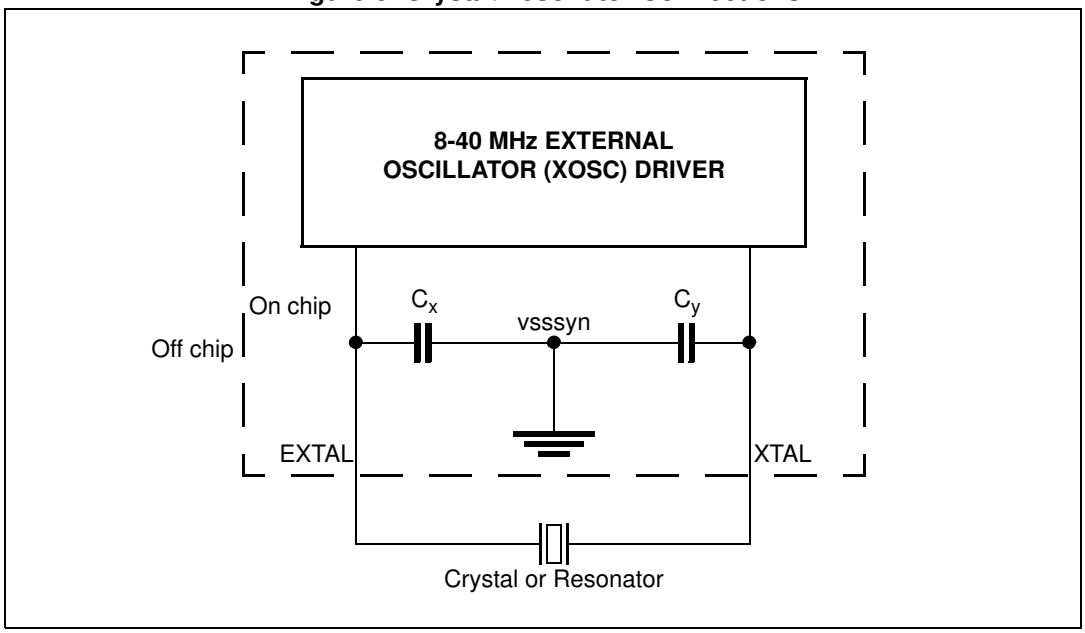
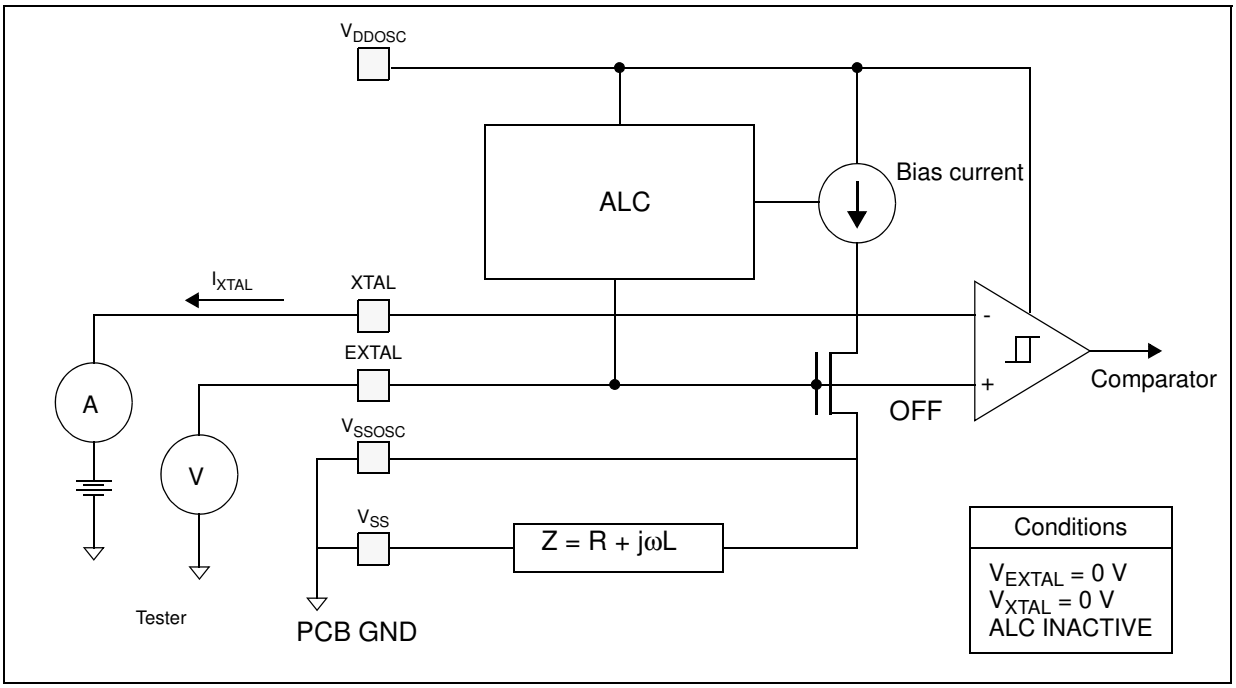


Table 30. Selectable load capacitance

load_cap_sel[4:0] from DCF record	Capacitance offered on EXTAL/XTAL (Cx and Cy)(1) (pF)
00000	1.032
00001	1.976
00010	2.898
00011	3.823
00100	4.751
00101	5.679
00110	6.605
00111	7.536
01000	8.460
01001	9.390
01010	10.317
01011	11.245
01100	12.173
01101	13.101
01110	14.029
01111	14.957

1. Values are determined from simulation with a tolerance of ±15%.

Figure 9. Test circuit



4.17 Internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 31. Internal RC oscillator electrical specifications

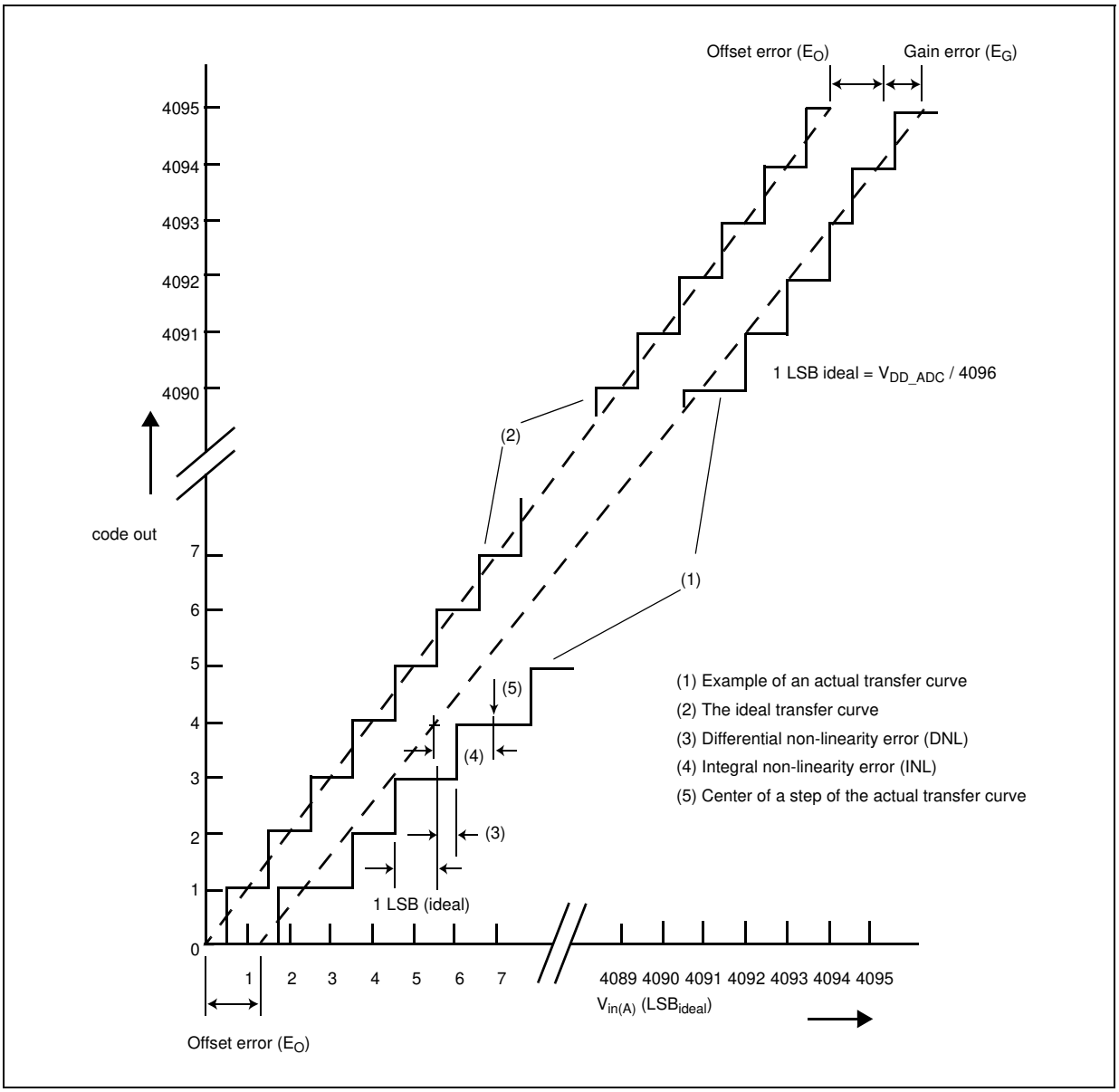
Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{Target}	CC	D	IRC target frequency	—	—	16	—	MHz
δf_{var_noT}	CC	P	IRC frequency variation across temperature and voltage	—	-6	—	+6	%
δf_{var_SW}	—	T	IRC software trimming accuracy	Trimming temperature	-0.5	—	+0.5	%
t_{start_noT}	CC	T	Startup time to reach within f_{var_noT}	Factory trimming already applied	—	—	5	µs

4.18 ADC electrical characteristics

4.18.1 Introduction

The device provides a 12-bit Successive Approximation Register (SAR) analog-to-digital converter.

Figure 10. ADC characteristic and error definitions



4.18.2 ADC electrical characteristics

Figure 11 shows the input equivalent circuit for 12-bit SAR channel.

Figure 11. Input equivalent circuit (12- bit SAR)

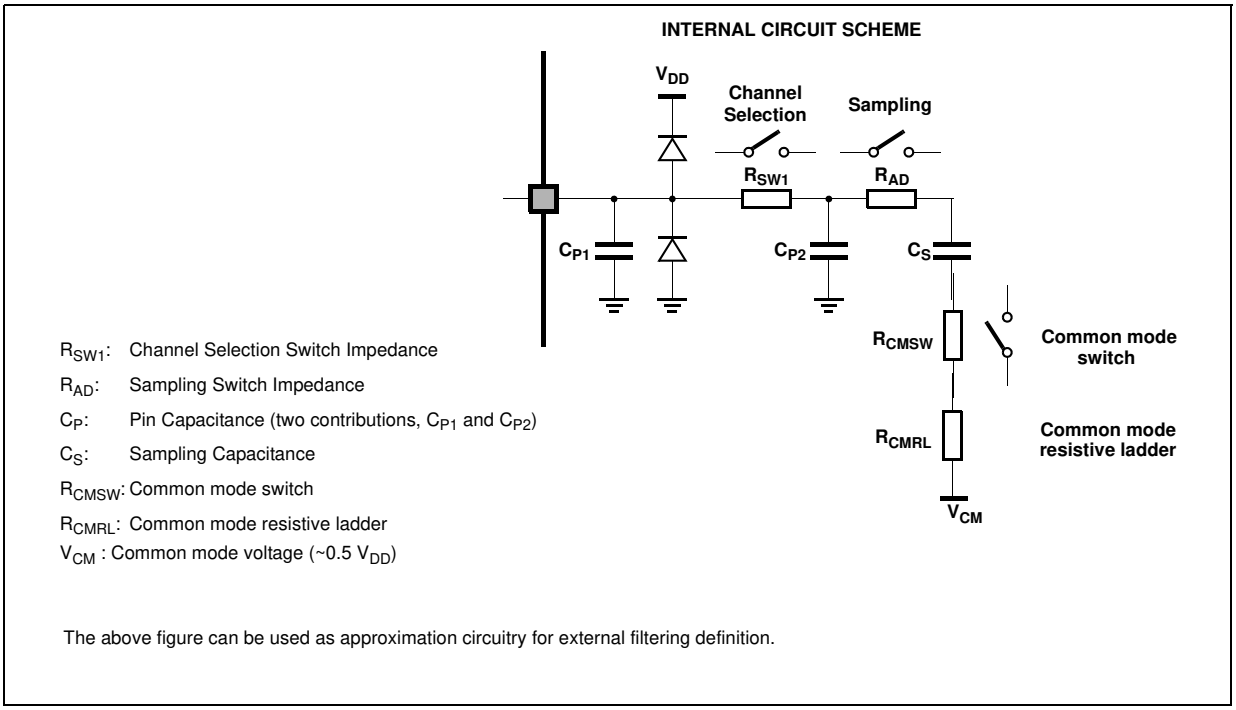


Table 32. ADC input leakage current

Symbol		Parameter	Conditions		Value		Unit
					Min	Max	
I_{LKG}	CC	Input leakage current, two ADC channels input with weak pull-up and weak pull-down	T_j < 40 °C	No current injection on adjacent pin	—	70	nA
			T_j < 150 °C		—	220	

Table 33. ADC pin specification(1),(2)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
I_{LKG}	CC	—	Input leakage current, two ADC channels on input-only pin.	See *Table 14: I/O input DC electrical characteristics*, parameter I_{LKG}	—		
$I_{INJ1,2}$	T	—	Maximum DC injection current for analog pad during overload condition.	Per pin, applies to all analog pins.	-3	3	mA
C_{P1}	C	D	Digital input capacitance	—	—	10	pF
C_{P2}	CC	D	Internal routing capacitance	SAR12-bit channels	—	1	pF

Table 33. ADC pin specification(1),(2) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
C_S	CC	D	SAR ADC sampling capacitance	SARn 12bit	—	5	pF
R_{SWn}	CC	D	Analog switches resistance	SAR 12-bit channels	—	1.8	kΩ
R_{AD}	CC	D	ADC input analog switches resistance	SAR 12-bit	—	0.8	kΩ
R_{CMSW}	CC	D	Common mode switch resistance	sum of the two resistances	—	9	kΩ
R_{CMRL}	CC	D	Common mode resistive ladder				kΩ
A_{BGAP}	CC	D	ADC digital bandgap accuracy		-1.5	+1.5	%

1. Specifications in this table apply to both packaged parts and Known Good Die (KGD) parts, except where noted.
2. All specifications in this table valid for the full input voltage range for the analog inputs.

Table 34. ADC conversion characteristics

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{IN}	SR		ADC input signal	$0 < V_{IN} < V_{DD_HV_IO}$	$V_{SS_HV_ADR}$(1)	V_{REFH_ADC}	V
f_{ADCK}	SR	P	Clock frequency	—	7.5	12	MHz
$t_{ADCPRECH}$	SR	T	ADC precharge time	—	83	—	ns
V_{PRECH}	SR	D	Precharge voltage	—	—	0.25	V
ΔV_{INTREF}	CC	P	Internal reference voltage precision	Applies to all internal reference points ($V_{SS_HV_ADR}$, 1/3 * V_{REFH_ADC}, 2/3 * V_{REFH_ADC}, V_{REFH_ADC})	–0.20	0.20	V
$t_{ADCSAMPLE}$	SR	P	ADC sample time	SAR – 12-bit configuration	0.5	—	µs
$t_{ADCEVAL}$	SR	P	ADC evaluation time	12-bit configuration (12 clock cycles)	1.000	—	µs
		D		10-bit configuration (10 clock cycles)	0.833		
$I_{ADCREFH}$(2)	CC	C	ADC high reference current (average across all codes)	Run mode	—	15	µA
				Power Down mode	—	1	
I_{ADCVDD}	CC	P	$V_{DD_HV_ADC_TSENS}$ power supply current	Run mode	—	4.0	mA
				Power Down mode	—	0.04	
TUE_{12}	CC	T	Total unadjusted error in 12-bit configuration	$V_{REFH_ADC} > 3$ V	-6	6	LSB (12b)
				3 V > V_{REFH_ADC} > 2 V	-9	9	

Table 34. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
ΔTUE_{12}	CC	D	TUE degradation due to V_{REFH_ADC} offset with respect to $V_{DD_HV_ADC_TSENS}$	$V_{IN} < V_{DD_HV_ADC_TSENS}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [0:25 mV]	—	±1	LSB (12b)
		D		$V_{IN} < V_{DD_HV_ADC_TSENS}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [25:50 mV]	—	±2.0	
		D		$V_{IN} < V_{DD_HV_ADC_TSENS}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [50:75 mV]	—	±3.5	
		D		$V_{IN} < V_{DD_HV_ADC_TSENS}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [75:100 mV]	—	±6.0	
		D		$V_{DD_HV_ADC_TSENS} < V_{IN} < V_{REFH_ADC}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [0:25 mV]	—	±2.5	
		D		$V_{DD_HV_ADC_TSENS} < V_{IN} < V_{REFH_ADC}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [25:50 mV]	—	±4.0	
		D		$V_{DD_HV_ADC_TSENS} < V_{IN} < V_{REFH_ADC}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [50:75 mV]	—	±7.0	
		D		$V_{DD_HV_ADC_TSENS} < V_{IN} < V_{REFH_ADC}$ $V_{REFH_ADC} - V_{DD_HV_ADC_TSENS} \in$ [75:100 mV]	—	±12.0	
DNL	CC	P	Differential non-linearity	$V_{DD_HV_ADC_TSENS} > 3.0$ V	-1	2	LSB (12b)

1. $V_{SS_HV_ADR}$ is connected to exposed pad for the device.
2. The consumption values are given after power-up when steady state is reached. Extra consumption of up to 2 mA can be required during internal circuitry setup.

4.19 Temperature sensor

The following table describes the temperature sensor electrical characteristics.

Table 35. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
—	CC	C	Temperature monitoring range	—	-40	—	165	°C
T_{SENS}	CC	P	Sensitivity	—	—	5.18	—	mV/°C
T_{ACC}	CC	C	Accuracy	T_J < 150 °C	-3	—	3	°C
I_{TEMP_SENS}	CC	C	VDD_HV_ADC_TSENS power supply current	—	—	—	700	µA

4.20 JTAG interface timings

Table 36. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at V_{DDC}/2)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40% - 70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	5	—	ns
6	t_{DOV}	D	TCK low to TDO data valid	—	—	30	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	30	ns
9	t_{BSDV}	D	TCK falling edge to output valid	—	—	50	ns
10	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
11	t_{BSDHZ}	D	TCK falling edge to output high impedance	—	—	50	ns
12	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
13	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 12. JTAG test clock input timing

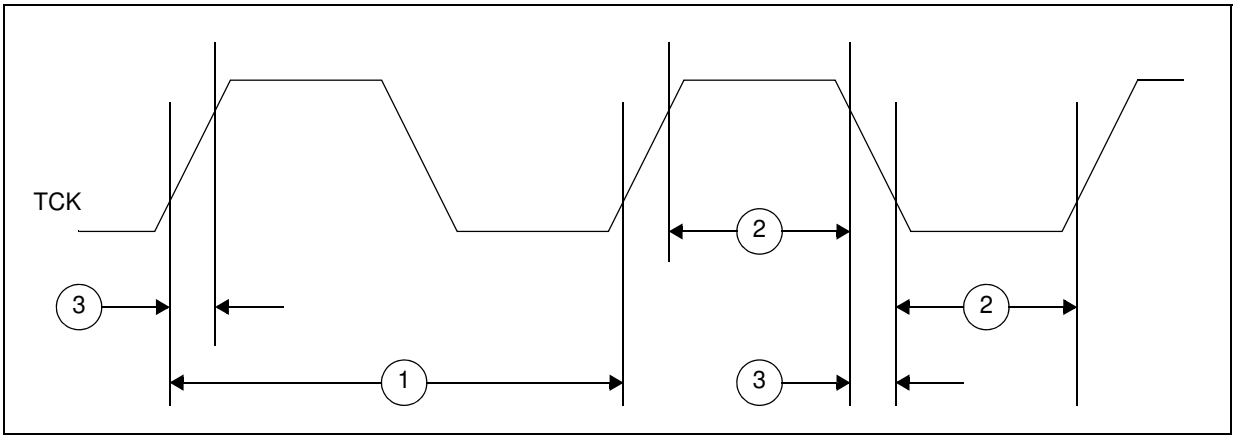


Figure 13. JTAG test access port timing

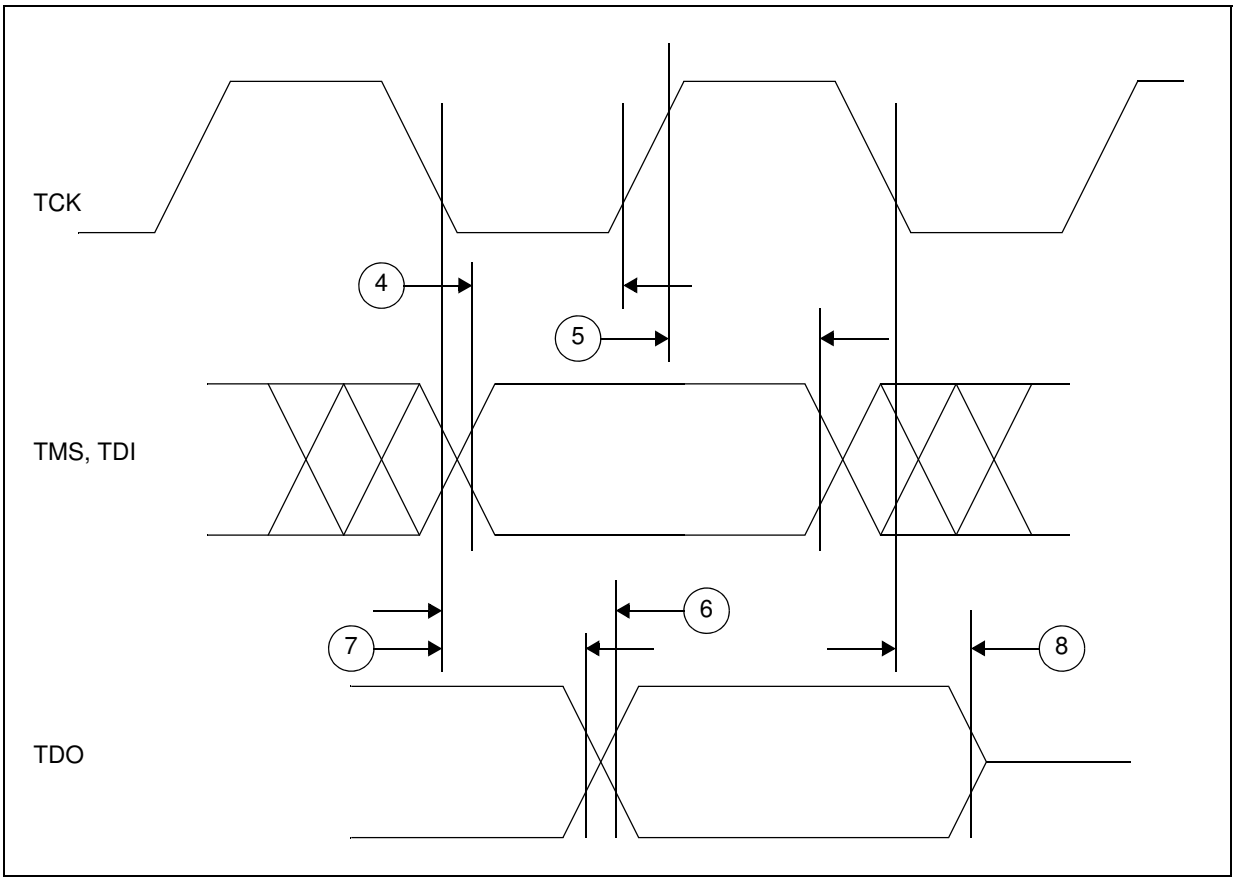
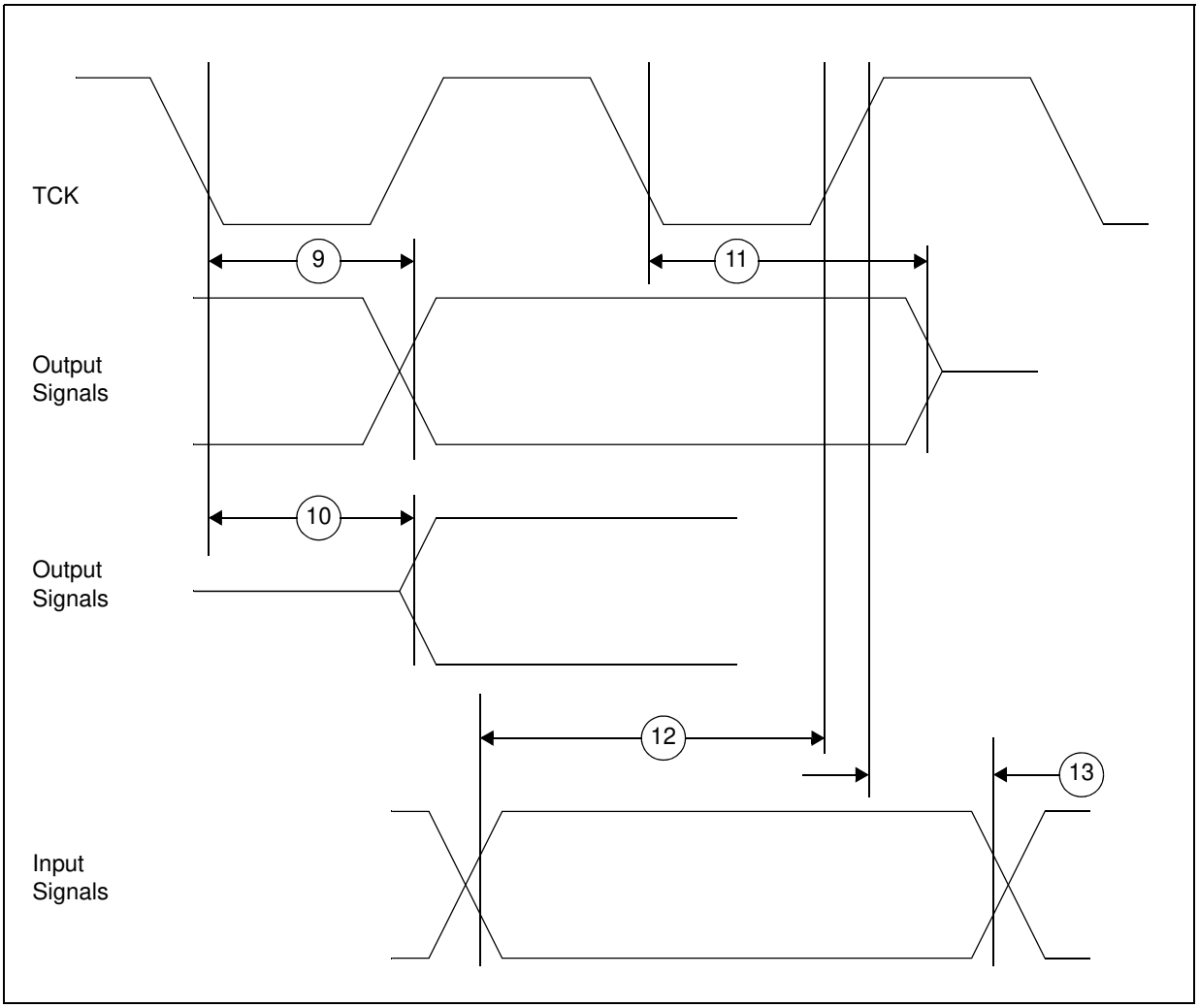


Figure 14. JTAG boundary scan timing



4.21 DSPI CMOS master mode timing

4.21.1 Classic timing

Table 37. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0[1]

#	Symbol		C	Characteristic	Condition		Value[2]		Unit
					Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	75	—	ns
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	50	—	ns

Table 37. DSPI CMOS master classic timing (full duplex and output only) – MTFE = 0(1)

#	Symbol		C	Characteristic	Condition		Value(2)		Unit
					Pad drive(3)	Load (C_L)	Min	Max	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	53	—	ns
4	t_{SDC}	CC	D	SCK duty cycle(4)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	ns
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time(5)	PCS and PCSS drive strength				
					Very strong	25 pF	25	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time(5)	PCS and PCSS drive strength				
					Very strong	25 pF	25	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK(6)	SCK drive strength				
					Very strong	25 pF	32	—	ns
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK(6)	SCK drive strength				
					Very strong	0 pF	0	—	ns
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK(7)	SOUT and SCK drive strength				
					Very strong	25 pF	—	5	ns
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK(7)	SOUT and SCK drive strength				
					Very strong	25 pF	2	—	ns

1. Protocol clock is 40 MHz and all pads are configured as very strong.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
5. PCSx and PCSS using same pad configuration.
6. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL / Automotive voltage thresholds.
7. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 15. DSPI CMOS master mode – classic timing, CPHA = 0

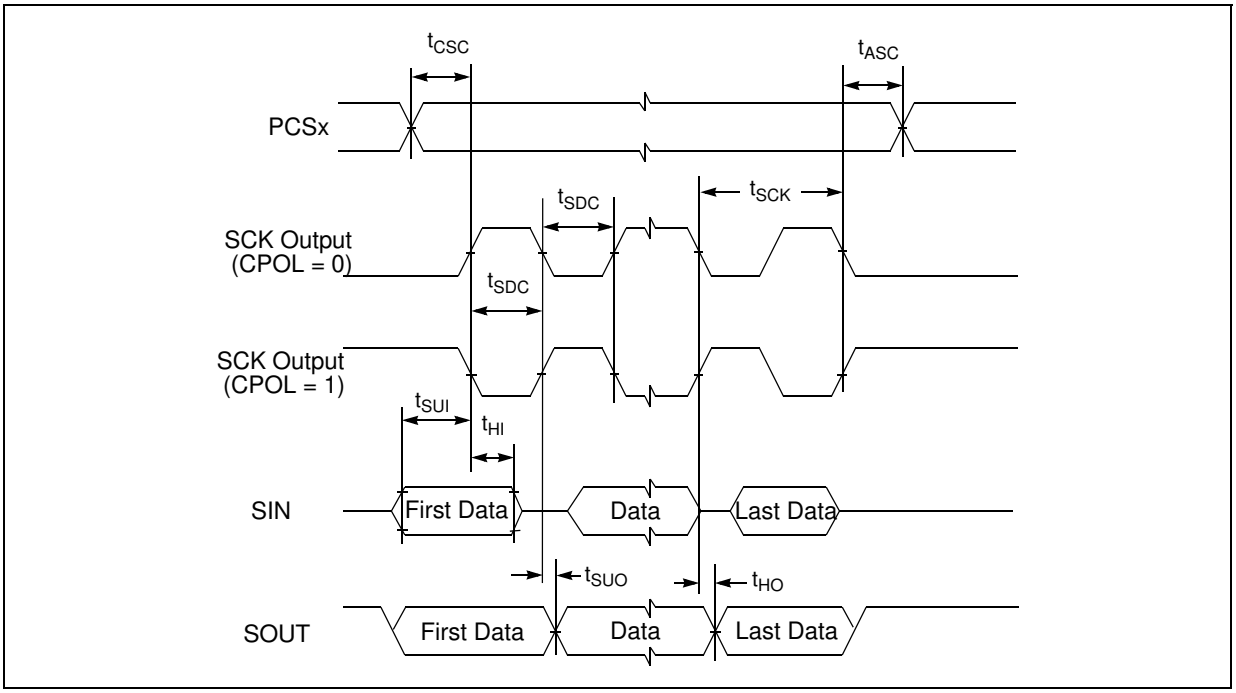


Figure 16. DSPI CMOS master mode – classic timing, CPHA = 1

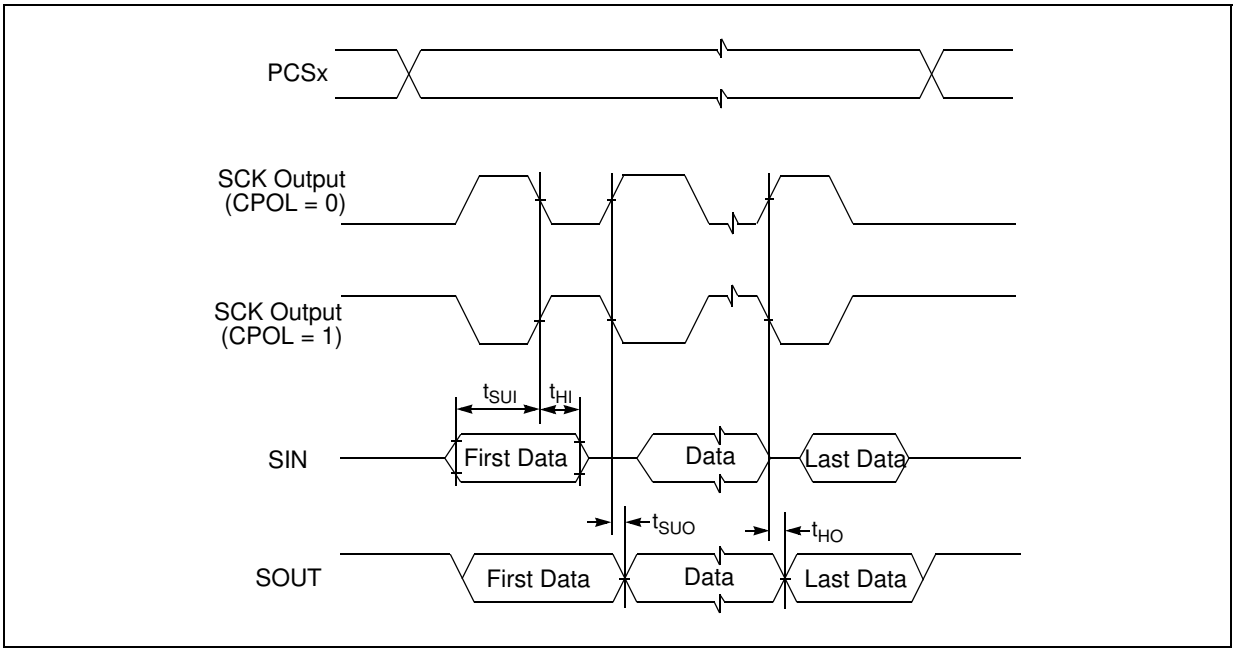
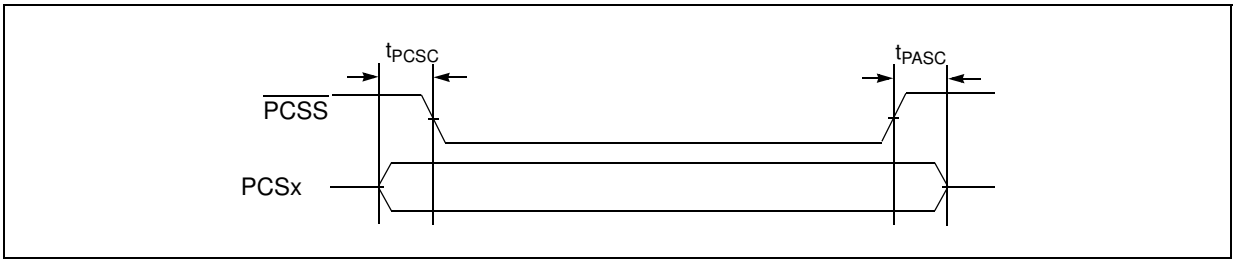


Figure 17. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



4.21.2 Modified timing

Table 38. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1(1)

#	Symbol		C	Characteristic	Condition		Value(2)		Unit
					Pad drive(3)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	50	—	ns
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	50	—	ns
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	53	—	ns
4	t_{SDC}	CC	D	SCK duty cycle(4)	SCK drive strength				
					Very strong	0 pF	$^1/_2t_{SCK}$ - 2	$^1/_2t_{SCK}$ + 2	ns
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time(5)	PCS and PCSS drive strength				
					Very strong	25 pF	25	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time(5)	PCS and PCSS drive strength				
					Very strong	25 pF	25	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK	SCK drive strength				
					Very strong	25 pF	20	—	ns
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK	SCK drive strength				
					Very strong	0 pF	0	—	ns
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK	SOUT and SCK drive strength				
					Very strong	25 pF	—	6	ns

Table 38. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1[1] (continued)

#	Symbol	C	Characteristic	Condition		Value[2]		Unit
				Pad drive[3]	Load (C_L)	Min	Max	
SOUT data hold time (after SCK edge)								
10	t_{HO}	CC	D	SOUT data hold time after SCK	SOUT and SCK drive strength			
					Very strong	25 pF	2	—	ns

1. Protocol clock is 40 MHz and all pads are configured as very strong.
2. All timing values for output signals in this table are measured to 50% of the output voltage.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
4. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
5. PCSx and PCSS using same pad configuration.

Figure 18. DSPI CMOS master mode – modified timing, CPHA = 0

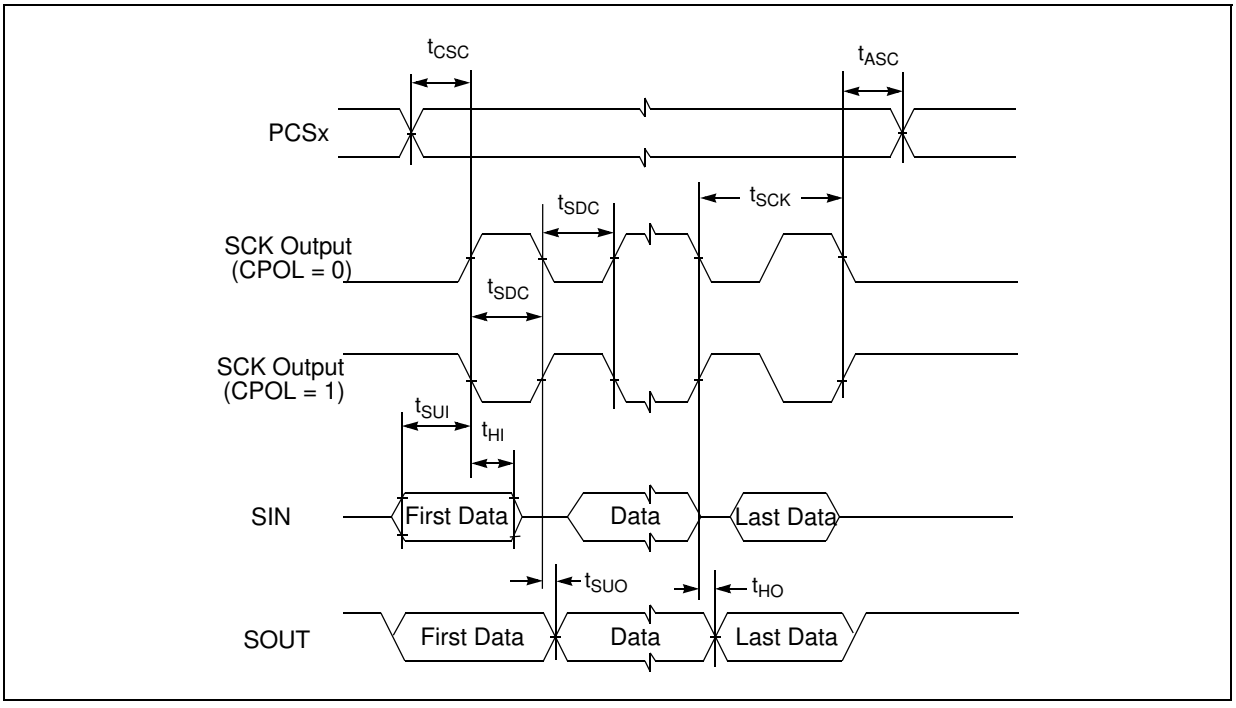


Figure 19. DSPI CMOS master mode – modified timing, CPHA = 1

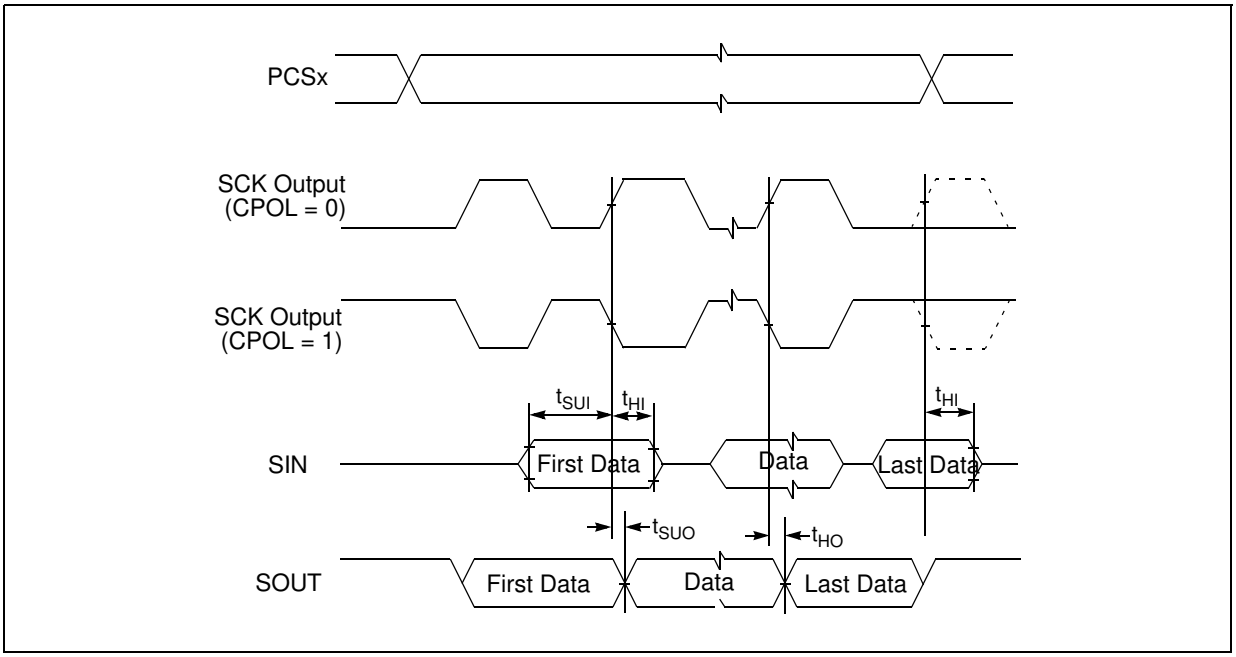
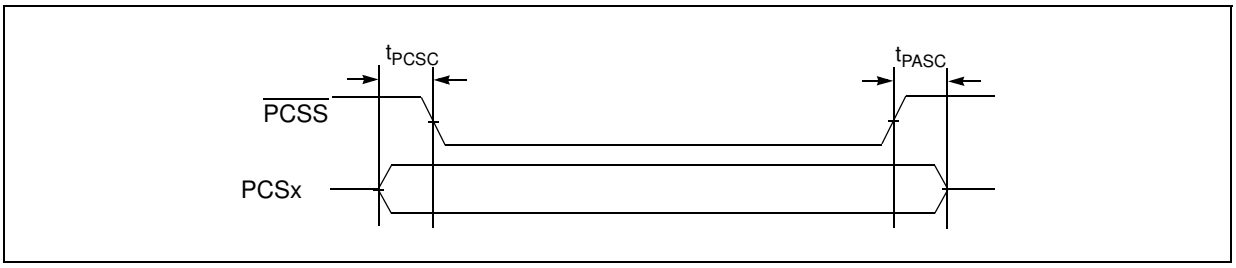


Figure 20. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

5.1 eTQFP64 package information

Figure 21. eTQFP64 package outline

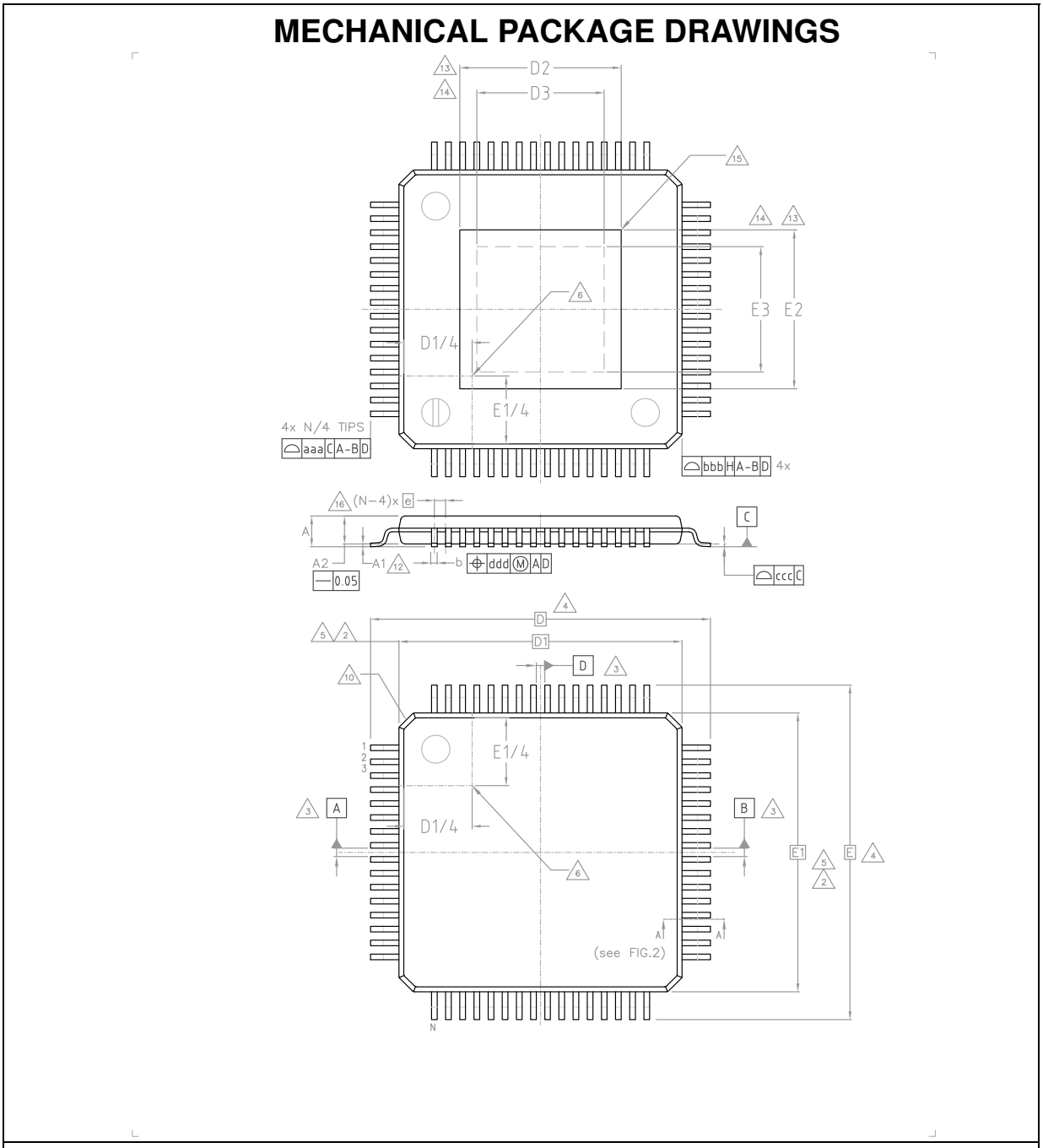


Table 39. eTQFP64 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A[2]	—	—	1.2	—	—	0.047
A1[3]	0.05	—	0.15	0.002	—	0.006
A2[2]	0.95	1.00	1.05	0.037	0.039	0.041
b[4], [5]	0.17	0.22	0.27	0.007	0.009	0.0106
b1[5]	0.17	0.2	0.23	0.007	0.0079	0.0091
c[5]	0.9	—	0.2	0.0354	—	0.0079
c1[5]	0.9	—	0.16	0.0354	—	0.0062
D[6]	12			0.4724		
D1[7], [8]	10			0.3937[2], [5]		
D2[9]	—	—	4.98	—	—	0.1961
D3[10]	3.29	—	—	0.1295	—	—
e	0.5			0.0197		
E[6]	12			0.4724		
E1[7], [8]	10			0.3937		
E2[9]	—	—	4.98	—	—	0.1961
E3[10]	3.29	—	—	0.1295	—	—
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1	1			0.0394		
N	64			2.5197		
R1	0.08	—	—	0.0031	—	—
R2	0.08	—	0.2	0.0031	—	0.0079
S	0.2	—	—	0.0079	—	—

1. Values in inches are converted from mm and rounded to 3 decimal digits.
2. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
3. A1 is defined as the distance from the seating plane to the lowest point on the package body.
4. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. To be determined at setting datum plane C.
7. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
8. The Top package body size may be smaller than the bottom package size by much as 0.15 mm.
9. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located. It includes all metal protrusions from exposed pad itself.

10. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.

Note: TQFP stands for Thin Quad Flat Package.

5.2 eTQFP100 package information

Figure 22. eTQFP100 package outline

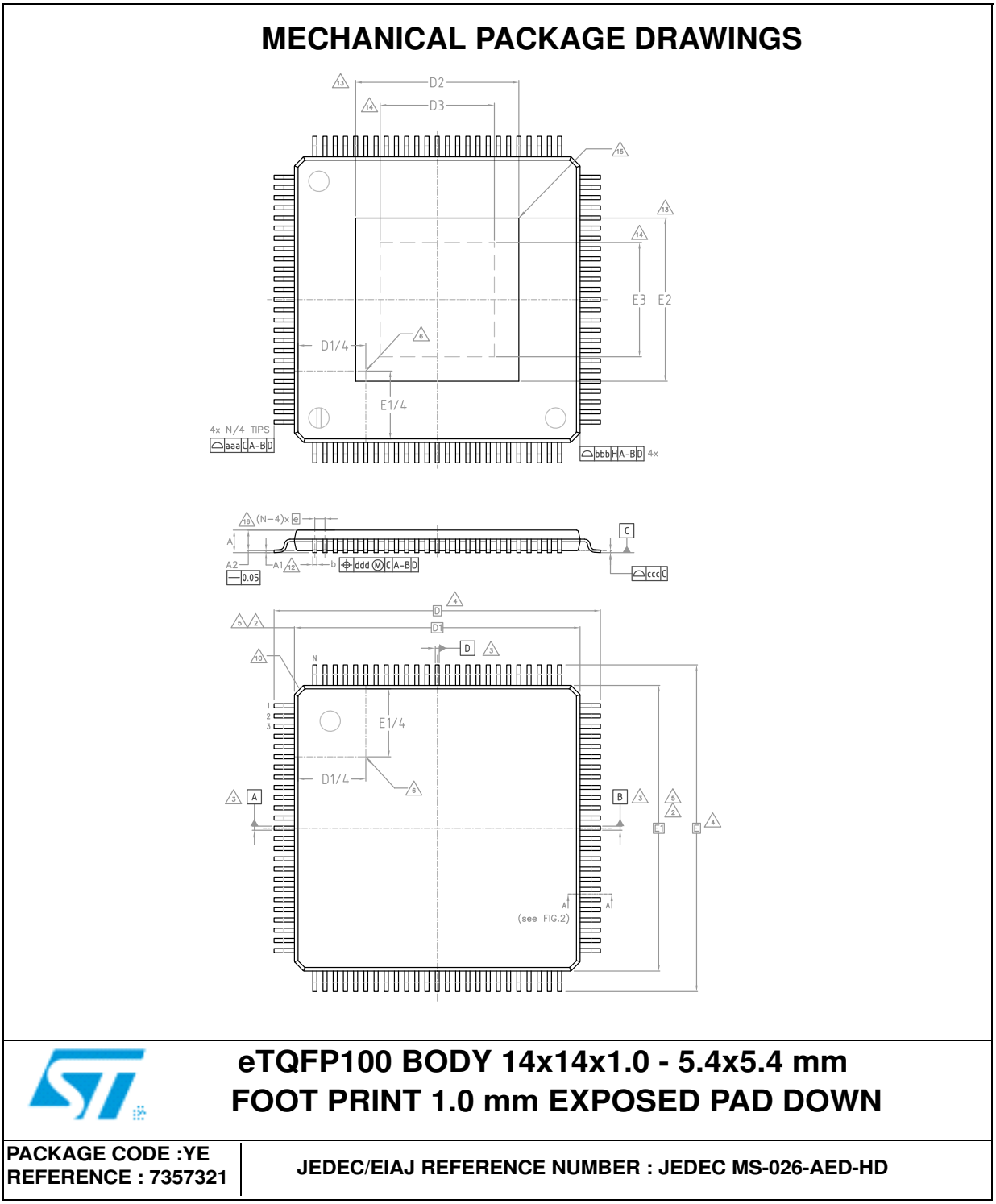


Table 40. eTQFP100 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A[2]	—	—	1.2	—	—	0.0472
A1[3]	0.05	—	0.15	0.019	—	0.0059
A2[2]	0.95	1.00	1.05	0.0374	0.0394	0.0413
b[4], [5]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[5]	0.17	0.2	0.23	0.0067	0.0079	0.0091
c[5]	0.09	—	0.2	0.0035	—	0.0079
c1[5]	0.09	—	0.16	0.0035	—	0.0063
D[6]	16			0.6299		
D1[7], [8]	14			0.5512		
D2[9]	—	—	5.67	—	—	0.2232
D3[10]	4.0	—	—	0.1575	—	—
E[6]	16			0.6299		
E1[7], [8]	14			0.5512		
E2[9]	—	—	5.67	—	—	0.2232
E3[10]	4.0	—	—	0.1575	—	—
e	0.5			0.0197		
L[11]	0.45	0.6	0.75	0.0178	0.0236	0.0295
L1	1			0.0394		
aaa[12], [13]	0.2			0.0079		
bbb[12], [13]	0.2			0.0079		
ccc[12], [13]	0.08			0.0031		

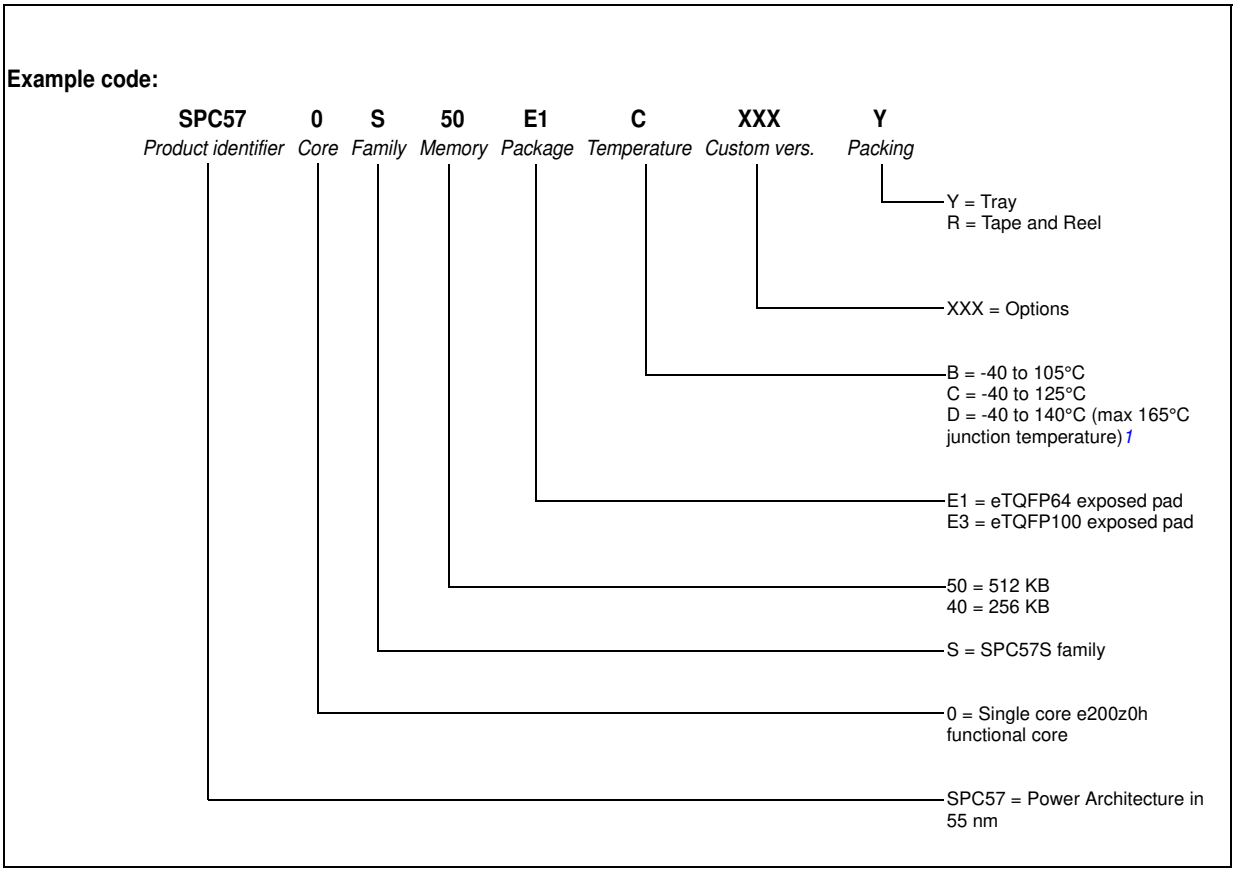
1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.
2. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
3. A1 is defined as the distance from the seating plane to the lowest point on the package body.
4. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. To be determined at setting datum plane C.
7. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
8. The Top package body size may be smaller than the bottom package size by much as 0.15 mm.
9. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located. It includes all metal protrusions from exposed pad itself.
10. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.

11. L dimension is measured at gauge plane at 0.25 above the seating plane.
12. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
13. Tolerance.

Note: TQFP stands for Thin Quad Flat Package.

6 Ordering information

Figure 23. Ordering information scheme



1. Refer to technical note "SPC570S family - High Temperature "D" Grade (DocID031416 - TN1262)" for specification limitation applying for this temperature range to this specification.

7 Revision history

Table 41. Document revision history

Date	Revision	Changes
08-Apr-2013	1	Initial release
21-Sep-2013	2	Updated Disclaimer
03-Jun-2014	3	Updated the tables in Section 3.2.4: Pin multiplexing, *Section 3.3: Package pads/pins* and *Section 4.9.3: I/O output DC characteristics* Updated *Table 5: Parameter classifications* Updated *Table 25: Flash memory program and erase specifications*
12-Jun-2014	4	Changed timing values in *Table 25: Flash memory program and erase specifications* Added *Table 26: Flash memory Life Specification*
26-Mar-2015	5	Throughout the document: – Editorial and formatting updates – Changed device name from SPC570S40Ex to SPC570S – Used slow/medium/fast/veryfast to describe pad strength – Replaced all occurrences of PLL by PLL0 and FMPLL by PLL1 – Renamed $V_{DD_HV_OSC}$ as $V_{DD_HV_OSC_PMC}$ – Renamed $V_{DD_HV_ADV}$ and $V_{DD_ADC_TSENS}$ as $V_{DD_HV_ADC_TSENS}$ – Renamed $V_{DD_HV_ADR}$ as V_{REFH_ADC} – Renamed $V_{DD_HV_IO_MAIN}$ and $V_{DD_HV_IO_JTAG}$ as $V_{DD_HV_IO}$ – Renamed $V_{SS_HV_IO}$ as V_{SS} Clarified descriptions of *Figure 6: Noise filtering on reset signal* Removed subsections of *Section 3.2: Pin descriptions* with referral to the "Signal description" chapter in the devices' reference manual Added *Section 4.4: Electromagnetic compatibility (EMC)* Added *Section 4.5: Electrostatic discharge (ESD)* Added *Section 4.8: Current consumption* Updated *Section 4.11: Power management electrical characteristics* Added *Section 4.12: PMU monitor specifications* Added *Section 4.16: External oscillator (XOSC) electrical characteristics* Added *Section 4.19: Temperature sensor* Added *Section 4.20: JTAG interface timings* Added *Section 4.21: DSPI CMOS master mode timing* Added *Table 2: SPC570S40Ex, SPC570S50Ex device configuration differences* *Table 6: Absolute maximum ratings* – Added: *VDD_HV_OSC_PMC*, *VDD_HV_ADC_TSENS*, *VREFH_ADC*, *IMAXSEG* – Changed values for: *Cycle*, *VIN*, *IMAXD* – Added condition for t_{XRAY} – Removed T_J – Updated footnote *1.* and parameter descriptions for *IINJD* and *IINJA*

Table 41. Document revision history (continued)

Date	Revision	Changes
26-Mar-2015	5	*Table 9: Device operating conditions*: – Added: *VDD_HV_OSC_PMC*, *VREFH_ADC - VDD_HV_ADC_TSENS*, *VIN*, *IMAXSEG* – Changed values for: *VDD_HV_IO* – Updated parameter descriptions for: *VREFH_ADC*, *VREFH_ADC - VDD_HV_ADC_TSENS* – Updated classification tags and footnotes for: *VDD_HV_IO* and *VDD_HV_OSC_PMC* – Removed: V_{DD_LV} *Table 14: I/O input DC electrical characteristics* – Added *ILKG* – Changed conditions for: *VIH*, *VIL*, *VHYST*, *VIHCMOS_H*, *VIHCMOS(2)*, *VILCMOS_H(2)*, *VILCMOS(2)*, *VHYSCMOS* – Changed values for: *VIH*, *VIL*, *CIN* – Removed 4.0 V < $V_{DD_HV_IO}$ < 4.5 V conditions from the *Automotive* section Updated *Table 15: I/O pull-up/pull-down DC electrical characteristics* Removed “Min” values from tables: *16*, *17*, *18*, *20* Removed “Typ” values from tables: *16*, *17*, *18*, *19*, *20* Renamed *Table 20: I/O output characteristics for pads 4, 9, 11, 55, 56* to include the pad numbers *Table 21: Reset electrical characteristics* changed conditions and values for: *IOL_R*, *|IWPU|*, *|IWPD|* *Table 22: Voltage regulator electrical characteristics* – changed values and condition description for *CDECBV* – removed $I_{MREGINT}$ *Table 25: Flash memory program and erase specifications* changed values for: *tPSUS*, *tESUS* *Table 31: Internal RC oscillator electrical specifications* – Removed condition and changed values for *dfvar_noT* – Changed values for *dfvar_SW* *Table 34: ADC conversion characteristics* – Changed values for: *IADCREFH*, *IADCVDD*, *DNL* – Added footnotes for *VSS_HV_ADR* and *IADCREFH*
23-Sep-2015	6	*Table 6: Absolute maximum ratings*: – Updated t_{XRAY} *Table 12: Current consumption*: – Updated IDD information – Added classification tag, Min Typ and Max columns – Updated value of maximum consumption during boot time M/LBIST Tables *16*, *17*, *18*, *19*: – Added classification tag, Min Typ and Max columns *Table 23: Trimmed (PVT) values*: – Updated POR200 lower limit Removed “(pending silicon Qualification)” from the titles of *Table 25* and *Table 26* Corrected *Section 4.12.2: Power up/down sequencing* Reverted to using weak/medium/strong/very strong to describe pad strength

Table 41. Document revision history (continued)

Date	Revision	Changes
31-Jan-2018	7	Throughout the document: – Editorial and formatting updates Updated Cover Page – The following “feature” is added: “AEC-Q100 qualified.” – The following “feature” is updated: “Junction temperature range -40 °C to 150 °C.” to “Junction temperature range -40 °C to 150 °C (165 °C grade optional).” Updated *Table 1: SPC570Sx device feature summary (Family Superset Configuration)* – Added Junction Temperature value, “165 °C grade optional”. – New footnote is added, “Refer to technical note "SPC570S family - High Temperature "D".....specification limitation." *Figure 1: Block diagram* – Added blocks “CMU_3” and “WKPU”. *Table 6: Absolute maximum ratings*: – Updated t_{XRAY} to X-rays dose. *Table 9: Device operating conditions* – Updated T_J by adding a new value, “165 °C grade optional”. – New footnote is added, “Refer to technical note "SPC570S family - High Temperature "D".....specification limitation.” *Figure 7: Recommended parasitics on board* – Added VDD_HV_IO (ballast supply) (61, 95) *Section 4.7: Thermal characteristics* – Added *Table 11: Thermal characteristics for eTQFP100* *Section 4.11.1: Voltage regulator electrical characteristics* – Added a note “All 1.2 V pins should be shorted externally on board with minimum resistance and minimum inductance..... more than 5 mohm resistance and 0.5 nH inductance.” *Table 26: Flash memory Life Specification* – Updated all the parameters of “N_{DER16K}” to “N_{DER8K}” Updated *Section 4.18.2: ADC electrical characteristics* – Added *Figure 11: Input equivalent circuit (12- bit SAR)* – Added *Table 33: ADC pin specification,* *Table 40: eTQFP100 package mechanical data* – Updated the values of D2 and E2. Updated *Section 4.18: ADC electrical characteristics* – Added *Figure 11: Input equivalent circuit (12- bit SAR)* – Added *Figure 33: ADC pin specification,* *Figure 23: Ordering information scheme* – Updated the value of E1 (Package), “D= -40 to 140 °C” to “D= -40 to 140 °C” (165 °C junction temperature maximum) – Added a figure footnote “Refer to technical note "SPC570S family - High Temperature “D” .....for specification”.

Table 41. Document revision history (continued)

Date	Revision	Changes
31-Jan-2018	7 (contd.)	Updated *Section 5.1: eTQFP64 package information* – *Figure 21: eTQFP64 package outline* updated. – *Figure 39: eTQFP64 package mechanical data* updated. Updated *Section 5.2: eTQFP100 package information* – *Figure 22: eTQFP100 package outline* updated. *Table 40: eTQFP100 package mechanical data* updated.

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