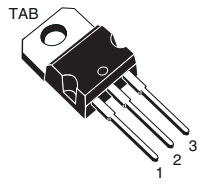
STP170N8F7

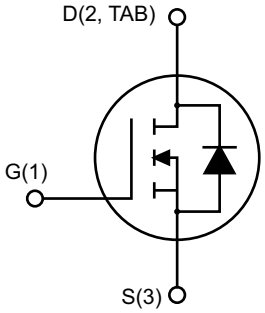
N-channel 80 V, 0.003 Ω typ., 120 A, STripFET™ F7 Power MOSFET in TO-220 package

Datasheet — production data



TO-220

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STP170N8F7	80 V	0.0039 Ω	120 A	250 W

- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order code	Marking	Package	Packaging
STP170N8F7	170N8F7	TO-220	Tube

This is information on a product in full production. www.st.com

Contents

1 Electrical ratings 3

2 Electrical characteristics 4

2.1 Electrical characteristics (curves) 6

3 Test circuits 8

4 Package mechanical data 9

5 Revision history 11

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous)	120	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	120	A
I_{DM}	Drain current (pulsed)	480	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	250	W
T_J	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		°C

1. Limited by package and rated according to $R_{thj\text{-}c}$.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.6	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max.	62.5	°C/W

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current, (pulse width limited by T_{jmax})	35	A
E_{AS}	Single pulse avalanche energy (starting TJ = 25 °C, $I_D = I_{AV}$, V_{DD} = 50 V)	615	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 250 µA	80			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 80 V			1	µA
		V_{GS} = 0, V_{DS} = 80 V, T_C=125 °C			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = +20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS}= 10 V, I_D= 60 A		0.003	0.0039	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS}=0, V_{DS} =40 V, f=1 MHz	-	8710	-	pF
C_{oss}	Output capacitance		-	1330	-	pF
C_{rss}	Reverse transfer capacitance		-	78	-	pF
Q_g	Total gate charge	V_{DD}=40 V, I_D = 120 A V_{GS} =10 V *Figure 14*	-	120	-	nC
Q_{gs}	Gate-source charge		-	43	-	nC
Q_{gd}	Gate-drain charge		-	26	-	nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 40 V, I_D= 60 A, R_G= 4.7 Ω, V_{GS}= 10 V *Figure 13*	-	38	-	ns
t_r	Rise time		-	53	-	ns
$t_{d(off)}$	Turn-off delay time		-	79	-	ns
t_f	Fall time		-	37	-	ns

Table 8. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		120	A
I_{SDM}(1)	Source-drain current (pulsed)		-		480	A
V_{SD}(2)	Forward on voltage	V_{GS}=0, I_{SD} = 120 A	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 120 A, di/dt = 100 A/µs, V_{DD}= 64 V, T_j=150 °C	-	54		ns
Q_{rr}	Reverse recovery charge		-	78		nC
I_{RRM}	Reverse recovery current		-	2.9		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

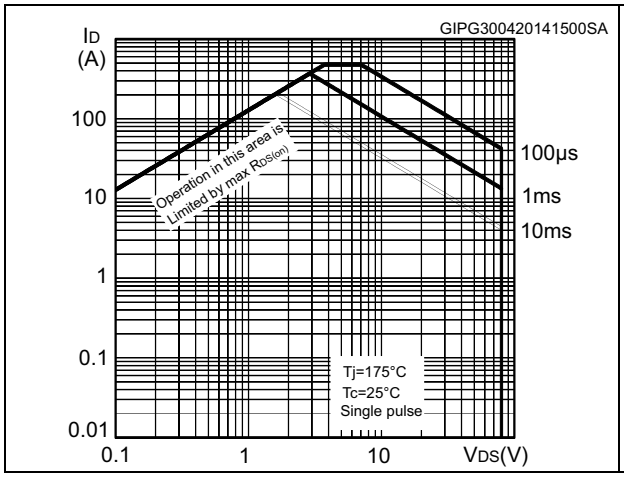


Figure 3. Thermal impedance

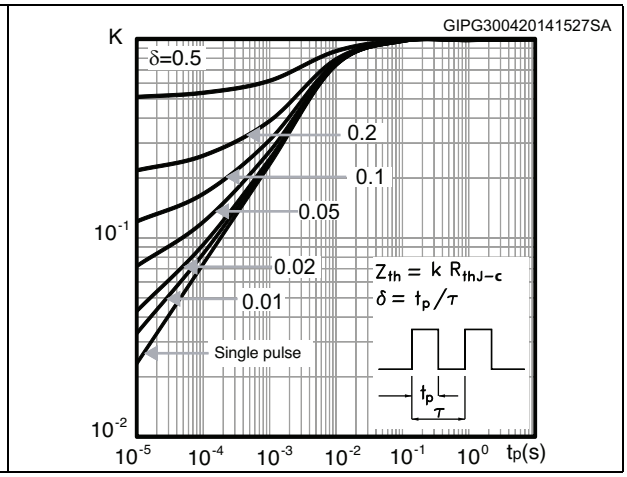


Figure 4. Output characteristics

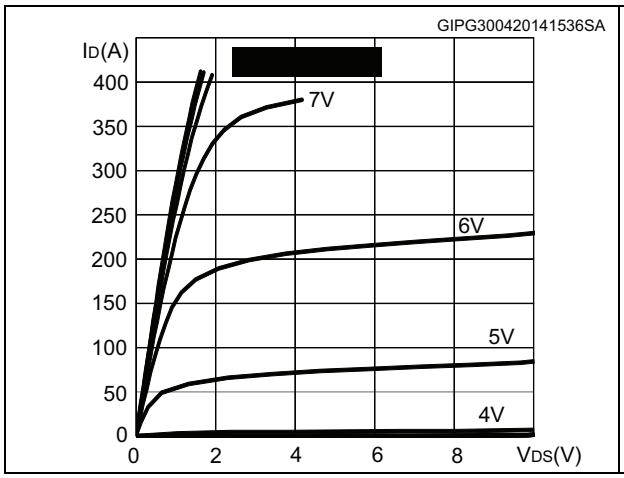


Figure 5. Transfer characteristics

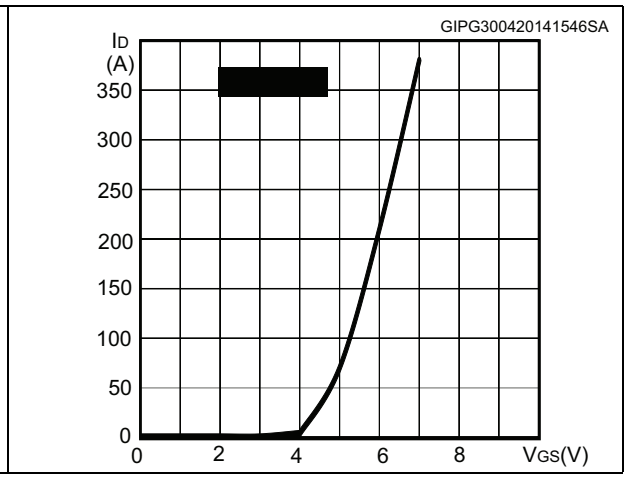


Figure 6. Gate charge vs gate-source voltage

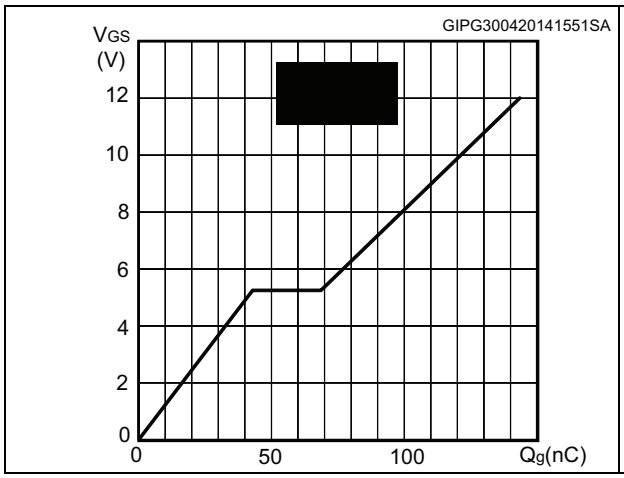


Figure 7. Static drain-source on-resistance

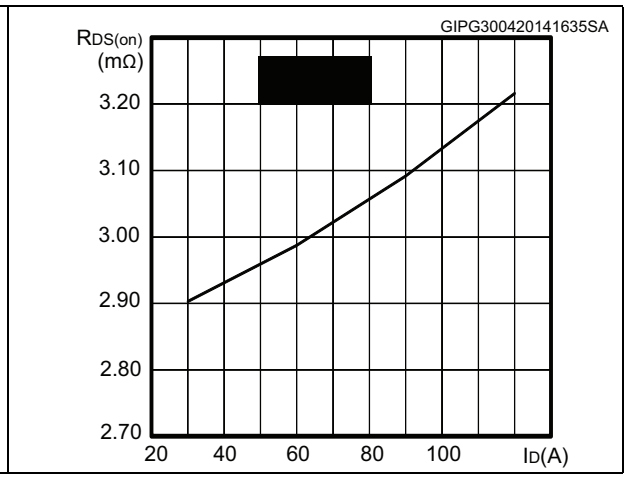


Figure 8. Capacitance variations

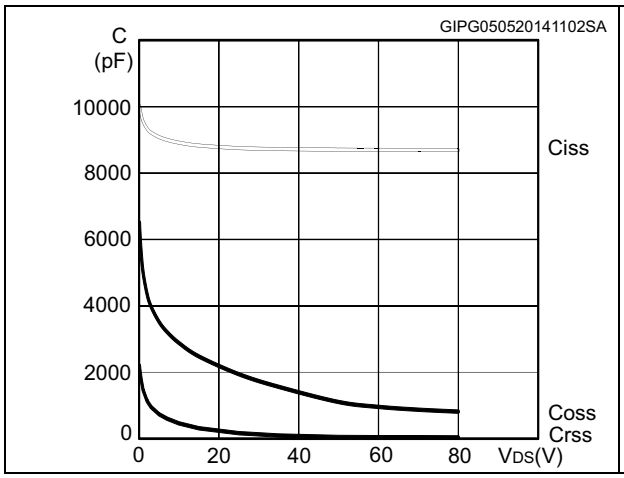


Figure 9. Normalized gate threshold voltage vs temperature

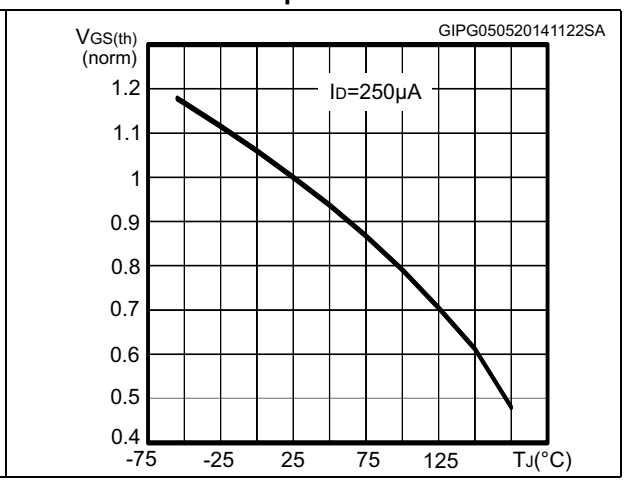


Figure 10. Normalized on-resistance vs temperature

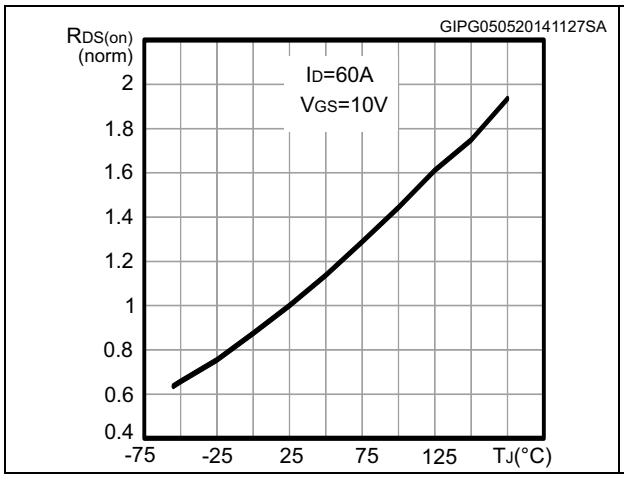


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

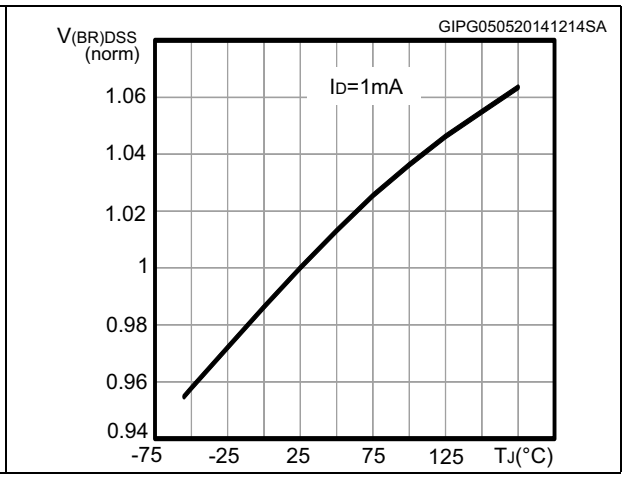
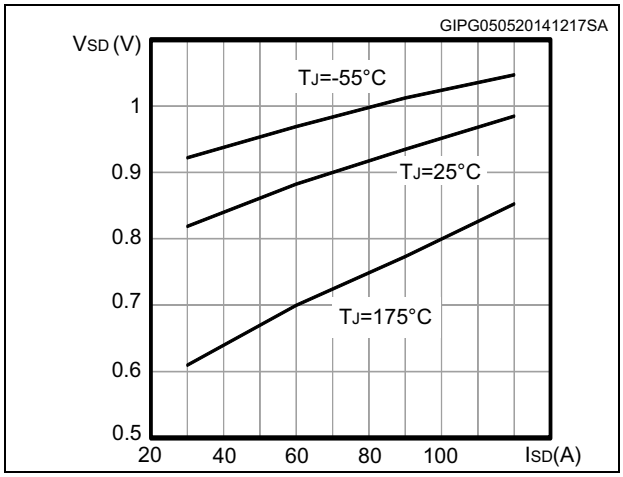


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

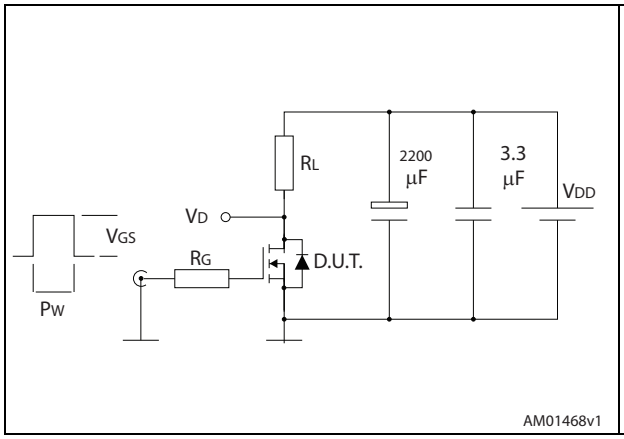


Figure 14. Gate charge test circuit

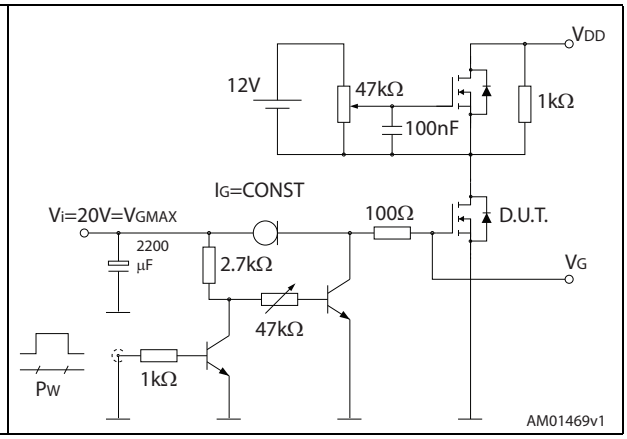


Figure 15. Test circuit for inductive load switching and diode recovery times

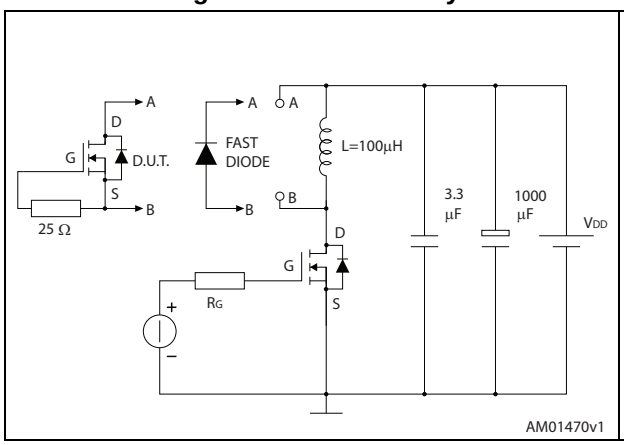


Figure 16. Unclamped inductive load test circuit

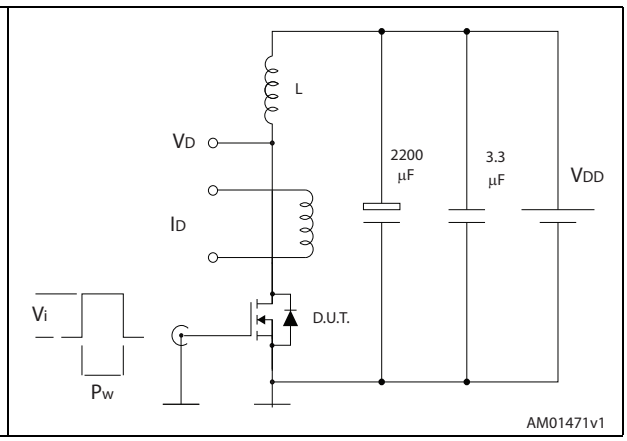


Figure 17. Unclamped inductive waveform

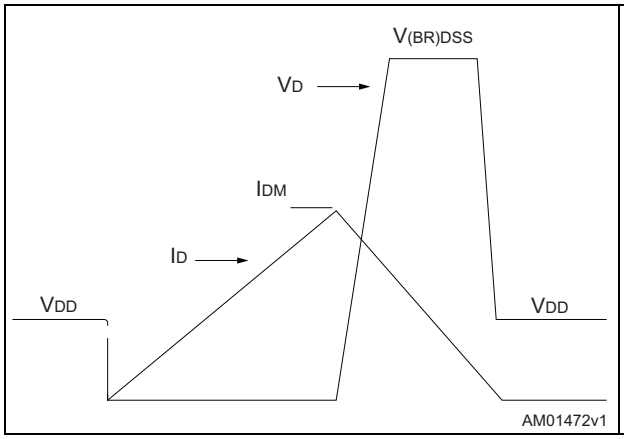
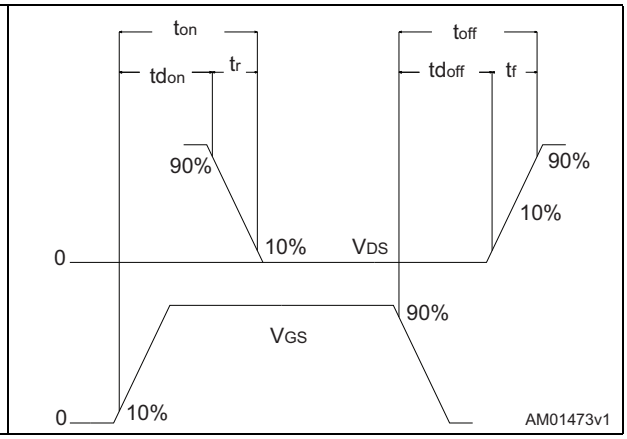


Figure 18. Switching time waveform



4 Package mechanical data

Figure 19. TO-220 type A drawing

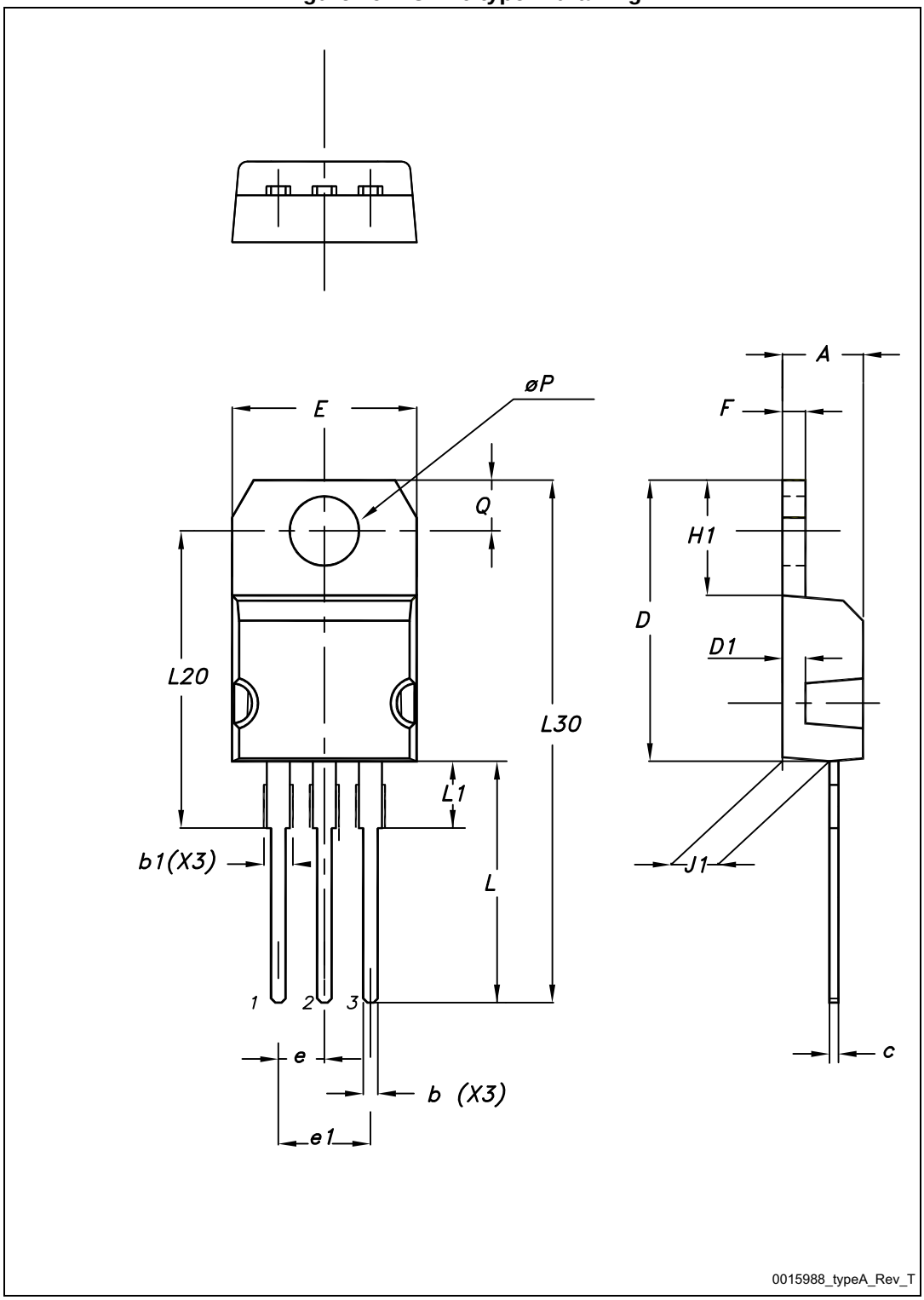


Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
16-Apr-2013	1	First release.
15-May-2014	2	– The part number STH170N8F7-2 has been moved to a separate datasheet – Modified: $R_{DS(on)}$ in cover page – Modified: *Figure 1* – Modified: I_D (T_C = 100 °C), P_{TOT} and E_{AS} values in *Table 2* – Modified: $R_{thj\text{-}case}$ value in *Table 3* – Added: *Table 4* – Modified: I_{DSS}, $V_{GS(th)}$ and $R_{DS(on)}$ values in *Table 5* – Modified: the entire typical values in table *Table 6*, *7* and *8* – Added: *Section 2.1: Electrical characteristics (curves)* – Updated: *Section Figure 19.: TO-220 type A drawing* – Minor text changes
20-Feb-2015	3	– Updated title, features and description in cover page.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved