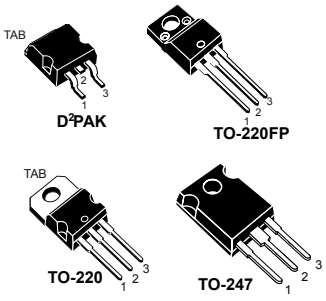
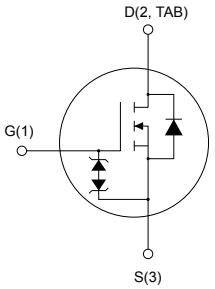
STB10N95K5, STF10N95K5
STP10N95K5, STW10N95K5

Datasheet

N-channel 950 V, 650 mΩ typ., 8 A MDmesh K5 Power MOSFETs in D²PAK, TO-220FP, TO-220 and TO-247 packages





AM01476v1_tab

Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D
STB10N95K5	950 V	800 mΩ	8 A
STF10N95K5			
STP10N95K5			
STW10N95K5			

- Very low FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status links
STB10N95K5
STF10N95K5
STP10N95K5
STW10N95K5

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D²PAK, TO-220, TO-247	TO-220FP	
V_{GS}	Gate-source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25 °C	8	8(1)	A
	Drain current (continuous) at T_C = 100 °C	5	5(1)	
I_{DM}(2)	Drain current (pulsed)	32		A
P_{TOT}	Total power dissipation at T_C = 25 °C	130	30	W
dv/dt(3)	Peak diode recovery voltage slope	4.5		V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)		2.5	kV
T_J	Operating junction temperature range	-55 to 150		°C
T_{stg}	Storage temperature range			°C

1. *Limited by maximum junction temperature.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 8 A, di/dt ≤ 100 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$.*
4. *V_{DD} ≤ 760 V.*

Table 2. Thermal data

Symbol	Parameter	Value				Unit
		D²PAK	TO-220	TO-247	TO-220FP	
R_{thJC}	Thermal resistance, junction-to-case	0.96			4.2	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	30(1)	62.5	50	62.5	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	2.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	122	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	950			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 950 V			1	µA
		V_{GS} = 0 V, V_{DS} = 950 V, T_C = 125 °C(1)			50	
I_{GSS}	Gate body leakage current	V_{GS} = ±20 V, V_{DS}= 0 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4 A		650	800	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	630	-	pF
C_{oss}	Output capacitance		-	50	-	pF
C_{rss}	Reverse transfer capacitance		-	0.6	-	pF
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{DS} = 0 to 760 V, V_{GS} = 0 V	-	77	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related		-	28	-	pF
R_g	Gate input resistance	f = 1 MHz, I_D = 0 A	-	6.5	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 8 A, V_{GS} = 0 to 10 V (see Figure 19. Test circuit for gate charge behavior)	-	22	-	nC
Q_{gs}	Gate-source charge		-	5	-	nC
Q_{gd}	Gate-drain charge		-	15	-	nC

1. *$C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*
2. *$C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 475 V, I_D = 4 A, R_G = 4.7 Ω , V_{GS} = 10 V (see Figure 18. Test circuit for resistive load switching times and Figure 23. Switching time waveform)	-	22	-	ns
t_r	Rise time		-	14	-	ns
$t_{d(off)}$	Turn-off delay time		-	51	-	ns
t_f	Fall time		-	15	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8	A
I_{SDM}(1)	Source-drain current (pulsed)		-		32	A
V_{SD}(2)	Forward on voltage	I_{SD} = 8 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 20. Test circuit for inductive load switching and diode recovery times)	-	404		ns
Q_{rr}	Reverse recovery charge		-	5.2		µC
I_{RRM}	Reverse recovery current		-	25.5		A
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 20. Test circuit for inductive load switching and diode recovery times)	-	596		ns
Q_{rr}	Reverse recovery charge		-	6.9		µC
I_{RRM}	Reverse recovery current		-	23		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for D²PAK, TO-220

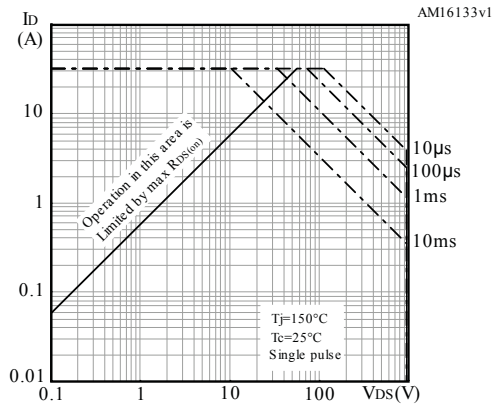


Figure 2. Normalized transient thermal impedance for D²PAK, TO-220

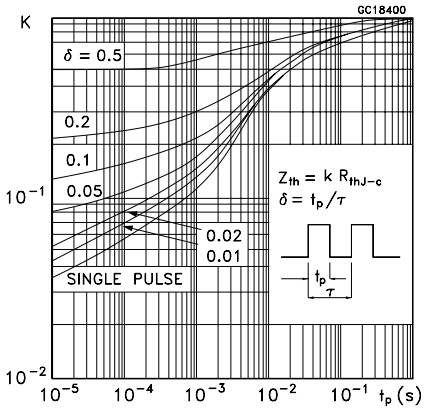


Figure 3. Safe operating area for TO-220FP

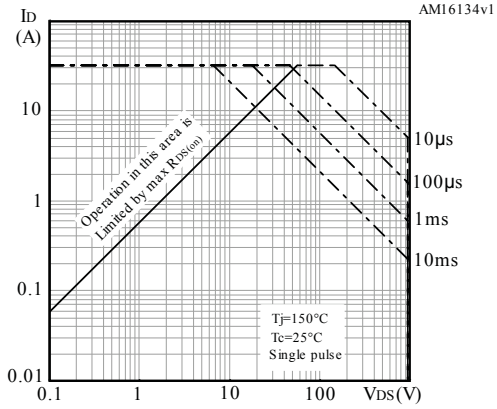


Figure 4. Normalized transient thermal impedance for TO-220FP

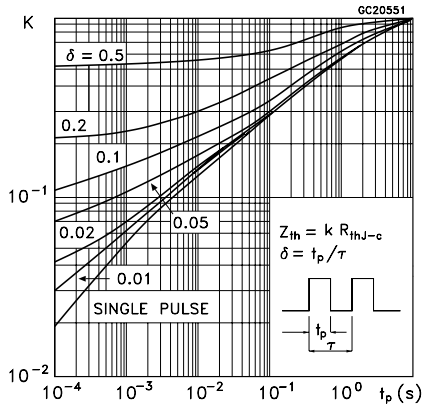


Figure 5. Safe operating area for TO-247

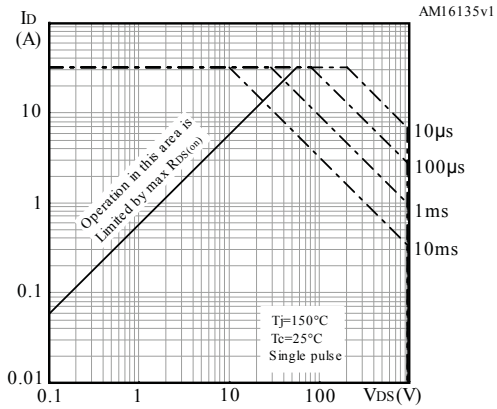


Figure 6. Normalized transient thermal impedance for TO-247

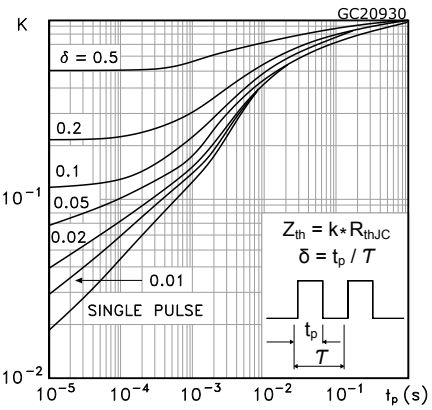


Figure 7. Typical output characteristics

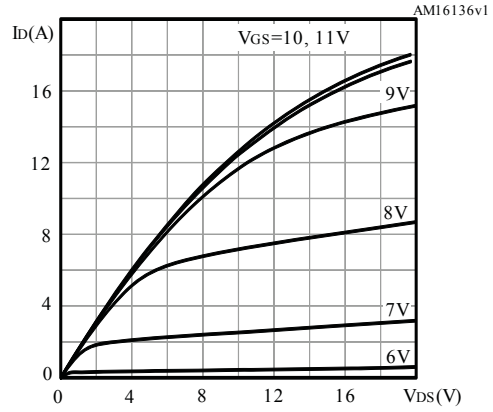


Figure 8. Typical transfer characteristics

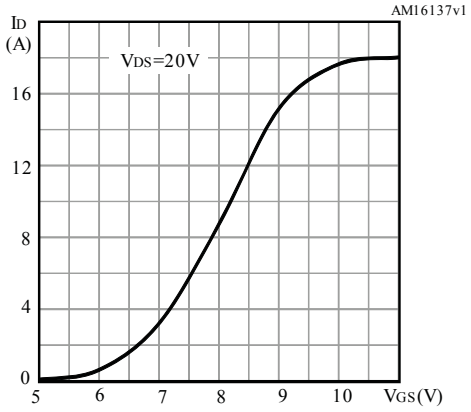


Figure 9. Typical gate charge characteristics

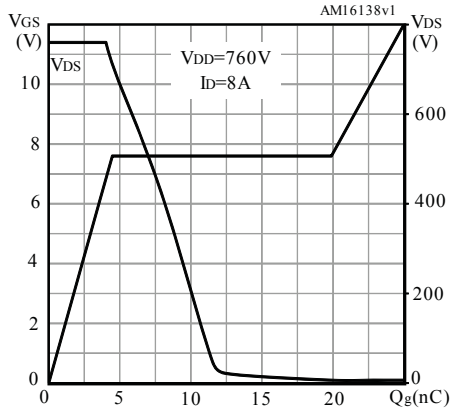


Figure 10. Typical drain-source on-resistance

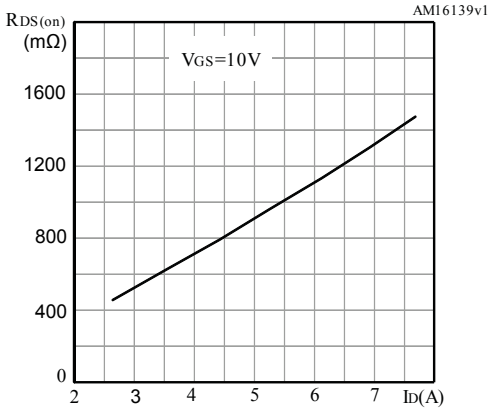


Figure 11. Typical capacitance characteristics

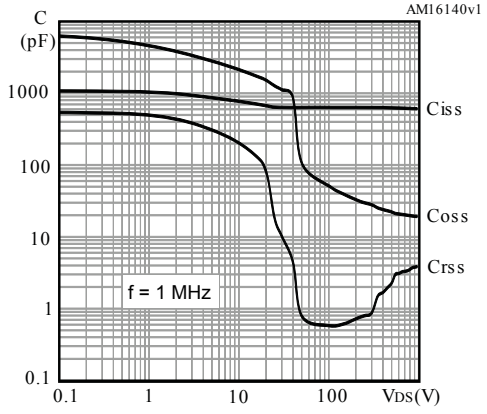


Figure 12. Typical output capacitance stored energy

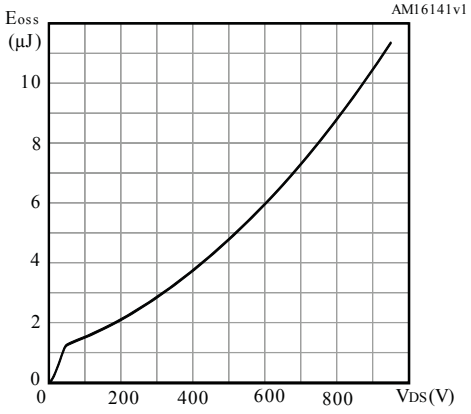


Figure 13. Normalized gate threshold vs temperature

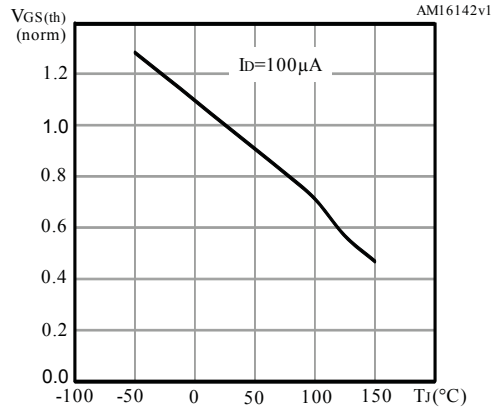


Figure 14. Normalized on-resistance vs temperature

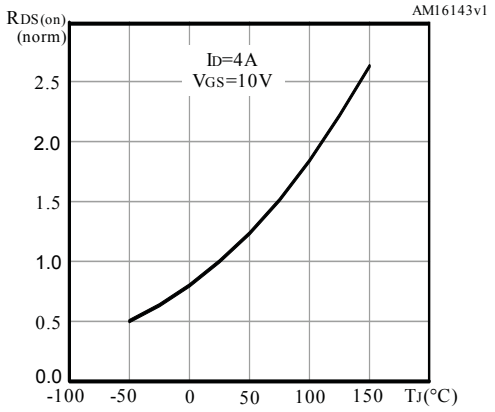


Figure 15. Typical reverse diode forward characteristics

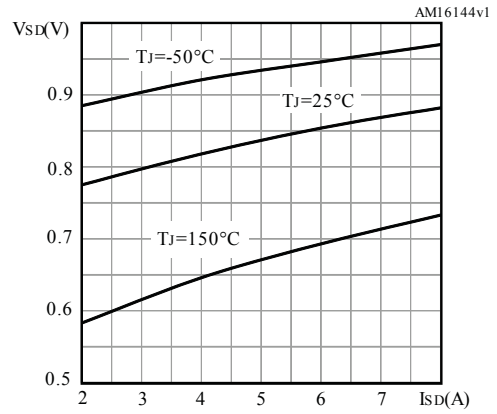


Figure 16. Normalized breakdown voltage vs temperature

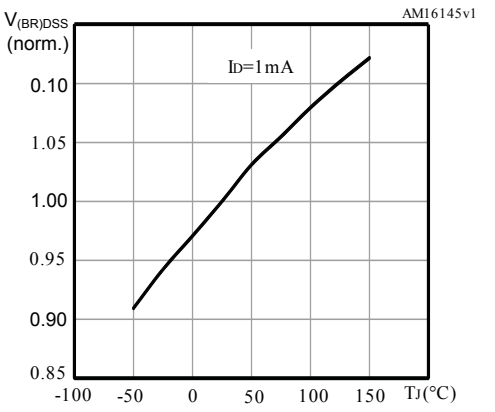
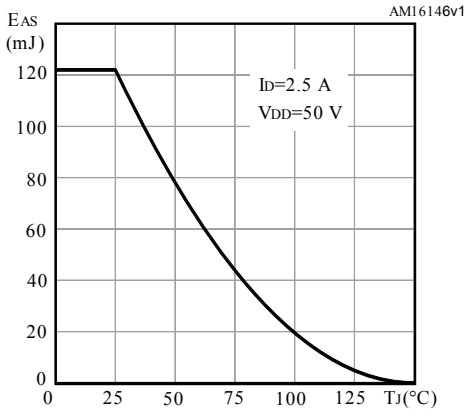
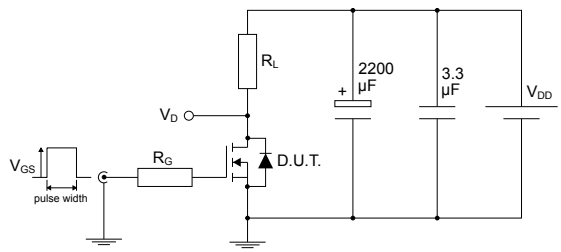


Figure 17. Maximum avalanche energy vs temperature



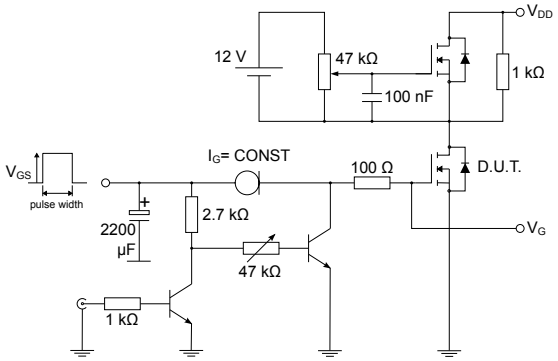
3 Test circuits

Figure 18. Test circuit for resistive load switching times



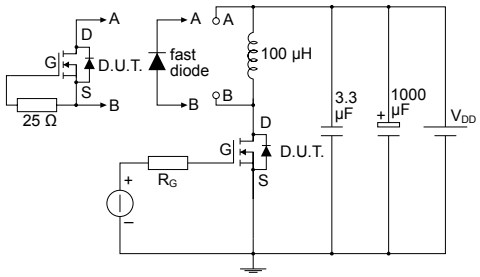
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Figure 19. Test circuit for gate charge behavior



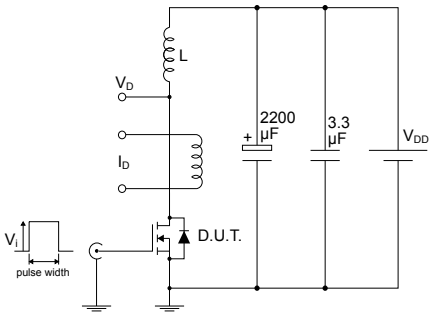
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Figure 20. Test circuit for inductive load switching and diode recovery times



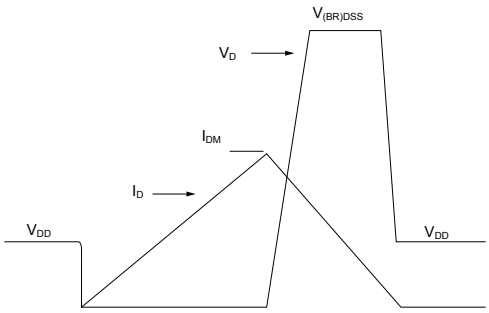
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Figure 21. Unclamped inductive load test circuit



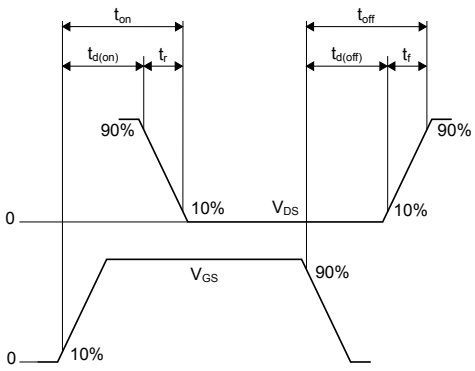
AM01471v1

Figure 22. Unclamped inductive waveform



AM01472v1

Figure 23. Switching time waveform



AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 24. **D²PAK (TO-263) type A package outline**

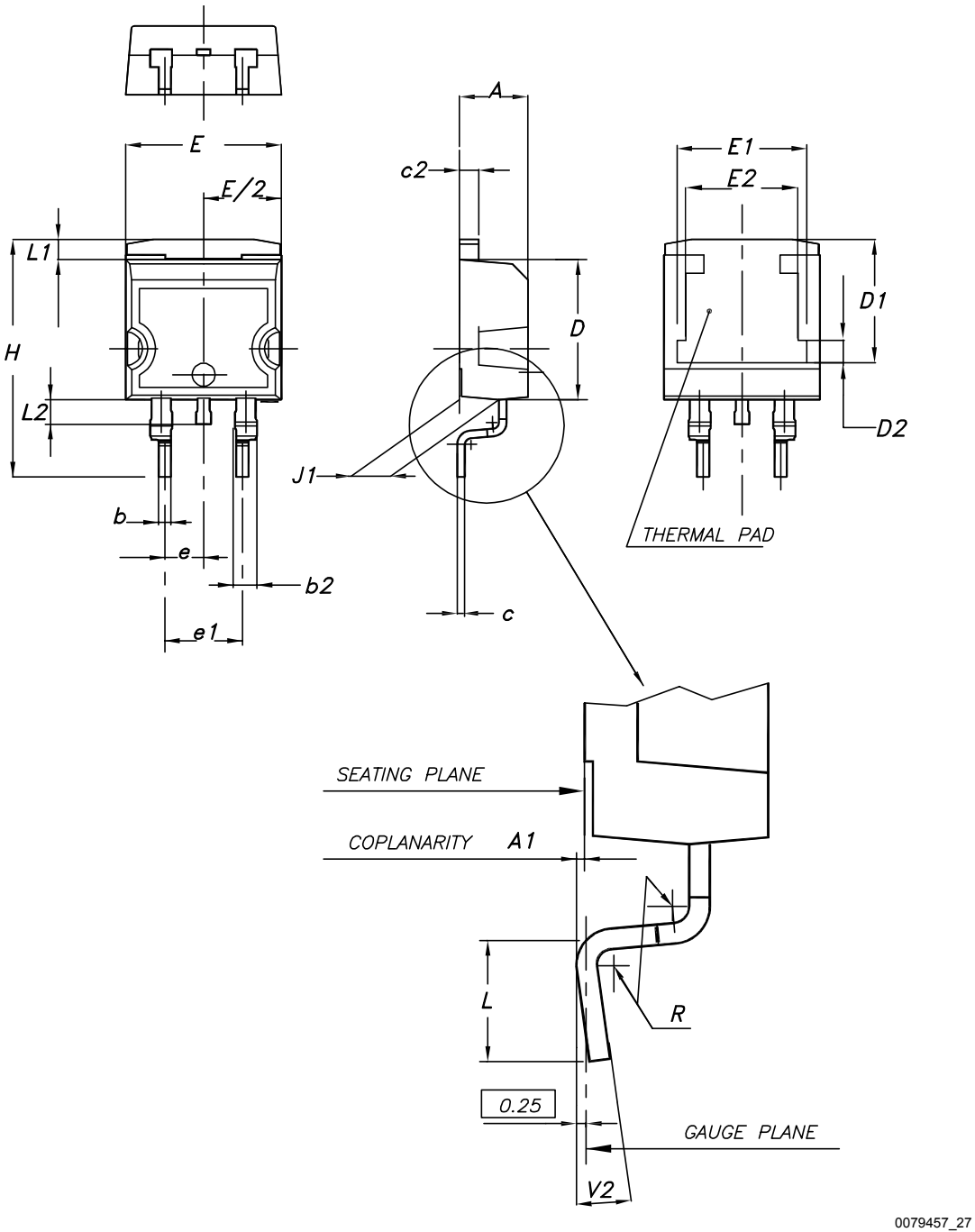
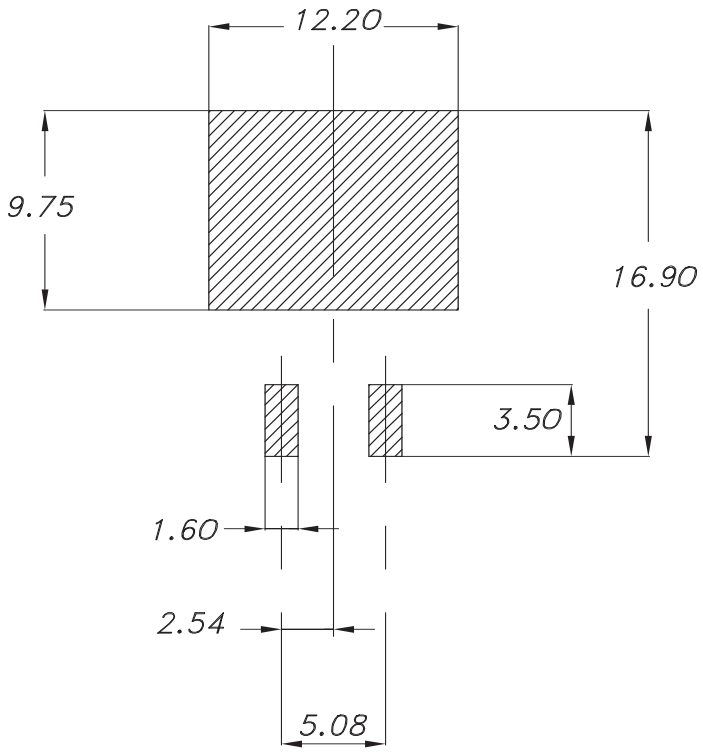


Table 8. D²PAK (TO-263) type A package mechanical data

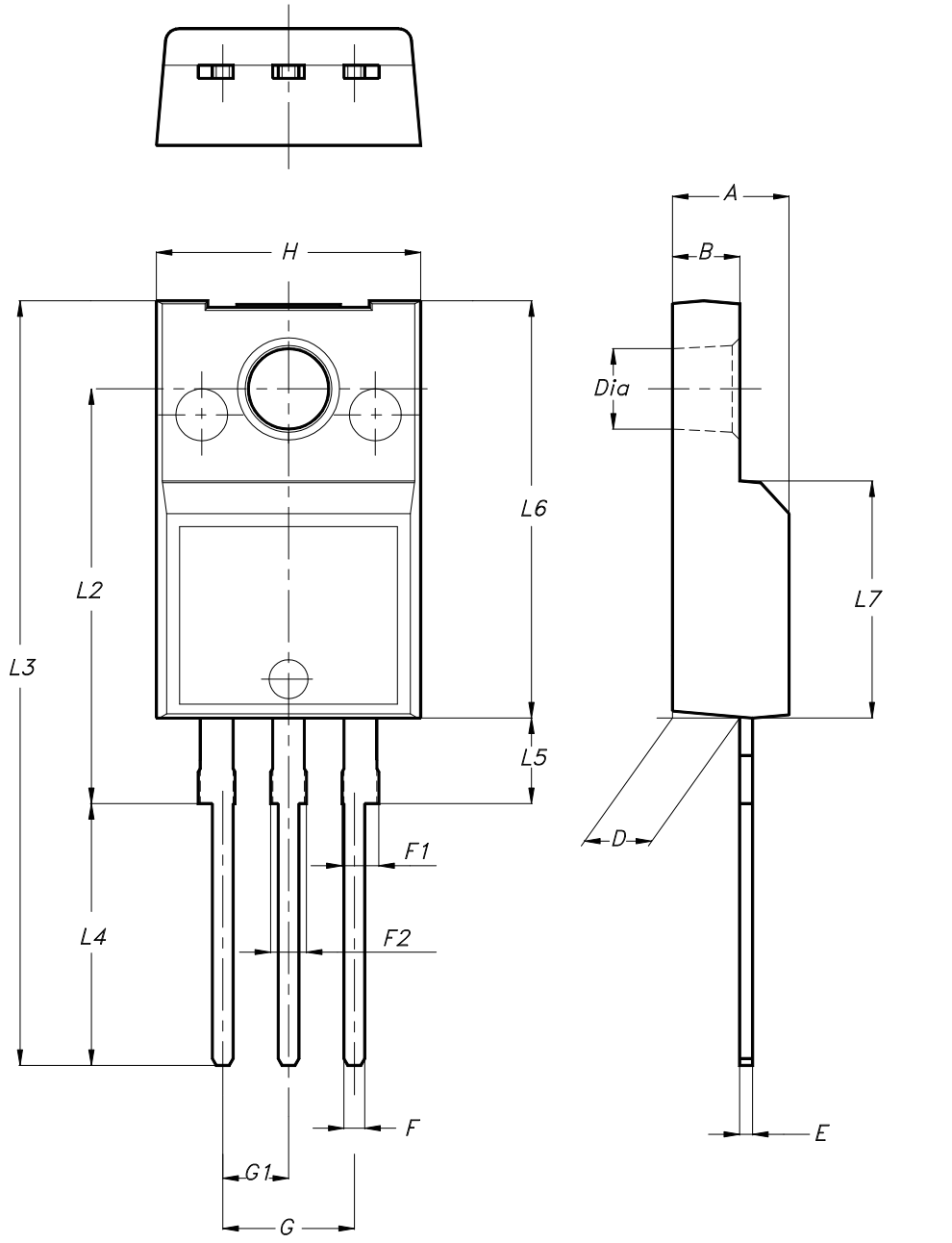
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 25. **D²PAK (TO-263) recommended footprint (dimensions are in mm)**



4.2 TO-220FP package information

Figure 26. **TO-220FP type B package outline**



7012510_B_rev.14

Table 9. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.3 TO-220 type A package information

Figure 27. **TO-220 type A package outline**

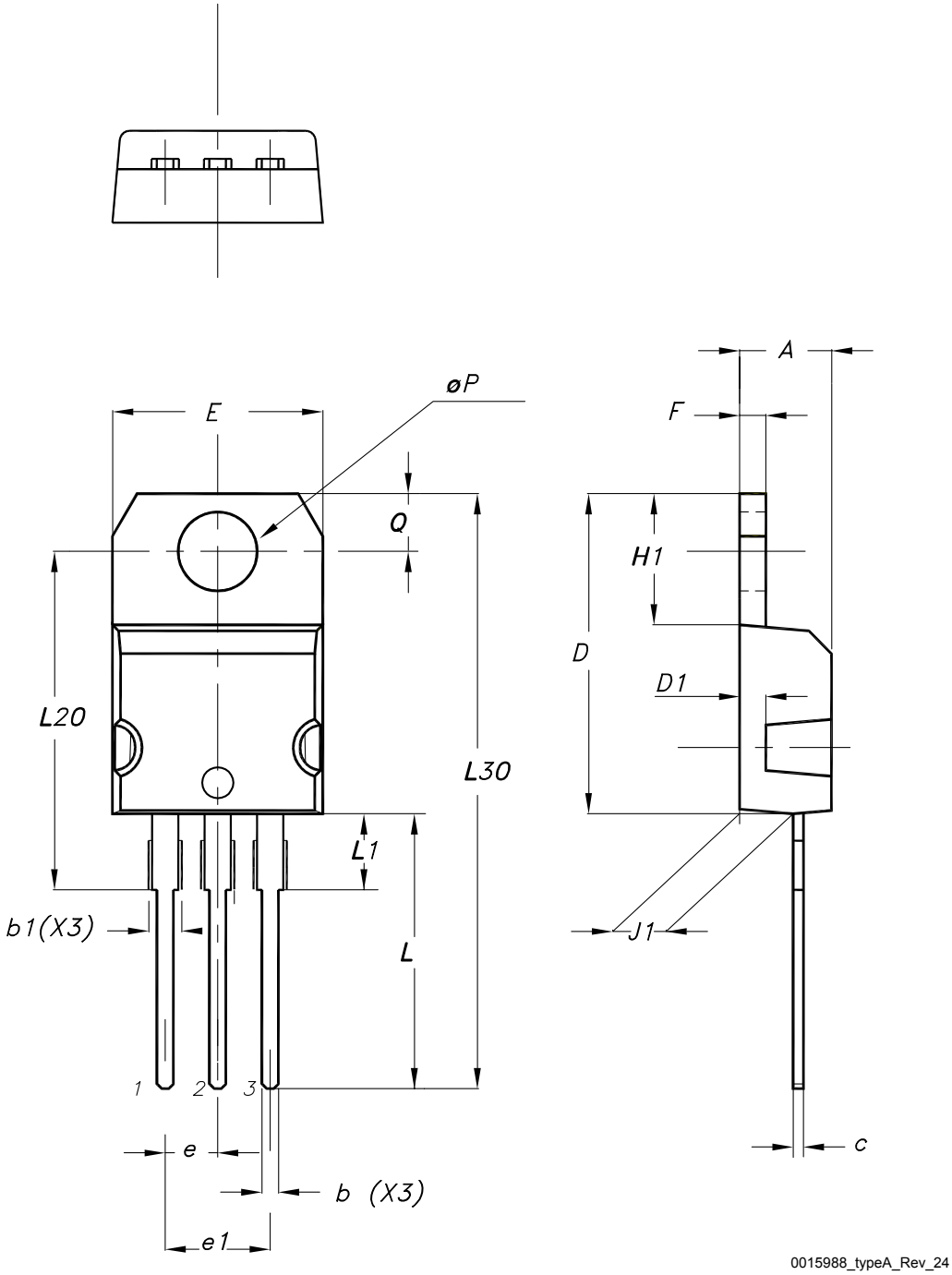
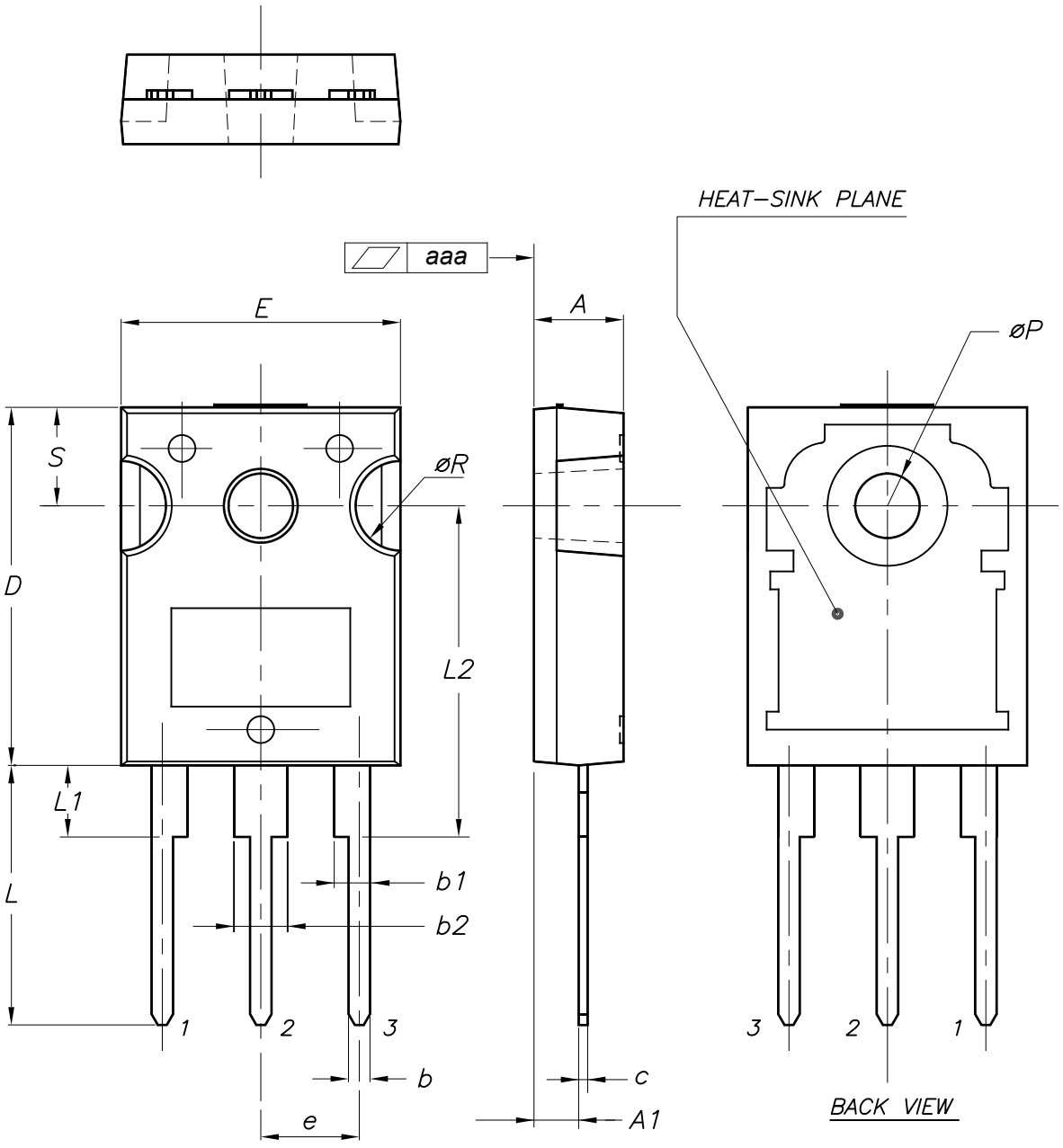


Table 10. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.4 TO-247 package information

Figure 28. **TO-247 package outline**



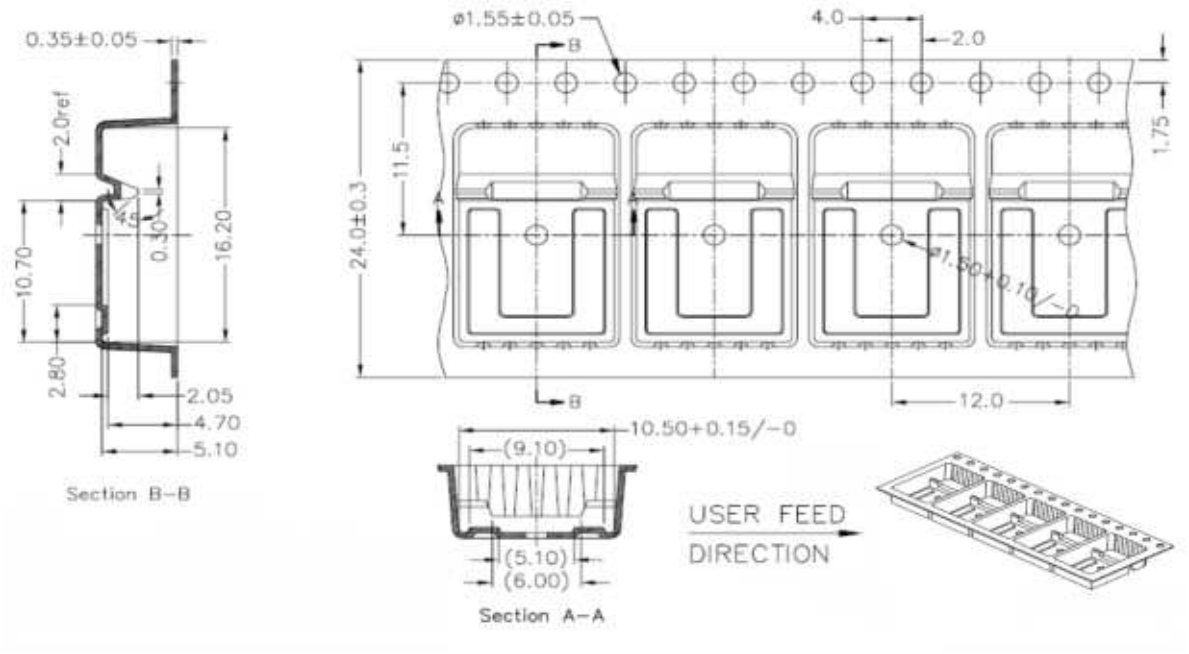
0075325_10

Table 11. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10

4.5 D²PAK packing information

Figure 29. **D²PAK tape drawing (dimensions are in mm)**



DM01095771_2

5 Ordering information

Table 12. **Order codes**

Order codes	Marking	Package	Packing
STB10N95K5	10N95K5	D²PAK	Tape and reel
STF10N95K5		TO-220FP	Tube
STP10N95K5		TO-220	
STW10N95K5		TO-247	

Revision history

Table 13. **Document revision history**

Date	Version	Changes
24-Jun-2013	1	First release.
07-Oct-2013	2	– Added: D^2PAK package – Modified: *note 4* in *Table 2* – Added: Thermal resistance junction-pcb max parameter – Modified: typical values in *Table 5*, *6* and *7* – Added: *Section 2.1: Electrical characteristics (curves)* – Updated: *Section 4: Package mechanical data* – Minor text changes
29-Jan-2014	3	– Datasheet status promoted from preliminary data to production data – Minor text changes
27-Oct-2025	4	Updated Section 4: Package information. Minor text changes.

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